DESIGN AND FABRICATION OF A 4-TERMINAL IN-PLANE NANOELECTROMECHANICAL RELAY

Yingying Li[1], *Simon J. Bleiker*[1], *Pierre Edinger*[1], *Elliott Worsey*[2], *Mukesh Kumar Kulsreshath*[2], *Qi Tang*[2], *Alain Yuji Takabayashi*[3], *Niels Quack*[3], *Peter Verheyen*[4], *Wim Bogaerts*[4,5], *Kristinn B. Gylfason*[1], *Dinesh Pamunuwa*[2] *and Frank Niklaus*[1]
[1]KTH Royal Institute of Technology, Sweden
[2]Univeristy of Bristol, U.K.
[3]École Polytechnique Fédérale de Lausanne (EPFL), Switzerland
[4]IMEC, Belgium and
[5]University of Ghent, Belgium

ABSTRACT

We present 4-terminal (4-T) silicon (Si) nanoelectron-mechanical (NEM) relays fabricated on silicon-on-insulator (SOI) wafers. We demonstrate true 4-T switching behavior with isolated control and signal paths. A pull-in voltage (V_{pi}) as low as 11.6 V is achieved with the miniaturized design. 4-T NEM relays are a very promising candidate for building ultra-low-power logic circuits, since they enable novel circuit architectures to realize logic functions with far fewer devices than CMOS implementations, while also allowing the dynamic power consumption to be reduced by body-biasing.

KEYWORDS

4-T NEM relays, in-plane Si relays, decoupled signals, low pull-in voltage, ultra-low power consumption

INTRODUCTION

NEM relays have been known for their attractive properties, such as zero off-state leakage, ultra-low static power consumption and abrupt switching transition, which make it possible to overcome the energy-efficiency limit of CMOS technology [1]. The robustness of NEM relays also makes them outstanding in harsh environments, such as extreme temperature and radiation levels, where CMOS transistors cannot survive [2]. Therefore, NEM relays have been proposed as a promising candidate for ultra-low power computing applications, e.g., energy-efficient field-programmable gate arrays (FPGAs) [3]. Among the various NEM logic relays, 4-T NEM relays offer great potential for novel circuit architectures to realize logic functions with far fewer devices and much higher energy efficiency than CMOS implementations. As much as a five-fold reduction in device count can be achieved in commonly used logic functions such as multiplexer and demultiplexer circuits [4]. However, to achieve practical 4-T NEM circuits, a reliable fabrication method is required to miniaturize the dielectric plug together with the 4-T relays for achieving a compact circuit layout, which remains a challenge.

Previously reported 4-T NEM relays were made of metal and formed by conventional manufacturing processes within the metallic interconnect layers of a CMOS process [5-6]. Although they can achieve small footprints down to 0.055 μm^2 [7], the metal relays suffer from fatigue during repeated actuation, which limits their long-term reliability. In contrast, the Si NEM relays have been proven to exhibit excellent mechanical properties and longevity, but the Si 4-T NEM relays with miniaturized dielectric plugs have not been demonstrated. Overall, currently available 4-T relays have either a large footprint [4,8], occupying a significant chip area, or a high pull-in voltage [4-5,8], resulting in considerable dynamic energy consumption.

Here we report on a miniaturized Si 4-T NEM relay with an integrated dielectric plug, fabricated on SOI substrates. We describe the design and fabrication methodology for the miniaturized 4-T NEM relay and demonstrate switching behavior with independent control and signal paths. This method enables compact NEM circuit layout, while also improving energy efficiency.

DEVICE CONCEPT AND FABRICATION

The design of an in-plane Si 4-T NEM relay is illustrated in Figure 1. This 4-T NEM relay uses electrostatic actuation with a single contact point. It consists of four terminals: two movable beams connected to the *source* and the *body* terminals, respectively, and fixed *drain* and *gate* terminals. Each terminal is electrically connected to an aluminum (Al) contact pad for electrical contacting of the relay.

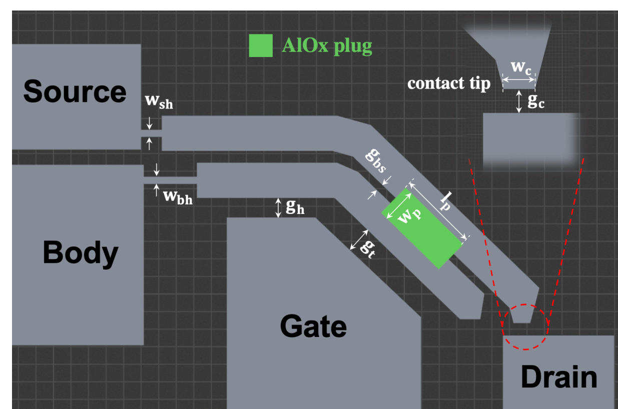

Figure 1: 2D illustration of the in-plane 4-T NEM relay realized in an SOI wafer process (the AlO_x plug is shown in green).

The unique feature of our 4-T relay is the dielectric aluminum oxide (AlO_x) plug between the two beams (shown in green in Figure 1). This plug electrically insulates the data signal (*source-drain*) from the control

Authorized licensed use limited to: IMEC. Downloaded on June 02,2024 at 13:41:08 UTC from IEEE Xplore. Restrictions apply.

signal (*body-gate*), which enables body biasing, as well as the device count reduction of NEM-based circuits [2].

The fabrication process of the 4-T NEM relays is illustrated in Figure 2. Steps (i) to (ii) are performed on SOI wafers with a 220 nm thick device layer and a 2 µm thick buried oxide (BOX) layer. The NEM structures are firstly patterned with sub-200 nm feature stepper lithography and etched by reactive ion etching (RIE). After that, a 70 nm thin layer of AlO_x is deposited on the entire chip, which is selectively patterned and removed later with a photoresist mask to form the dielectric AlO_x plug (step iii). To improve the conductivity of the relay contacts, we adopt a standard lift-off process to deposit 80 nm of gold (Au) only on the tip of the NEM relays (step iv to step v). The partial release is conducted before the Au deposition to avoid undesired short-circuits between the *drain* and the *source*. Finally, we use vapor hydrofluoric acid (vHF) release etch to fully suspend the movable beams (step vi).

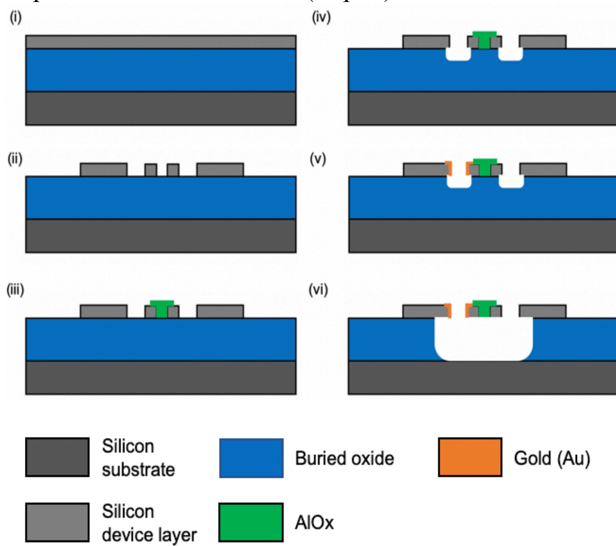

Figure 2: Schematic cross-section of the fabrication flow: (i) Blank SOI wafer with 220 nm-thick device layer, (ii) Define the NEM relay pattern, (iii) Deposit and etch the AlO_x plugs (iv) Partial release of the NEM relays, (v) Metallize the contact of the NEM relays with Au, (vi) Full release of NEM relays.

A typical AlO_x plug etching result after step (iii) is shown in Figure 3. We studied the dielectric plug design to find the limit of this fabrication process, which is mainly determined by the resolution and alignment accuracy of the lithography process.

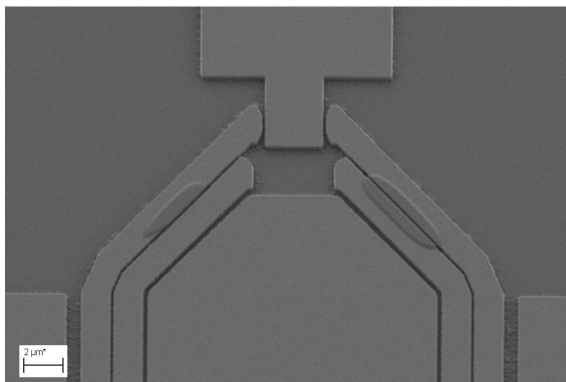

Figure 3: Top view SEM micrograph of two 4-T NEM relays with AlO_x plugs.

In Figure 3, a misalignment shift of ~ 200 nm to the top-left of the relay is clearly visible. Due to the direction of the misalignment, this caused the left AlO_x plug to miss the gap between the two beams, while the right AlO_x plug remained aligned with the gap.

RESULTS AND DISCUSSION

A Scanning Electron Microscope (SEM) image of a fabricated 4-T NEM relay is shown in Figure 4. The design parameters of this 4-T relay are listed in Table 1.

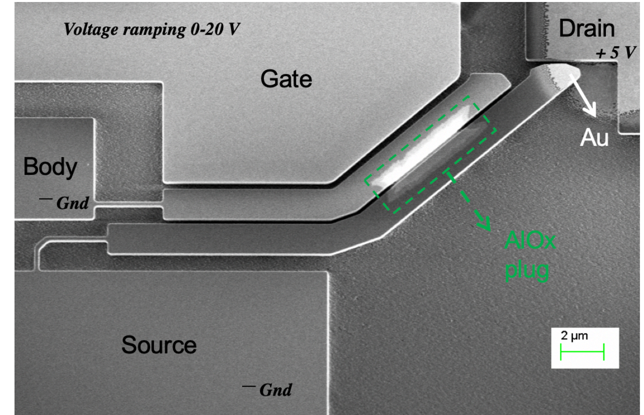

Figure 4: Top view SEM micrograph of a 4-T NEM relay with AlO_x plug and ~80 nm Au contact. The image is captured after step (v) in Figure 2.

Table 1: Design parameters of the 4-T NEM relay

Parameters	Size
Silicon device layer thickness	220 nm
Source hinge width w_{sh}	200 nm
Body hinge width w_{bh}	200 nm
Body-gate airgap horizontal g_h	300 nm
Body-gate airgap tilted g_t	350 nm
Body-source airgap g_{bs}	200 nm
Plug-length l_p	7.0 μm
Plug-width w_p	2.4 um
Contact width w_c	1.0 μm
Contact airgap g_c	200 nm

Actuation of a 4-T NEM relay

To actuate the 4T NEM relay, we directly contact the Al pads with probe needles and applied a voltage ramp V_{gb} = (0 V → ~15 V → 0 V) between the *gate* and the *body* terminals. A drain bias voltage was applied between the *drain* and the *source* terminals (V_{ds} = 5 V), while both the *source* and *body* terminals were kept at ground level. As shown in Figure 5, the 4-T relay shows a clear pull-in when ramping the gate voltage up to V_{pi} = 11.6 V, under a 10 nA current compliance. The contact got stuck on the drain after the first actuation due to the high adhesion force, which is the main problem induced by using Au as the contact material.

Authorized licensed use limited to: IMEC. Downloaded on June 02,2024 at 13:41:08 UTC from IEEE Xplore. Restrictions apply.

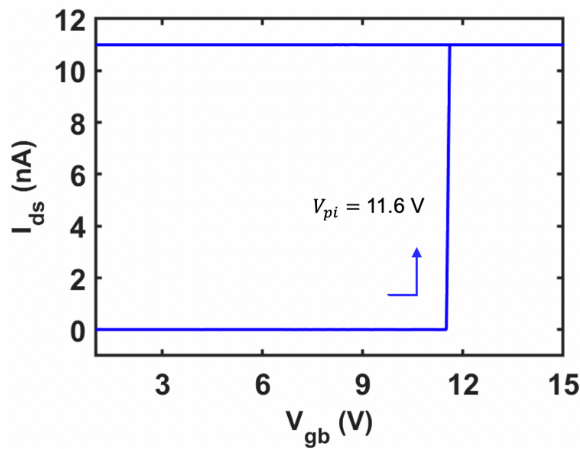

Figure 5: Measured actuation of a 4-T NEM relay. The abrupt drain-source current (I_{ds}) increase indicates successful pull-in.

Demonstration of dielectric plug insulation

To prove true 4-T actuation behavior, we confirmed that there is only ~pA current flowing through the body electrode during the actuation (as shown in Figure 6), which indicates good insulation between the *source* and the *body* terminals, i.e., the AlO_x plug is providing adequate insulation between the two beams. Also, the current on the *gate* is also at noise-level (pA).

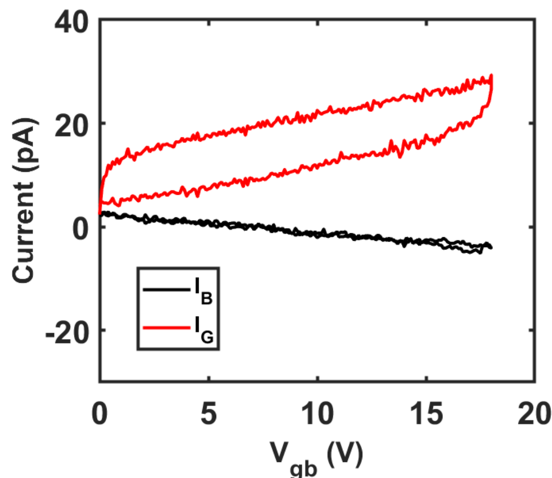

Figure 6: Measured current flowing through body and gate terminals versus gate voltage of the 4-T NEM relay.

CONCLUSION

We implemented a nano-scale Si 4-T NEM relay on an SOI substrate. We demonstrated true 4-T switching with insulated data and control signals, which enables body biasing that significantly lowers the pull-in voltage and the dynamic power consumption. This design and fabrication technology shows promise for making compact NEM relay-based circuits for high-volume applications. Future work is needed to find compatible contact solutions with sufficient switching reliability to improve the lifetime of the NEM relays during hot-switching. Possible candidates of the contact coating include Ti, W and Ru, which provide improved hardness and good electrical conductivity.

ACKNOWLEDGEMENTS

This project has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreements No.780283 (MORPHIC) and No.871740 (ZeroAMP).

REFERENCES

[1] T. Cao et al, "Research Status and Development Trend of MEMS Switches: A Review," *Micromachines*, 11, 694.

[2] A. Peschot et al., "Nanoelectromechanical switches for low-power digital computing," *Micromachines*, 6, pp. 1046-1065, 2015.

[3] S. Rana et al., "Nanoelectromechanical relay without pull-in instability for high-temperature non-volatile memory." *Nat. Commun.*, 11:1181, 2020.

[4] J. D. Reynolds et al., "Single-contact, four-terminal Microelectromechanical relay for efficient digital logic," *Advanced Electronic Materials*, 2200584, 2022.

[5] U. Sikder et al., "Toward monolithically integrated hybrid CMOS-NEM circuits," *IEEE Trans. Electron Devices*, Vol.68, No.12, 2021.

[6] Y.H. Yoon et al., "A low contact resistance 4-terminal MEMS relay: theoretical analysis, design, and demonstration," *J. Microelectromech Syst.*, Vol.27, No.3, 2018.

[7] U. Sikder et al., "Non-volatile Nano-electro-mechanical switches and hybrid circuits in a 16 nm CMOS back-end-of-line process," *IEEE Trans. Electron Devices*, Vol.44, No.1, pp.136-139, 2023.

[8] J. Jeon et al., "Perfectly Complimentary Relay Design for Digital Logic Applications," *IEEE Electron Device Lett.*, Vol.31, No.4, pp. 371-373, 2010.

CONTACT

*Y. Li, tel: +46-769657385; yingyli@kth.se

Authorized licensed use limited to: IMEC. Downloaded on June 02,2024 at 13:41:08 UTC from IEEE Xplore. Restrictions apply.