PHOTONICS RESEARCH GROUP

LUCEDA PHOTONICS · GHENT UNIVERSITY · imec

INTRODUCTION TO SILICON PHOTONICS CIRCUIT DESIGN

Wim Bogaerts

Short Course 454 - OFC 2021

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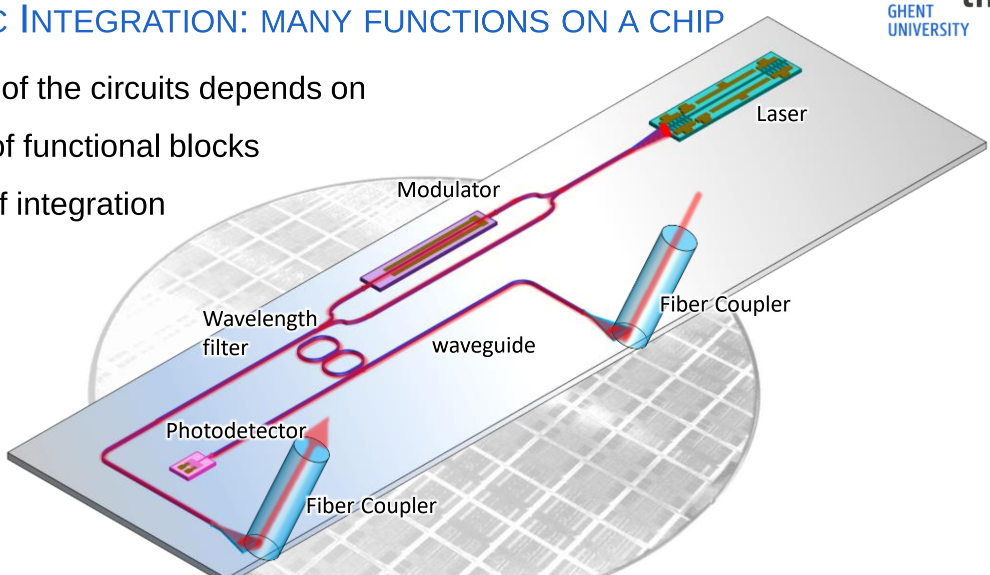
PHOTONIC INTEGRATION: MANY FUNCTIONS ON A CHIP

Complexity of the circuits depends on

- number of functional blocks
- density of integration



Circuits connect elements together with waveguides

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Manipulating light on Chips

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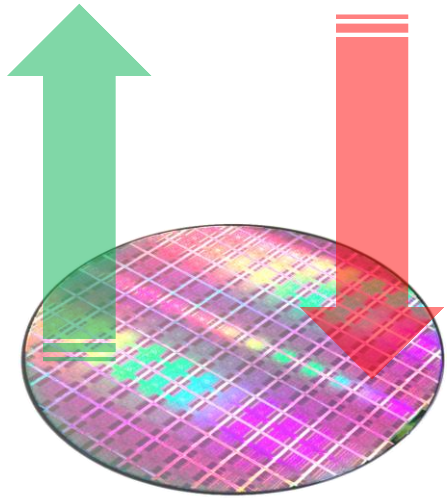
Complexity

Overall Performance

Reliability

Ergonomy

goes up



Power consumption

Ecological Footprint

Cost

goes down

The benefits of scale

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Photonic Integration: many functions on a chip

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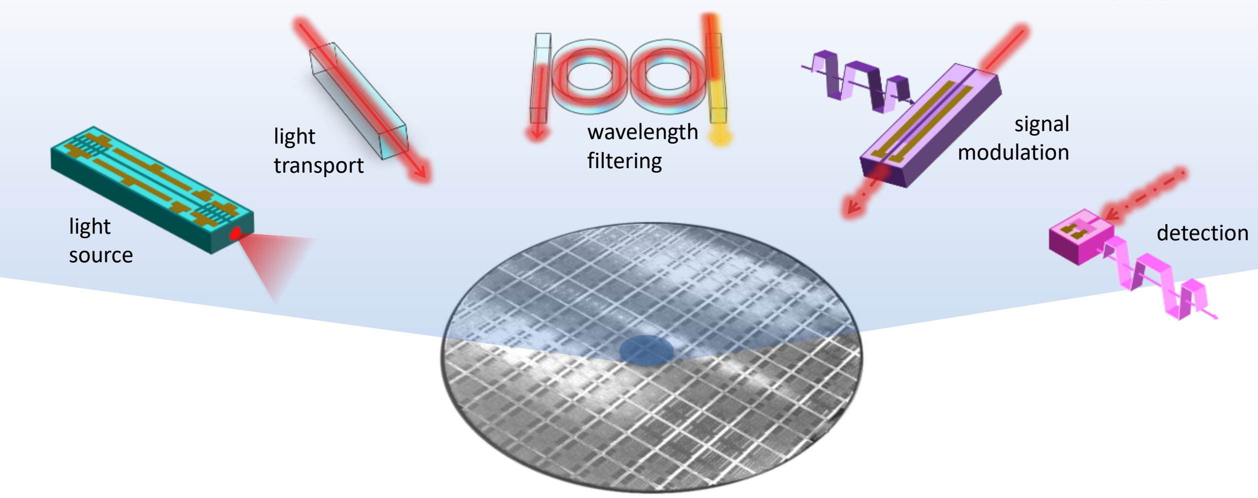

Circuits connect elements together with waveguides

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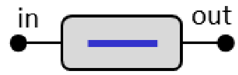
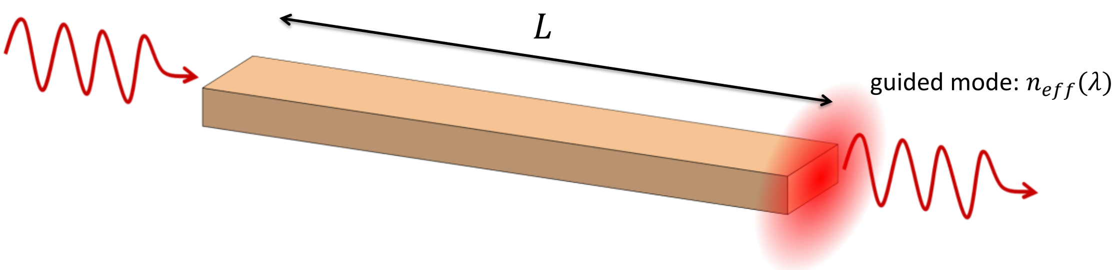
Waveguides

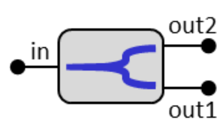


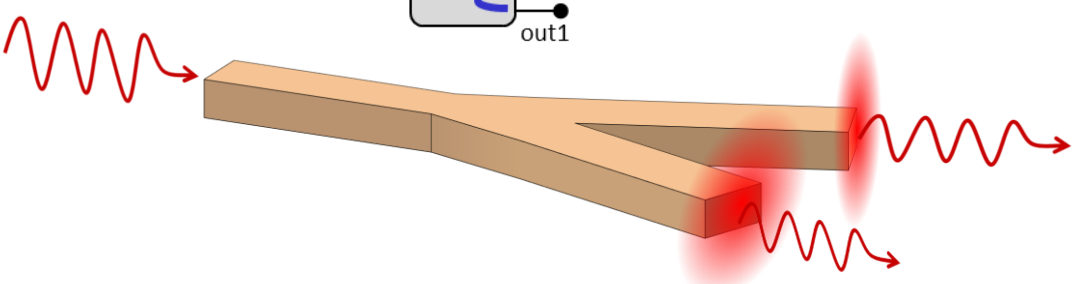


Propagate light from the input to the output

- wavefronts propagate with velocity $v_{ph}(\lambda) = \frac{c}{n_{eff}(\lambda)}$
  ($n_{eff}(\lambda)$= effective refractive index)
- Dispersion: $n_{eff}(\lambda)$ is wavelength dependent
- Group velocity: time delay of a wave packet: $v_g(\lambda) = \frac{c}{n_g(\lambda)}$

Splitters



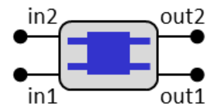


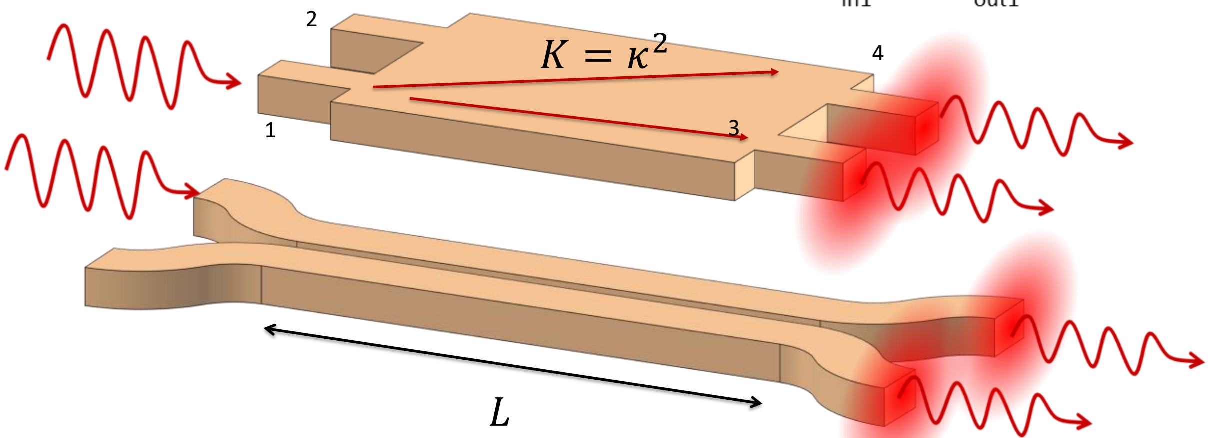
Splits light in two equal parts

- one input
- two outputs
- symmetric

Reciprocal: Also has 3dB loss when used as a combiner.

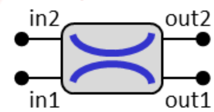
2×2 COUPLERS





Can be based on an MMI or other designs

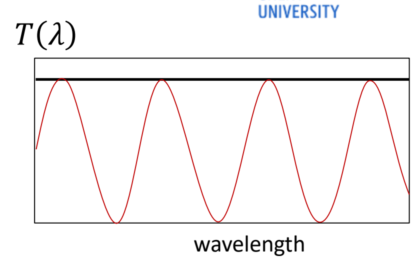
Couples fraction $K = \kappa^2$ of the power to another waveguide



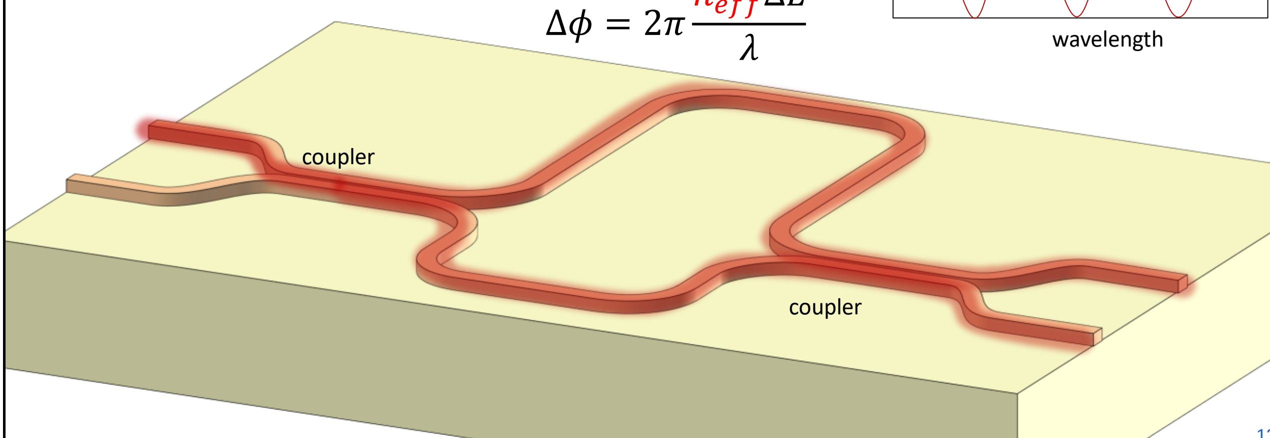
MACH-ZEHNDER INTERFEROMETER

beam splitters + waveguides

delay line will give a wavelength dependent response



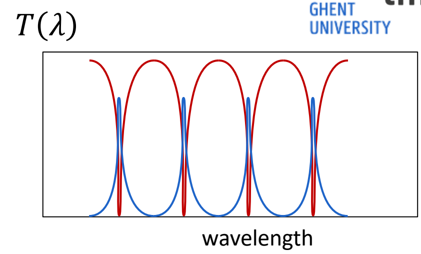
$$\Delta\phi = 2\pi \frac{n_{eff}\Delta L}{\lambda}$$

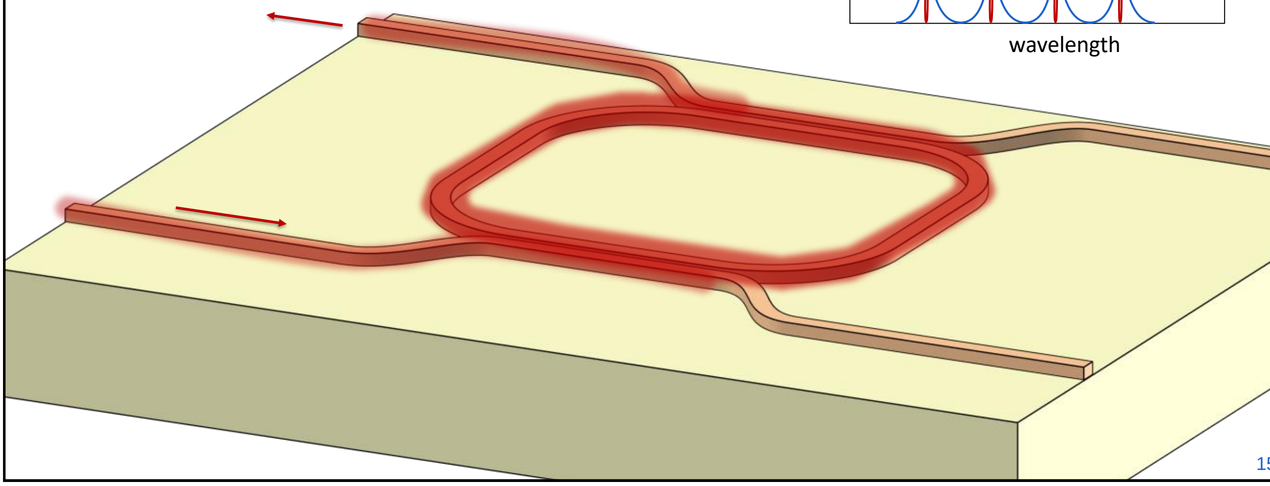


Ring Resonators

Optical feedback loop

Resonance when $n_{eff} L_{ring} = m.\lambda$





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Wavelength Filtering

channel drop filter

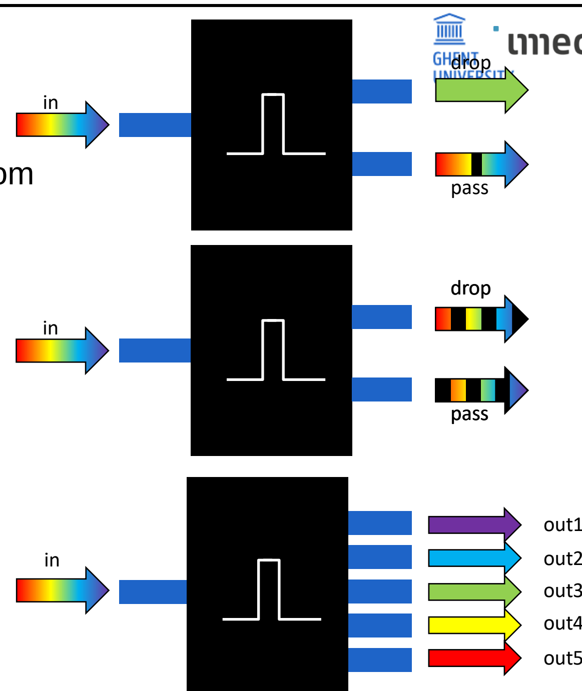
- selects a passband from a wavelength range

interleaver

- separates alternating wavelength bands

demultiplexer

- separates multiple wavelength channels



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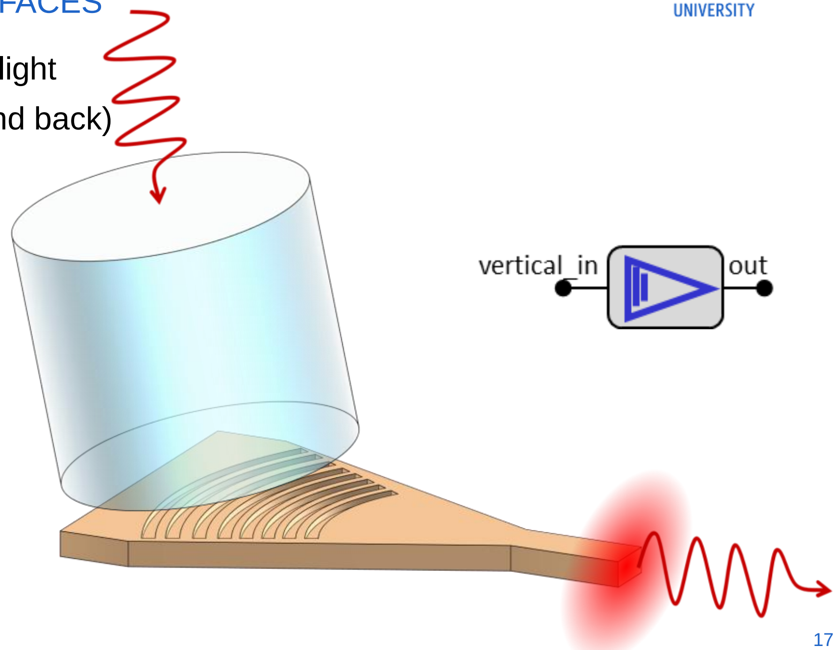
VERTICAL FIBER INTERFACES

Diffraction grating couples light from fiber to waveguide (and back)

- wavelength dependent



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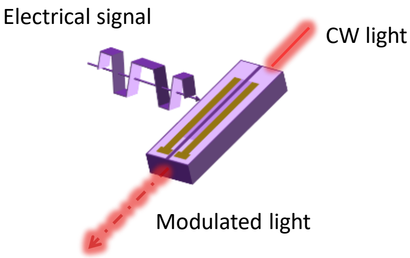
ELECTRICAL MODULATION



Electrical actuation: Switching and modulation

- Thermal
- Carrier injection/extraction
- Electro-optics

Different applications:

- Tuning: slow, analog
- Switching: slow, digital (<kHz), full amplitude
- Signal modulation: fast (GHz – 100GHz)
  - amplitude
  - phase

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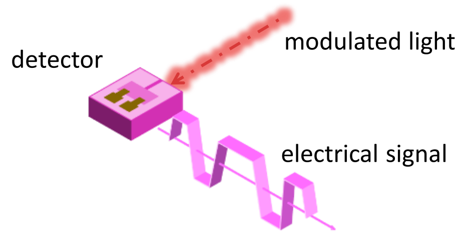
PHOTODETECTION



Mechanisms

- **photodiodes**: absorbed photon creates electron-hole pair.
  - p-i-n diode
  - metal-semiconductor-metal diode
- **photoconductors**: absorbed photon creates free carriers
- **photobolometers**: absorbed photon heats material, which then changes electrical resistivity

Examples

- III-V semiconductors (visible, telecom, MIR)
- Germanium (telecom)
- Silicon (visible, NIR)

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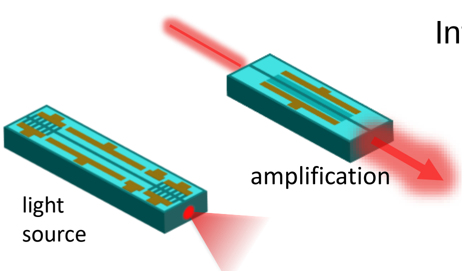
LASERS AND AMPLIFIERS



Introducing optical gain on a PIC

- semiconductors (III-V, Germanium) can be electrically pumped
- rare-earth (Erbium) can be incorporated in glass waveguides
- parametric gain (four wave mixing) requires nonlinear material

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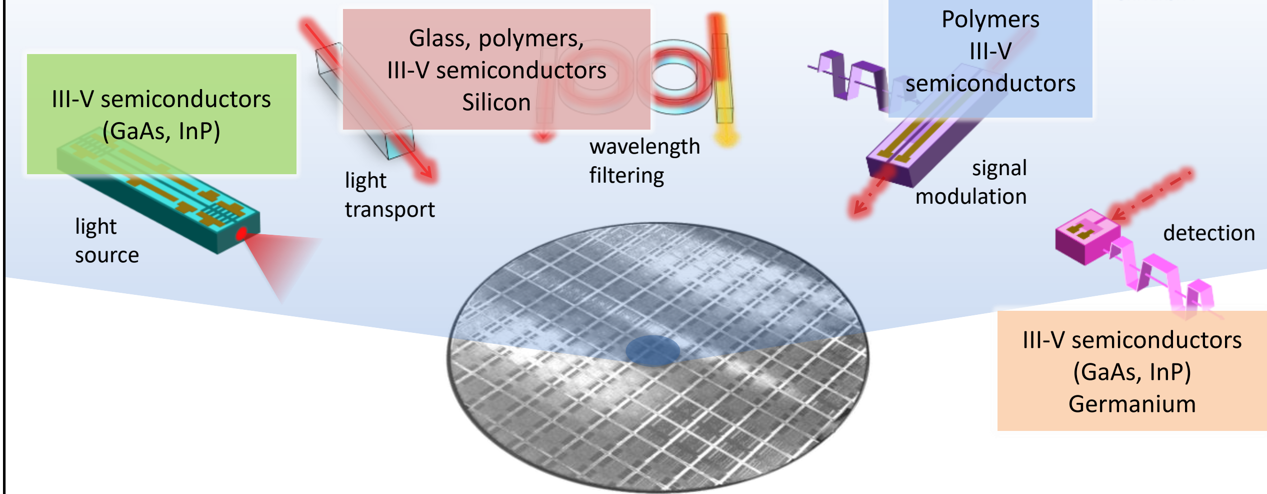
PHOTONIC INTEGRATION: A MIX OF MATERIALS



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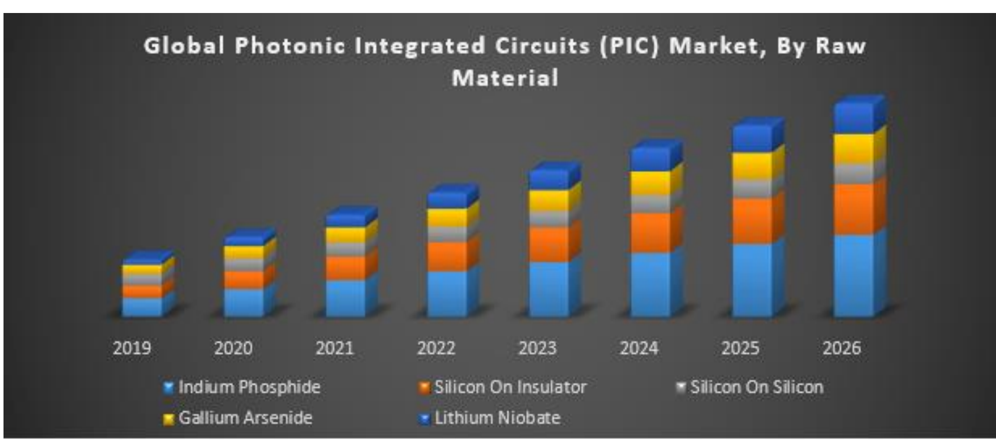
GROWING PHOTONIC CHIP MARKET

Different material systems



75% = semiconductor technology

source: maximizemarketresearch

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WHAT IS SPECIAL ABOUT "SILICON PHOTONICS"?

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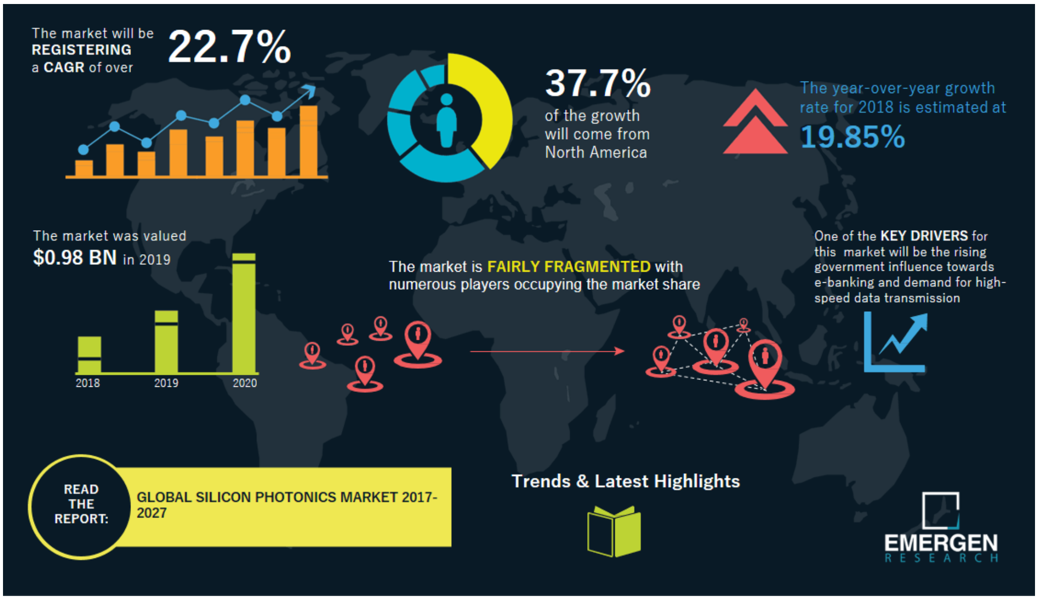

source: emergen research

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WHAT IS <u>SILICON</u> PHOTONICS?

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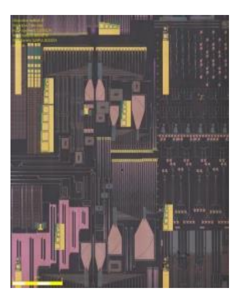
The implementation of <u>high density</u> photonic integrated circuits by means of CMOS process technology <u>in a CMOS fab</u>



Enabling complex optical functionality
on a compact chip at low cost

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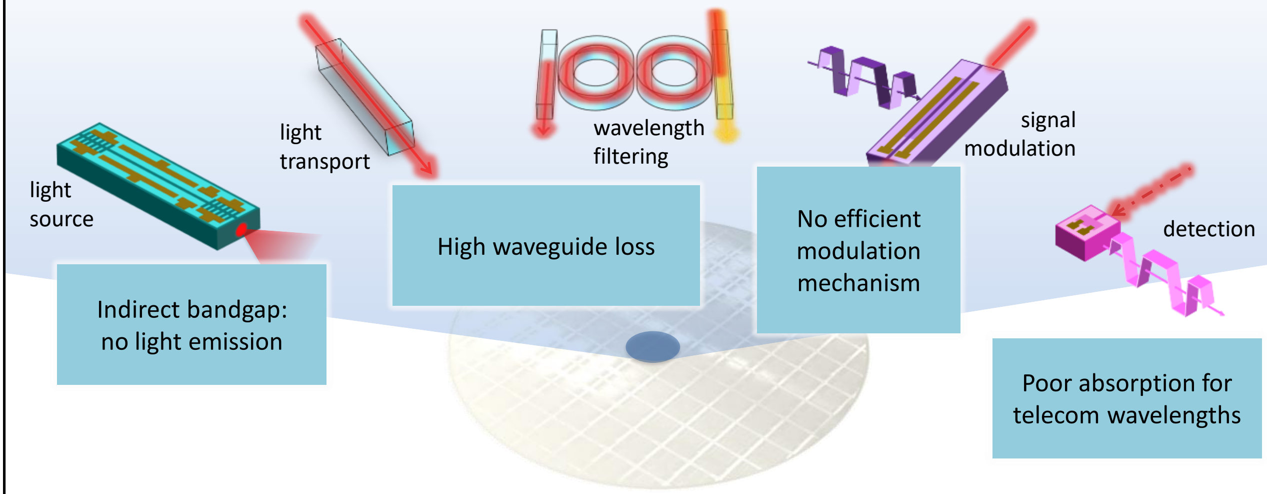
SILICON IS NOT A GOOD PHOTONIC MATERIAL



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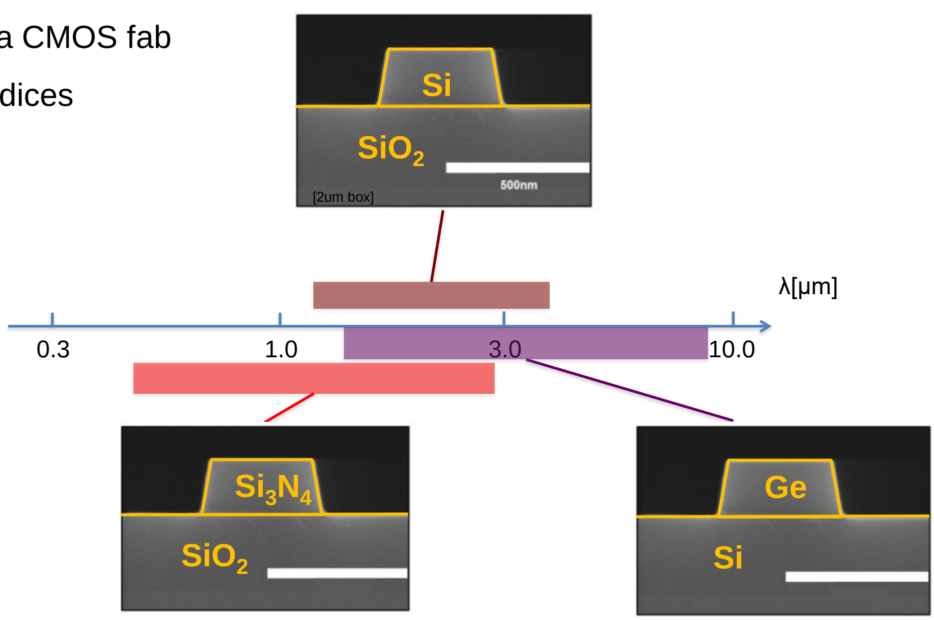
SILICON PHOTONICS: WAVELENGTHS AND MATERIALS

Compatible with a CMOS fab

High refractive indices



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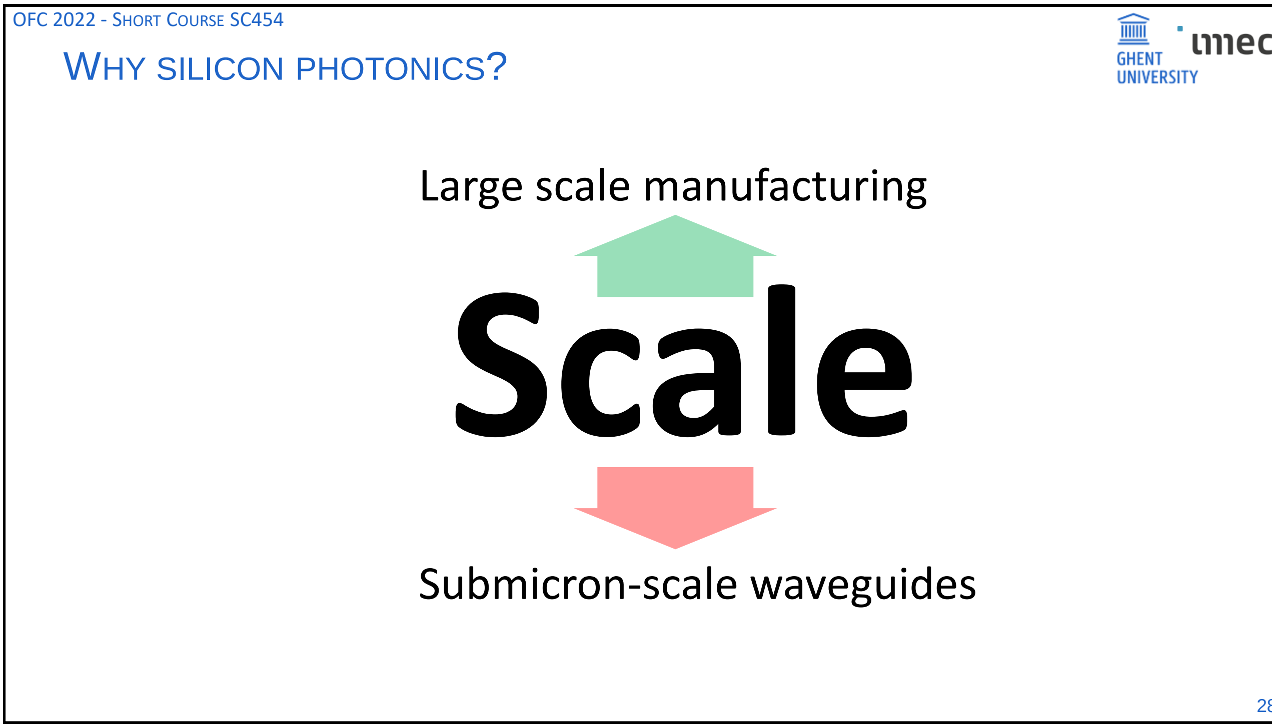
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Why silicon photonics?
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Large scale manufacturing
Scale
Submicron-scale waveguides
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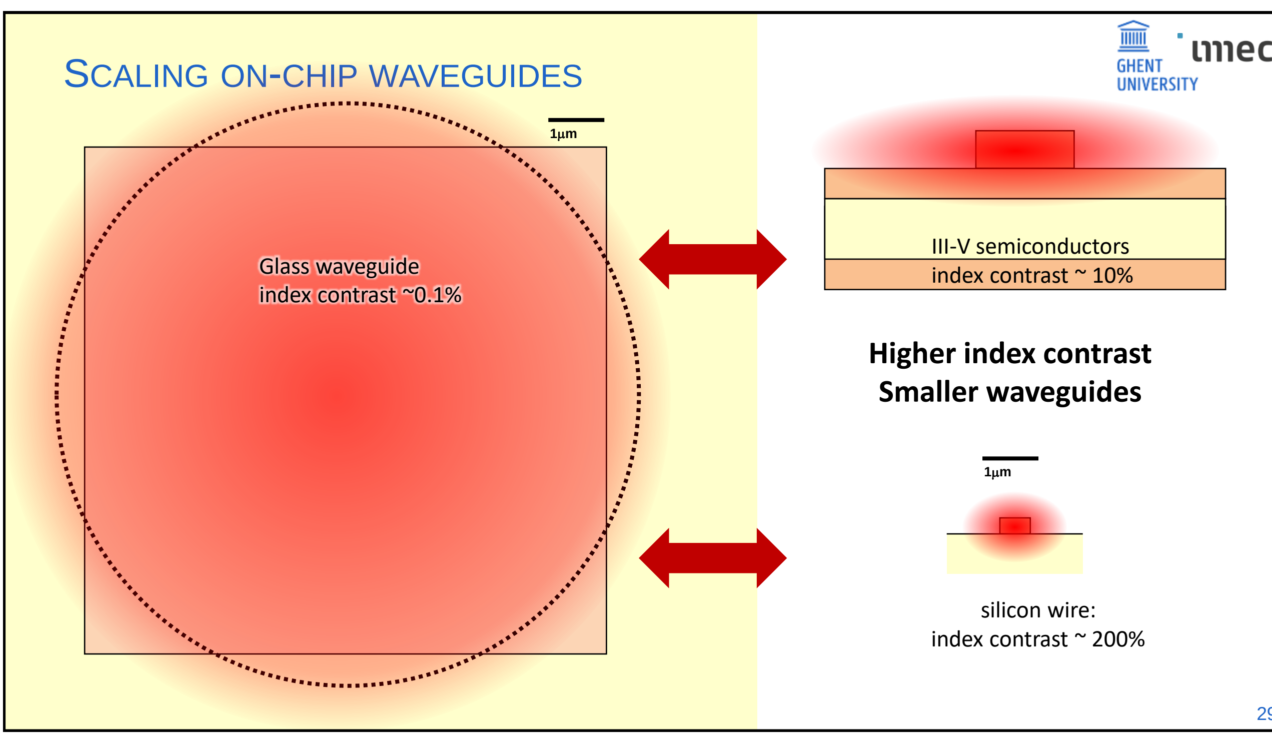
Scaling on-chip waveguides
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imec
1μm
Glass waveguide
index contrast ~0.1%
III-V semiconductors
index contrast ~ 10%
Higher index contrast
Smaller waveguides
1μm
silicon wire:
index contrast ~ 200%
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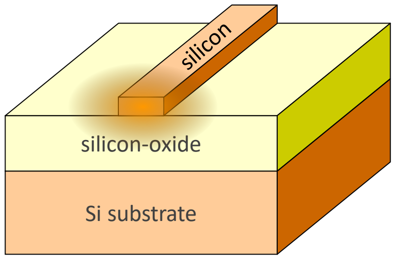
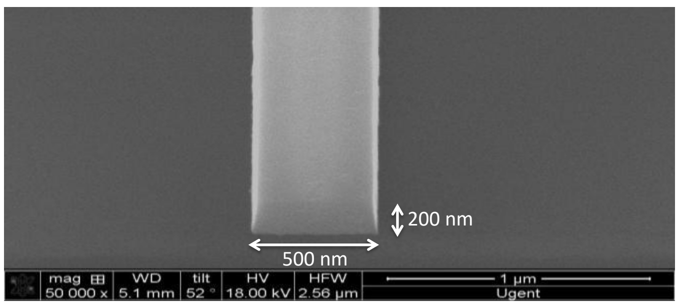
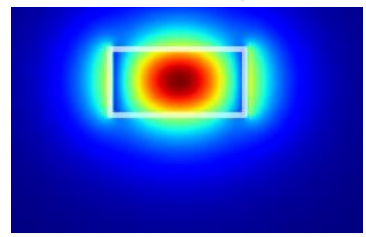
Silicon Photonic Waveguides



$$n_{core} = 3.45$$
$$n_{cladding} = 1.45$$

High intensity on sidewalls





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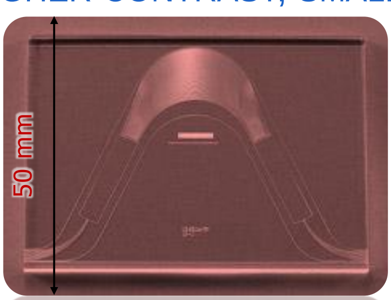
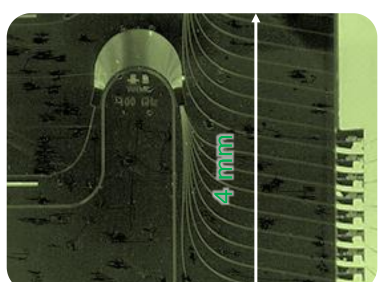
Higher Contrast, Smaller Cores, Tighter Bends



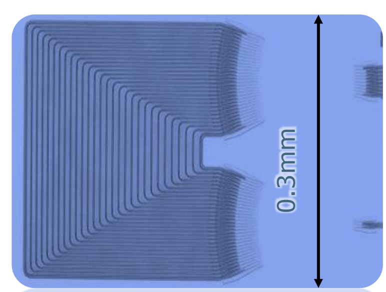
Silica on silicon

Contrast ~ 0.01 – 0.1
Mode diameter ~ 8µm
Bend radius ~ 5mm
Size ~ 10 cm²



Indium Phosphide

Contrast ~ 0.2 – 0.5
Mode diameter ~ 2µm
Bend radius ~ 0.5mm
Size ~ 10mm²



Silicon on insulator

Contrast ~ 1.0 – 2.5
Mode diameter ~ 0.4µm
Bend radius ~ 5µm
Size ~ 0.1mm²

10000 ×

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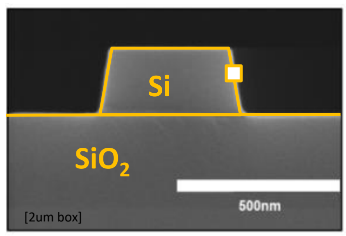
High index contrast: a blessing and a curse

Every nm^3 matters

CMOS technology is the only manufacturing technology with sufficient nm-process control to take advantage of the blessing without suffering from the curse



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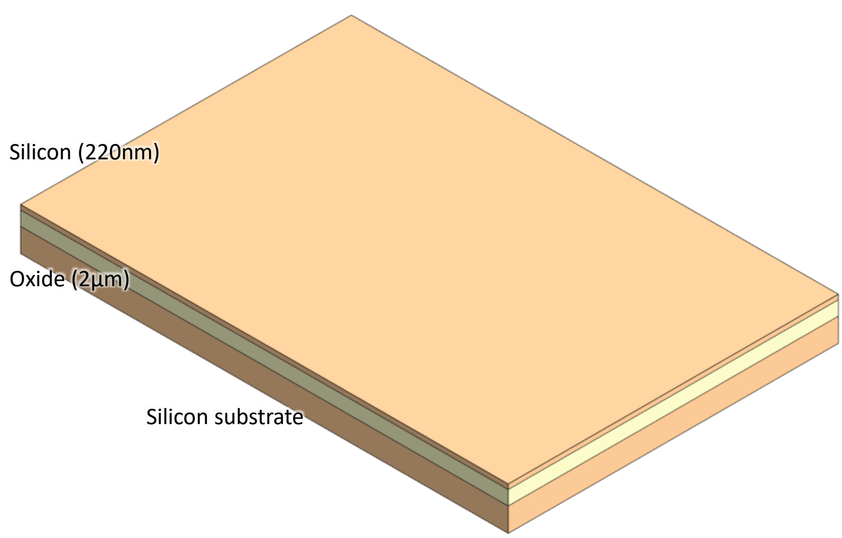
Bare Silicon-on-Insulator Wafer



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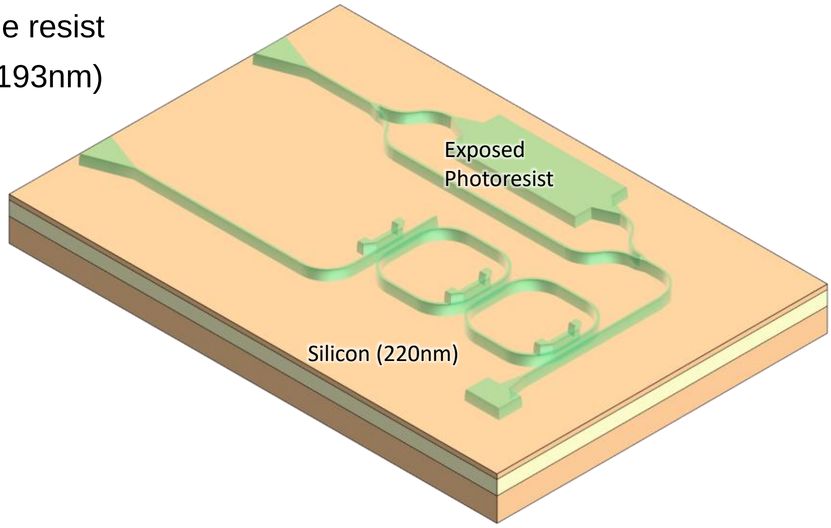
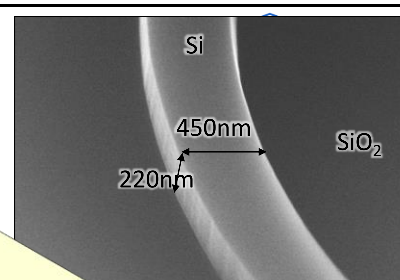
Photolithography

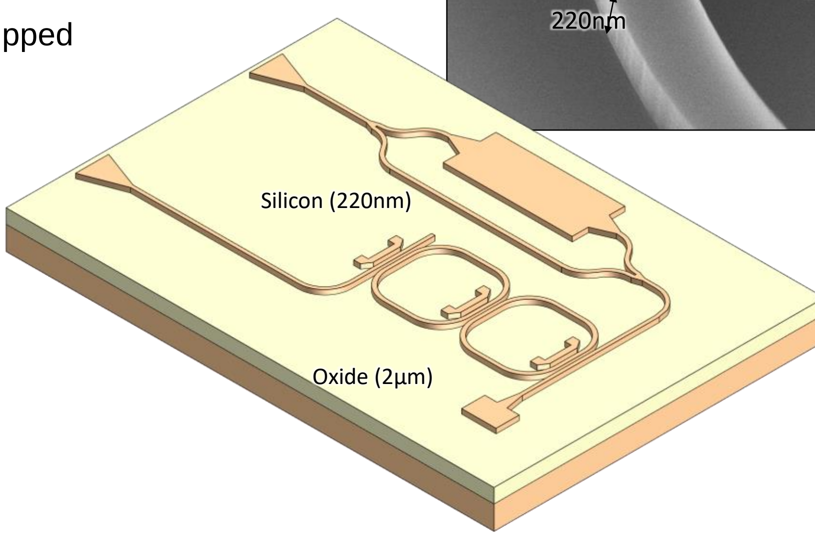
1. Spin-coat Photoresist + pre-bake
2. Mask is projected in the resist
   (UV light at 248nm or 193nm)
3. Post-Exposure bake
4. Resist is developed



Silicon Etching

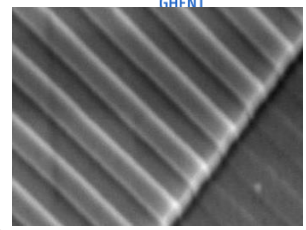
1. Plasma etches the exposed silicon
2. Remaining resist is stripped

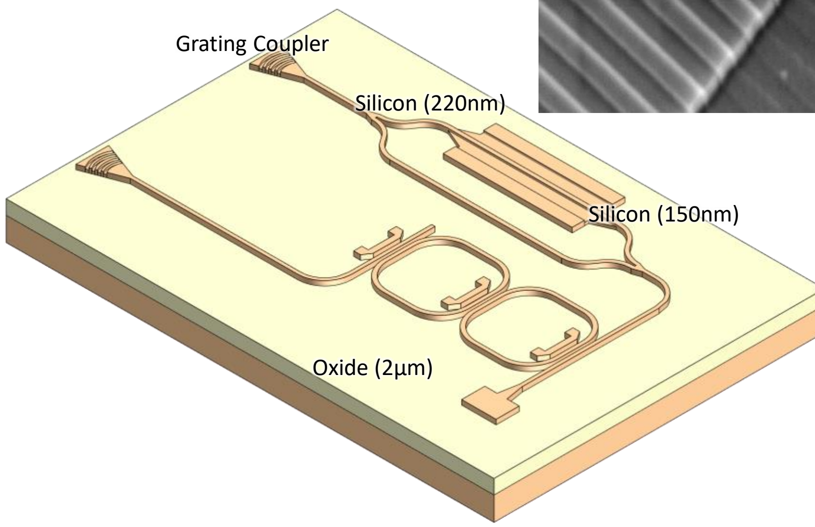




Partial Silicon Etching

1. Lithography of second layer
2. Plasma etching
3. Resist Stripping





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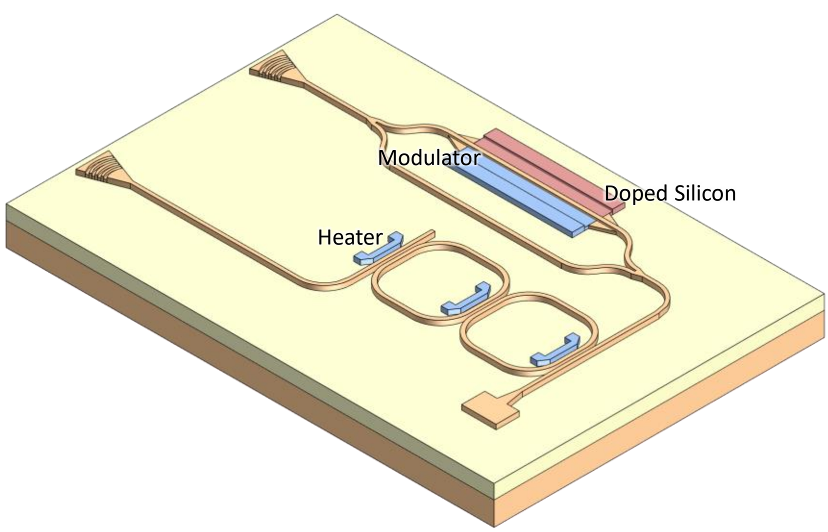
Doped regions for Modulators and Heaters

1. Lithography of windows
2. Ion implantation
3. Resist Stripping



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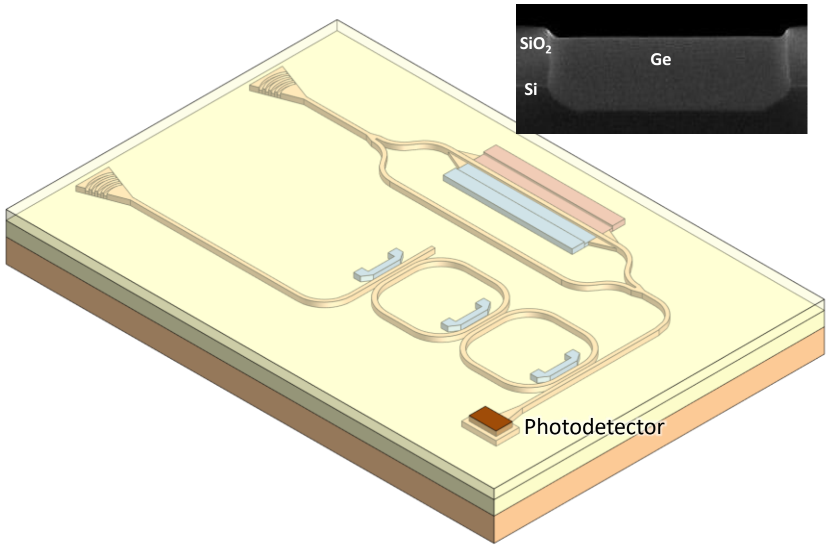
GERMANIUM PHOTODETECTORS

1. Oxide cladding
2. Planarization (CMP)
3. Opening of window
4. Epitaxial Growth of Ge
5. Planarization (CMP)



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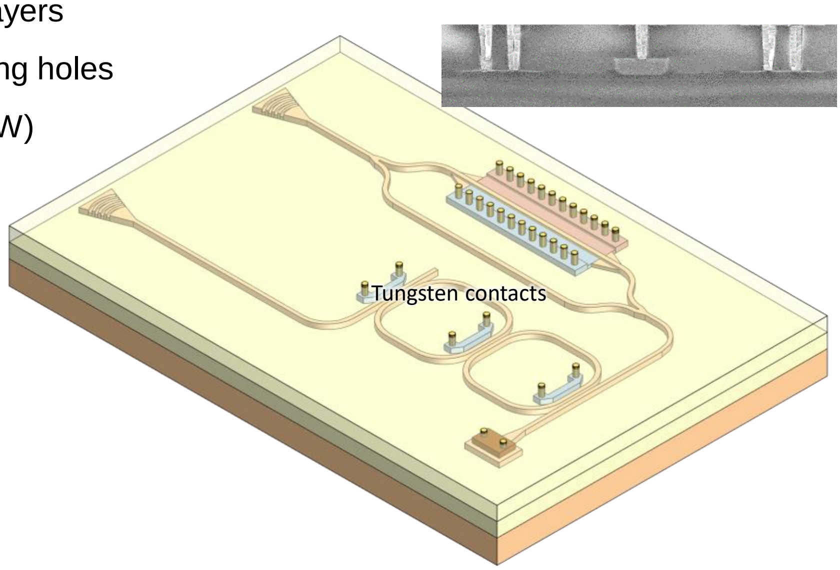
ELECTRICAL CONTACTS: DAMASCENE PROCESS

1. Depositing dielectric layers
2. Lithography and Etching holes
3. Filling with Tungsten (W)
4. Planarization (CMP)



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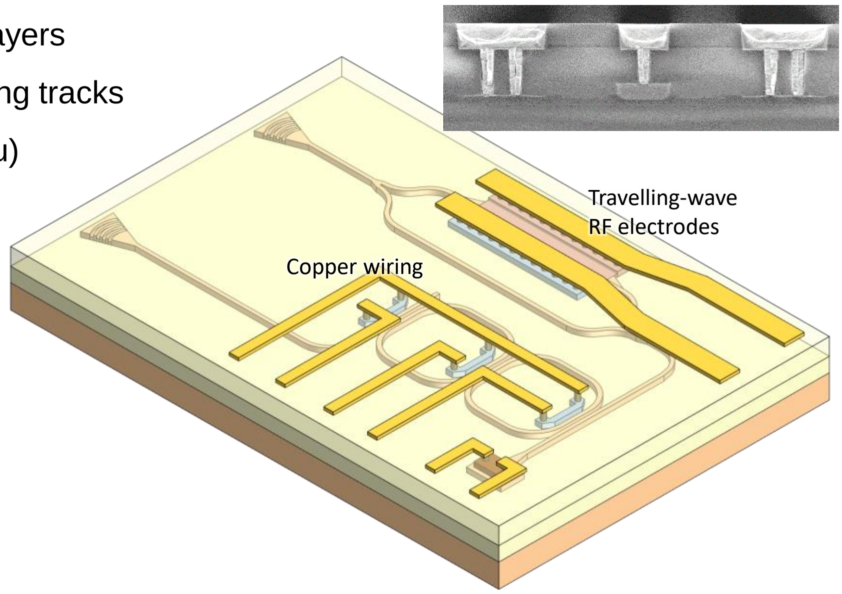
Metal Interconnects: Damascene process

1. Depositing dielectric layers
2. Lithography and Etching tracks
3. Filling with Copper (Cu)
4. Planarization (CMP)

Repeat for more layers



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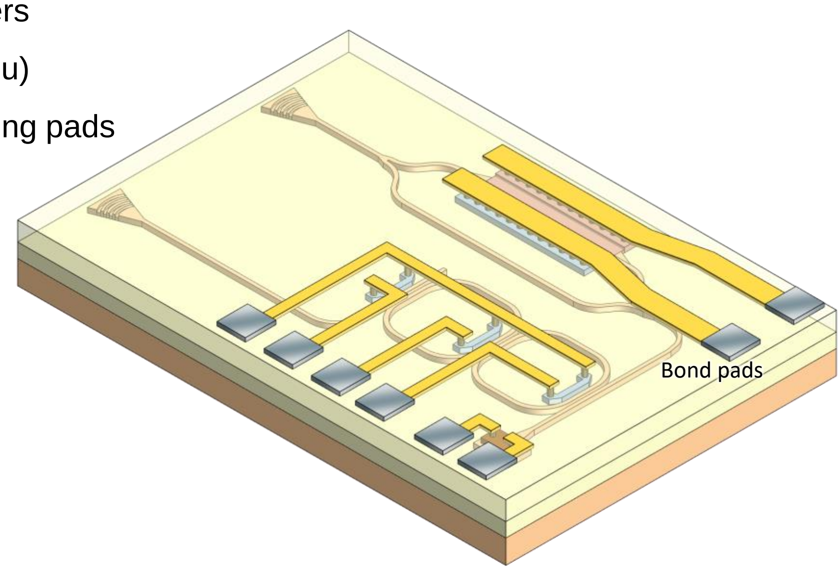
Metal Bondpads

1. Deposit dielectric layers
2. Depositing Metal (AlCu)
3. Lithography and Etching pads



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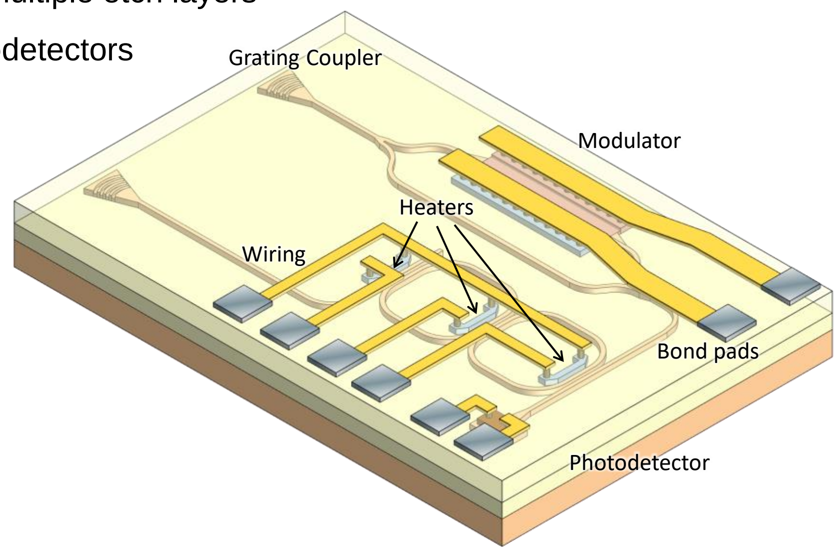
Silicon Photonics Chips

1. Passive circuits with multiple etch layers
2. Modulators and Photodetectors
3. Metal wiring



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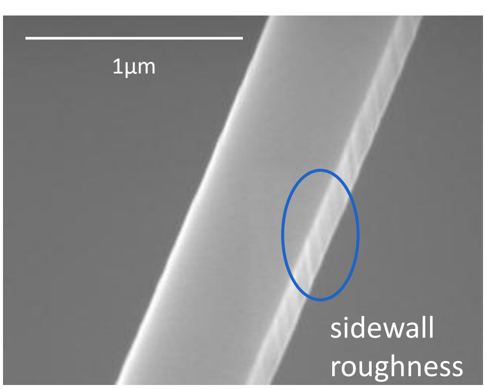
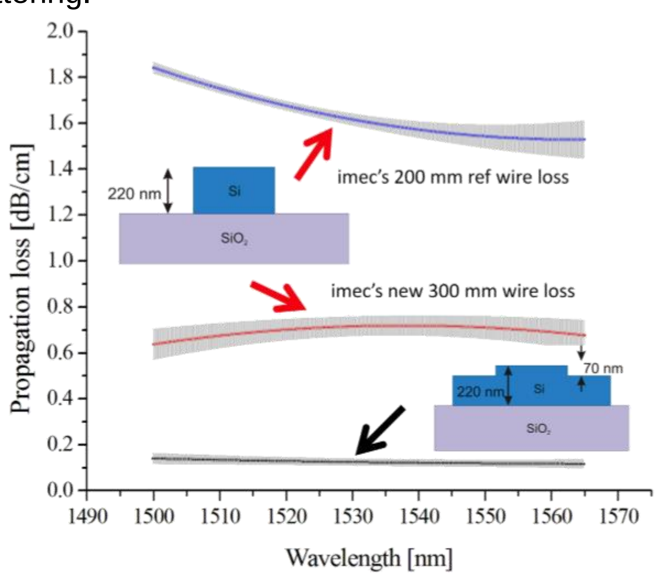
Waveguides

Waveguide losses dominated by scattering.

Use better litho + etch





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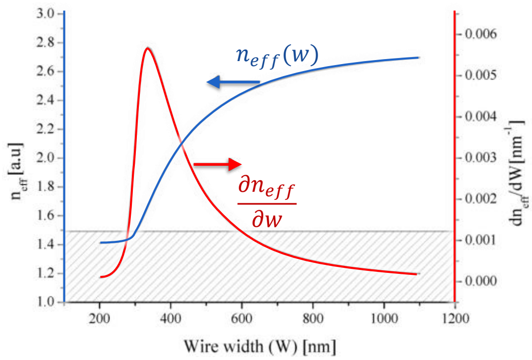
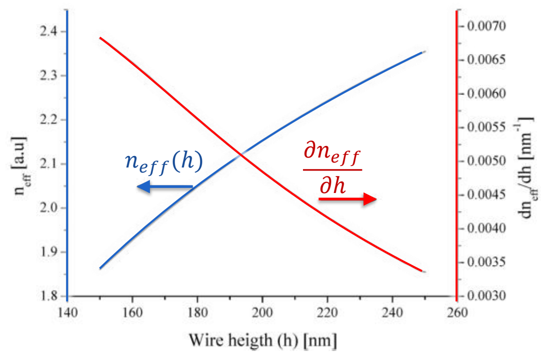
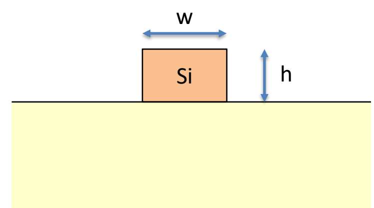
DIMENSIONAL DEPENDENCE OF A WAVEGUIDE







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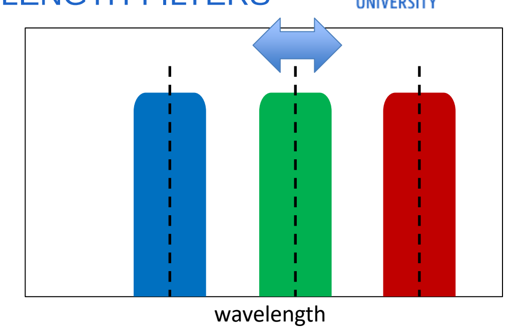
SENSITIVITY OF SILICON PHOTONICS WAVELENGTH FILTERS

Especially wavelength filters are sensitive:

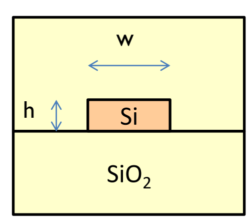
- geometry
- stress
- temperature



wire width $\frac{\partial \lambda}{\partial w} \approx 1\, {}^{nm}/_{nm}$

wire height $\frac{\partial \lambda}{\partial h} \approx 2\, {}^{nm}/_{nm}$

temperature $\frac{\partial \lambda}{\partial T} \approx 0.08\, {}^{nm}/_{K}$



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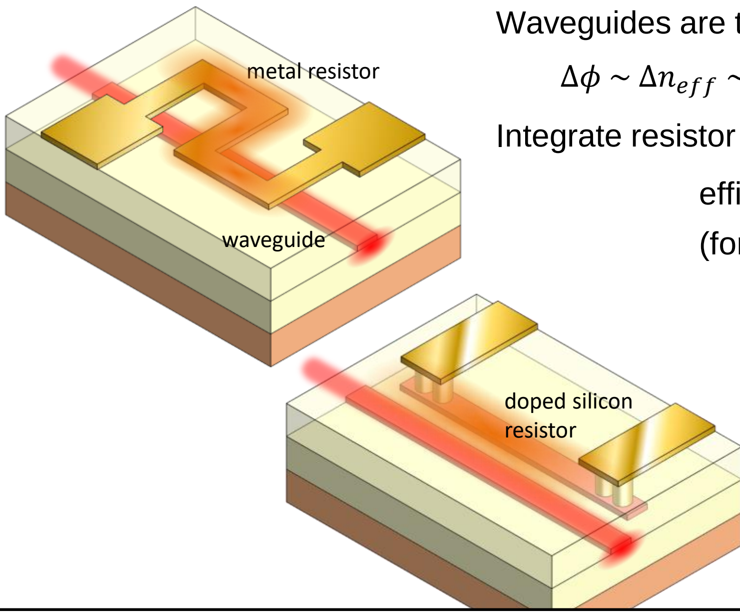
THE BASIC OPTICAL PHASE SHIFTER: A HEATER



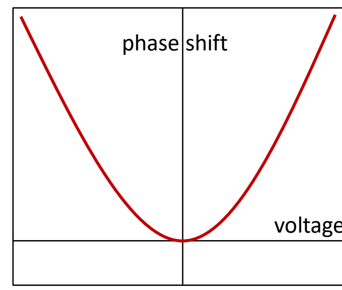
Waveguides are thermally sensitive:

$$\Delta\phi \sim \Delta n_{eff} \sim T \sim P_{elec} \sim V^2 \sim I^2$$

Integrate resistor close to the waveguide

efficiency: $P_\pi \approx 5 - 30mW$

(for silicon waveguides)



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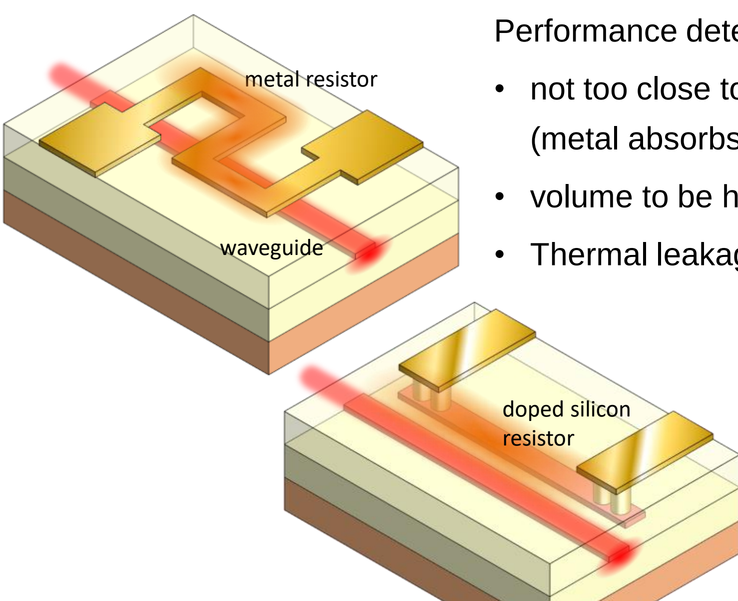
THE BASIC OPTICAL PHASE SHIFTER: A HEATER



Performance determined by geometry

- not too close to waveguide (metal absorbs)
- volume to be heated (thermal mass)
- Thermal leakage paths

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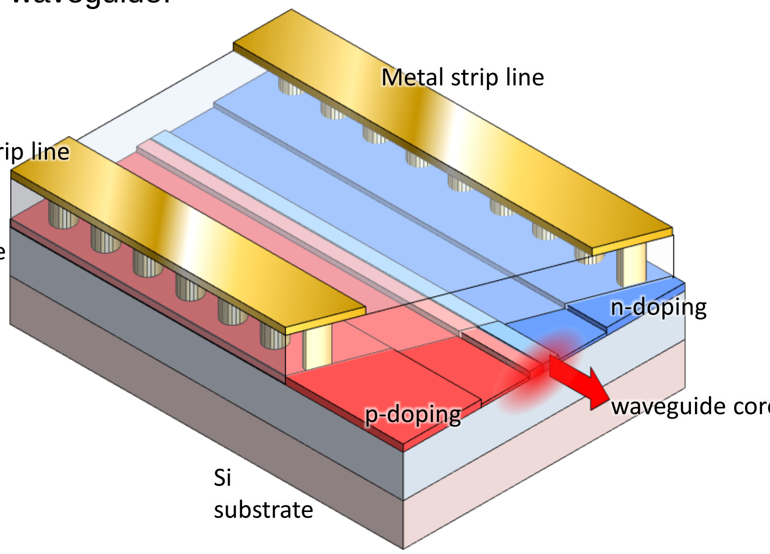
ELECTRICAL SIGNAL MODULATION

Add doped junction to silicon waveguide: modulate refractive index



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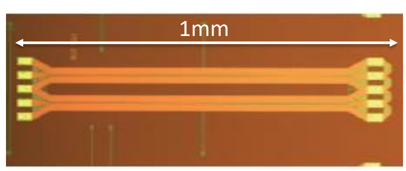
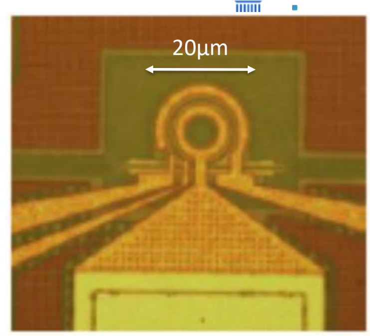
ELECTRICAL SIGNAL MODULATION

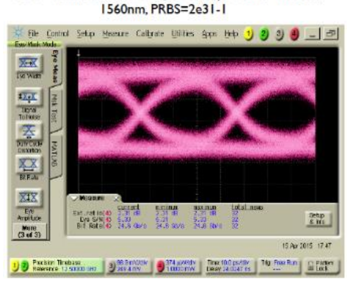
Add doped junction to silicon waveguide: modulate refractive index

- travelling wave modulator
- ring resonator modulator

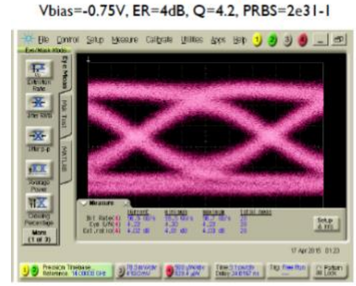




25Gb/s, 1Vpp
Vbias= -0.2V, ER = 2.3dB, Q = 5.3, Opt. Power=13dbm, 1560nm, PRBS=2e31-1



56Gb/s, 2.5Vpp
Vbias=-0.75V, ER=4dB, Q=4.2, PRBS=2e31-1



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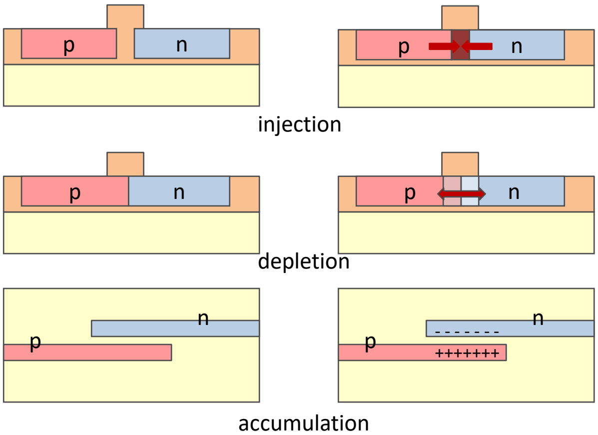
Carrier-based modulation



Refractive-index of semiconductors depends on local carrier density

Modulate carrier density in waveguide

- phase modulation
- (spurious) amplitude modulation (free carrier absorption)

Modulation mechanisms

- carrier injection (in pin diode) speed limited by carrier recombination (~GHz)
- carrier depletion (in pn diode) speed limited by RC constant
- carrier accumulation (in capacitor) speed limited by RC constant

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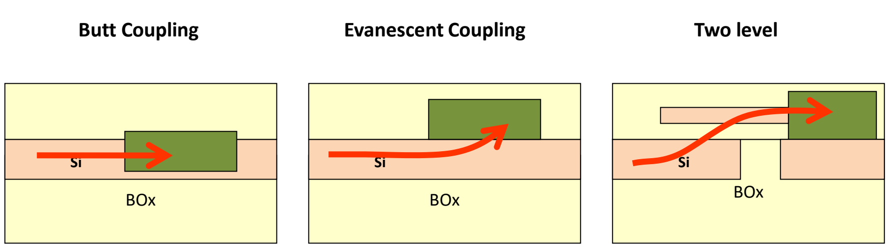
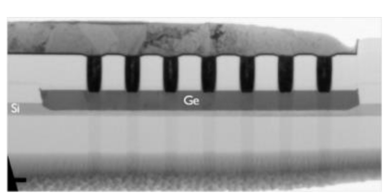
Ge-detectors coupling from silicon waveguides





Relevant parameters

- Responsivity (A/W)
- Bandwidth (GHz)
- Dark current (nA)

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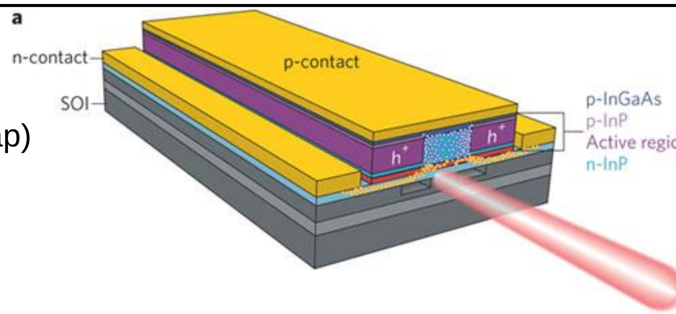
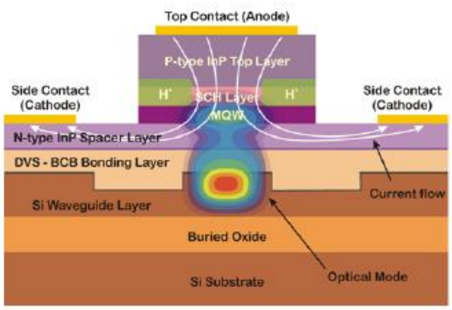
III-V LASERS ON SILICON

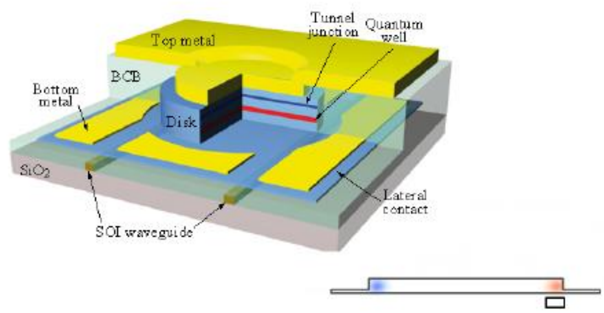
Silicon does not emit (indirect bandgap)

Bonding of III-V layer stack on silicon

Careful engineering of the transitions







source: UCSB, UGent

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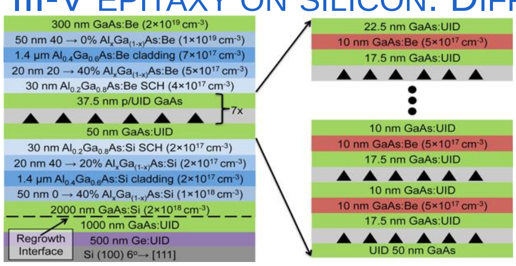
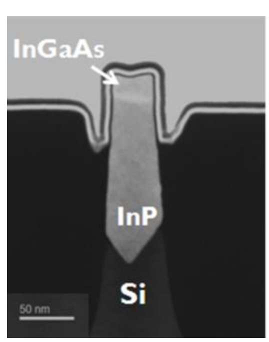
III-V EPITAXY ON SILICON: DIFFICULT





Challengin

- lattice constant mismatch
- polar vs. apolar material

Solutions:

- Thick buffer layers
- high aspect ratio growth
- quantum dots

First lasing demonstrated (optically pumped)

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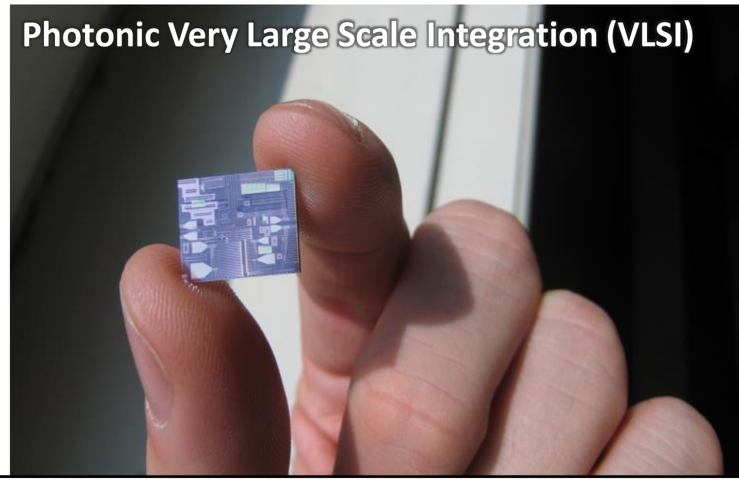
Small building blocks → Large circuits

µm-scale building blocks

cm-scale chips

→ thousands – millions components



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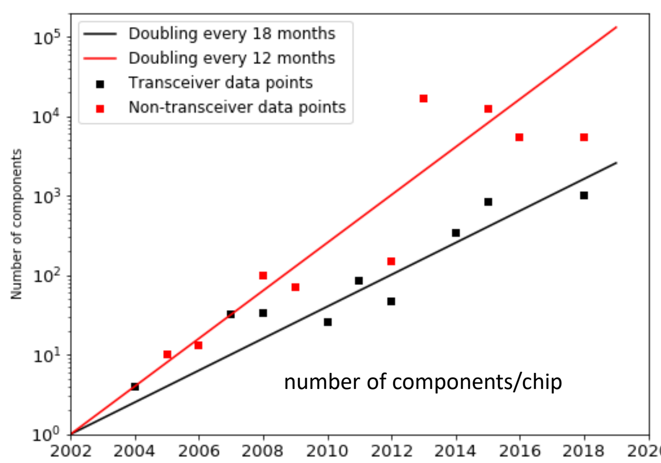
Silicon Photonic Circuit Scaling

Rapidly growing integration

- O(1000) components on a chip
- photonics + electronic drivers
- different applications (mostly comms)
- Relatively small chip volumes (compared to electronics)



All photonic circuits are ASICs

Khanna et al. 2016

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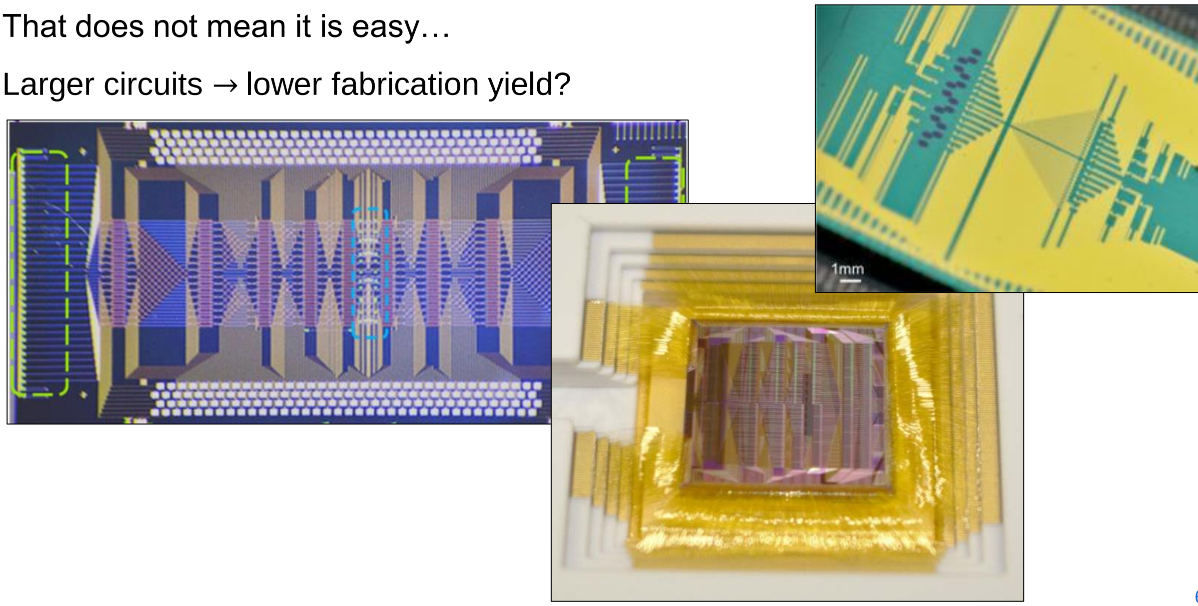
Photonic Large-scale integration is here

That does not mean it is easy…

Larger circuits → lower fabrication yield?



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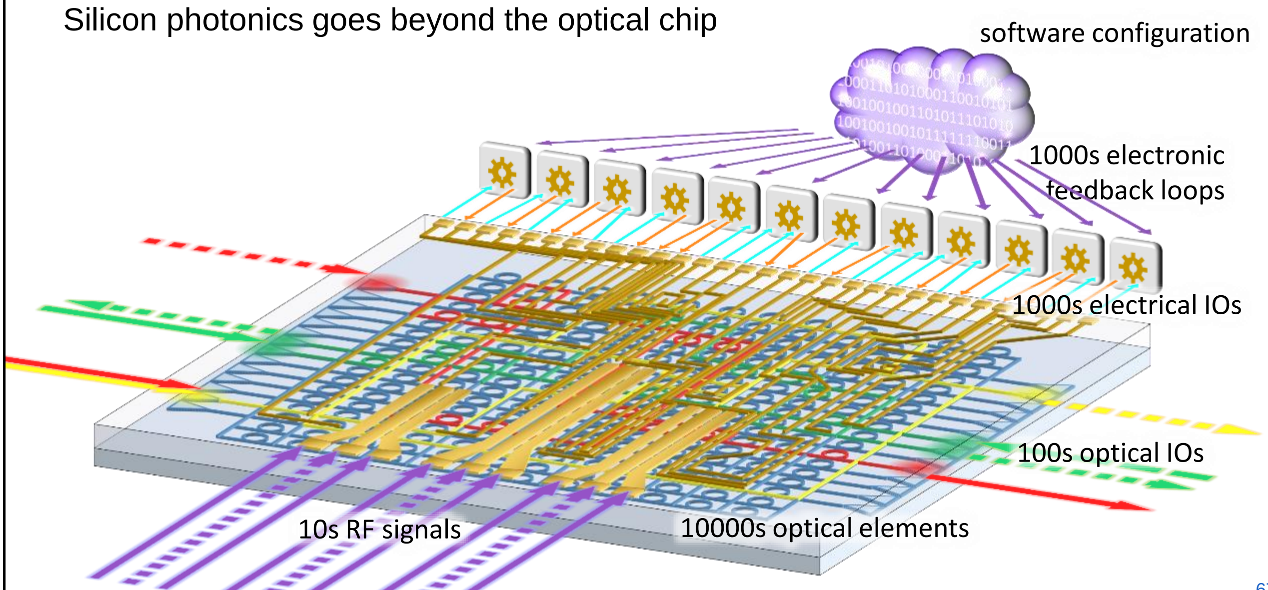
More than just photons

Silicon photonics goes beyond the optical chip



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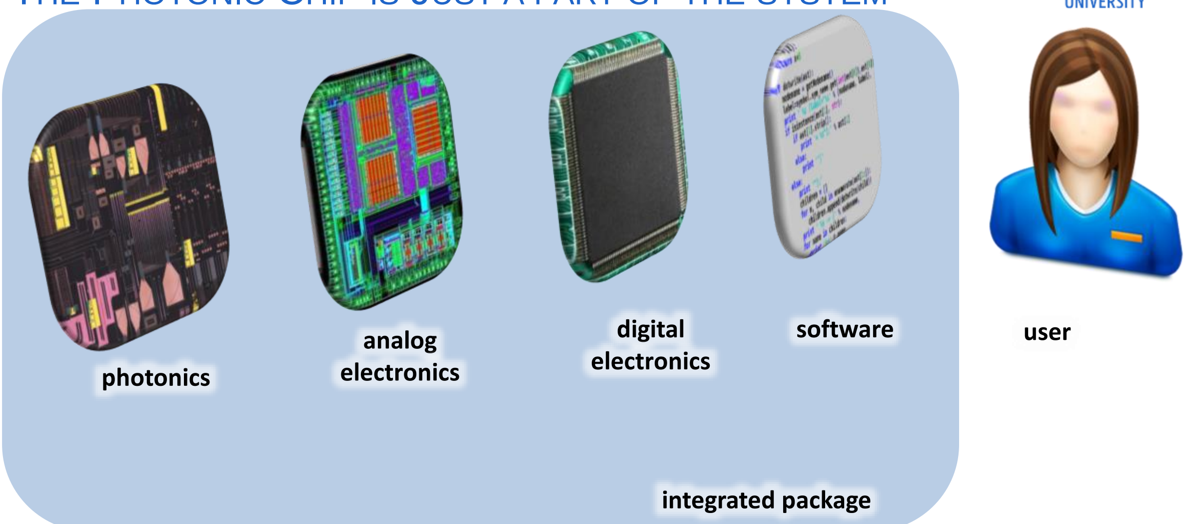
THE PHOTONIC CHIP IS JUST A PART OF THE SYSTEM



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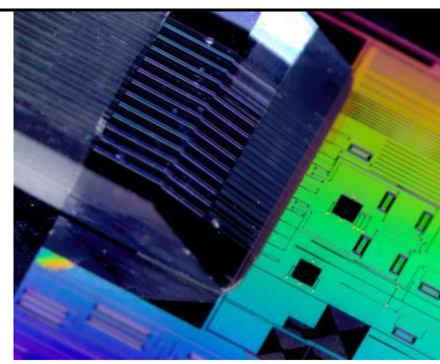
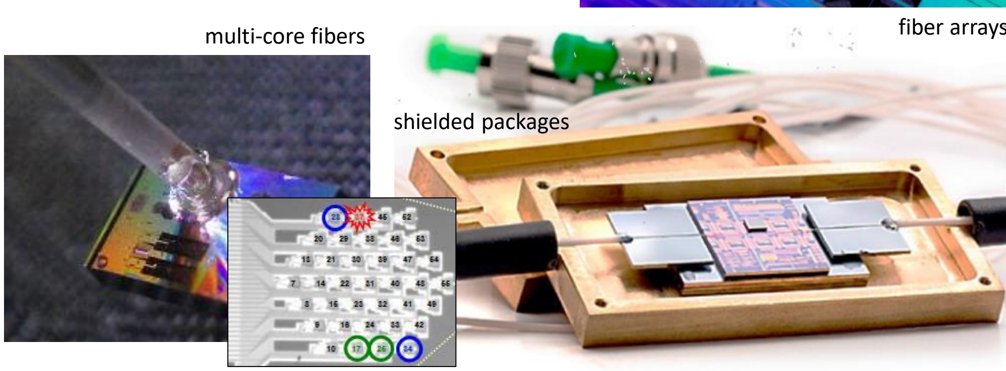
PACKAGING TECHNOLOGY

- Combining photonics and electronics
- Fiber interfaces
- RF connections
- Thermal and mechanical





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Fabless Silicon Photonics

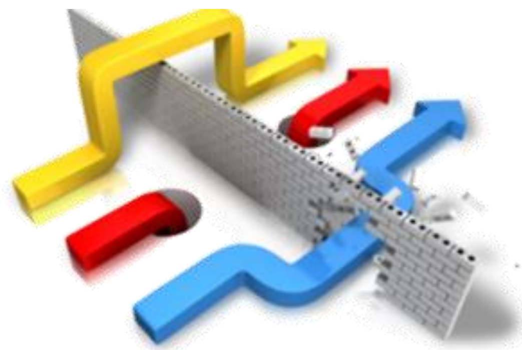
Many fabless Silicon Photonics companies have emerged

- from direct collaboration with fabs (Luxtera, ...)
- starting from MPW (Caliopa, Genalyte, Acacia)

Established players are also partnering

- e.g. Finisar with ST
- Many keep their fab a secret

How to enter as a new (fabless) startup?



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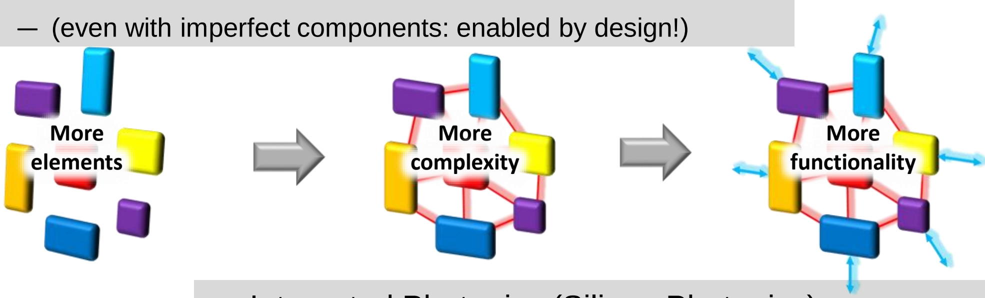
Complexity as an Enabler

Integrated Electronics

- billions of digital gates: unprecedented logic performance
- millions of analog transistors: unprecedented control

— (even with imperfect components: enabled by design!)



Integrated Photonics (Silicon Photonics)

- **technological potential** of 10000+ photonic elements on a chip
- not even scratched the surface of what this could do

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Photonic Circuit Design

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Enabling complexity in Photonics

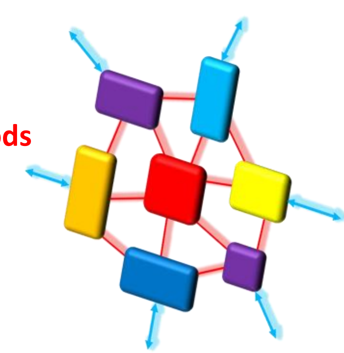
Industrial PIC technology platforms (Si, InP, …)

- demonstrations of sensors, spectrometers, …
- commercial products

But: fairly simple circuits ~ 1970s ICs

More complexity is enabled by design methods

- Design capture: translating ideas to circuits
- Circuit simulation (electrical+photonic)
- Variability analysis on circuits
- Yield prediction and improvement



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COMPLEX CIRCUITS ≠ COMPLICATED BUILDING BLOCKS

You can do a lot with a few building blocks

Electronics: Transistors, Resistors, Diodes, …
Photonics: Waveguides, Directional couplers, …

Complexity emerges from connectivity

But you need to support complexity

- Accurate models
- Variability
- Parasitics

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DESIGNING PHOTONIC INTEGRATED CIRCUITS

Can we learn from electronic ICs?

- Millions of analog transistors
- Billions of digital transistors
- Power, timing and yield
- **First time right designs**

- Very mature Electronic Design Automation (EDA) tools!
- A well established design flow

Can we repurpose this for photonics?

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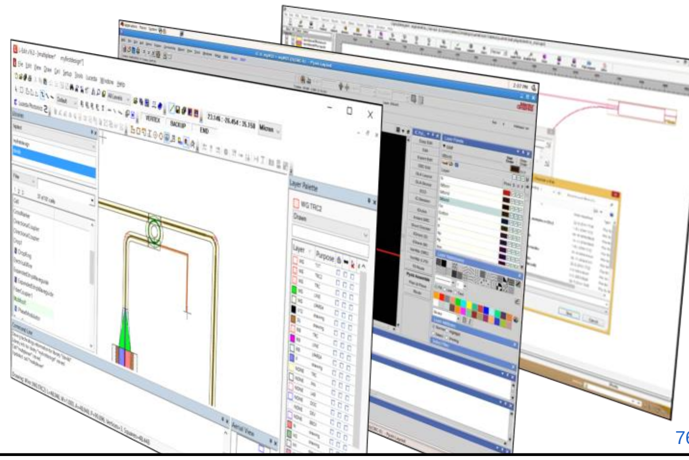
Design Environments are Emerging

Combinations of Photonics Design and EDA

Physical simulation combined with circuit design

Physical and functional verification

First PDKs with basic models



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What is a design flow?

“Design is the creation of a plan or convention for the construction of an object or a system”

Design Flow

“a repeatable pattern of activity, usually involving multiple tasks with a specific set of outcomes”

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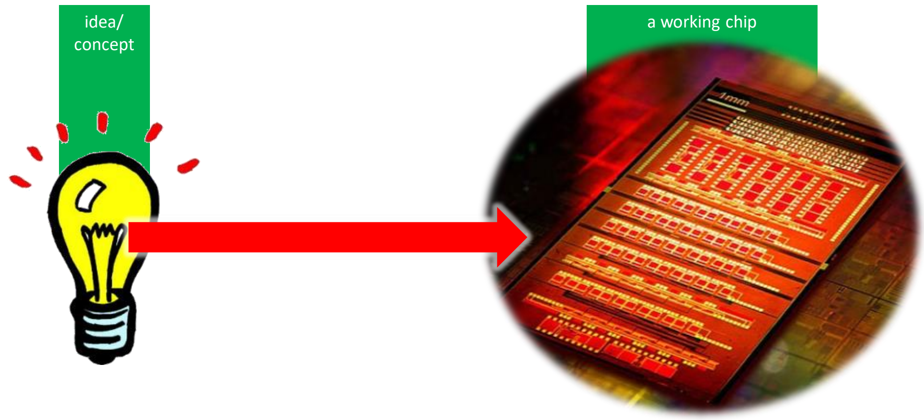
What is the purpose of a design flow?



to translate an idea into a **WORKING** chip.

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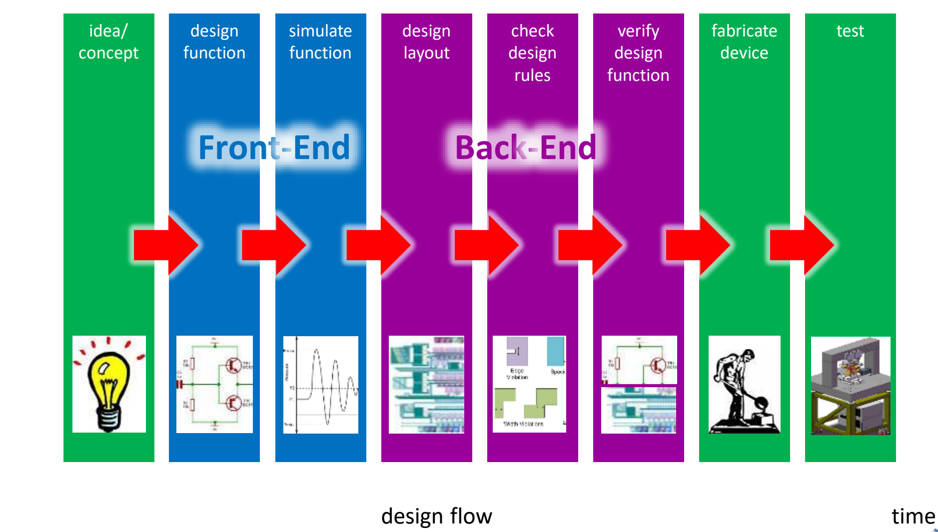
A typical design cycle



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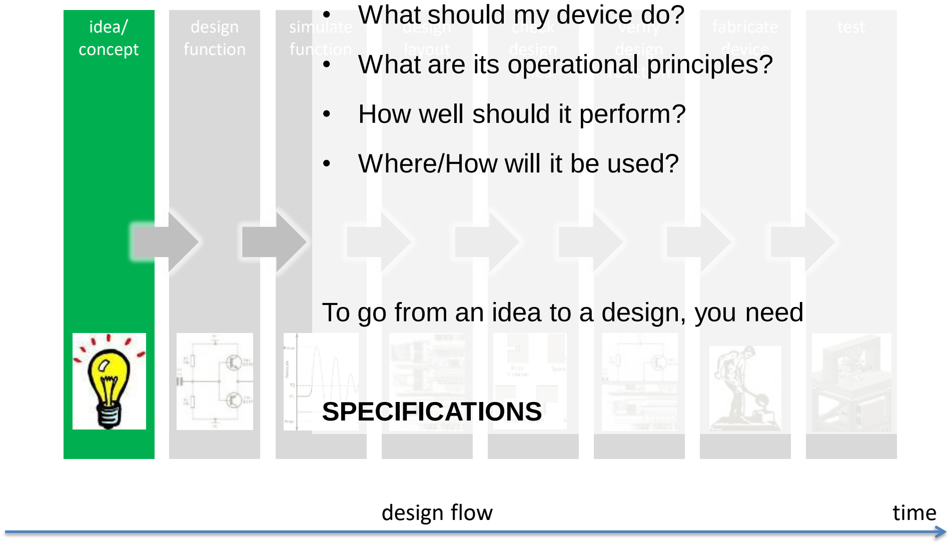
A GREAT IDEA?

Questions to be asked

- What should my device do?
- What are its operational principles?
- How well should it perform?
- Where/How will it be used?



To go from an idea to a design, you need

SPECIFICATIONS

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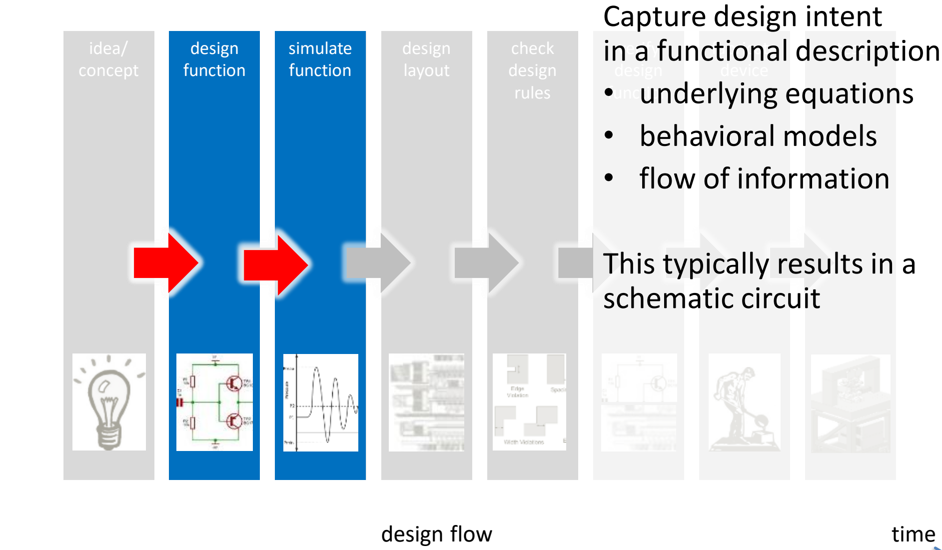
DESIGN CAPTURE AND SIMULATION



Capture design intent
in a functional description

- underlying equations
- behavioral models
- flow of information

This typically results in a schematic circuit

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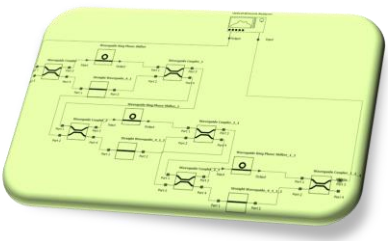
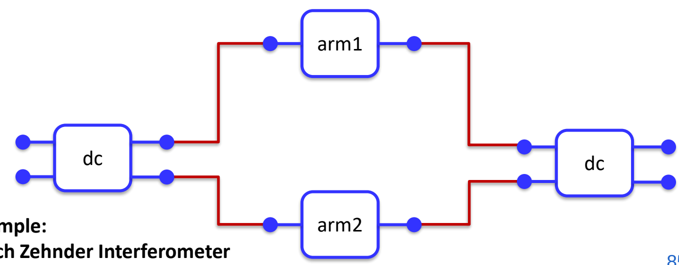


DESIGN CAPTURE

Select/construct functional blocks

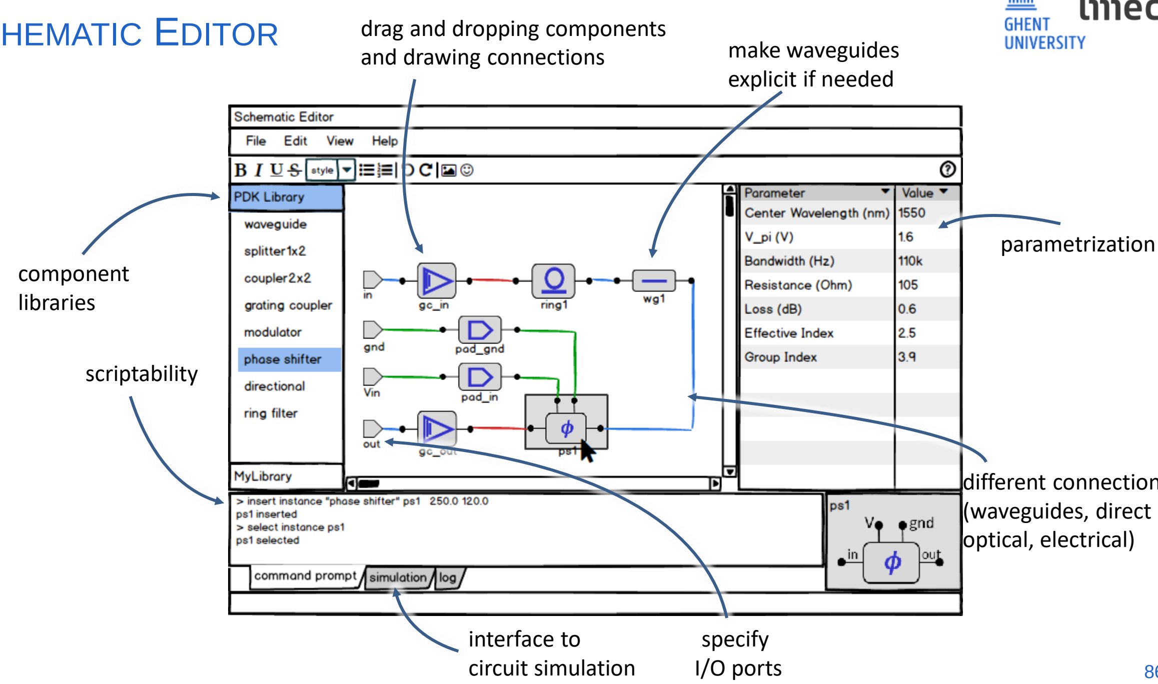
Connect them together

- **Netlist**:
  list of connections ("Nets") and which components the nets are attached to.
- **Schematic**:
  graphical representation of a netlist, with placements



Example:
Mach Zehnder Interferometer

SCHEMATIC EDITOR



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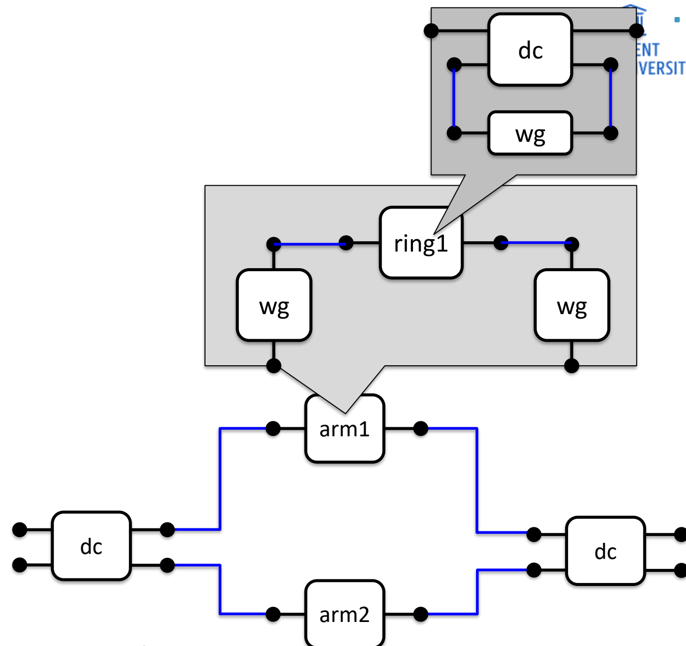
HIERARCHY

Netlists are hierarchical

- Hierarchical cells:
  contain another netlist
- Atomic cells:
  contain a circuit model



Example:
Ring-Loaded Mach Zehnder Interferometer

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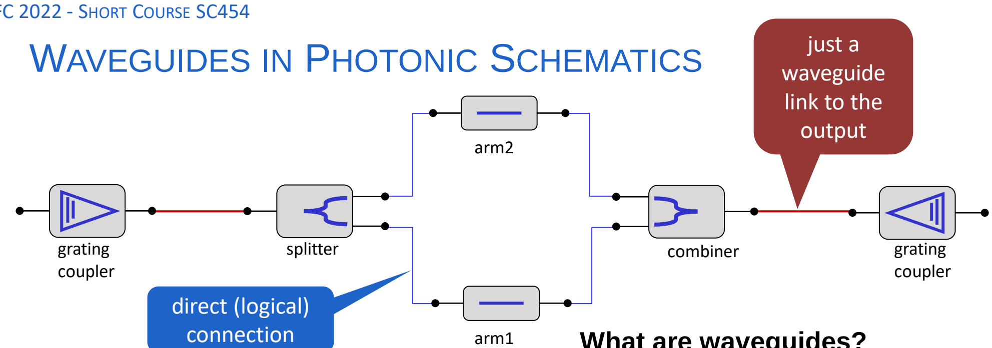
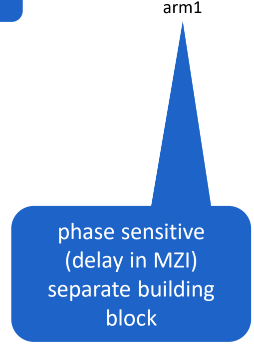
WAVEGUIDES IN PHOTONIC SCHEMATICS





What are waveguides?
Simple connections between building blocks

- the length and shape does not really matter
- it should just provide a good connection
- similar as an electrical wire

Functional blocks with a certain phase/time delay

- length and shape are very important
- should be treated as a building block

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Models for Circuit Simulation

Should allow simulation in a larger circuit

- based on equations
- based on measurement data
- based on EM simulations

Photonics: Nothing really standardized

- No standardized simulation method
- No standard model description
- No standard signals

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A Good Circuit Model

- Maps input signals correctly to output signals
- In frequency domain and time domain
- Is efficient (for circuit simulations)
- Has meaningful parameters
- Can be extracted from measurements

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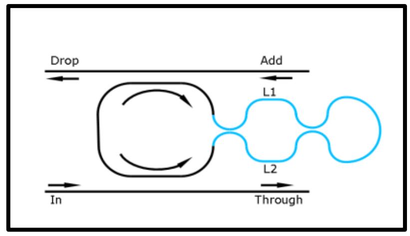
BLACK-BOX VS. WHITE-BOX MODEL

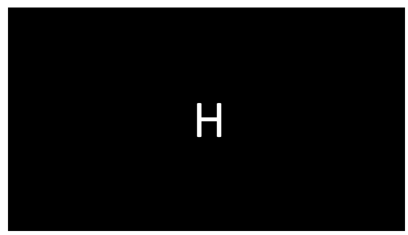
White-box:

- knows the circuit
- captures the physics

$S_{in}(t)$ →  → $S_{out}(t)$

Black-box:

- internals unknown
- mathematical 'fit'

$S_{in}(t)$ →  → $S_{out}(t)$

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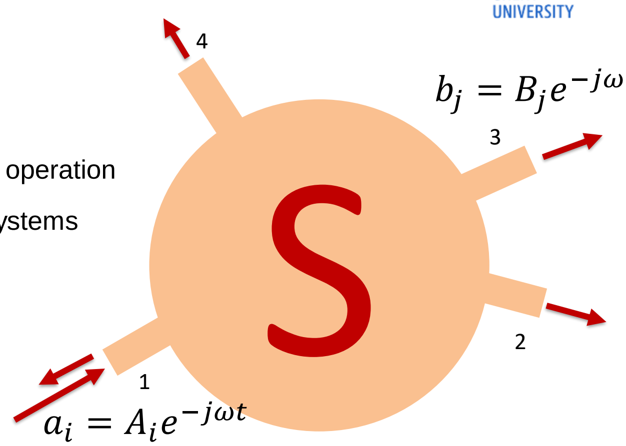
OPTICAL CIRCUIT SIMULATION

Generalized scattering of an incoming wave

- Calculates one wavelength at a time
- gets response between all ports in one operation
- Can only model linear, time-invariant systems



$S_{21}(\omega)$

out in frequency (wavelength) dependent

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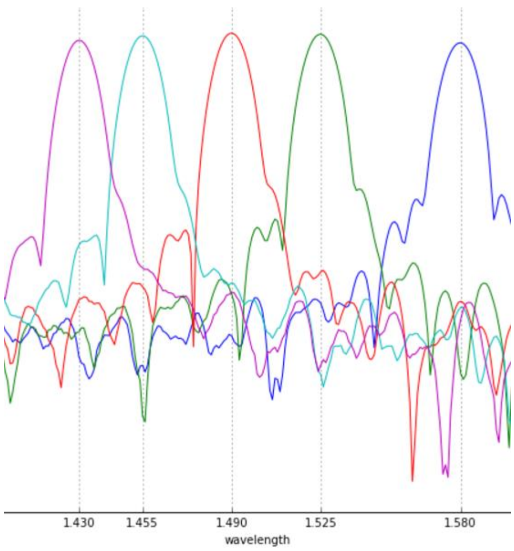
Frequency Domain Simulations



Frequency domain simulations are very useful for calculating

- Insertion losses
- Backreflections
- Dispersion (wavelength dependence)
- Wavelength filter response

and can also be extended to model

- Slowly varying effects
- Certain optical nonlinearities

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What is a port of a waveguide component?

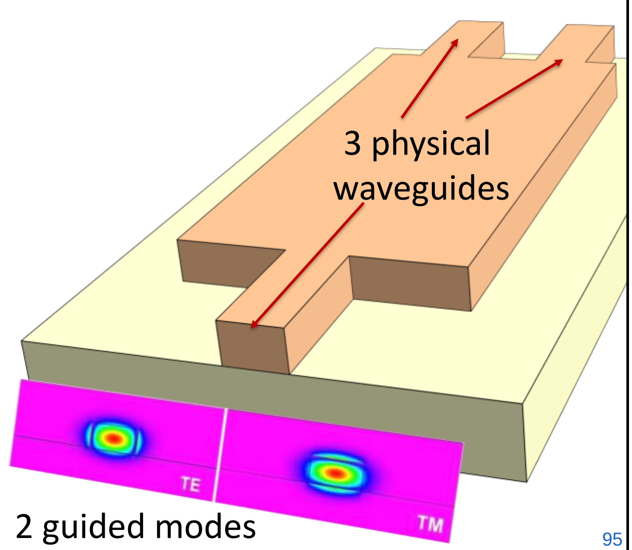
Orthogonal states

- Physically separated waveguides
- Each mode in the waveguide

Example: 6 “ports” → 6×6 S-matrix

In practice:

Only use the relevant modes (rest is “loss”)



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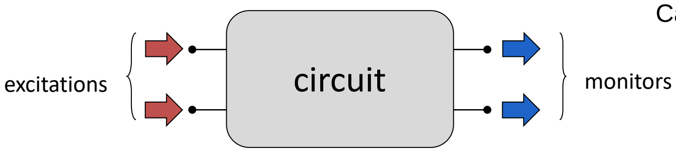
TIME DOMAIN OPTICAL CIRCUIT SIMULATION



Calculate time response of a circuit

- to a stimulus (or combination of excitations)
- at certain output monitors
- using discrete time steps

Pro:

- Faster than electromagnetic simulations
- Supports large circuits

Con:

- Slower than frequency domain
- Only response to specific stimulus

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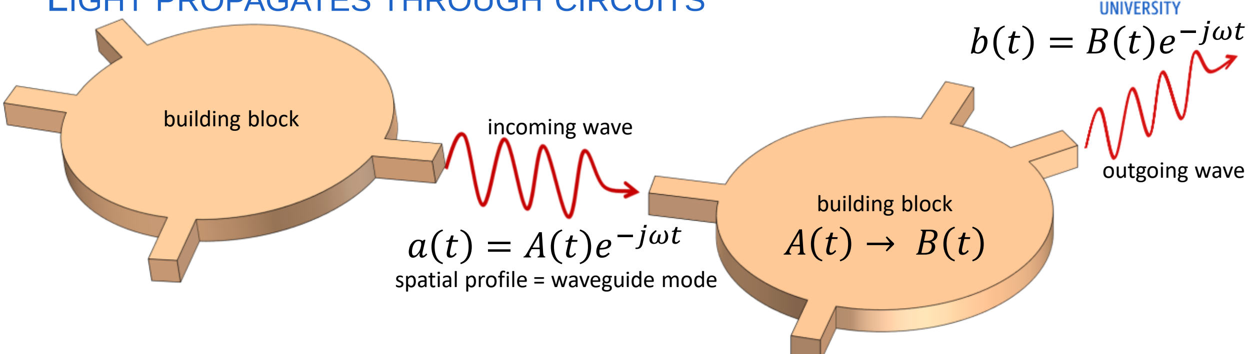
LIGHT PROPAGATES THROUGH CIRCUITS



Time domain:

- time-varying signals propagating between nodes
- Linear, nonlinear and electro-optic systems
- Basically any equation can describe a node
- Still fast, but slower than frequency-domain
- Every excitation needs a new simulation

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Optical vs. Electrical Circuit Simulation

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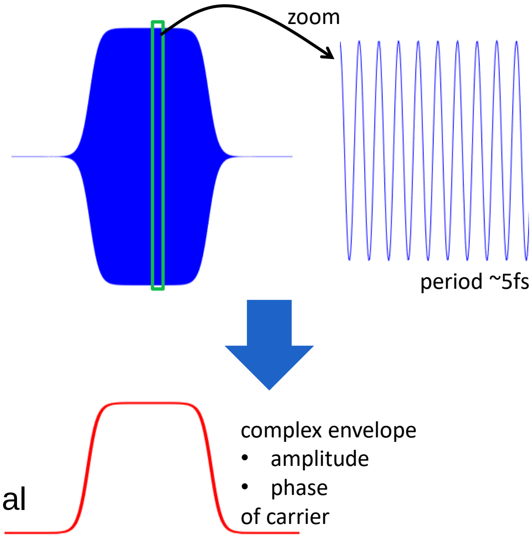
optical = electrical … at very high frequency

- ultra-small time steps (fs)
- ultra-long simulations (10^{12} time steps)
- high-bandwidth signals (200THz)



impractical!

Solution: analytic signal

= complex amplitude on carrier

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Optical Signals

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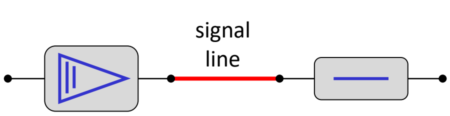
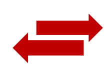
An optical link carries an an optical signal…



two directions



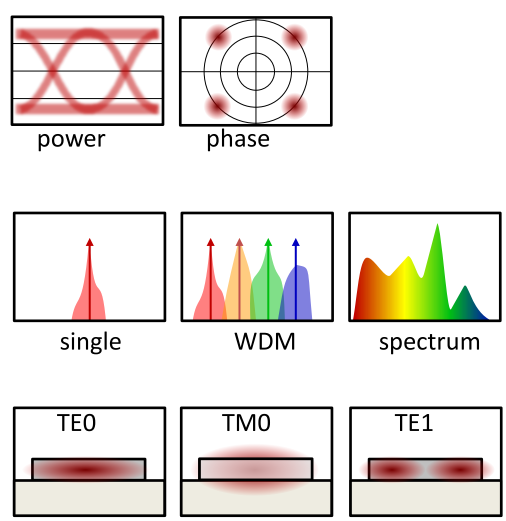
2 × 2 × N × M

not all simulators support all combinations

complex number

wavelength: N channels

mode/polarization: M modes



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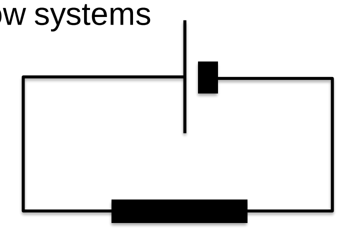
Simulating Linear Circuits

Photonics does not fit easily in Spice

Effort-flow systems



Electrical	Voltage	Current
Fluidic	Pressure	Flow
Thermal	Temperature	Heat Flow*
Mechanical	Force	Motion
Photonic?	E-field	H-field

Not the best formalism for photonics
(more like an RF wave)

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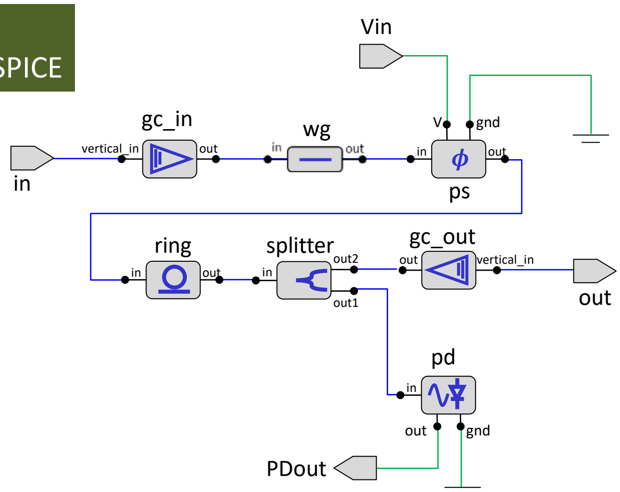
Photonics and Electronics Use Different Formalisms

electrical:
- effort-flow / SPICE

How to co-simulate?



optical:
- Scattering waves

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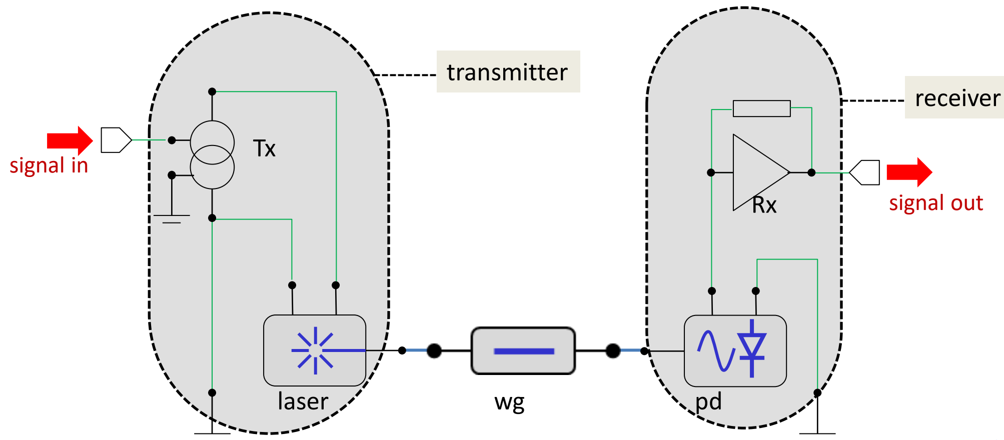
Simulating Photonics + Electronics

Real system: photonics + electronics

Example: optical link



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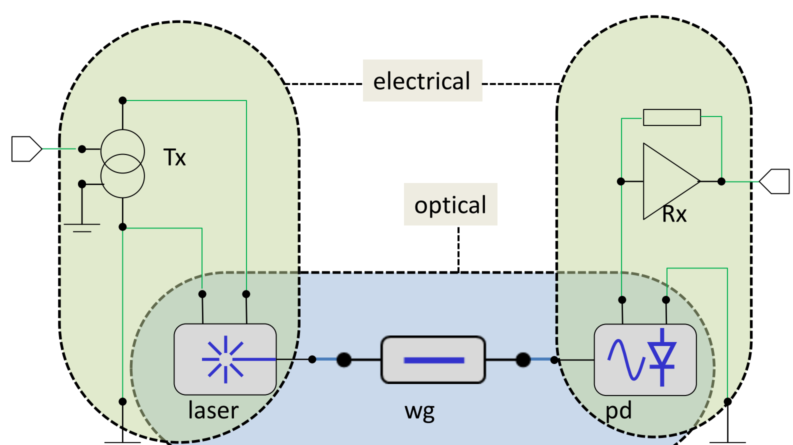
Simulating Photonics + Electronics

Circuit has optical and electrical parts:

Some components overlap



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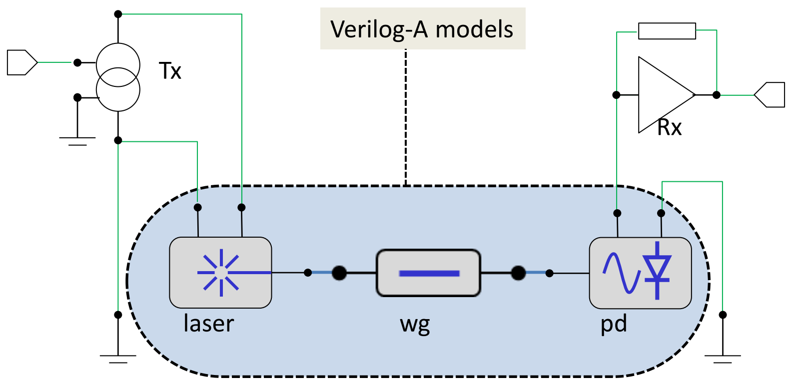
SIMULATING PHOTONICS + ELECTRONICS

Simulating everything in electrical simulator (SPICE – MNA)

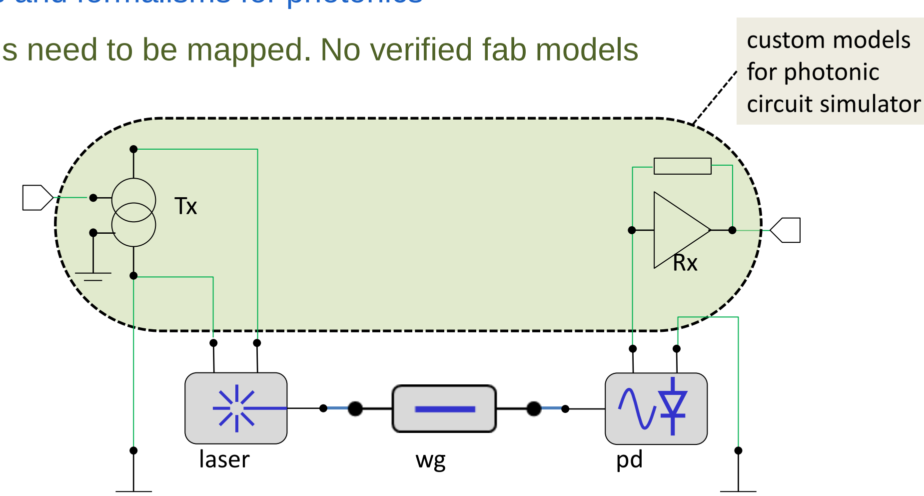
- Use native, verified models for electronics
- Build Verilog-A models for photonics



SIMULATING PHOTONICS + ELECTRONICS

Simulate everything in a photonics simulator (Interconnect, Caphe, OptSim)

- Optimized models and formalisms for photonics
- Electronics models need to be mapped. No verified fab models



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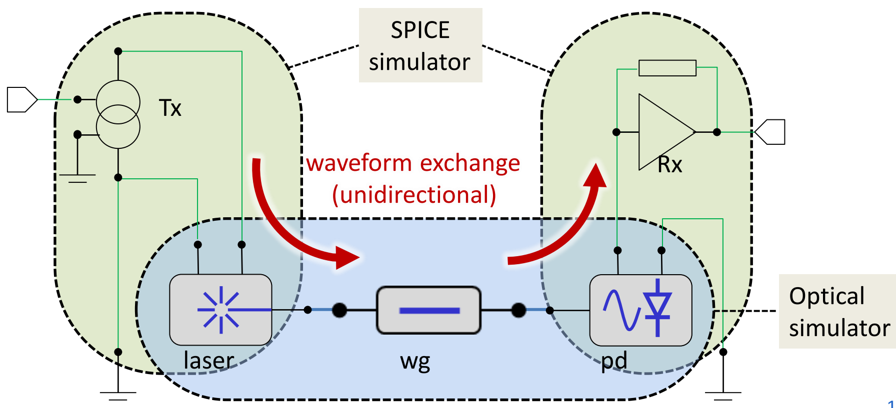
Simulating Photonics + Electronics

Co-simulate with waveform exchange

- Photonics and electronics in optimized model, executed sequentially
- Output of one simulation = input of next simulation



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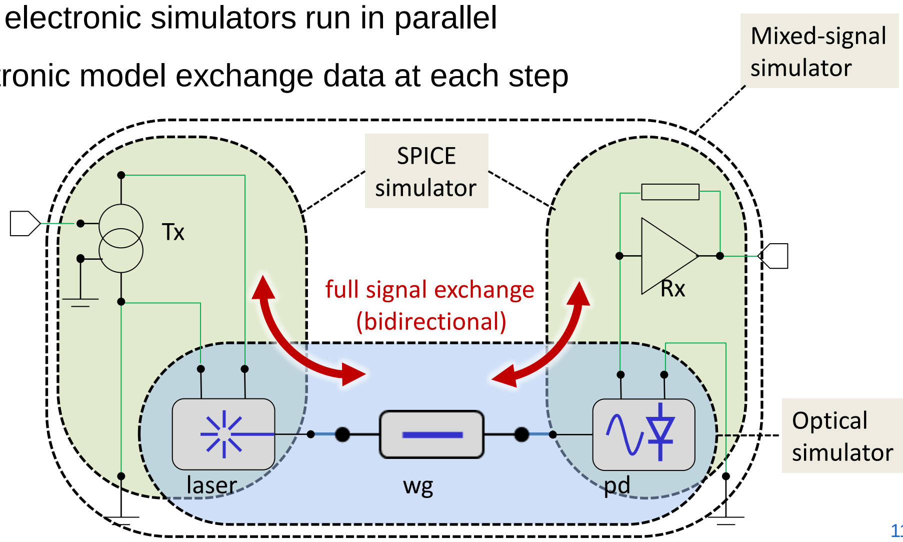
Simulating Photonics + Electronics

True cosimulation (photonics and electronics in lockstep)

- Both photonic and electronic simulators run in parallel
- Photonic and electronic model exchange data at each step



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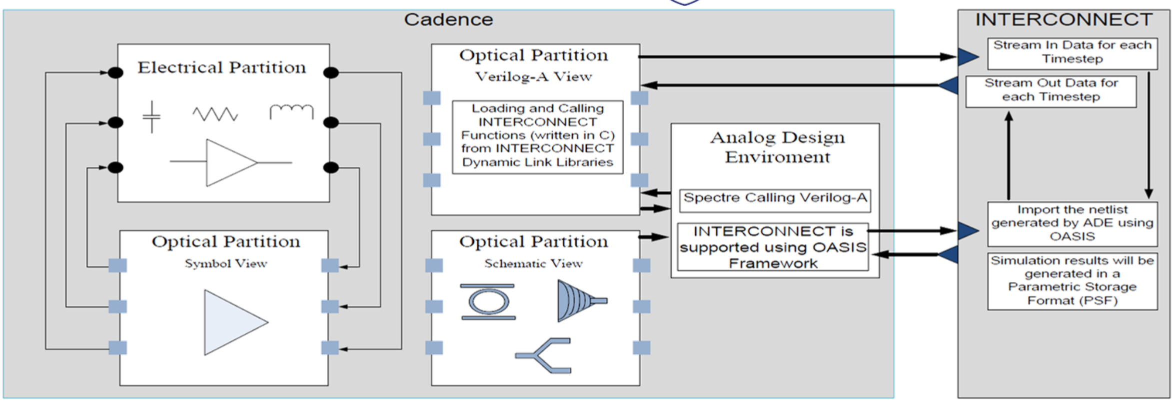
Co-simulation



Optical and electrical co-design in Virtuoso Schematic

Photonic simulation in Lumerical Interconnect

A. Farsaei, APC 2016, JTu4A.1

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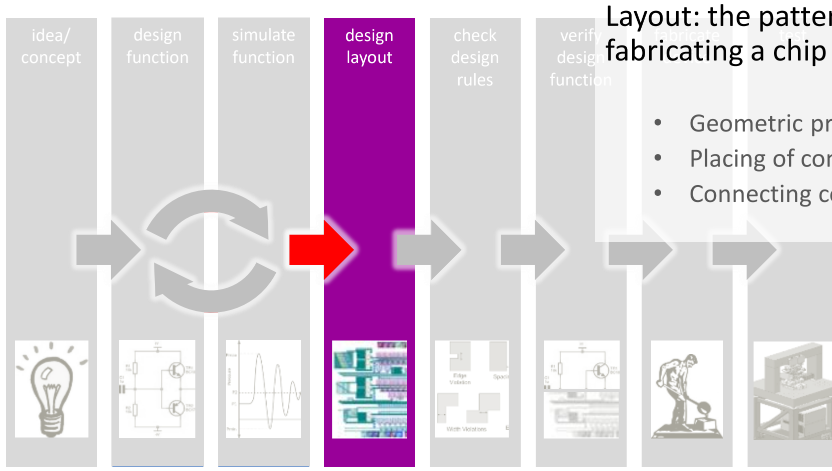
From Function to Layout



Layout: the patterns used for fabricating a chip

- Geometric primitives
- Placing of components
- Connecting components

design flow time

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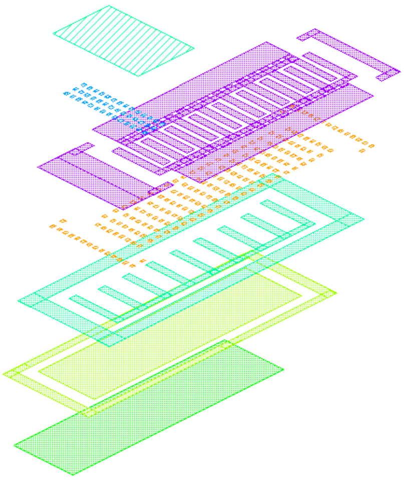

Layout

Geometric patterns

- Originally drawn by hand
- Now drawn by computer
- or programmed using scripts

Different layers

- correspond to process steps: Mask layers
- or to logical operations (e.g. Boolean operations)

Different purposes

- Intent of the drawn shape: process, exclusion, annotation, …

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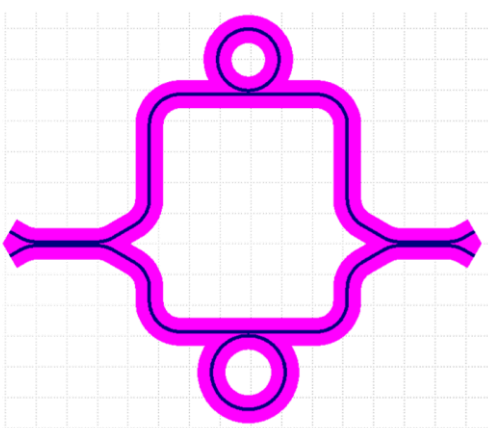

Layout: Circuits

Organized in (reusable) Cells

- placement
- transformations

Hierarchy: Cells contain other cells

Routing

- Optical connectivity with waveguides
- Electrical connectivity with metal wiring
- Avoid crossings/shorts/disconnects

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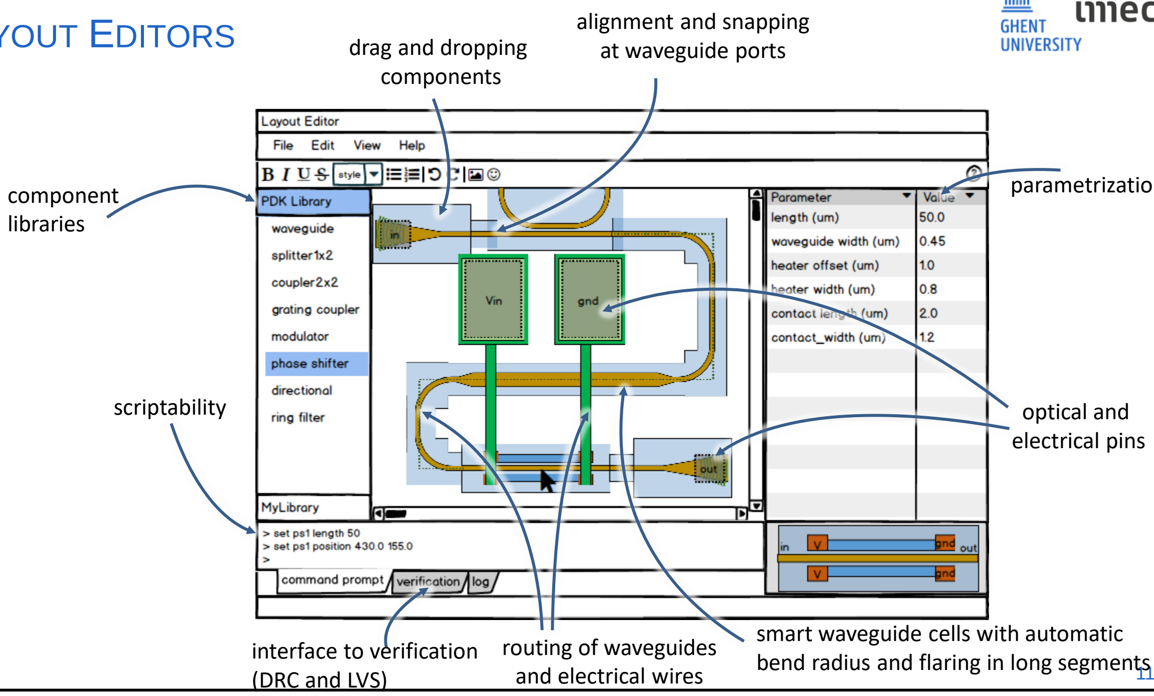
Layout Editors



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A Design Cell

combines the different aspects of the design

- symbolic representation
- layout (shapes on mask layers)
- location and orientation of the ports
- a model

Static content: can be stored in a file (e.g. EDIF)

Easy exchange, tool vendor independent

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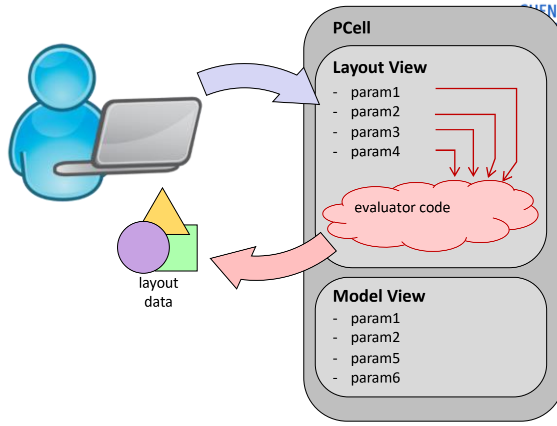
A Parametric Cell

Same as a cell, but the content is generated based on parameters

Input: user parameters

Output: data



in the middle: an ***evaluator*** function

- a piece of software code
- tool vendor dependent

Storage: in a database

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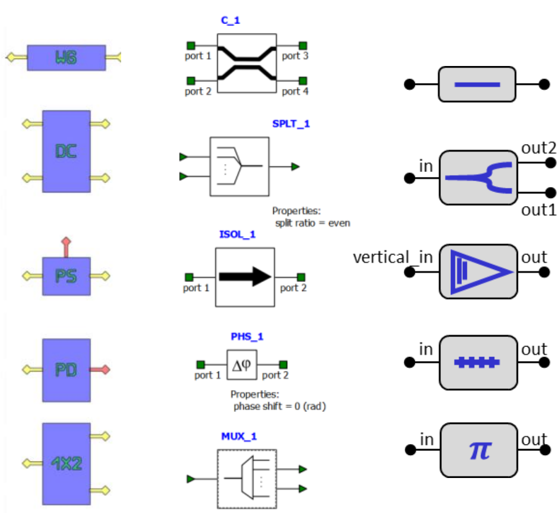

The Symbol View

Abstract representation of a component

- Symbolic drawing
- I/O ports/terms (optical/electrical)
- Parameters

There is a standard in electronics (EDIF files) but not between photonics tools.

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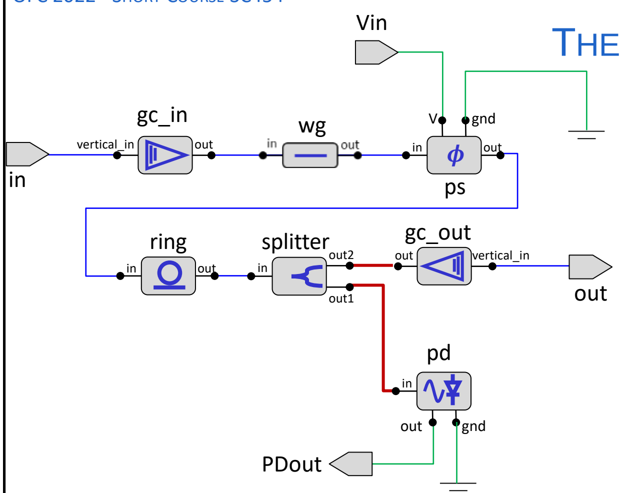
THE NETLIST/SCHEMATIC VIEW



The netlist describes the internal connectivity of a (sub)circuit

- Circuit elements (instances)
  gc_in, gc_out - grating coupler
  wg - waveguide
  ps - phase shifter
  …
- Connection between ports
  gc_in:out – wg:in
  wg:out – ps:in
  ps:out – ring:in
  ring:out – splitter:in
  …
- Connections with outside world
  gc_in:vertical_in – in
  gc_out:vertical_in – out
  pd:out – PDout
  pg:gnd – GND
  …

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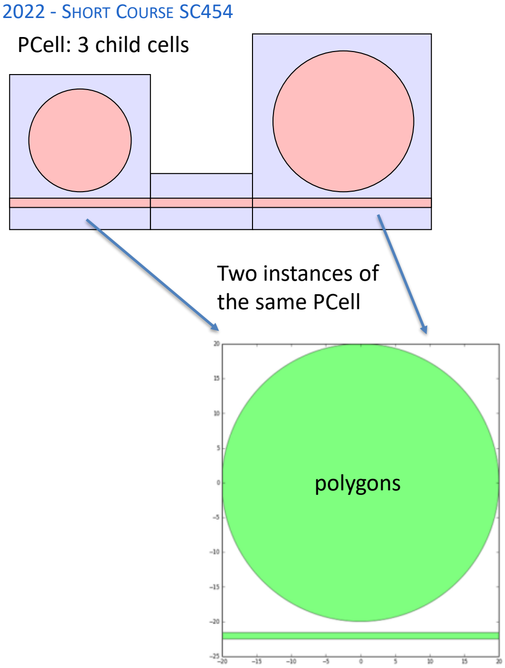
THE LAYOUT VIEW



Hierarchical description of polygons on layers

- Raw polygons
- Instances of other cells
  - single
  - array

Here parametrization is used most intensively

- calculate complex shapes
- perform repetitive placements

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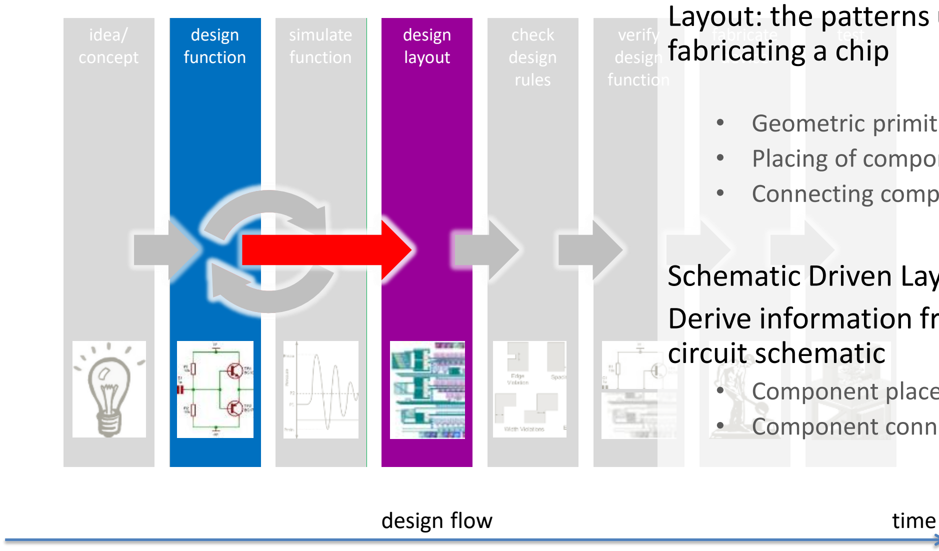
Schematic Driven Layout (SDL)



Layout: the patterns used for fabricating a chip

- Geometric primitives
- Placing of components
- Connecting component

Schematic Driven Layout:

Derive information from circuit schematic

- Component placement
- Component connectivity

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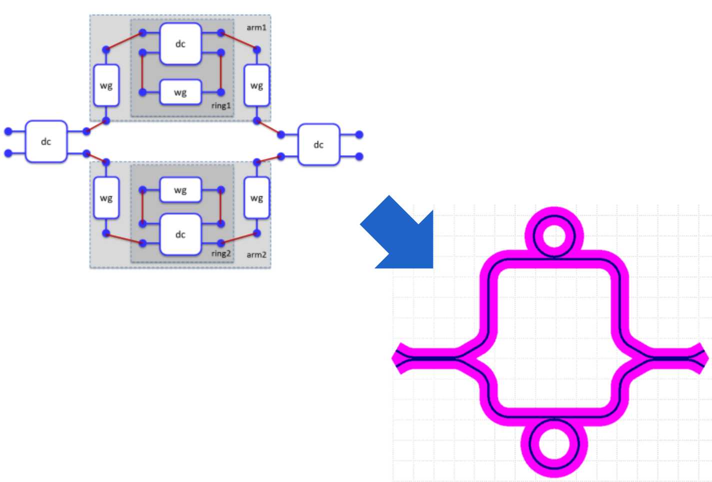
Schematic Driven Layout (SDL)



Derive the physical layout from the schematic

- Generate the Layout (P)Cells
- Place the Layout Cells
- Connect the layout cells together

Not trivial to fully automate

- What is the optimal placement?
- Is the topology possible?
- Constraints for length matching?
- On which layer to route?
- Waveguide bends and crossings?

Combination of manual + auto

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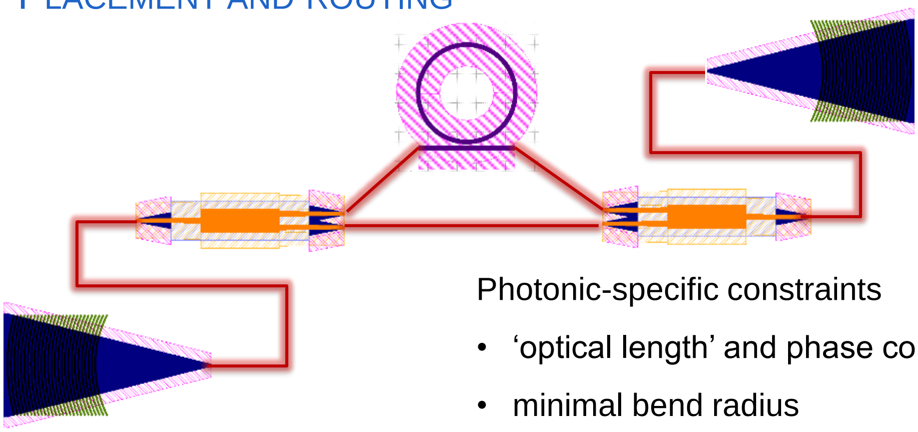
Placement and Routing



Photonic-specific constraints

- 'optical length' and phase control
- minimal bend radius
- waveguide spacing
- matching port direction
- single routing layer!

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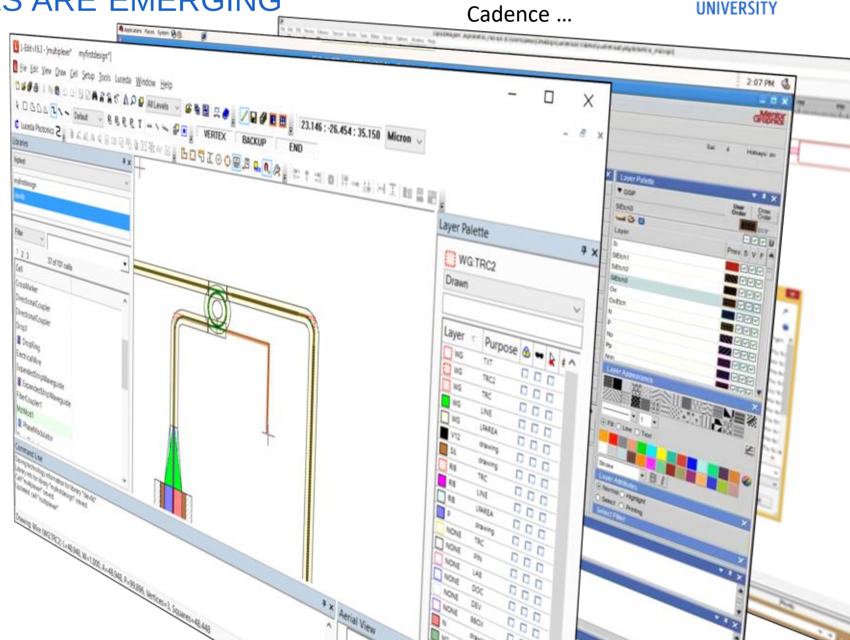
Photonic SDL tools are emerging

Luceda, Synopsys, Mentor Graphics, Cadence ...

Pure photonics
or based on EDA tools

- define connections
- place components
- route waveguides



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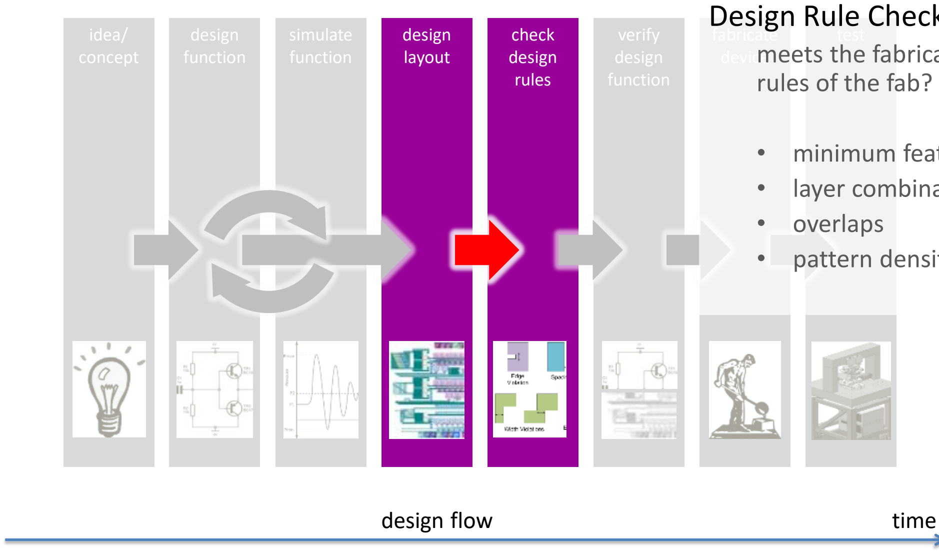
IS THE LAYOUT VALID?



Design Rule Checking

meets the fabrication rules of the fab?

- minimum features
- layer combinations
- overlaps
- pattern density

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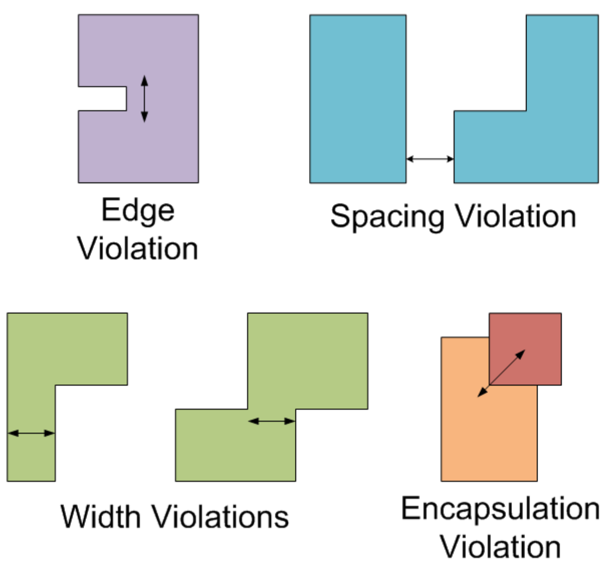
DESIGN RULE VIOLATIONS: EXAMPLES



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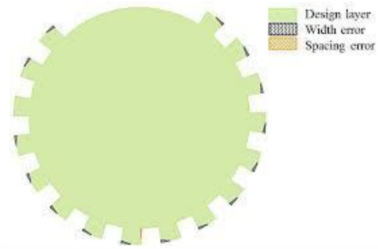
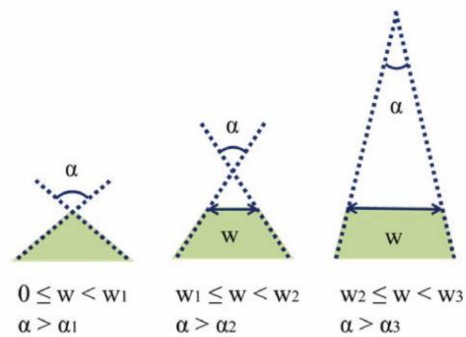
PHOTONIC PROBLEMS WITH DRC?

DRC techniques were designed for electronics: 90-degree angles…

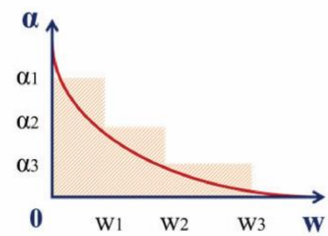
Silicon Photonics:

- All-angle waveguides – discretized…
- Nanometer scale sensitivities
- Arbitrary geometries (e.g. slot waveguides, PhC)





What is bad?
What is intentional?



R. Cao, VSLI-SoC 2014 128

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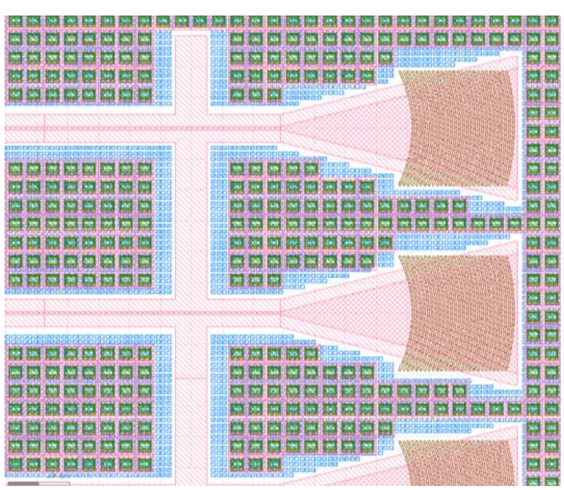

PATTERN DENSITIES

Pattern density must be sufficiently uniform

- Etch rate control
- Avoid CMP dishing

Tiles are added

There must be sufficient room to add tiles

- Slab areas (AWG)
- Dense waveguide arrays
- …

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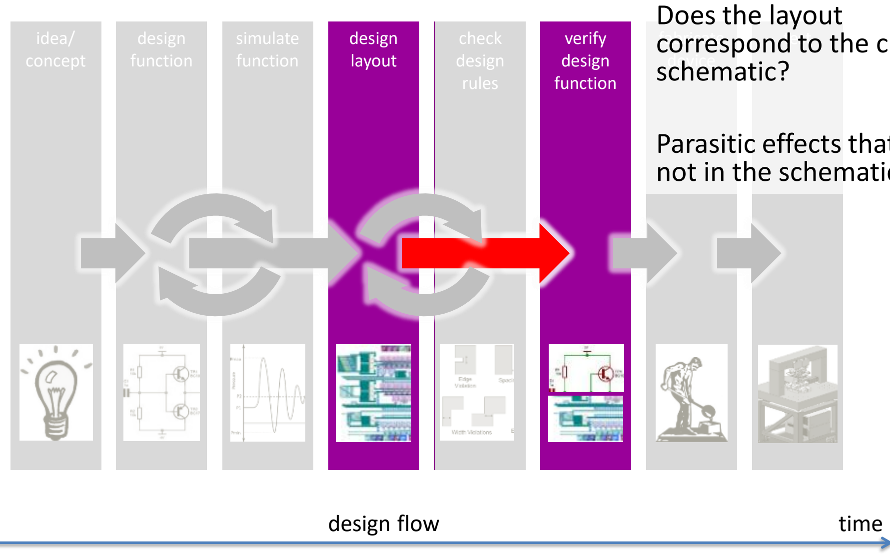
FUNCTIONAL VERIFICATION

Does the layout correspond to the circuit schematic?

Parasitic effects that were not in the schematic



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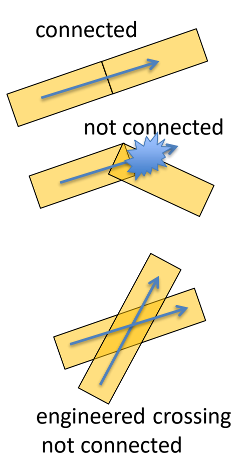
FUNCTIONAL VERIFICATION: LAYOUT VERSUS SCHEMATIC

Check Connectivity

Are the correct components placed?

Are they properly connected?

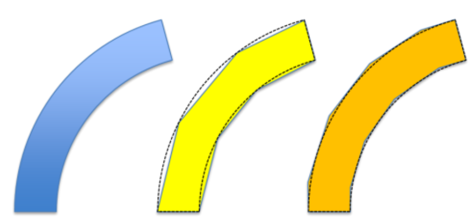


Check functionality

Did we use the right parameters?

Does the layout perform the correct function?

e.g. does the waveguide have the correct width (i.e. optical length)



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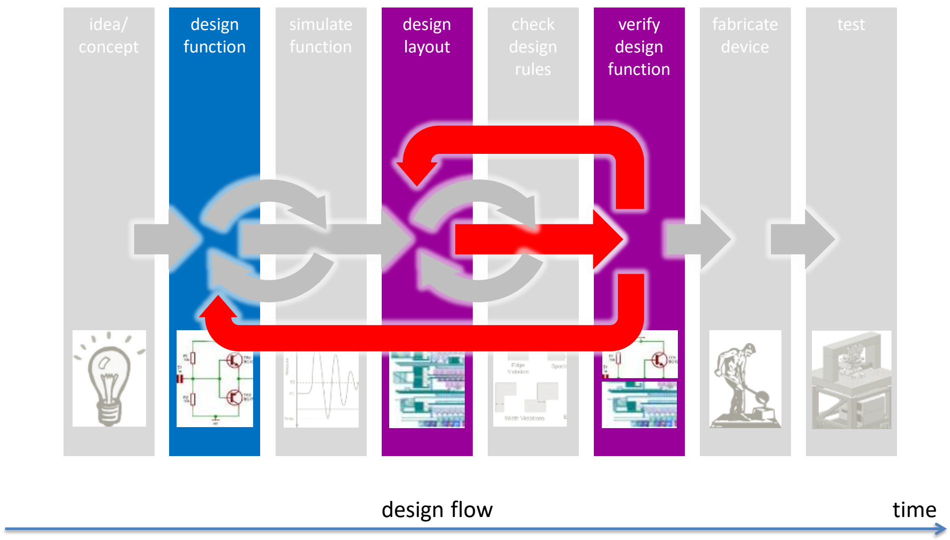
FUNCTIONAL VERIFICATION



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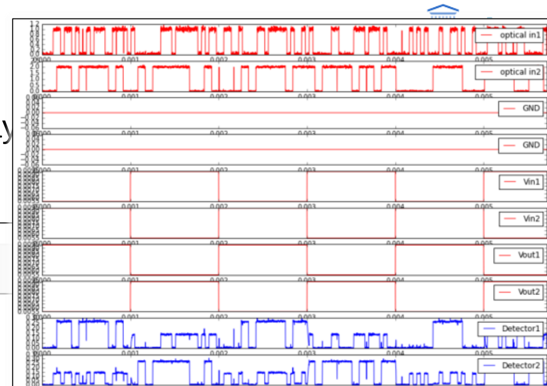
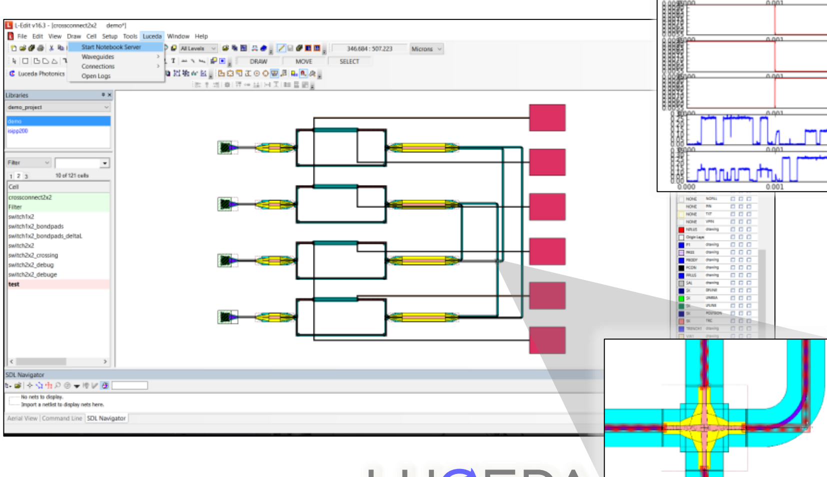
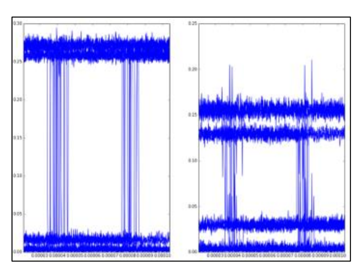
POST-LAYOUT SIMULATION

Resimulate the circuit based on the actual lay

Include lengths, crossings, reflections, …







LUCEDA

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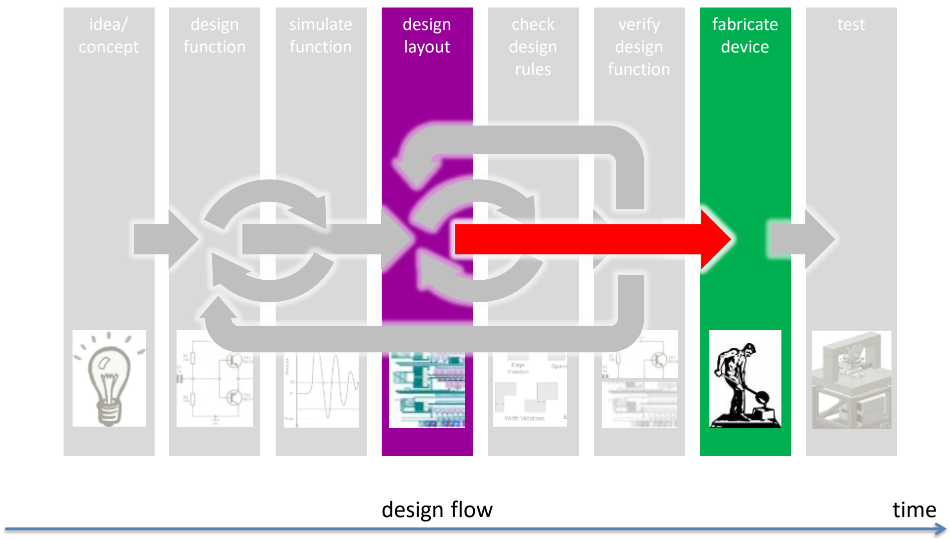
FABRICATION

"no plan survives contact with the enemy"

H. von Moltke (misquoted)



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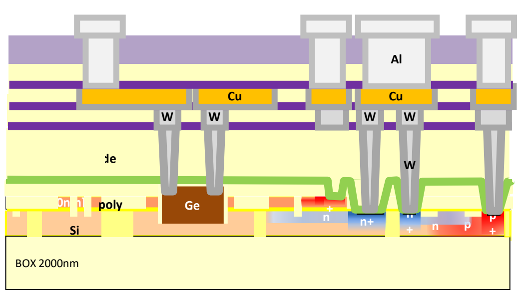
THE ACTUAL FABRICATION PROCESS



example: IMEC silicon Photonics

- Layer depositions
- Pattern definition (lithography)
- Pattern transfer (etch)
- Planarization
- Thermal treatment
- Doping and implantation
- …

and each step with imperfections and variability

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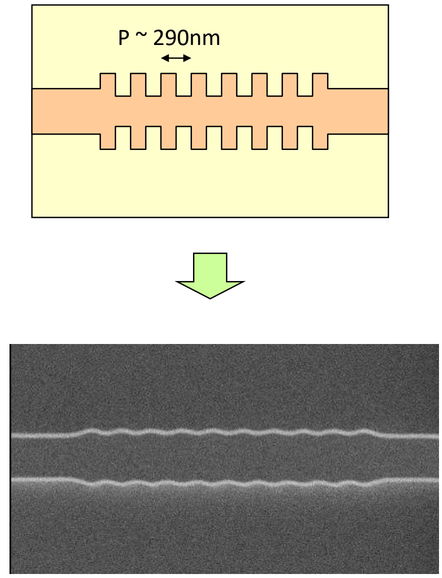
LITHOGRAPHY: NOT PERFECT

Spatial low-pass filter

- Minimum feature size
- Minimum pitch
- Pattern rounding

Example: Bragg grating



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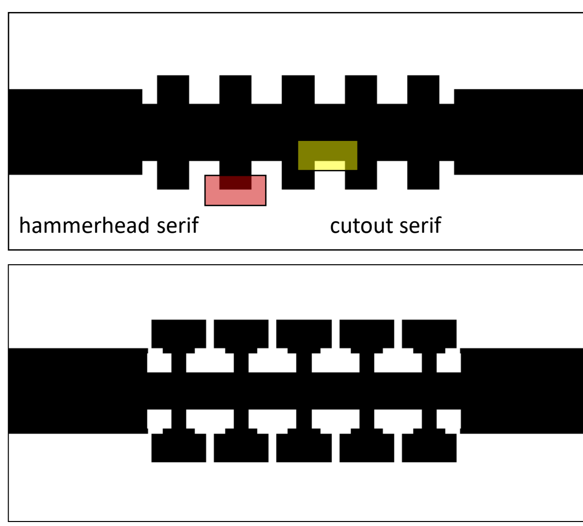
OPTICAL PROXIMITY CORRECTIONS (OPC)

Overcome rounding: add OPC

- serifs
- cutouts

Makes mask more complex (and costly)

Not always possible without violating DR



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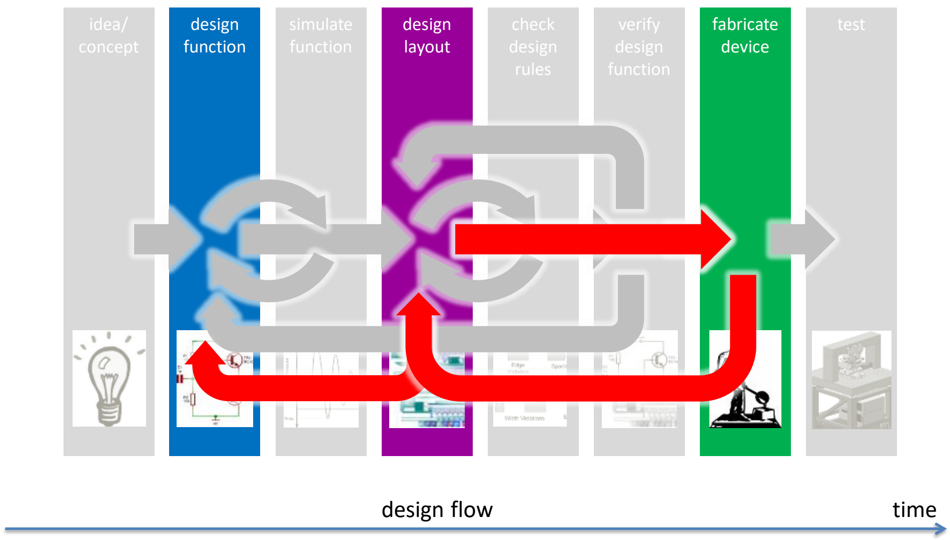
Fabrication: In-line data



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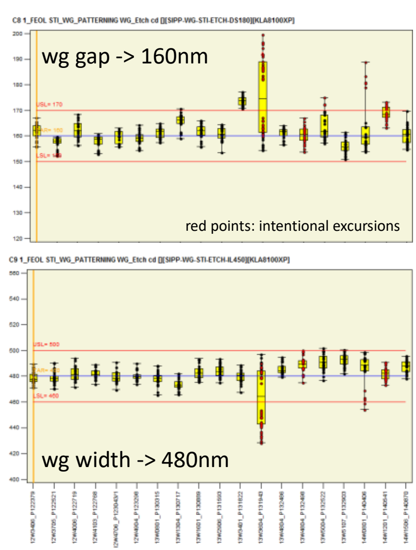

In-line process data

Collect data from wafers as they are being processed

- Line width
- Etch depth
- Layer thickness
- …

Feed in design process

- FRONT-END: Predict behavioural change
- BACK-END: Adjust layout

STATISTICS!

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THERE ARE MANY SOURCES OF NON-UNIFORMITY

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Reticle/Mask
- CD uniformity
- Flatness
- Transmission

Litho tool
- Exposure dose
- Slit uniformity
- Chuck flatness
- Focus stability
- Scan direction
- Source spectrum

Resist process
- BARC uniformity
- Resist uniformity
- PEB °C Uniformity
- Developer
- Metrology

Wafer
- Wafer flatness
- Stack uniformity
- Topography

Etch process
- Plasma Chemistry
- Coil power stability
- Bias stability
- Resist coverage
- °C stability
- Metrology

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DESCRIBING VARIABILITY AT DIFFERENT LEVELS

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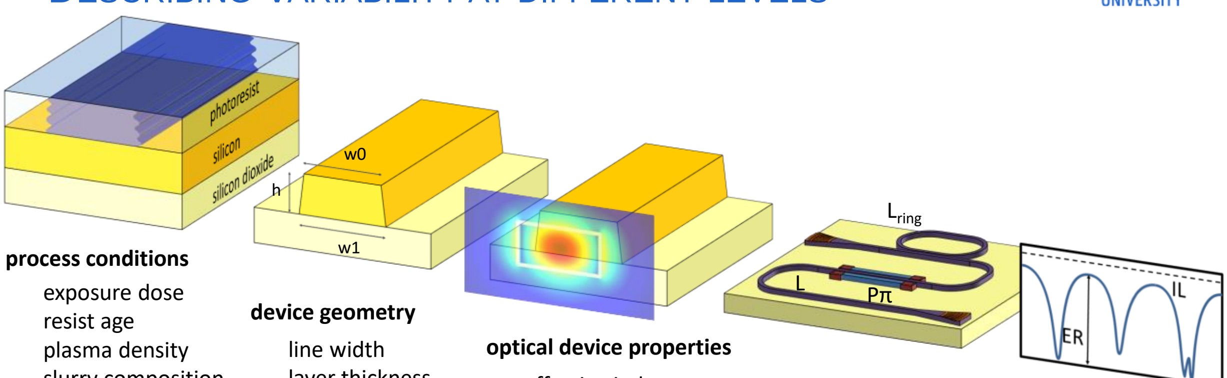

process conditions
- exposure dose
- resist age
- plasma density
- slurry composition
- …

device geometry
- line width
- layer thickness
- sidewall angle
- doping profile
- …

optical device properties
- effective index
- group index
- coupling coefficients
- center wavelength
- …

circuit properties
- optical delay
- path imbalance
- tuning curve
- …

system performance
- insertion loss
- crosstalk
- noise figures
- power consumption
- …

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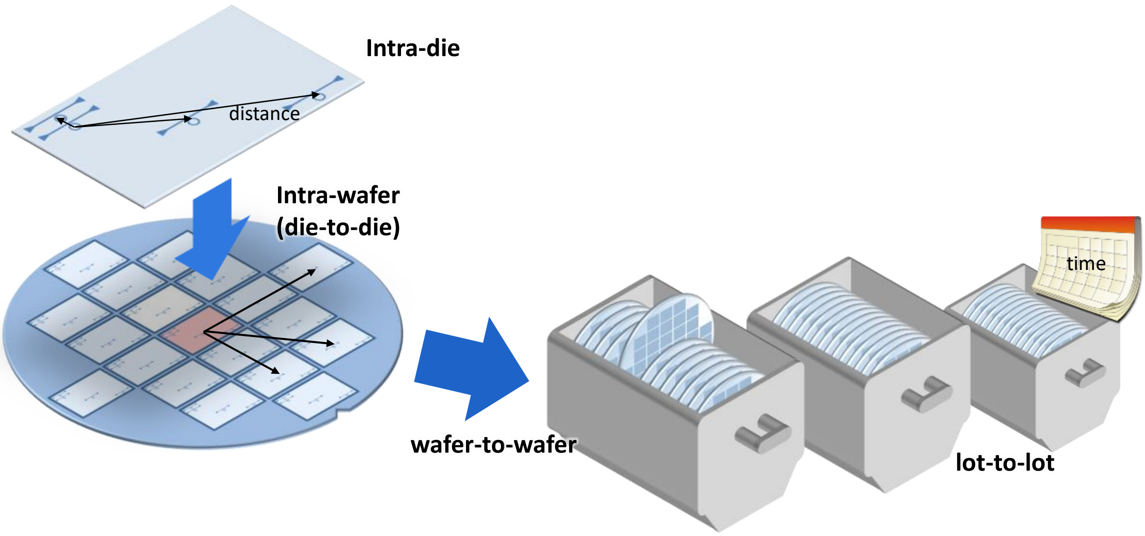
Variability Effects Work on Different Scales



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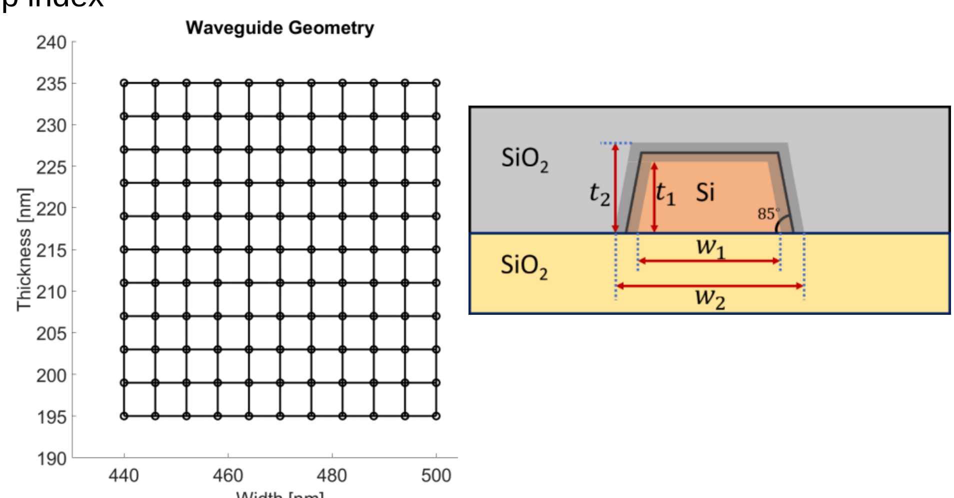
Mapping Geometry on Optical Properties

- width/thickness
- effective/group index



Y. Xing, Phot.Res. 2018

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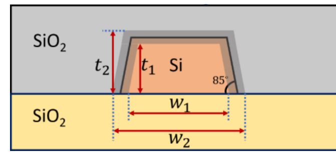
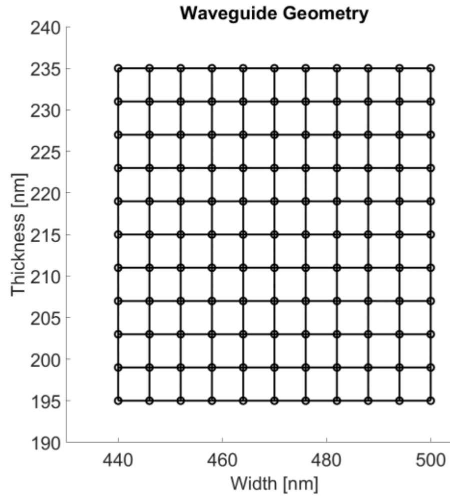
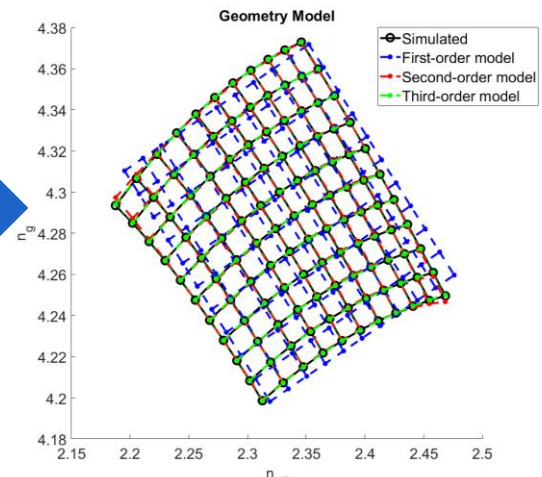
Mapping Geometry on Optical Properties

- width/thickness
- effective/group index







Y. Xing, Phot.Res. 2018

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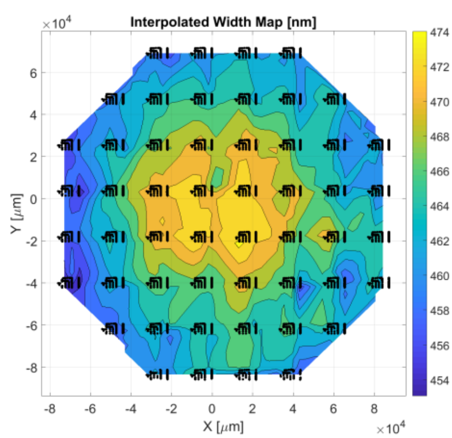
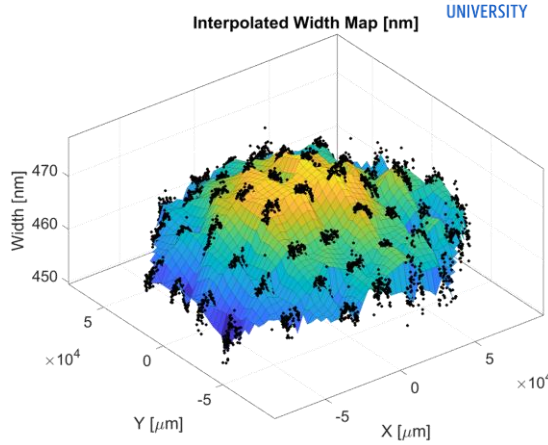
Linewidth Map





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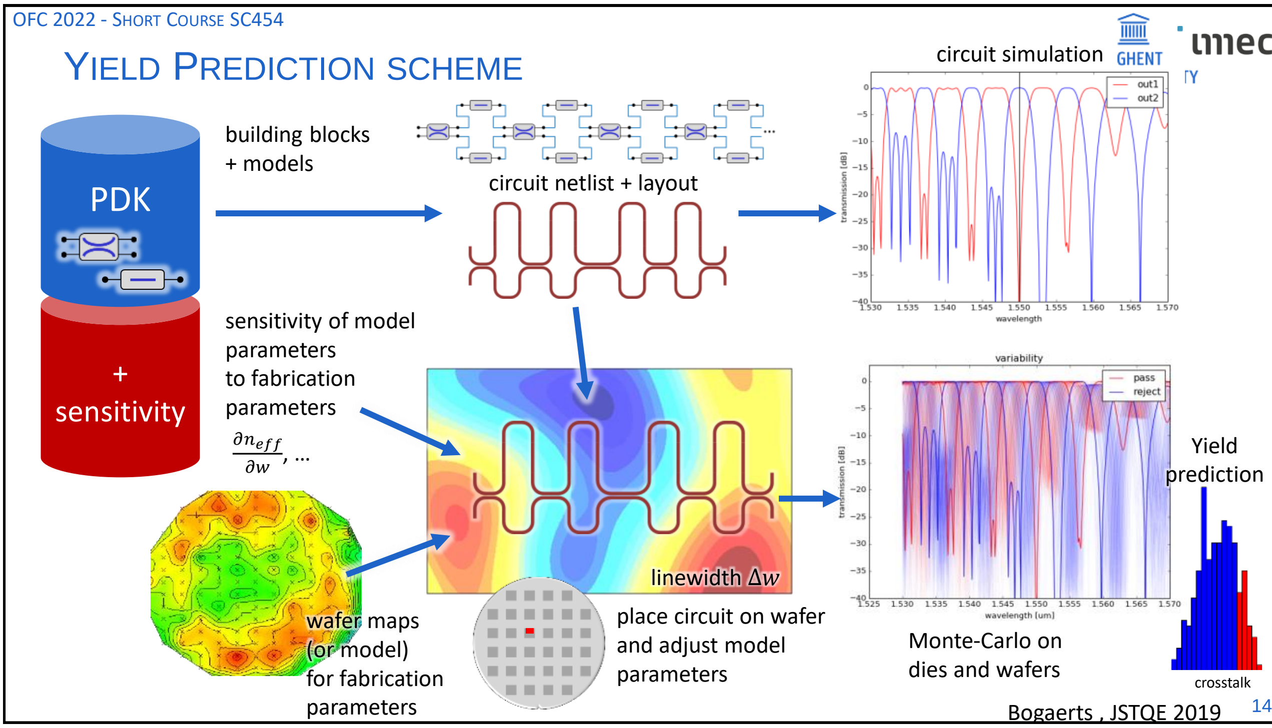
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Yield Prediction Scheme
PDK
+ sensitivity
building blocks + models
circuit netlist + layout
circuit simulation
sensitivity of model parameters to fabrication parameters
$\frac{\partial n_{eff}}{\partial w}$, ...
wafer maps (or model) for fabrication parameters
linewidth Δw
place circuit on wafer and adjust model parameters
variability
pass
reject
Monte-Carlo on dies and wafers
Yield prediction
crosstalk
Bogaerts , JSTQE 2019
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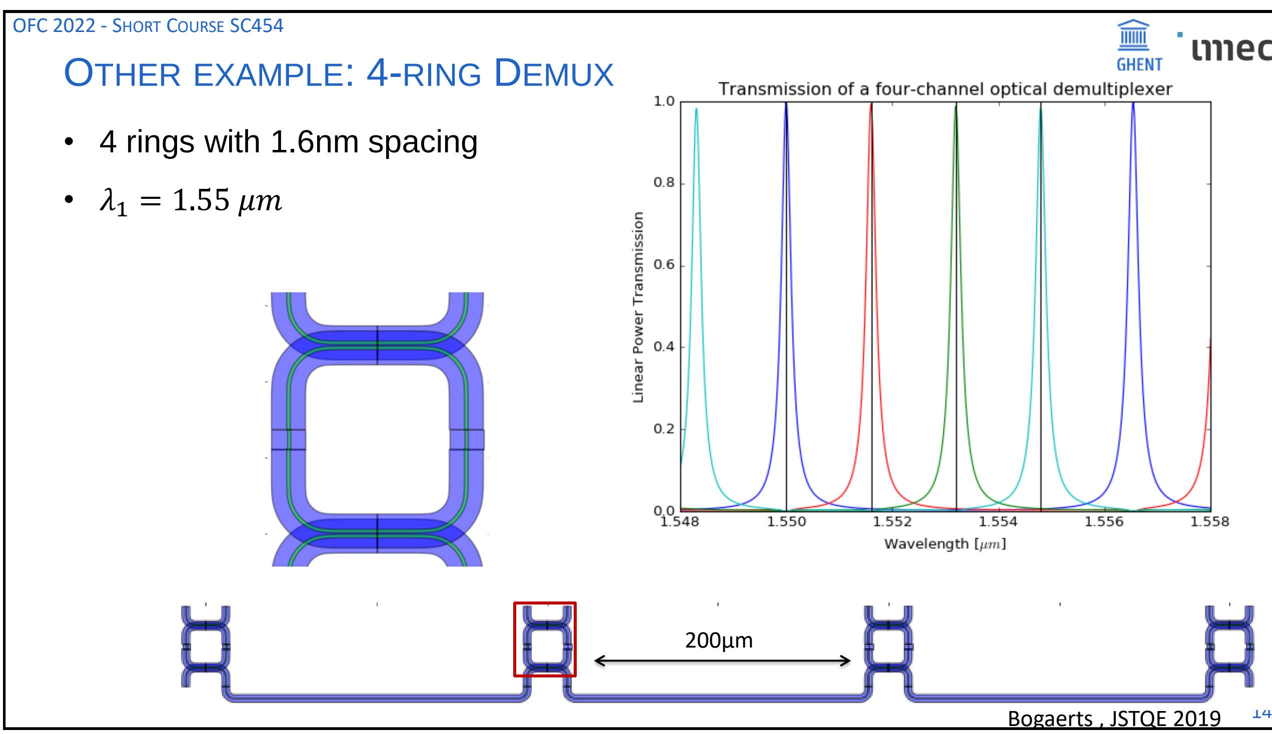
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Other Example: 4-Ring Demux
4 rings with 1.6nm spacing
$\lambda_1 = 1.55\ \mu m$
Transmission of a four-channel optical demultiplexer
Linear Power Transmission
Wavelength [μm]
200µm
Bogaerts , JSTQE 2019
147

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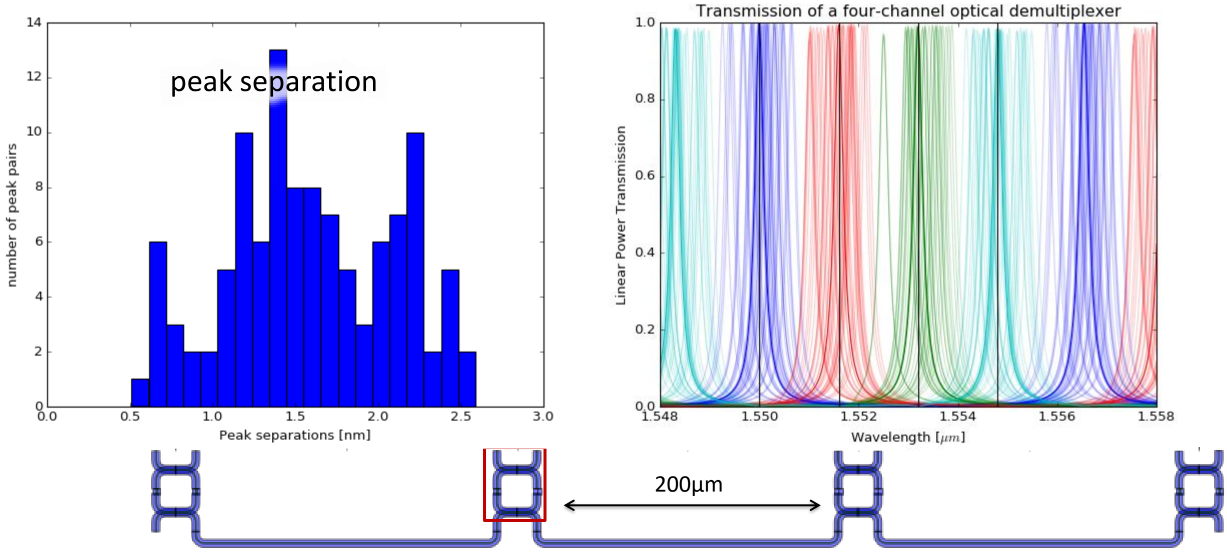
EFFECT OF LINEWIDTH VARIATION

fabrication linewidth variation only ($\sigma = 1nm$)



Bogaerts , JSTQE 2019

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BRINGING THE DEVICES CLOSER TOGETHER

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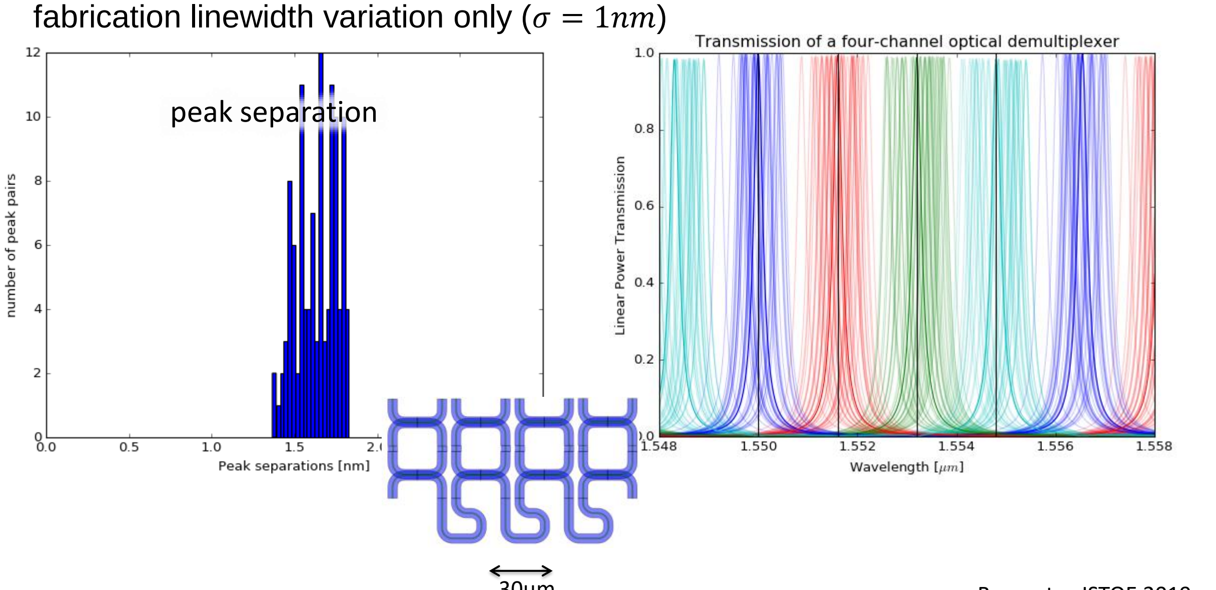
fabrication linewidth variation only ($\sigma = 1nm$)



Bogaerts , JSTQE 2019

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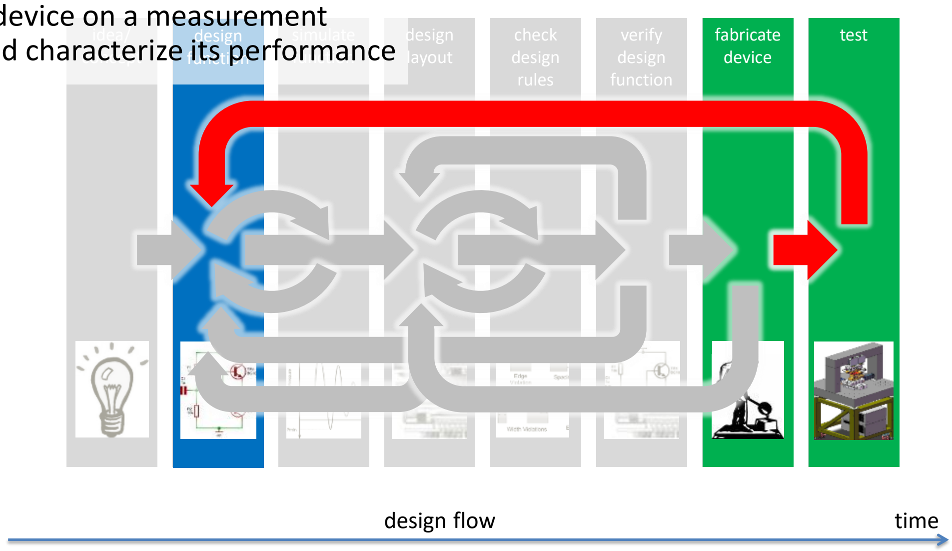
TESTING

Put the device on a measurement setup and characterize its performance



150

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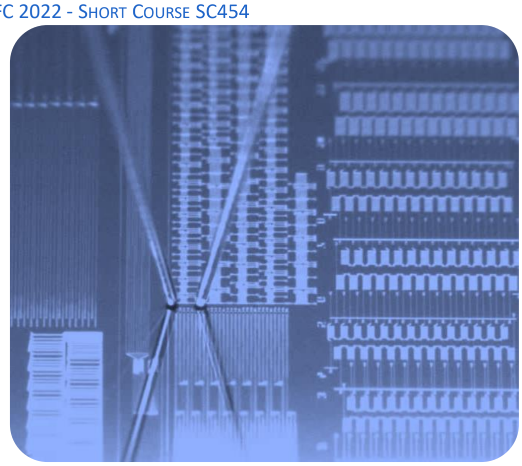


HOW TO TEST?

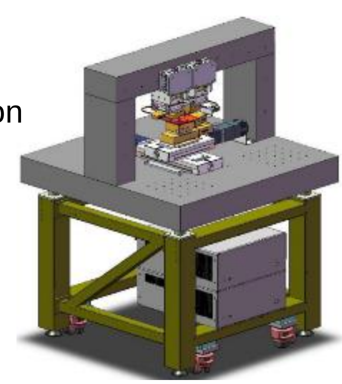
Electrical, optical, or both?

Wafer-scale testing -> grating couplers

Testing after packaging?

Need statistics?

depends on application



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CHALLENGE: DEFINING GOOD TESTS

You need to think about tests during the design stage

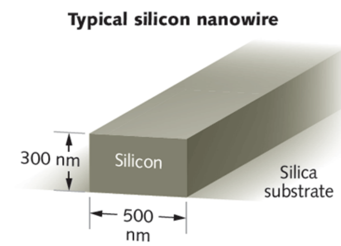
- Which structures are representative?
- How can I isolate them?
- What parameters do I want to measure?
- How will I analyse/fit the data?

Parameters for your component models!

- What makes a good model?

Example: waveguide model
- $n_{eff}(\lambda)$ -> polynomial?
- loss(λ) -> polynomial?
- nonlinearities?

How to measure n_{eff}?



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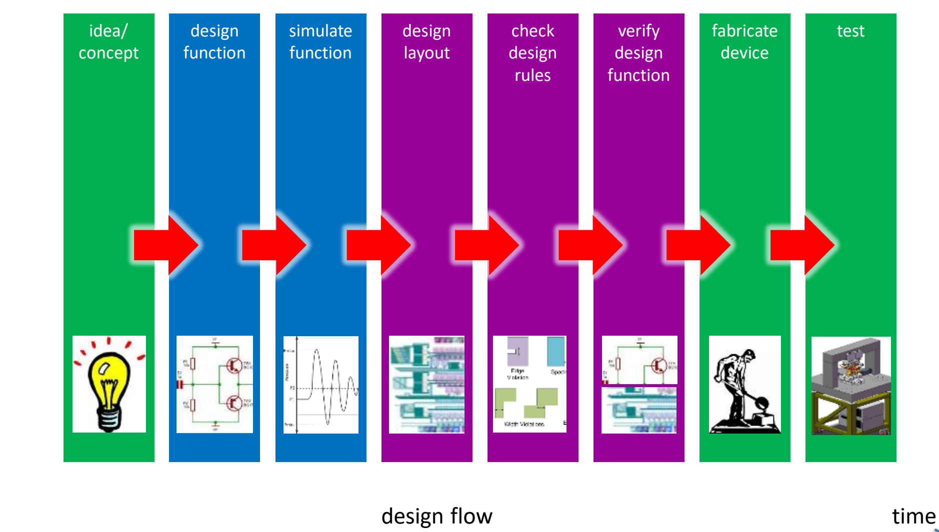
OUR SIMPLE DESIGN FLOW



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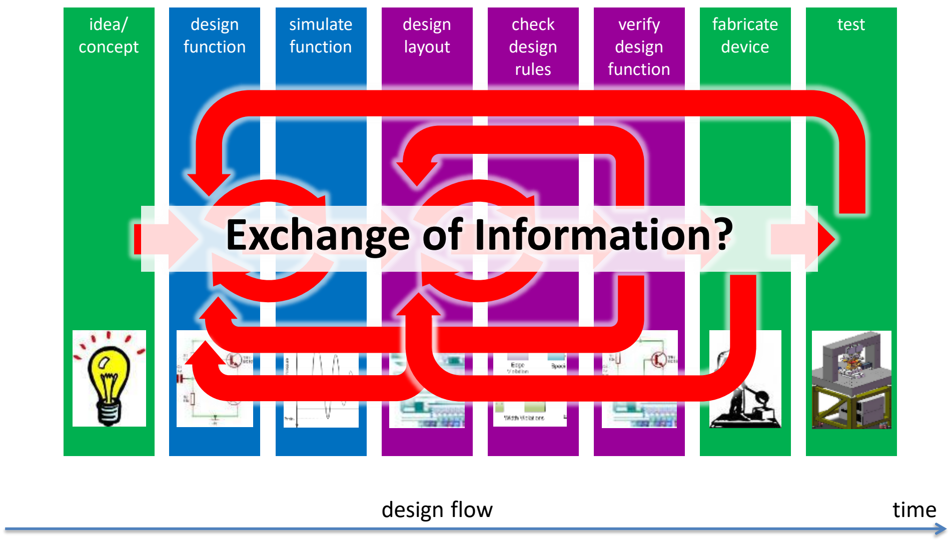
Our simple design flow



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Exchange of information

Files

- Layout: GDSII and OASIS
- Netlist/Schematic: Spice, EDIF
- Models: Spice, VerilogA, C++, Python
- PCell code: Skill, Python , Tcl
- Data: Touchstone, XML

Databases

- proprietary
- EDA standard: OpenAccess

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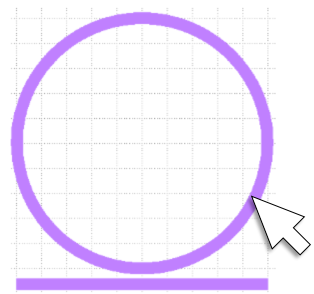
DESIGNING IN CODE VERSUS GUI

Designing in Code

```
from ipkiss3 import all as i3

class RingResonator(i3.PCell):

    class Layout(i3.LayoutView):

        ring_radius = i3.PositiveNumberProperty(default=20.0)
        wg_width = i3.PositiveNumberProperty(default=0.45)
        coupler_gap = i3.PositiveNumberProperty(default=0.3)

        def _generate_elements(self, elems):
            r = self.ring_radius
            g = self.coupler_gap
            w = self.wg_width

            elems += i3.CirclePath(layer=i3.Layer(2),
                                   radius=r,
                                   line_width=w)
            elems += i3.Line(layer=Layer(2),
                             begin_coord=(-r, -r-w-g),
                             end_coord=(+r, -r-w-g),
                             line_width=w)
            return elems
```

Designing in GUI



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DESIGNING IN CODE VERSUS GUI

Designing in Code

Pro:

- Easy to reuse
- Easy to upgrade design
- Easy to share and version
- Easy parametrize
- Easy to document and make examples
- Everything is numerically correct

Con:

- Harder to learn
- No immediate visual feedback

Designing in GUI

Pro:

- Intuitive quick start
- Visual feedback
- WYSIWYG
- Quick point and click

Con:

- Difficult to make complex things
- No calculations
- A lot of manual work
- Easy make small (invisible) mistakes

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DESIGNING IN CODE VERSUS GUI

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Designing in Code

- parameter sweeps
- calculated geometries
- circuit models
- automatic placement and routing

Designing in GUI

- schematic connectivity
- layout positioning (floorplanning)
- fixing the last DRC errors
- quick manual routing

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ABSTRACTIONS IN A CIRCUIT DESIGN FLOW

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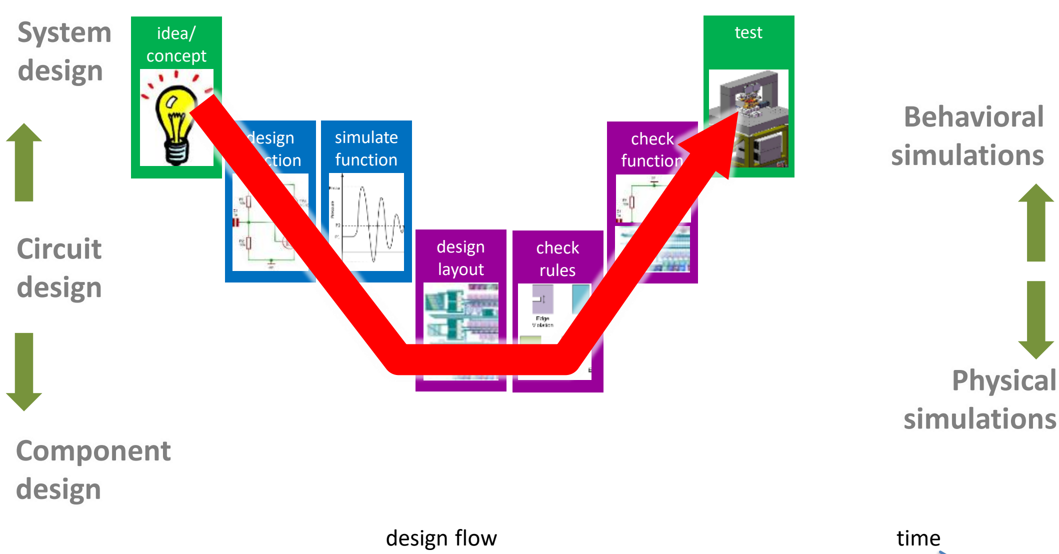

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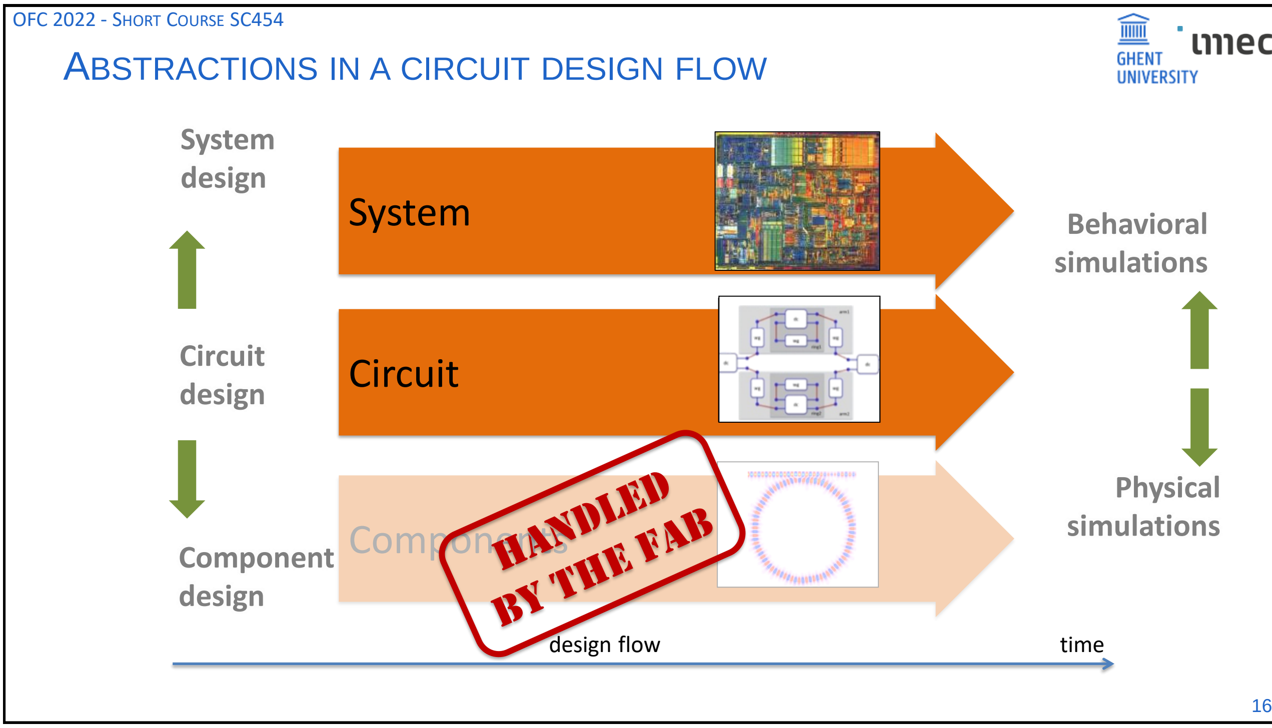
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Abstractions in a Circuit Design Flow
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imec
System design
Circuit design
Component design
System
Circuit
Components
HANDLED BY THE FAB
Behavioral simulations
Physical simulations
design flow
time
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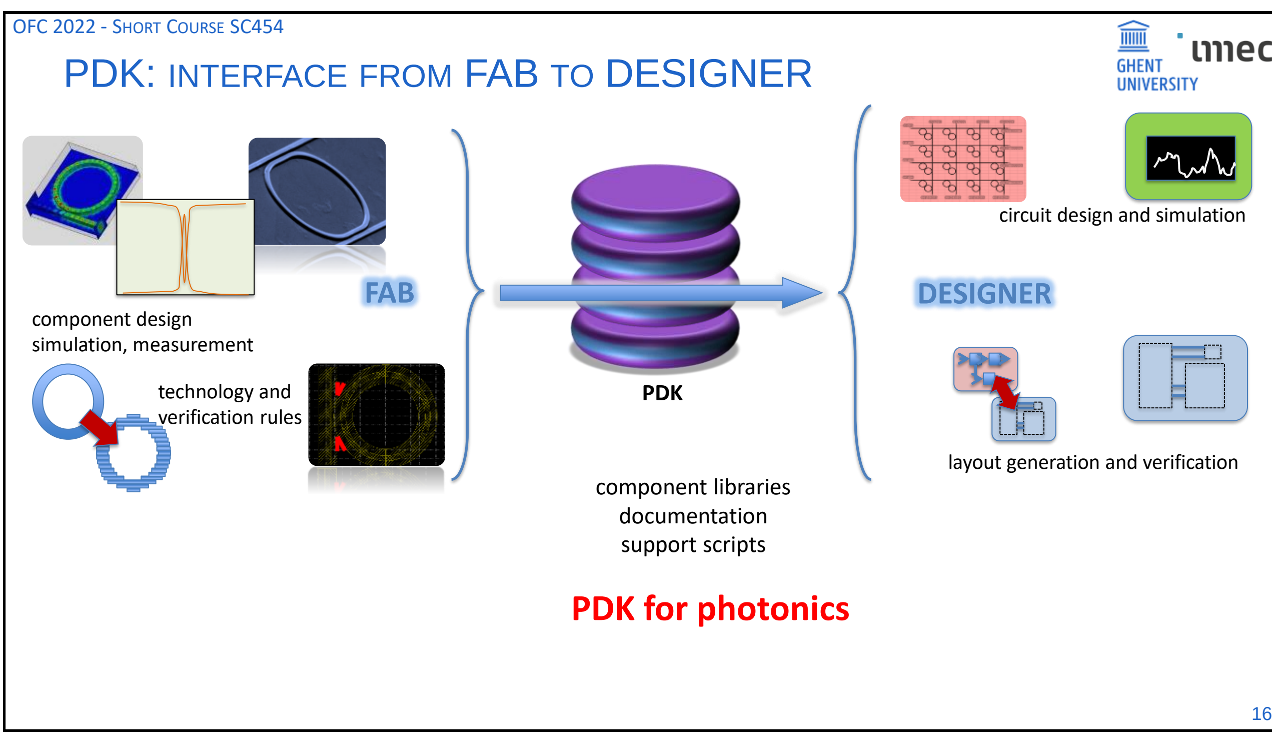
OFC 2022 - Short Course SC454
PDK: Interface from FAB to DESIGNER
GHENT UNIVERSITY
imec
FAB
component design
simulation, measurement
technology and
verification rules
PDK
component libraries
documentation
support scripts
DESIGNER
circuit design and simulation
layout generation and verification
PDK for photonics
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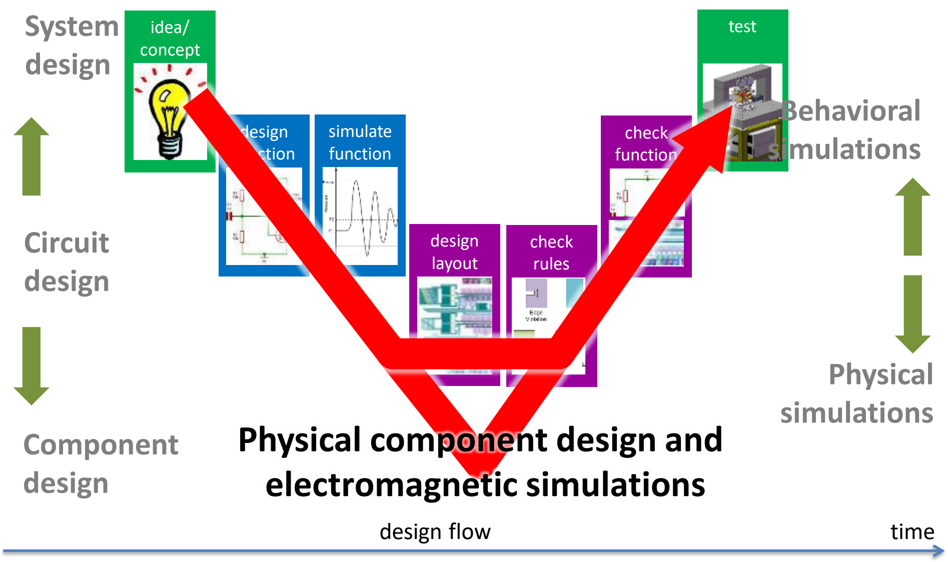
ABSTRACTIONS IN A DESIGN FLOW



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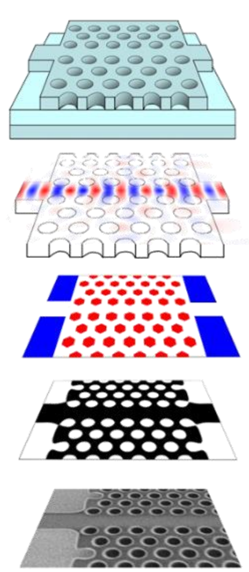
WHY MORE COMPONENT DESIGN IN PHOTONICS?



More geometric design freedom

- Photonic Crystals
- Subwavelength gratings
- Arbitrary holographic functions
- …

More complex behaviour

- Phase: interference effects
- Wavelength dependence
- Nonlinearities
- …

Requires accurate physical modelling

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COMPONENT DESIGN VS. CIRCUIT DESIGN

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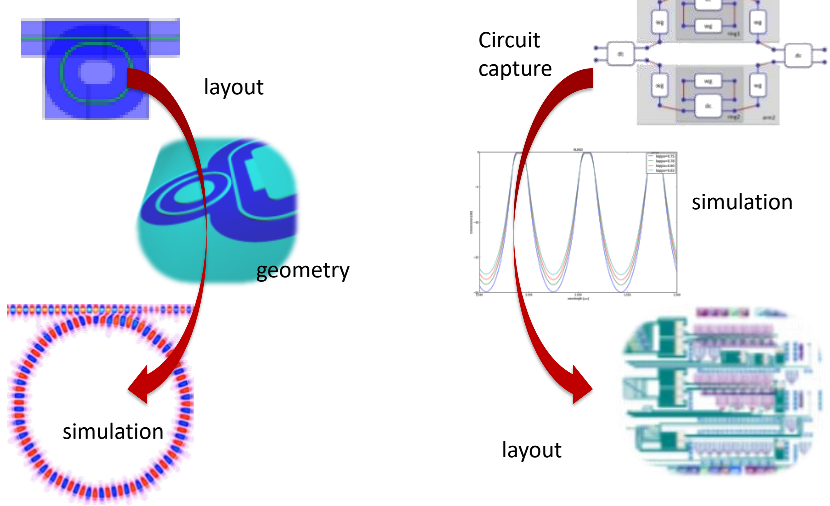
Component Design **Circuit design**



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PHOTONIC CIRCUIT DESIGN TOOLS

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Optiwave
SIMULIA
VPIphotonics DESIGN AUTOMATION
FILARETE
LUCEDA
Photon Design
Ansys lumerical illuminating the way
SYNOPSYS
cadence
SIEMENS Mentor
Nazca design

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TOOL CAPABILITIES

★ links to other tools (documented)

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	Component sim	Circuit Sim	Component Layout	Circuit Layout	Verification
SYNOPSYS	Fullwave Beamprop	OptSim	Optodesigner	Optodesigner	Optodesigner
cadence		Spectre AMS ★	Virtuoso	Virtuoso	Assura
SIEMENS Mentor		Eldo	L-Edit	L-Edit LightSuite	Calibre
LUCEDA	Camfr ★	Caphe	IPKISS	IPKISS	★
VPIphotonics	ModeDesigner	ComponentMaker			
lumerical Ansys	FDTDSolutions ModeSolutions Device	Interconnect			
Nazca design	★		Nazca	Nazca	
Photon Design	Fimmwave Omnisim	PICwave			
SIMULIA	CST studio				

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PHOTONIC CIRCUIT DESIGN: LEARNING CYCLES

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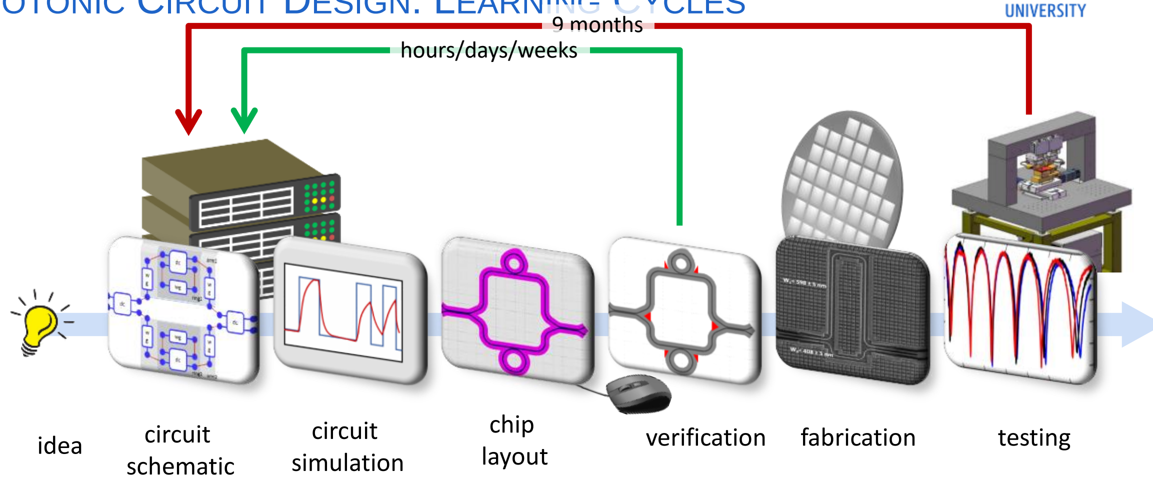

Learning cycles through fabrication take a lot of time.

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PROTOTYPING A NEW (SILICON) PHOTONIC IC

Design (4M)

Fabrication (6M)

Package (1M)

Test (2M)

Then you discover the bugs…

Repeat!

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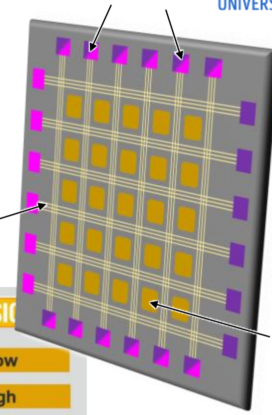
PROTOTYPING A NEW ELECTRONIC CIRCUIT

Select a suitable programmable IC: FPGA, DSP, μC (1d)

Program and test the chip (1-4w)

Only then, if needed:

- Design ASIC …



anysilicon	FPGA	ASI
Time to Market	Fast	Slow
NRE	Low	High
Design Flow	Simple	Complex
Unit Cost	High	Low
Performance	Medium	High
Power Consumption	High	Low
Unit Size	Medium	Low

AnySilicon.com

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The Photonic FPGAs?

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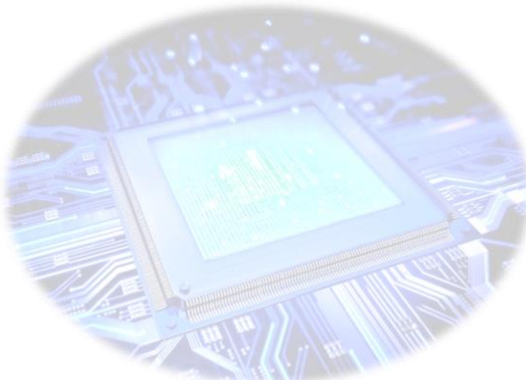
or programmable photonics

reconfigurable photonics

photonic processors

universal photonic circuits …



Photonic Integrated Circuits

that **can be reconfigured**

using **software**

to perform **different functions**.

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Programmable Photonic Chip

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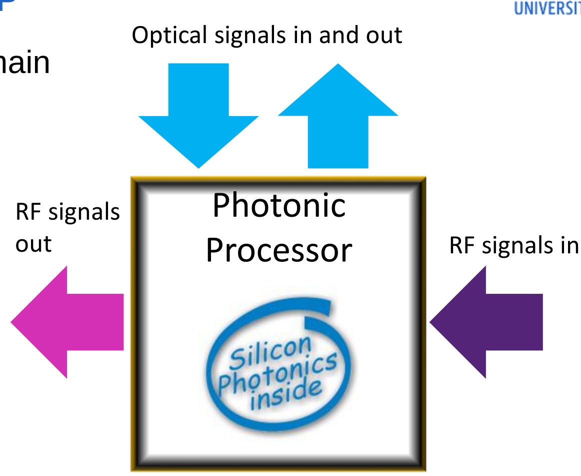
Can process signals in the optical domain

- balancing
- filtering
- transformations

Both on Optical and RF signals



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Generic Programmable Optical Processor

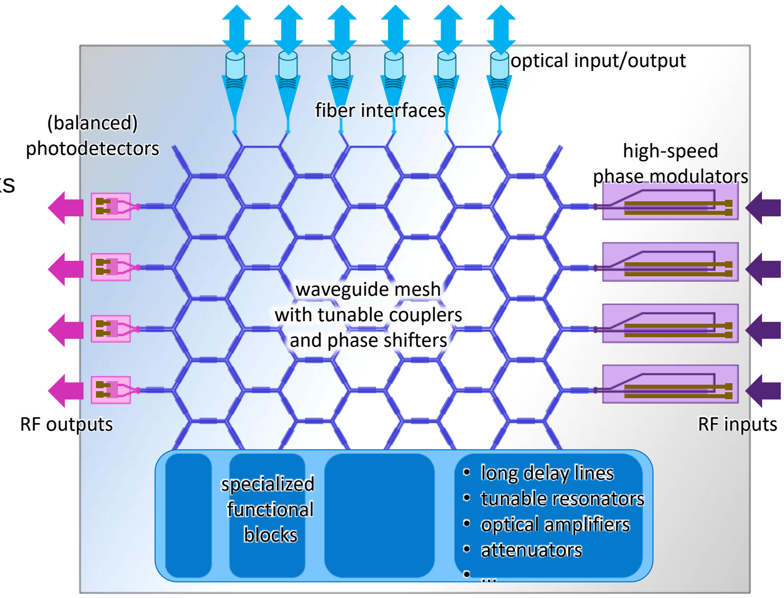
Optical inputs and outputs

RF inputs: modulators

RF outputs: balanced PDs

Specialized high performance blocks

Connected by a programmable linear optical circuit



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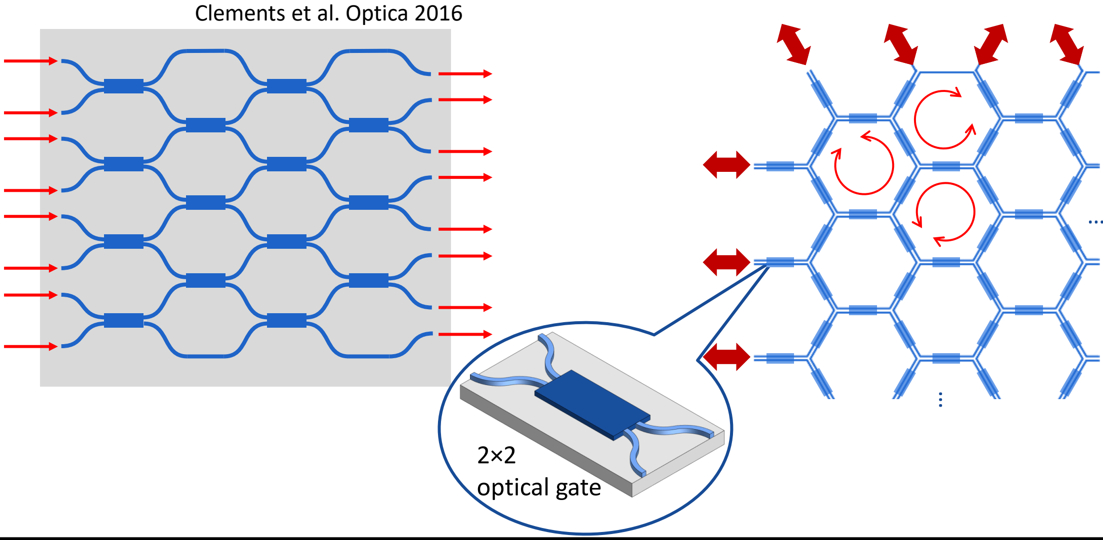
Programmable Waveguide Meshes

Forward meshes

Recirculating Meshes

Clements et al. Optica 2016



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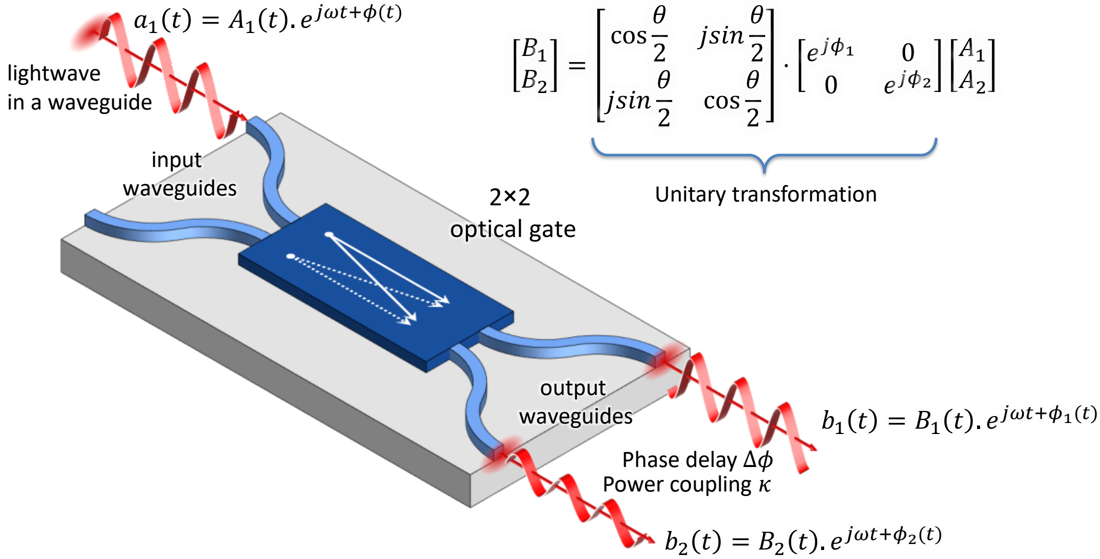
THE BASIC UNIT CELL: 2×2 UNITARY GATE

$$\begin{bmatrix} B_1 \\ B_2 \end{bmatrix} = \begin{bmatrix} \cos\frac{\theta}{2} & j\sin\frac{\theta}{2} \\ j\sin\frac{\theta}{2} & \cos\frac{\theta}{2} \end{bmatrix} \cdot \begin{bmatrix} e^{j\phi_1} & 0 \\ 0 & e^{j\phi_2} \end{bmatrix} \begin{bmatrix} A_1 \\ A_2 \end{bmatrix}$$

Unitary transformation



Review: Bogaerts et al, Nature 2020 177

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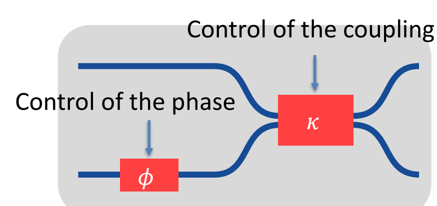
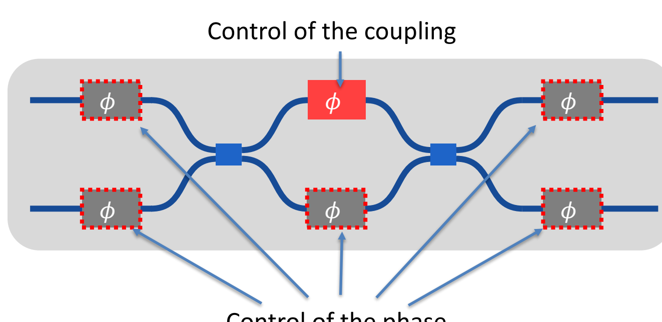
THE BASIC UNIT CELL: 2×2 UNITARY GATE

On-chip implementations:

at least 2 control points needed

- Phase shifter + Tunable Coupler
- Mach-Zehnder interferometer





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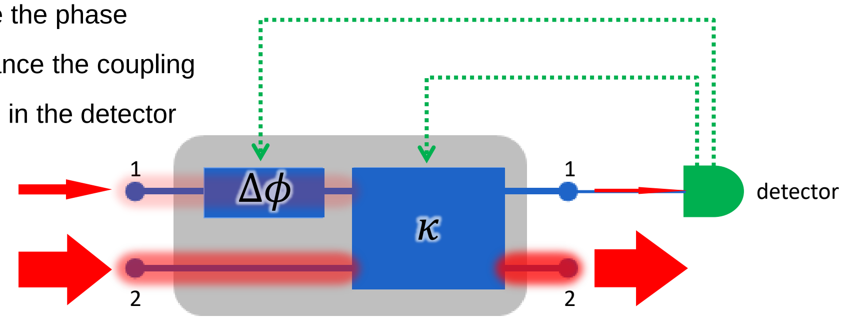
PROGRAMMING A 2X2 OPTICAL GATE

Coupling all light to output 2

Use monitor to tune the phase

Use monitor to balance the coupling

minimize the power in the detector



2x2 optical gate

Stanford University Miller, OpEx 2013 181

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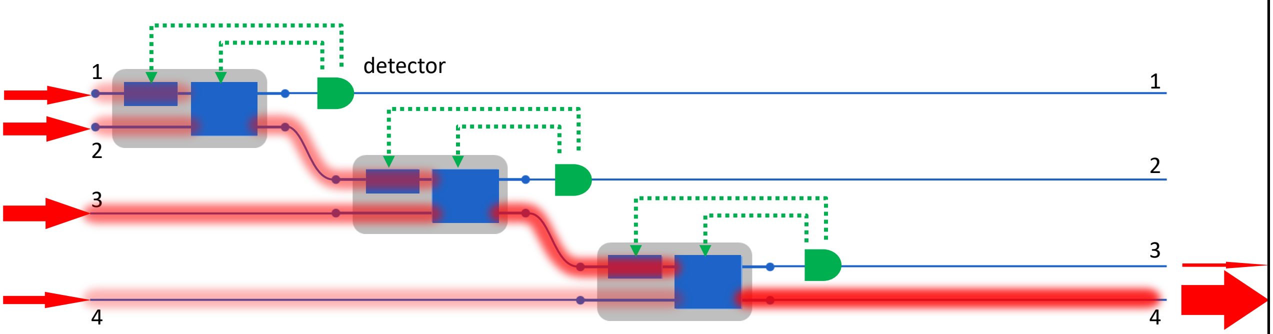
PROGRAMMING A 2X2 OPTICAL GATE



Cascading gates

Couple all light to output 4

Sequentially optimize 2x2 gates

Stanford University Miller, OpEx 2013 185

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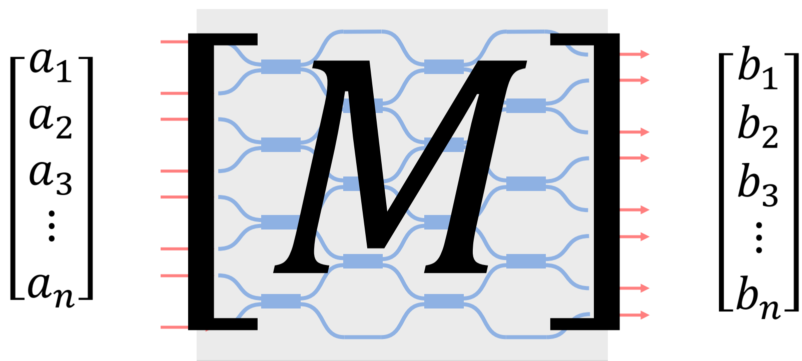
APPLICATIONS OF FORWARD-ONLY MESHES

Linear circuit performs real-time matrix-vector product (MAC operation)

$$\boldsymbol{b} = \boldsymbol{M} \cdot \boldsymbol{a}$$



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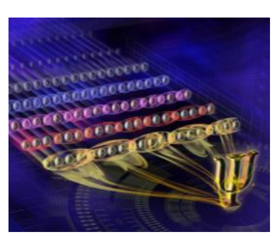
APPLICATIONS OF FORWARD-ONLY MESHES

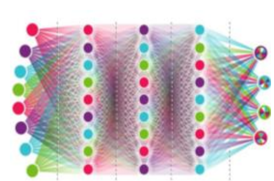
Linear circuit performs real-time matrix-vector product (MAC operation)

Basic operation in

$$\boldsymbol{b} = \boldsymbol{M} \cdot \boldsymbol{a}$$

- Pattern Recognition
- Linear Quantum Optics
- Artificial Neural Networks





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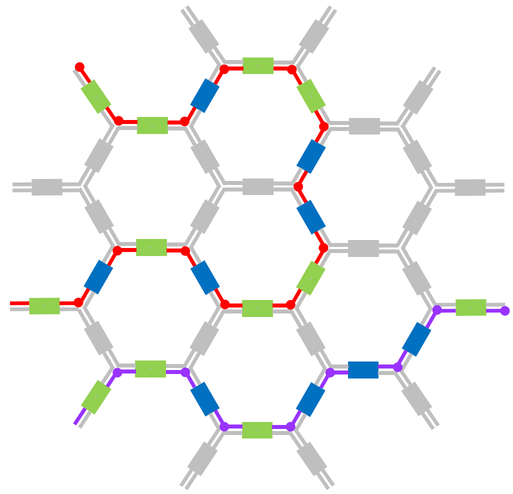
(Re)Routing light

Light can be arbitrarily routed

Multiple routes in the same mesh



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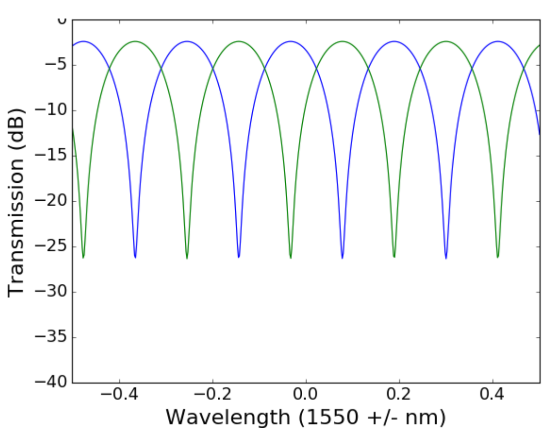
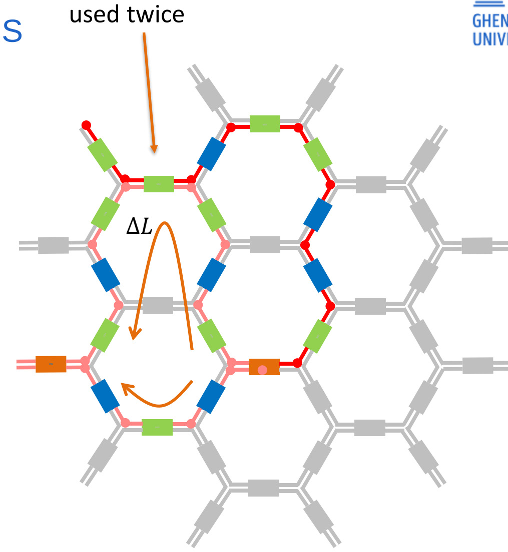
Mach-Zehnder interferometers

Basic building block for FIR filters

Delay can be adjusted per unit lengths





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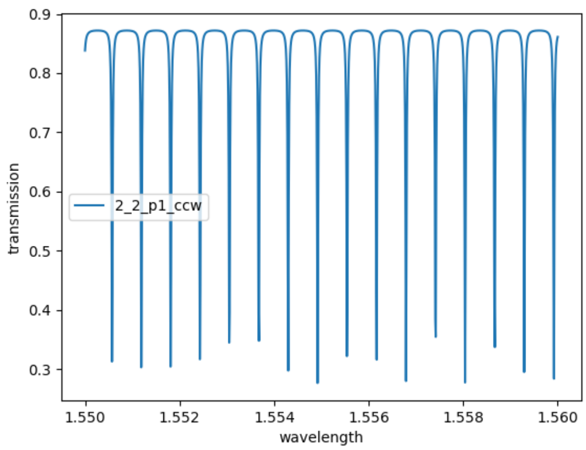
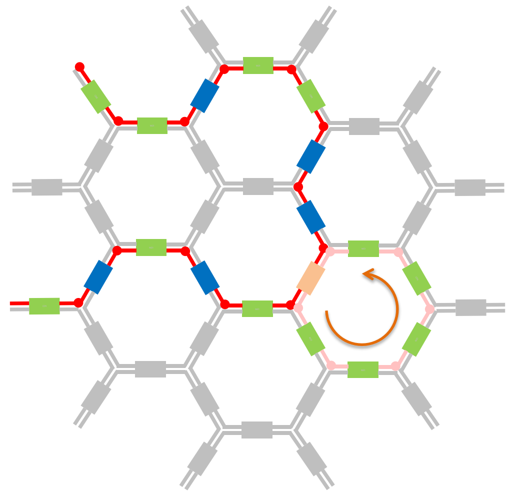
Ring Resonators

Loop light in itself

Coupler ring resonators together





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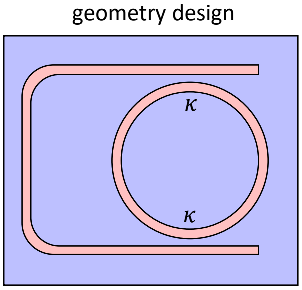
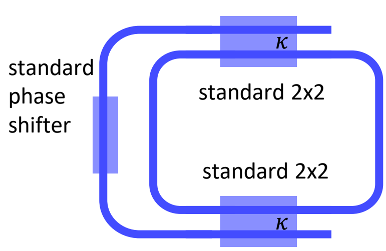
A New way of Designing Functionality

Full Custom design

geometry design

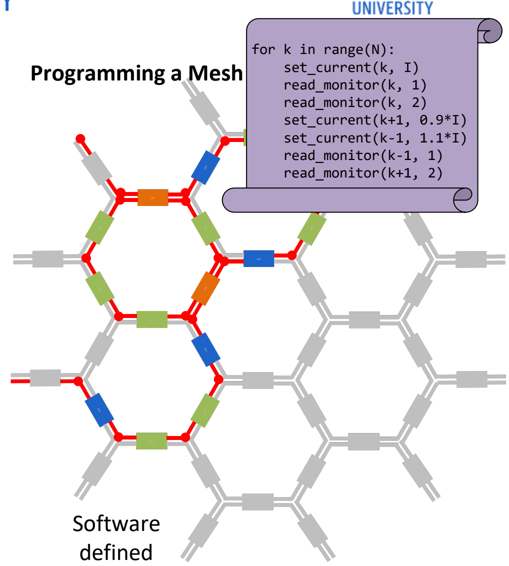


PDK-based Circuit Design



Custom circuit design with standard tunable couplers and phase shifters

Programming a Mesh



Software defined functionality

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NEW TYPES OF IP

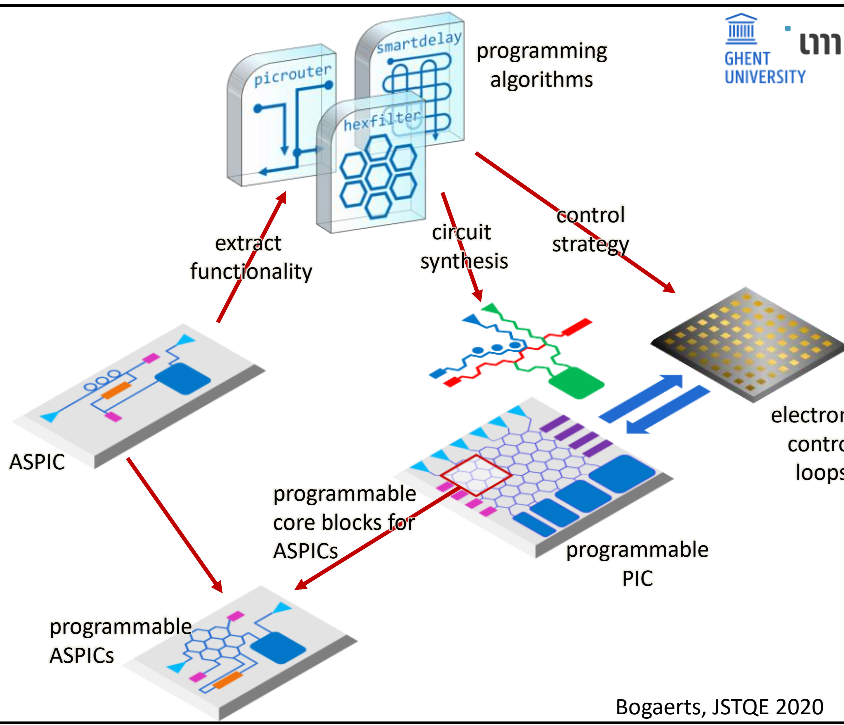
Programming routines

Circuit synthesis

Control strategies

Pluggable design IP

- linear cores
- electronic controls



Bogaerts, JSTQE 2020

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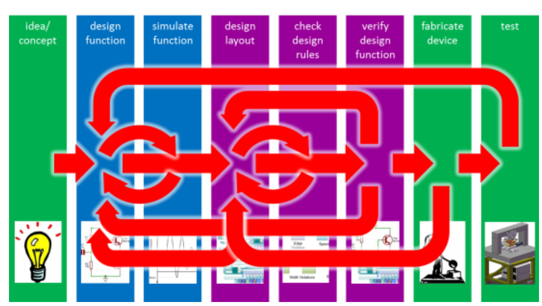
SUMMARY

(Silicon) Photonics is growing towards a circuit platform

- Technology supports larger circuits
- A circuit-oriented design flow is emerging (similar to electronics)
- Fabs are building PDKs

Challenges

- Schematic-driven Layout for photonics
- Variability: fabrication, performance, models
- Verification: DRC and LVS
- Design for manufacturability
- Photonic-electronic-software stacks
- New design methods for programmable photonics



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PRACTICAL SETUP

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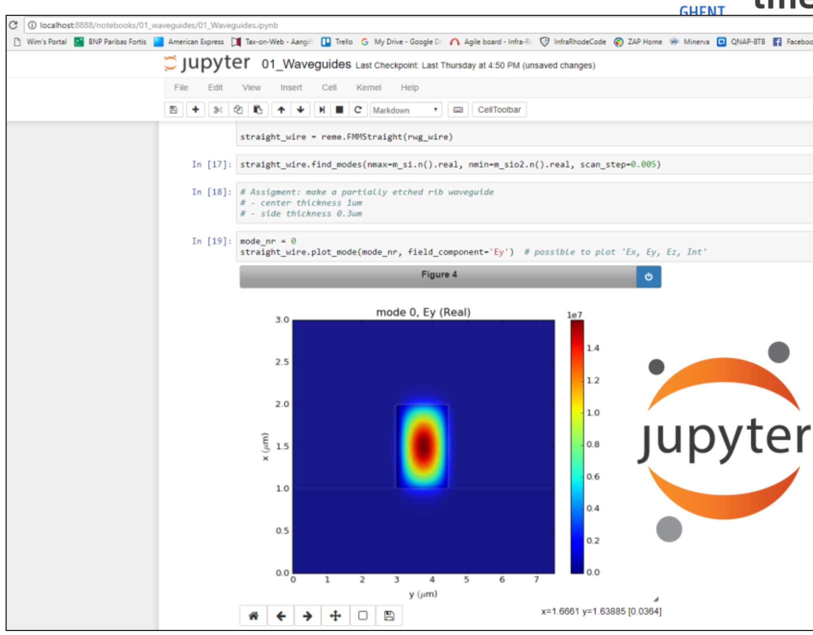
JUPYTER NOTEBOOKS

interactive notebook

- text, figures
- formulas
- python code

simulation and design

- built-in IPKISS



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The IPKISS Design Framework

LUCEDA GHENT UNIVERSITY imec

Design framework for Photonic Integrated Circuits

- Parametric design
- Focus on reuse and automation

History

- Developed at Ghent University – imec in 2000-2014
- Spin-off into Luceda Photonics in 2014
- Currently thousands of users worldwide

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The IPKISS Design framework

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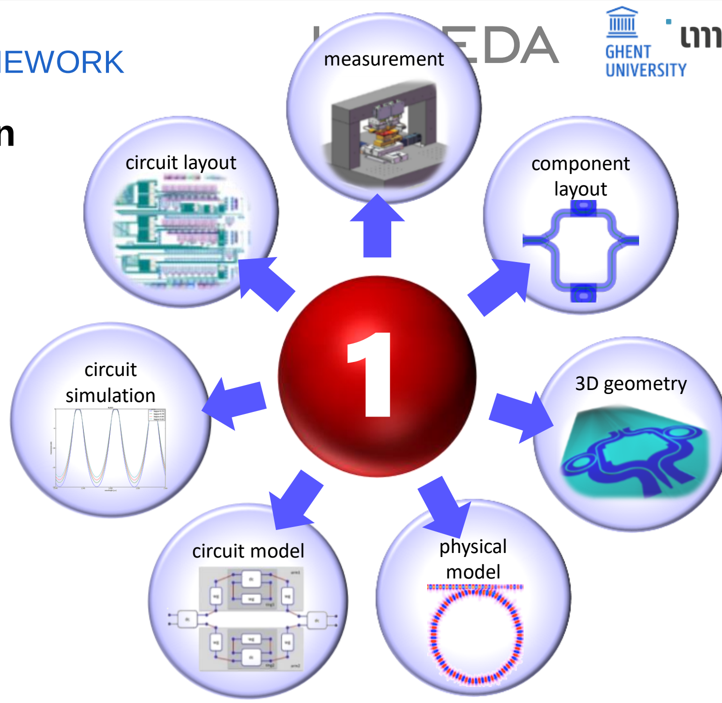
One component definition

for

Circuit design

Layout

Simulation



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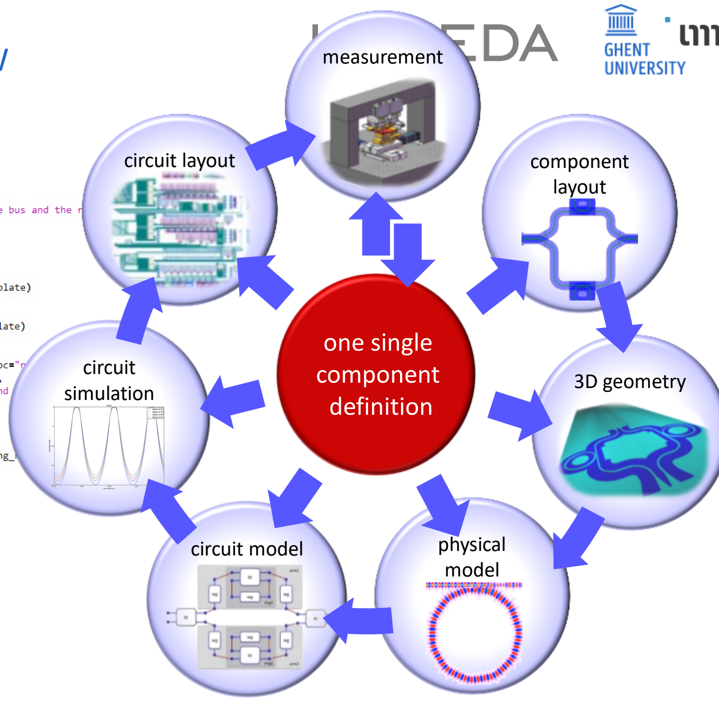
THE IPKISS DESIGN FLOW

Python script based

```
class RingResonator(i3.PCell):
    """A generic ring resonator class."""

    wg_template = i3.WaveguideTemplateProperty(default=TECH.PCELLS.WG.DEFAULT,
                                               doc="trace template used for the bus and the r

    bus = i3.ChildCellProperty(doc="bus waveguide")
    ring = i3.ChildCellProperty(doc="ring waveguide")

    def _default_ring(self):
        return i3.Waveguide(name=self.name+"_ring", trace_template=self.wg_template)

    def _default_bus(self):
        return i3.Waveguide(name=self.name+"_bus", trace_template=self.wg_template)

    class Layout(i3.LayoutView):
        ring_radius = i3.PositiveNumberProperty(default=TECH.WG.BEND_RADIUS, doc="r
        coupler_spacing = i3.PositiveNumberProperty(default=TECH.WG.DC_SPACING,
                                                    doc="spacing between bus and

        def _default_ring(self):
            ring_layout = self.cell.ring.get_default_view(i3.LayoutView)
            ring_layout.set(trace_template=self.wg_template,
                            shape=i3.ShapeCircle(center=(0, 0), radius=self.ring_
            return ring_layout

        def _default_bus(self):
            r, s = self.ring_radius, self.coupler_spacing
            bus_layout = self.cell.bus.get_default_view(i3.LayoutView)
            bus_layout.set(trace_template=self.wg_template,
                           shape=[(-r, -r-s), (+r, -r-s)])
            return bus_layout

        def _generate_instances(self, insts):
            insts += i3.SRef(name="ring", reference=self.ring)
            insts += i3.SRef(name="bus", reference=self.bus)
            return insts

        def _generate_ports(self, ports):
            ports += self.instances["bus"].ports
            return ports
```



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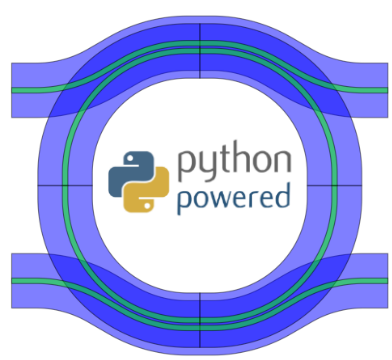
THE IPKISS DESIGN FLOW

LUCEDA

Python script based

```
class RingResonator(i3.PCell):
    """A generic ring resonator class."""

    wg_template = i3.WaveguideTemplateProperty(default=TECH.PCELLS.WG.DEFAULT,
                                               doc="trace template used for the bus and the ring")

    bus = i3.ChildCellProperty(doc="bus waveguide")
    ring = i3.ChildCellProperty(doc="ring waveguide")

    def _default_ring(self):
        return i3.Waveguide(name=self.name+"_ring", trace_template=self.wg_template)

    def _default_bus(self):
        return i3.Waveguide(name=self.name+"_bus", trace_template=self.wg_template)

    class Layout(i3.LayoutView):
        ring_radius = i3.PositiveNumberProperty(default=TECH.WG.BEND_RADIUS, doc="radius of ring")
        coupler_spacing = i3.PositiveNumberProperty(default=TECH.WG.DC_SPACING,
                                                    doc="spacing between bus and ring waveguide")

        def _default_ring(self):
            ring_layout = self.cell.ring.get_default_view(i3.LayoutView)
            ring_layout.set(trace_template=self.wg_template,
                            shape=i3.ShapeCircle(center=(0, 0), radius=self.ring_radius))
            return ring_layout

        def _default_bus(self):
            r, s = self.ring_radius, self.coupler_spacing
            bus_layout = self.cell.bus.get_default_view(i3.LayoutView)
            bus_layout.set(trace_template=self.wg_template,
                           shape=[(-r, -r-s), (+r, -r-s)])
            return bus_layout

        def _generate_instances(self, insts):
            insts += i3.SRef(name="ring", reference=self.ring)
            insts += i3.SRef(name="bus", reference=self.bus)
            return insts

        def _generate_ports(self, ports):
            ports += self.instances["bus"].ports
            return ports
```



- extremely flexible
- easy-to-read
- powerful engineering libraries
- industry standard

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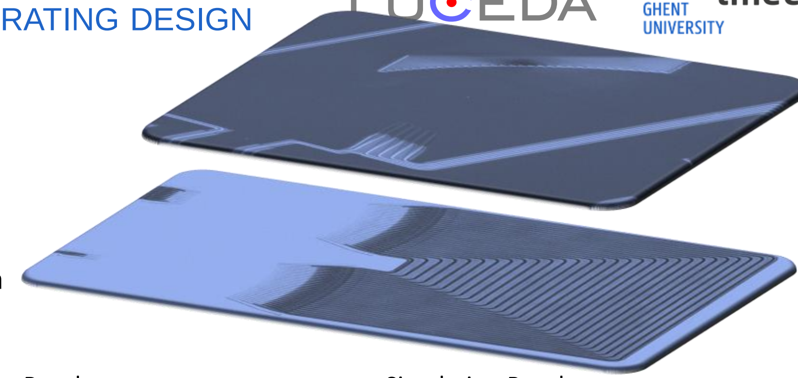
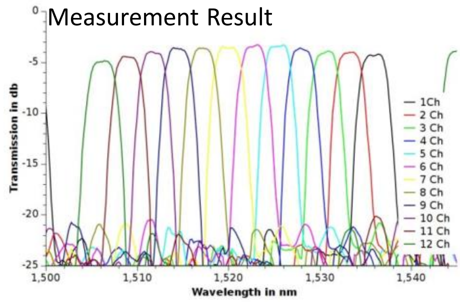
ARRAYED WAVEGUIDE GRATING DESIGN

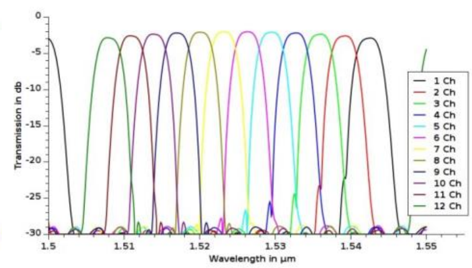
Arrayed Waveguide Gratings

Echelle Gratings

- Fully parametric
- Design from specifications
- Integrated layout and simulation
- Validated on fabricated devices







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IPKISS NOTEBOOKS

Explore your designs in a browser

Very rapid experimentation

Interactive code and plots

Widely supported community

Powered by jupyter

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FIRST NOTEBOOKS

Unfamiliar with Python?

/01_01_jupyter_notebooks: *How to use a notebook*

/01_02_python_getting_started: *basic Python tutorial*

/01_03_ numpy_and_plotting: *Numpy and Matplotlib*

Check if everything works and if you find your way around the notebook interface.

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PRACTICAL

1. Connect to the Wifi network
2. Open web browser (Chrome, Firefox, Opera)
3. Connect to Jupyter server
4. Log in with your personal ID/password

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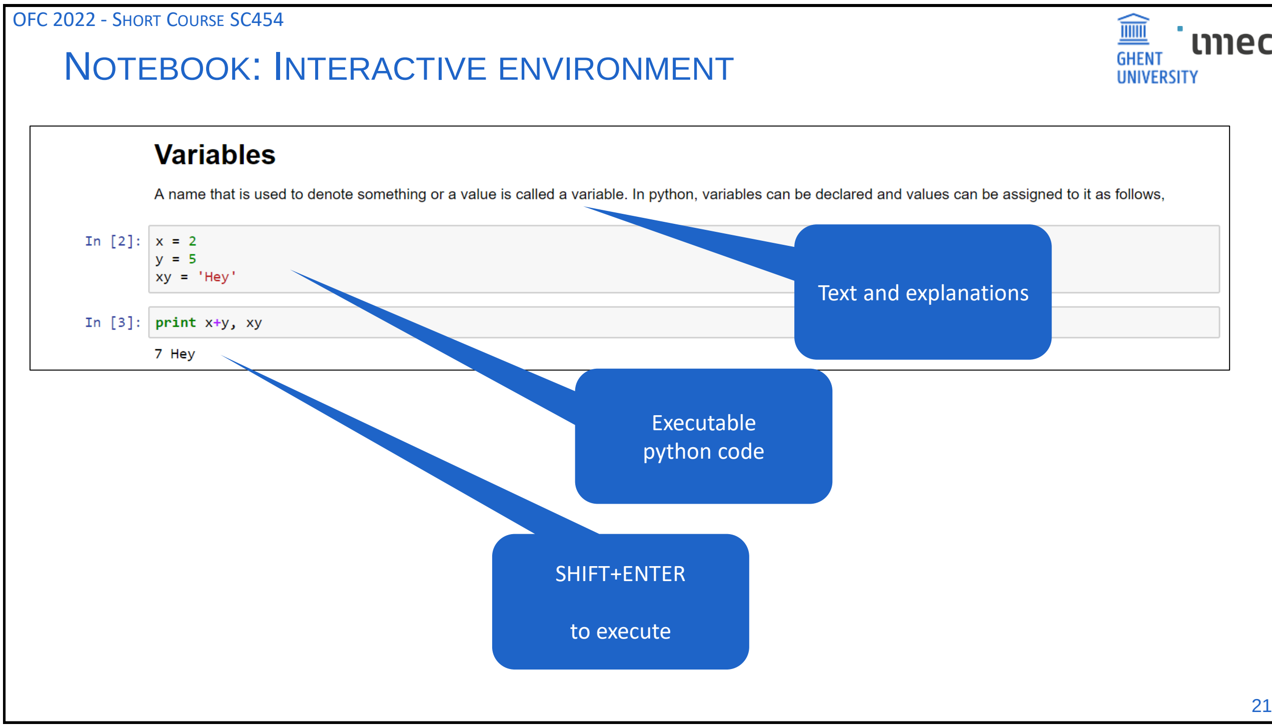
OFC 2022 - Short Course SC454
Notebook: Interactive environment
GHENT UNIVERSITY
imec
Variables
A name that is used to denote something or a value is called a variable. In python, variables can be declared and values can be assigned to it as follows,
In [2]: x = 2
y = 5
xy = 'Hey'
In [3]: print x+y, xy
7 Hey
Text and explanations
Executable python code
SHIFT+ENTER to execute
213

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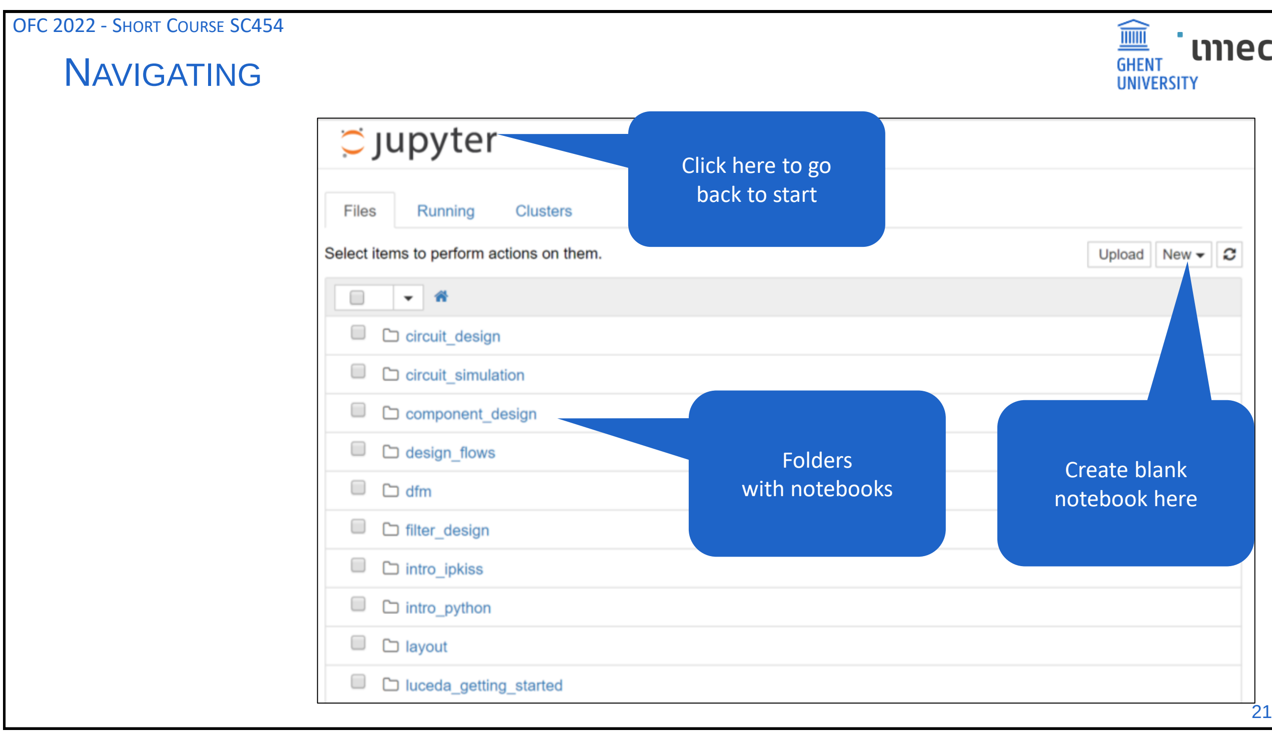
OFC 2022 - Short Course SC454
Navigating
GHENT UNIVERSITY
imec
jupyter
Click here to go back to start
Files
Running
Clusters
Select items to perform actions on them.
Upload
New
circuit_design
circuit_simulation
component_design
design_flows
dfm
filter_design
intro_ipkiss
intro_python
layout
luceda_getting_started
Folders with notebooks
Create blank notebook here
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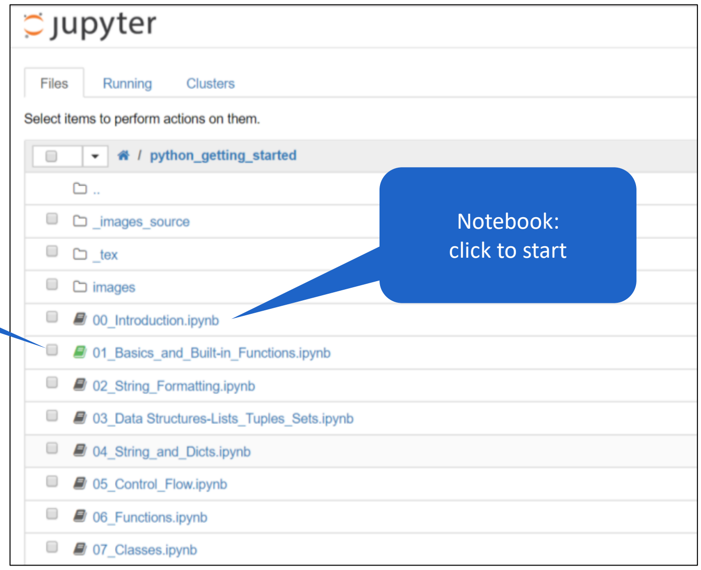
NAVIGATING

Running Notebook

Notebook: click to start



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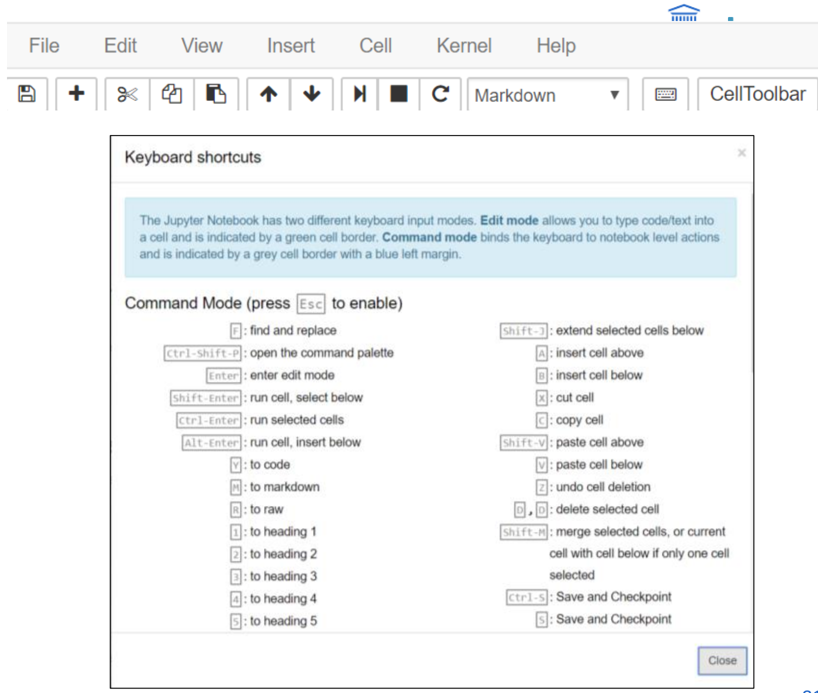
PRESS H FOR 'HELP'

Useful menu and toolbar

Keyboard shortcuts are extremely powerful



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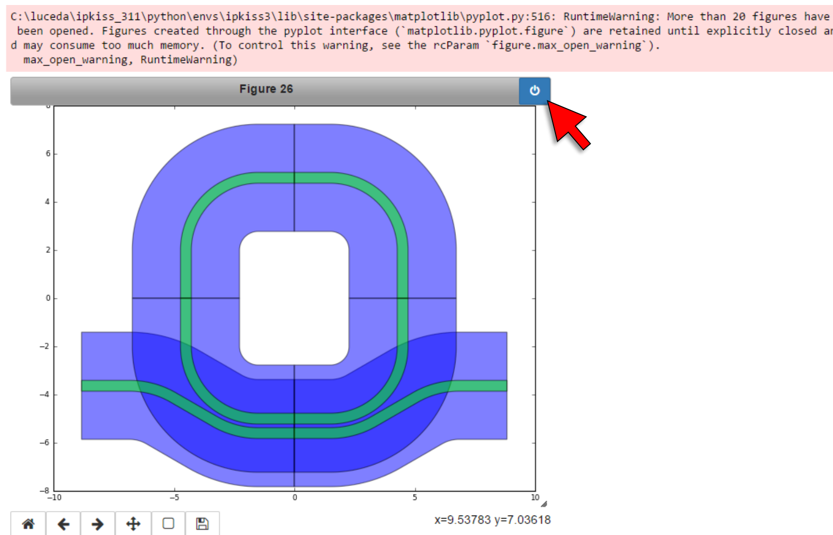
Take care of Memory

Interactive plots consume resources.

Close them when ready.



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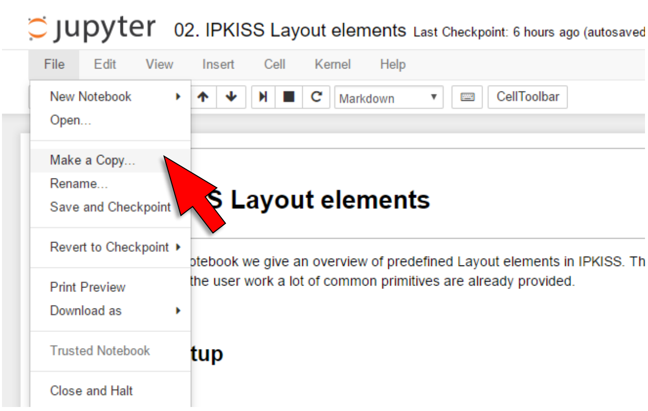
Getting started…



- open browser (Chrome, Firefox)
- connect to notebook server: https://wscarapils.intec.ugent.be
- notebook login / password

Launch a notebook

Step 1:
Copy the notebook

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Building your first Photonic Circuits

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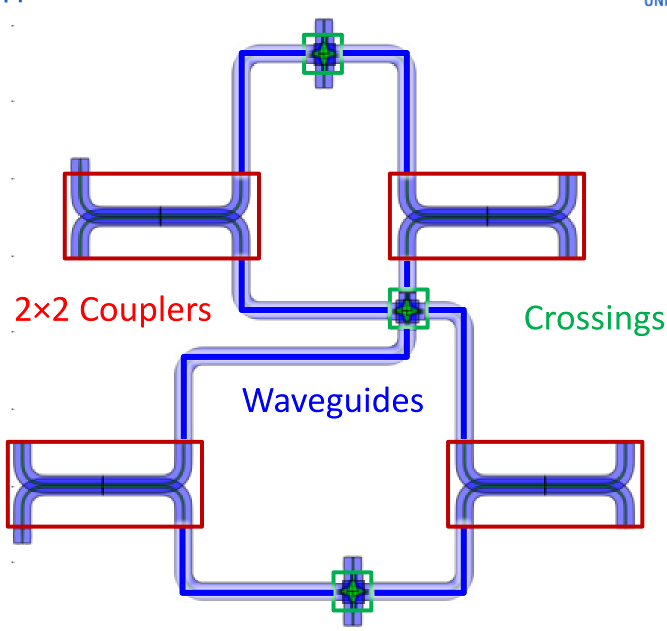
A simple passive circuit

- Four 2×2 couplers
- 3 Crossings
- Connection waveguides



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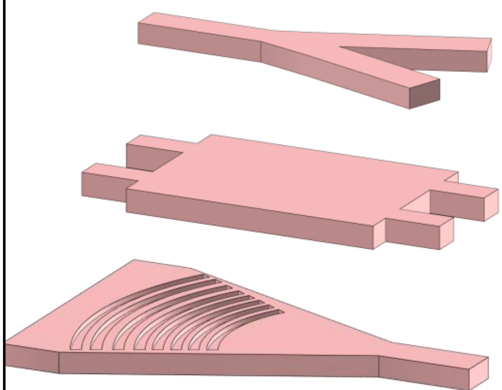
BUILDING BLOCKS



Passive: waveguides, splitters, couplers, crossings

Active: modulators, detectors, tuners

Where do they come from?

- Make them yourself
- Use existing blocks
  - From a shared library
  - From the fab : **Process Design Kit (PDK)**
- Building blocks are **process-specific**

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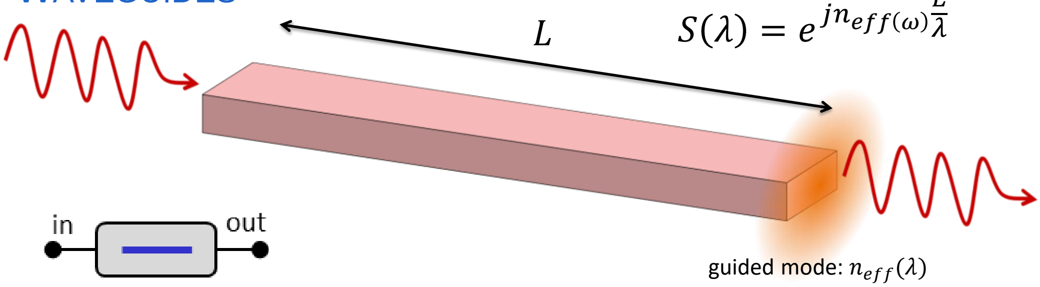
WAVEGUIDES

$$S(\omega) = e^{j2\pi c n_{eff}(\omega) L/\omega}$$

$$S(\lambda) = e^{j n_{eff}(\omega)\frac{L}{\lambda}}$$



Propagate light from the input to the output

- wavefronts propagate with velocity $v_{ph}(\lambda) = \frac{c}{n_{eff}(\lambda)}$
  ($n_{eff}(\lambda)$= effective refractive index)
- Dispersion: $n_{eff}(\lambda)$ is wavelength dependent
- Group velocity: time delay of a wave packet: $v_g(\lambda) = \frac{c}{n_g(\lambda)}$

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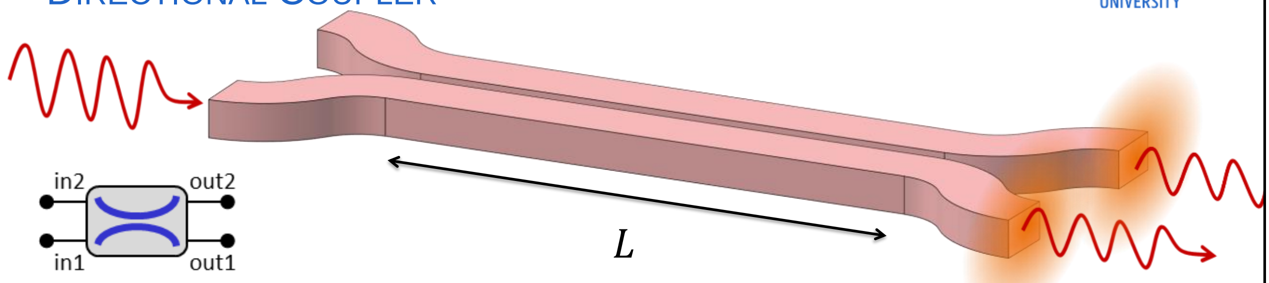
Directional Coupler



Very common implementation of 2×2 coupler

- based on interference of even and odd mode in waveguide pair
- Power coupling: $K = \sin^2(\kappa_0 + L.\kappa')$

coupling in the bends

coupling in straight section

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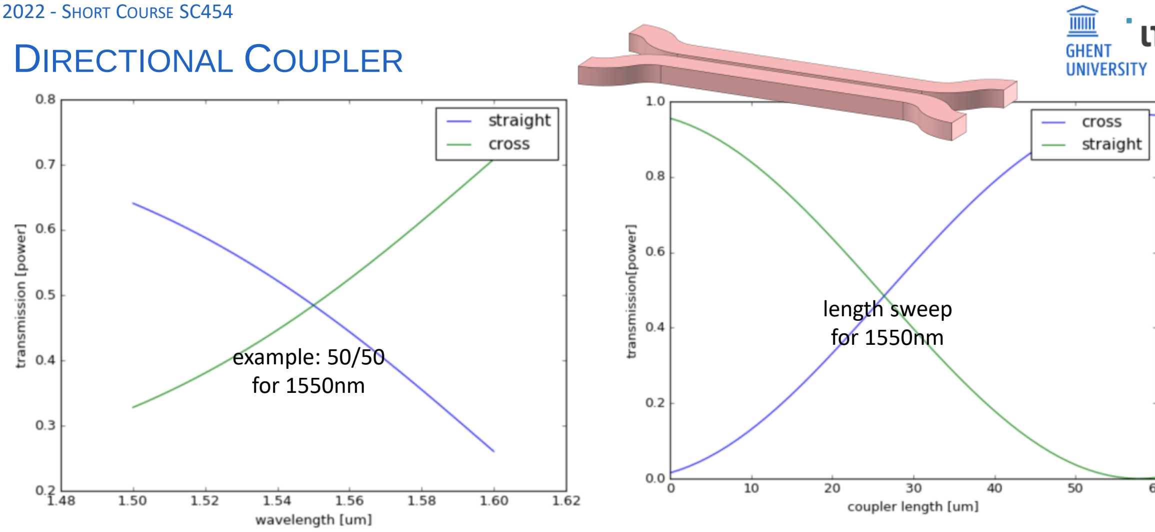
Directional Coupler



$K = \sin^2(\kappa_0 + L.\kappa')$

κ_0 and κ' are wavelength dependent

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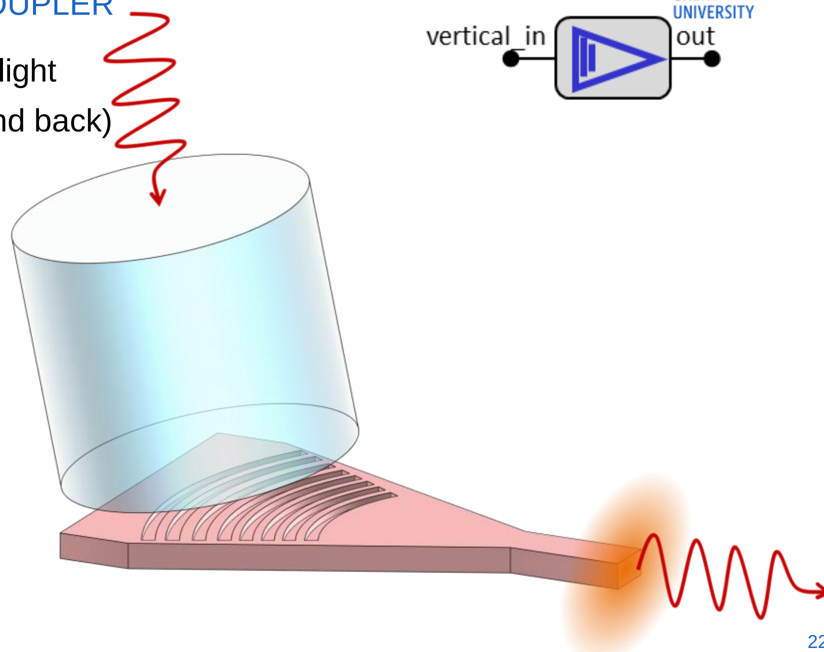
Example: Grating coupler

Diffraction grating couples light from fiber to waveguide (and back)

- wavelength dependent



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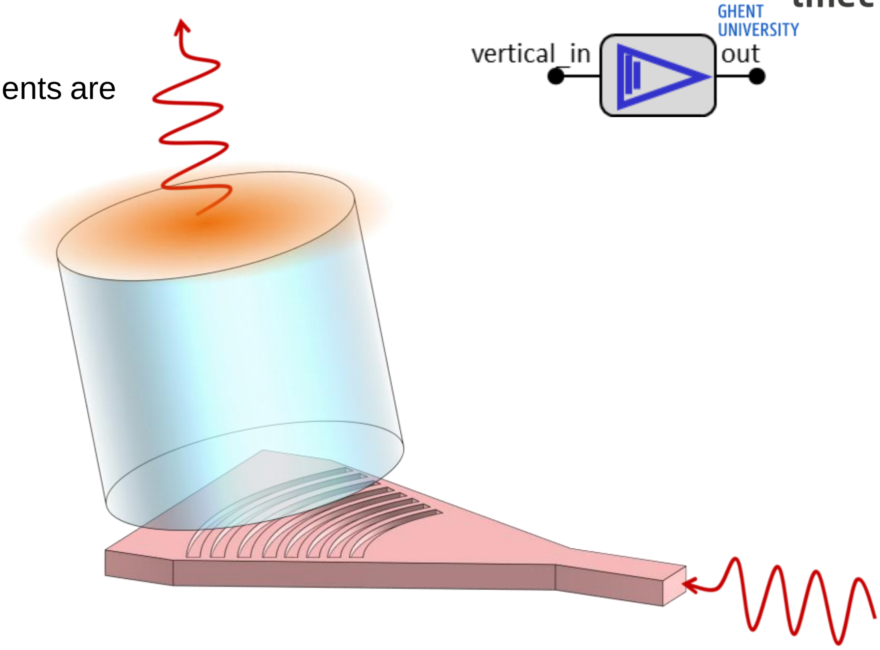
Reciprocity

Linear, passive components are reciprocal

$$S_{21}(\omega) = S_{12}(\omega)$$



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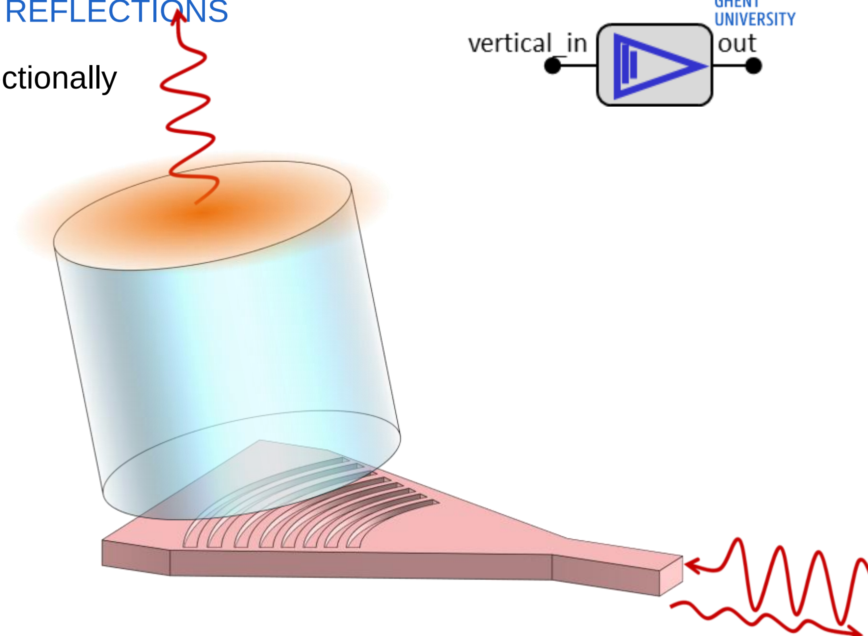
S-Matrix includes reflections



circuits propagate bidirectionally

e.g. Grating coupler
has reflections

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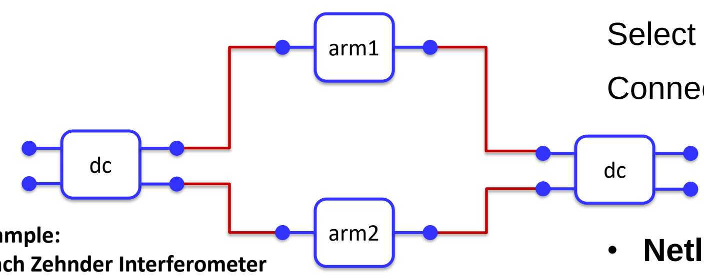
Connecting Components into Circuits



Example:
Mach Zehnder Interferometer

Select functional blocks

Connect them together

- **Netlist**:
  list of connections ("Nets") and which components the nets are attached to.
- **Schematic**:
  graphical representation of a netlist, with placements

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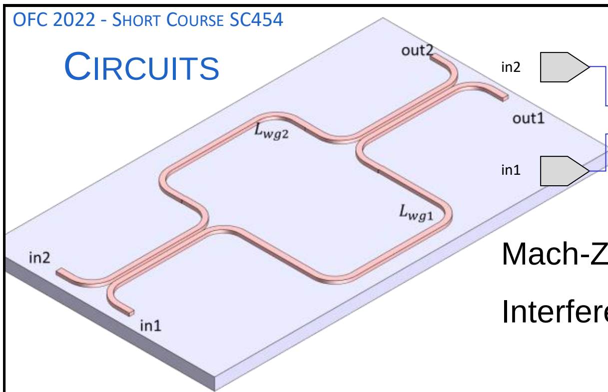
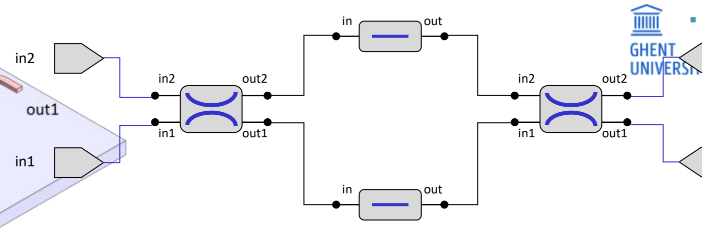
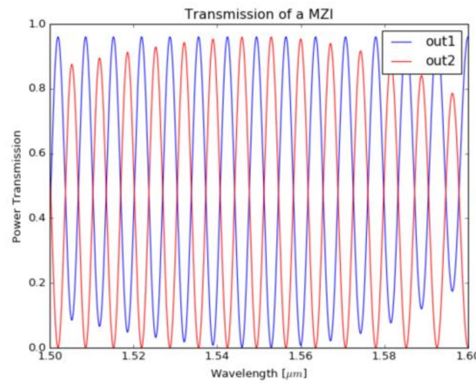
CIRCUITS





Mach-Zehnder interferometer

Interference with a delay: Periodic response



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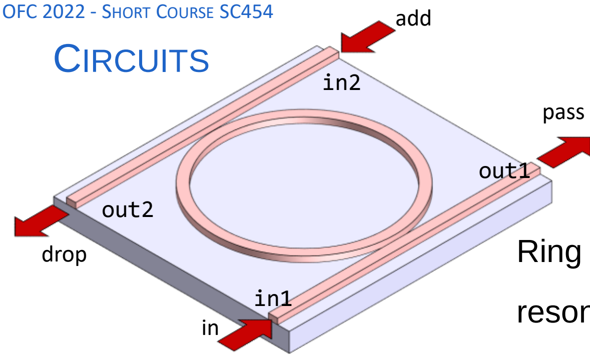
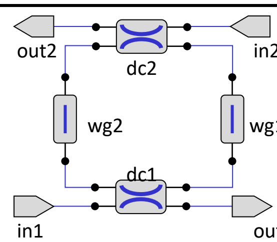
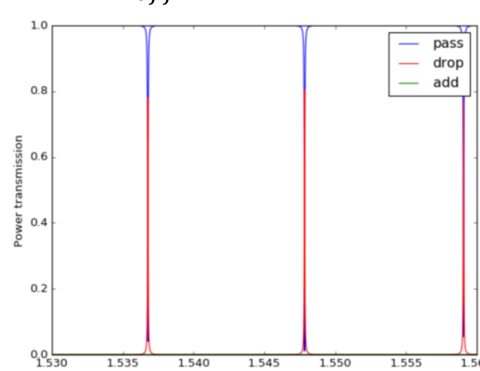
CIRCUITS





Ring Resonator: light circulates in the ring

resonance when $L.n_{eff}(\lambda) = m.\lambda$



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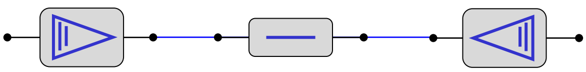
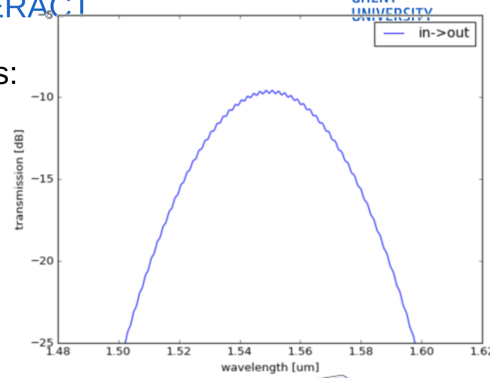
CIRCUIT EFFECTS: COMPONENTS CAN INTERACT

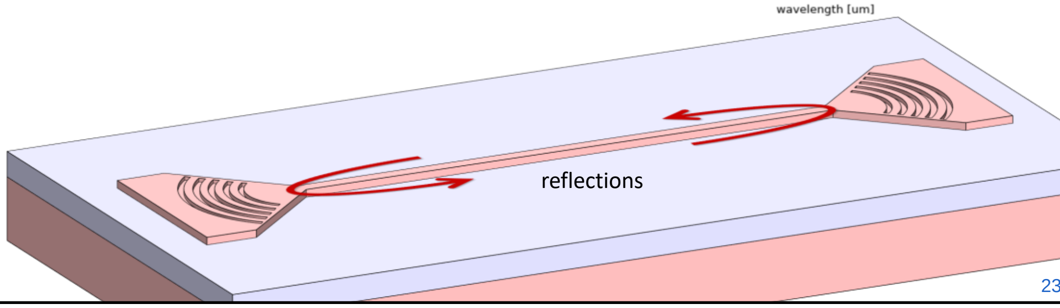
Example: weak reflections on two grating couplers:

A Fabry-Perot cavity is formed

Interference causes ripple on the transmission







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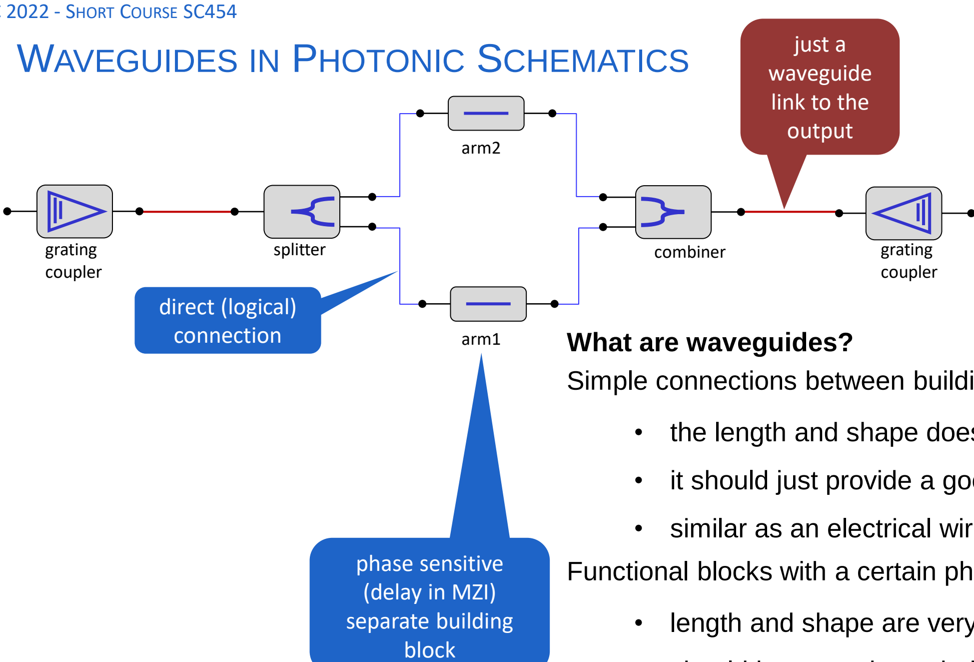
WAVEGUIDES IN PHOTONIC SCHEMATICS



What are waveguides?

Simple connections between building blocks

- the length and shape does not really matter
- it should just provide a good connection
- similar as an electrical wire

Functional blocks with a certain phase/time delay

- length and shape are very important
- should be treated as a building block

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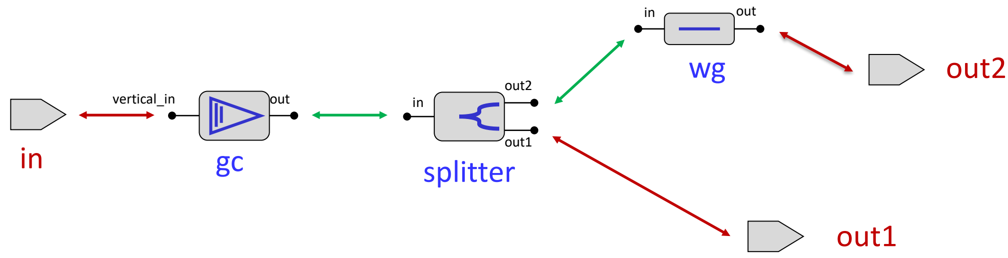
Building Circuits in a Jupyter Notebook



Define schematics in python code

- List building blocks (or subcircuits)
  - gc, splitter, wg
- List internal connections
  - gc:out↔splitter:in, splitter:out2↔wg:in
- List external ports
  - in ↔gc:vertical_in, out1 ↔ splitter:out1, out2 ↔wg:out

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Building Circuits: AutoPlaceAndConnect

Circuits with direct connections: no waveguide generation

```
from addon_luceda.auto_place_and_connect import AutoPlaceAndConnect

child_cells = {"dc1": my_dircoup,
               "dc2": my_dircoup,
               "wg1": my_wg,
               "wg2": my_wg}

links = [("dc1:out2", "wg1:in"),
         ("wg1:out" , "dc2:in2"),
         ("dc2:out2", "wg2:in"),
         ("wg2:out", "dc1:in2")]

external_port_names = {"dc1:in1"  : "in1",
                       "dc1:out1" : "out1",
                       "dc2:in1"  : "in2",
                       "dc2:out1" : "out2"}

my_ring = AutoPlaceAndConnect(child_cells=child_cells,
                              links=links,
                              external_port_names=external_port_names)
my_ring_lo = my_ring.Layout()
my_ring_lo.visualize(annotate=True)
```

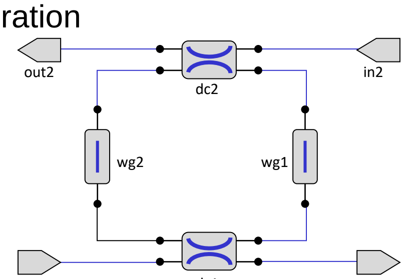
4 components

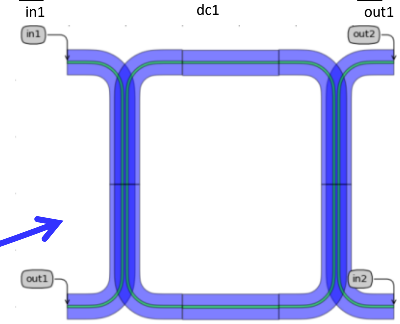
4 internal connections

4 input/output ports

automatic placement

auto-generate layout





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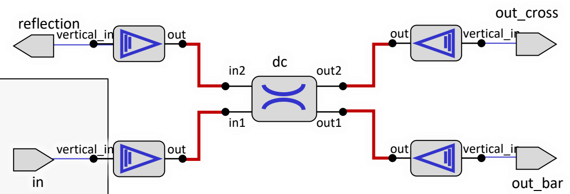
BUILDING CIRCUITS: PLACEANDAUTOROUTE

Generate waveguides for connections




```
from picazzo3.routing.place_route import PlaceAndAutoRoute

dc_circuit = PlaceAndAutoRoute(name="dc_with_gc",
                               child_cells={"dc": my_dc,
                                            "gc_in" : fc,
                                            "gc_out_bar" : fc,
                                            "gc_out_cross" : fc,
                                            "gc_reflection" : fc
                                            },
                               links=[("gc_in:out", "dc:in1"),
                                      ("gc_reflection:out", "dc:in2"),
                                      ("dc:out1", "gc_out_bar:out"),
                                      ("dc:out2", "gc_out_cross:out"),
                                      ],
                               external_port_names={"gc_in:vertical_in": "in",
                                                    "gc_out_bar:vertical_in": "out_bar",
                                                    "gc_out_cross:vertical_in": "out_cross",
                                                    "gc_reflection:vertical_in": "reflection"}
                               )

transformations = {"gc_in": i3.Translation((-100,-20)),
                   "gc_out_cross": i3.Rotation(rotation=180) + i3.Translation((100, +20)),
                   "gc_out_bar": i3.Rotation(rotation=180) + i3.Translation((100, -20)),
                   "gc_reflection": i3.Rotation(rotation=180) + i3.Translation((100, +60)),
                   }

dc_circuit_layout = dc_circuit.Layout(child_transformations=transformations,
                   bend_radius=10.0)
dc_circuit_layout.visualize(annotate=True)
```

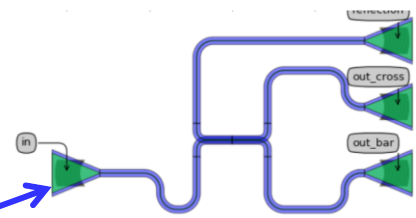
5 components

4 internal connections

4 input/output ports

manual placement

auto-generate layout



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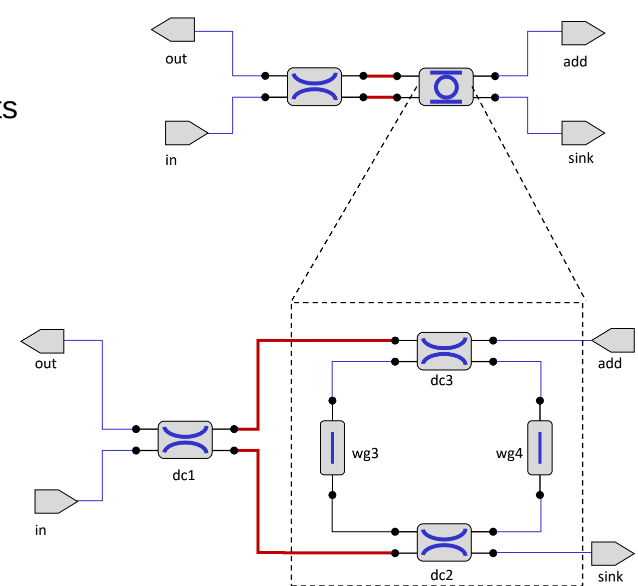
USE HIERARCHY: YOU CAN USE A CIRCUIT AS A BUILDING BLOCK

Circuits can be nested

Break up circuits into reusable parts



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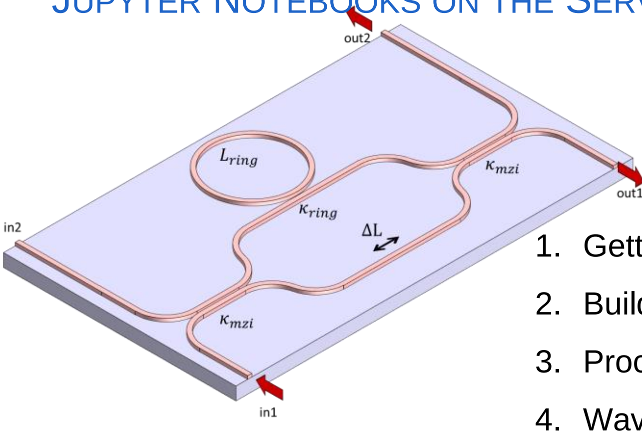
JUPYTER NOTEBOOKS ON THE SERVER



1. Getting started: Python, notebooks, IPKISS
2. Building a first circuit
3. Process Design Kits and Design Rule checking
4. Wavelength Filters: Rings, MZIs, AWGs
5. Programmable Photonics
6. Design Examples

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THE SMALL PRINT ON COPYRIGHT

The material on the server is copyrighted

- The IPKISS toolset
- The addon libraries
- The notebooks

Please do not download the material to your own PC. It will probably not work as the server has a specific set of pre-configured utilities.

Interested in using IPKISS, contact info@lucedaphotonics.com

Interested in using the course material, contact wim.bogaerts@ugent.be

You can continue to use the server until 30 June 2022.

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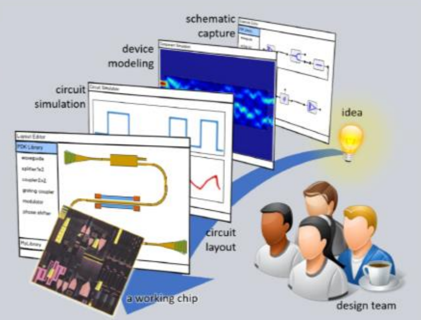
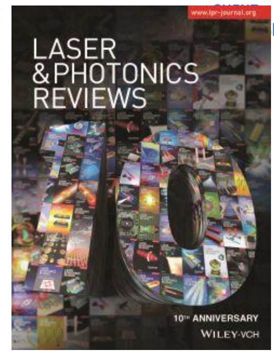
Further reading

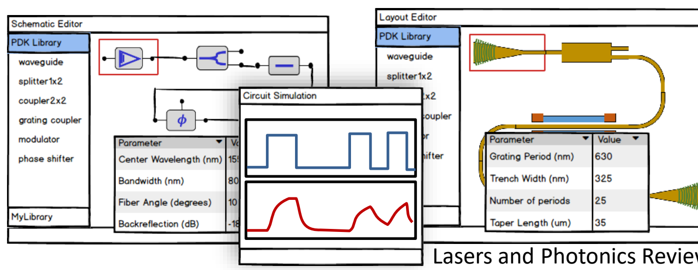
Abstract Silicon Photonics technology is rapidly maturing as a platform for larger-scale photonic circuits. As a result, the associated design methodologies are also evolving from component-oriented design to a more circuit-oriented design flow, that makes abstraction from the very detailed geometry and enables design on a larger scale. In this paper, we review the state of this emerging photonic circuit design flow and its synergies with electronic design automation (EDA). We cover the design flow from schematic capture, circuit simulation, layout and verification. We discuss the similarities and the differences between photonic and electronic design, and the challenges and opportunities that present themselves in the new photonic design landscape, such as variability analysis, photonic-electronic co-simulation and compact model definition.





Silicon Photonics Circuit Design: Methods, Tools and Challenges

Wim Bogaerts[1,2,*] **and Lukas Chrostowski**[3]



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