Open-Access Silicon Photonics Platforms in Europe

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***Abstract*—Offering open-access silicon photonics-based technologies has played a pivotal role in unleashing this technology from research laboratories to industry. Fabless enterprises rely on the open-access of these technologies for their product development. In the last decade, a diverse set of open-access technologies with medium and high technology readiness levels have emerged. This paper provides a review of the open-access silicon and silicon nitride photonic IC technologies offered by the pilot lines of European research institutes and companies. The paper also highlights upcoming features of these platforms and discusses how they address the long-term market needs.**

***Index Terms*—Silicon photonics, Silicon-on-Insulator, Silicon Nitride, CMOS, foundry, open-access, photonic integrated circuits, photonic manufacturing.**

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I. Introduction

THE key asset of silicon photonics stems from its ability to provide compact form-factor, high-performance and low-cost *Photonic Integrated Circuits* (PICs) [1], [2]. Silicon photonics uses high-index contrast material systems for PIC manufacturing to provide dense and large-scale integration of complex photonic functions. Such high-index contrast materials require a manufacturing process that can ensure nm-scale process control to deliver high-performance PICs [3]–[5]. This allows silicon photonics to benefit from the existing and well-established *Complementary Metal-Oxide Semiconductor* (CMOS) manufacturing technology, which results in the low-cost manufacturing of PICs through economics of scale [7], [9]. The cost-effectiveness of silicon photonics even holds for modest volumes by using the existing CMOS-fabs that are fully loaded with electronics CMOS manufacturing [6].

The public and private investment in R&D has led to a rapid development of silicon photonics technologies in the last two decades. CMOS pilot lines and advanced research institutes [10]–[17] have played a pivotal role by: (a) continuously evolving and maturing the technology platforms to reach a high *Technology Readiness Level* (TRL);[1] and (b) making these platforms accessible with minimal restriction and at low-cost to third parties for validating their design innovations. This open-access model enables an economically viable and low-barrier access to fabless companies where such companies bank on the off-the-shelf *Intellectual Property* (IP) and technology processes of pure-play foundries for PIC prototyping and manufacturing.

The open-access foundry model is one of the success stories of semiconductor electronics [18]. In Europe, CMOS pilot lines of advanced research institutes imitated this model for silicon photonics-based technologies. For example, ePIXfab – a joint

[1]The TRL-level of various open-access silicon photonics platforms discussed in this paper follows the definitions provided in the Appendix.

initiative by imec in Belgium and CEA-LETI in France – hosted from Ghent University in Belgium, pioneered open-access silicon photonics technologies in 2006 [7]. Later on this initiative expanded to include other European research institutes [8][2]. Followed by that, similar initiatives such as Optoelectronic Systems Integration in Silicon (OpSIS) [19], A*STAR Institute of Microelectronics (IME) [16] and American Institute for Manufacturing Integrated Photonics (AIM Photonics) [13] have emerged to strengthen the open-access foundry model for silicon photonics.

Open-access silicon photonics technologies are offered in different modes of access. The type of access-mode can depend on: (a) the nature of innovation (i-e, academic or industrial) or (b) the phase of the design innovation (i-e, a proof-of-concept, prototyping or scale-up for manufacturing). For example, the *Multiproject Wafer* (MPW) approach is the mode where a user shares the design area with various other users. The sharing of the mask and fabrication cost among these users make MPW an excellent low-cost path for proof-of-concept experiments at academic or industrial early stage R&D [6], [19], [20]. The platforms offered by MPW are versatile to address demands from a broad range of applications. Typically in MPW mode, each user gets a few tens of chips fabricated by using the generic baseline technology offered by the fab. On the other hand, through *(customized) dedicated engineering runs* an end-user gets the full reticle on a full lot of wafers (typically 20 to 25 wafers) with the optional flexibility to have customized processes to meet targeted specifications. Though considerably more expensive than MPW, they provide a large number of chips to determine the maturity of the design and fabrication process. As the PIC design meets the performance specifications, the customer may seek routes for low-, medium-, or high-volume manufacturing, depending on the needs of the application.[3] In some cases, CMOS pilot lines provide low- and medium-volume manufacturing of silicon PICs, typically up to several hundred wafers per order. With the growing industrial interest in high-volume manufacturing of silicon photonics products for telecommunication/datacommunication applications, which is the biggest driver for this technology since its inception, pure-play fabs have started developing open-access silicon photonics technologies [21]. In certain cases, the CMOS pilot lines and research institutes partner with pure-play CMOS fabs for the seamless translation from prototyping towards high-volume manufacturing [22].

While originally silicon photonics was synonymous for PIC-platforms based on *Silicon-on-Insulator* (SOI) wafers with waveguides with a silicon core, the field has diversified to some extent to include other material stacks that can be processed on silicon wafers in a CMOS-environment. Most noteworthy is the emergence of *Silicon Nitride* (SiN) platforms, in which the waveguide core is made of silicon nitride. More generally we see strong interest in heterogeneous platforms in which a variety of materials (III-V semiconductors, $LiNbO_3$, polymers etc) are combined with SOI or SiN either through front-end or through backend processes. The key unifying feature of silicon photonics is the capability to process PICs in a silicon technology environment on large wafers, typically 200 or 300 mm in diameter.

CMOS pilot lines and research institutes have acted as the gateway for the technological innovation in the field of silicon photonics. This paper provides a brief description of the various open-access technology platforms offered by European silicon photonics research institutes and companies,[4] the routes to access these technologies and the current status of these technology platforms. Each technology platform has features, which make it unique when compared with the other technologies. This diversity enables the uptake of silicon photonics technology for various emerging applications such as sensing and biophotonics [23], [24], light detection and ranging (LiDAR) for automotive industry [25], neuromorphic computing [26]–[28], machine learning [29], [30], quantum information processing [31], [32] and many more. The paper also highlights upcoming features in these technology platforms and how they are evolving to address the upcoming market needs.

II. Silicon-on-Insulator Technology Platforms

This section mentions the salient features of the open-access SOI-based technology platforms offered by various European fabs. The described platforms are diverse in terms of TRL ranging from 5 and upwards, access mechanism (i-e, directly from the fab or through a technology broker), the technology used for the fabrication of PICs (i-e., e-beam, *Ultra Violet* (UV), *Deep Ultra Violet* (DUV)) and the SOI material stack used (i-e, thin SOI with a thickness of the guiding layer ranging 220 nm to 500 nm and thick SOI with a thickness of more than 1 μm). The turnaround time for these technology platforms through MPW runs depends on the type of the process flow and type of the fab. A full process flow, which includes monolithically integrated (high-speed) modulators, (high-speed) detectors and the back end of line process, in a CMOS pilot line typically takes at least six months from design submission to chip delivery. Design submission to chip delivery for a passive process flow in a CMOS pilot line takes around three months. A comparable process flow through rapid prototyping services takes two to three weeks delivery time. All fabs are striving continuously towards bringing down the turnaround time to meet the end- user expectations. Therefore, the above mentioned turnaround times may evolve to shorter times in the near future.

[2]Since 2015, the MPW services offered by ePIXfab have been transferred to Europractice IC Service. ePIXfab represents the European silicon photonics ecosystem and has transformed itself into the European Silicon Photonics Alliance with the mission to promote silicon photonics science, technology and applications ([Online]. Available: http://epixfab.eu).

[3]The definition of manufacturing volume used here for silicon PICs is as follows: up to 50 wafers per order is termed as low-volume manufacturing, up to 500 wafers per order is termed as medium volume and beyond this is considered as high-volume manufacturing.

[4]ST Microelectronics' manufacturing platform, which is based on sub-micron SOI material system and has an integrated SiN layer, is not discussed in this review. The platform uses 193 nm immersion lithography and features high-performance passive devices, high-speed active devices and a capability for electronic IC and photonic 3-D IC integration using a micro-pillar technology. ST Microelectronics does not provide open-access to its technology. It only provides restricted access to customers that align well with ST Microelectronics' business strategy.

A. Imec's Silicon Photonics Platform

imec, in collaboration with Ghent University, was among the first to demonstrate the power of DUV lithography for silicon photonic ICs [3]. imec's ISIPP50G technology is based on a 130 nm CMOS node toolset. It uses SOI wafers with 220 nm thick guiding silicon layer with 2 μm BOX in its 200 mm R&D pilot line. The technology includes 193 nm lithography for high fidelity patterning of a variety of passive devices possible due to the provision of three etch levels (one full and two partial etch levels). The technology uses optimized *Inductively Coupled Plasma - Reactive Ion Etching* (ICP-RIE) dry etch processes. It offers a poly-silicon overlay layer for high-efficiency coupling to and from SOI chips. To achieve active functionalities, such as (high-speed) modulation, ISIPP50G platform offers four levels of P-type and N-type doping each. Photodetection is enabled by a low-defect epitaxially grown Germanium on silicon. The technology provides various features at the *Back-End-Of-Line* (BEOL) such as local removal of the dielectric stack for improving the coupling efficiency of the grating couplers and access to the *Front-End-Of-Line* (FEOL) and a deep etch through the full stack into the silicon substrate for fiber edge coupling.

imec's ISIPP50G technology finds a wide range of applications ranging from optical communication, sensing to spectroscopy. The technology has a high TRL of $\geq$7. The access to the technology is possible via MPW service provided by Europractice IC (http://www.europractice-ic.com/), which offers at least three MPW runs in a year. Moreover, imec also provides dedicated engineering runs as well as low-volume manufacturing.

The components library of imec includes a wide variety of passive and active devices for O- and C-band applications. The three etch levels support strip waveguides (typical loss of 1.6 dB/cm for C-band) and rib waveguides (for C-band, typical loss of 1.1 dB/cm and 0.7 dB/cm for deep and shallow etched waveguides, respectively). A variety of grating couplers (1D, curved and high-efficiency grating couplers) are part of the component library. It also includes low-loss and broadband edge couplers. For splitting and combing of light, the library includes directional couplers and MMI couplers (1×2 and 2×2) with a negligible power imbalance, good phase accuracy and small excess loss over the C-band. The key feature of imec's silicon photonics technology is the availability of 50G modulators and detectors for datacom/telecom applications operating in O- and C-band. The components library provides carrier depletion-based lateral PN junction *Mach-Zehnder modulator* (MZM) and ring modulator with an integrated thermal heater to tune the operating wavelength of the modulator. Recently, a compact Germanium *Electro-Absorption Modulator* (EAM) using the Franz-Keldysh effect is included in the component library. It provides up to 100 Gb/s modulation speed. The technology offers low dark current photodiodes with either high responsivity or high bandwidth to support up to 100 Gb/s data rates [10], [33]. An overview of the components offered by imec's ISIPP50G technology is shown in Fig. 1.

The capability to imec's ISIPP50G platform is illustrated by an ultra-dense 16×56 Gb/s NRZ transceiver. It uses a multicore fiber to implement a short-reach optical link with a transmission capacity of 896 Gb/s. The transceiver has a form factor of 1.47 mm^2 highlighting the dense photonic integration using silicon photonics technology. The transceiver uses the GeSi waveguide electro-absorption device as a modulator and a photodetector. The 16-channels of the demonstrator are driven at 56 Gb/s and are tested sequentially. An open eye diagram with an SNR of 3.05 to 3.92 dB has been recorded at 1565 nm (L-band) when driven with 2.5 V_{p-p} RF signal and -2.5 V reverse bias for the photodiode [34].

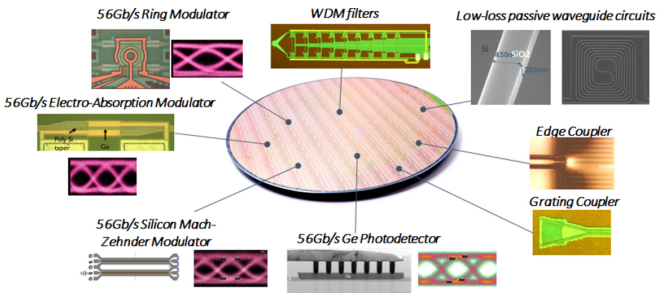

Fig. 1. imec's fully integrated silicon photonics platform for 1310 nm/1550 nm wavelengths comprising low-loss passive waveguide devices, efficient fiber I/O and >50 Gb/s modulators and detectors.

The *Process Design Kit* (PDK) is available via various EDA software vendors. The PDK contains the static GDS files, maturity levels and variability statistics of the library components. The PDK aids the designers for custom component designs by providing details of the technology, typical process tolerances, layer specifications and design rules. The future versions of the PDK will contain *Layout vs. Schematic* (LVS) verification to reduce design errors and *Lithography Friendly Design* (LFD) to improve the patterning predictability.

For the future, imec is developing efficient thermo-optic phase shifting elements by substrate undercutting. Such heaters can reduce the power consumption by a factor of 4. Furthermore, imec is developing technology to improve the performance of passive waveguide circuits through the integration of SiN in its technology platform.

To address the long-term market needs, imec, in collaboration with Ghent University, is actively engaged in developing technologies for low-cost integration of laser sources on its silicon photonics platform. As an example, transfer printing is developed for simultaneous transfer of multiple (semi-) processed III-V lasers from the source III-V wafer to the target silicon photonics wafer [35]. The technology promises massive richness of functionality and performance and allows for efficient use of III-V material.

B. CEA-Leti's Laser-Integration Compatible Silicon Photonics Platform

Leti has developed a fabrication platform for silicon photonics-based circuits allowing large-scale integration of active and passive devices in a flexible CMOS compatible process. This platform provides more than silicon with the integration of

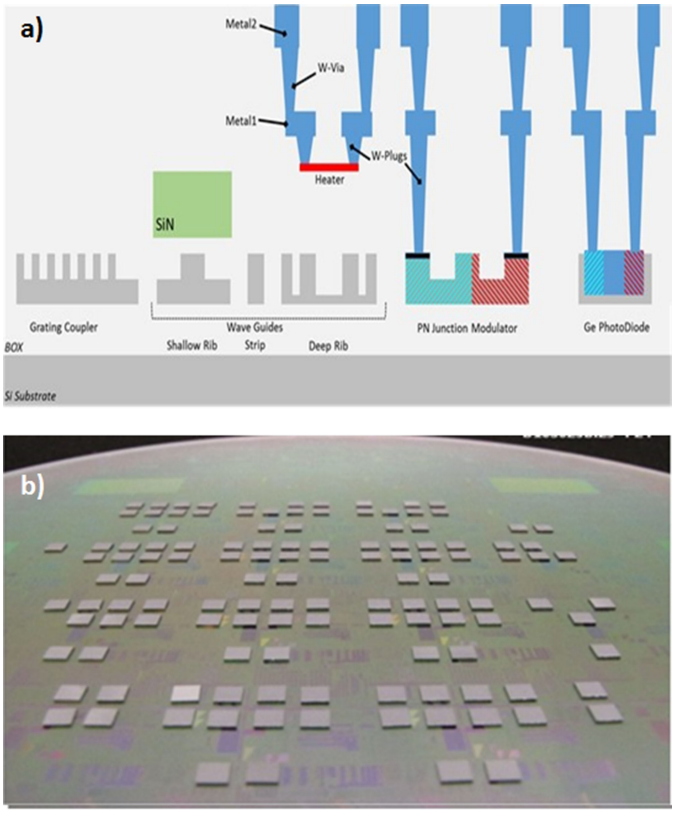

Fig. 2. CEA-Leti's silicon photonics platform: (a) Cross section of the overall platform. (b) III-V die bonded on patterned silicon.

a SiN layer and is compatible with III-V bonded epilayer on the same wafer, offering the advantages of each material. This convergence of different photonic platforms in this multi-materials process allows addressing various application needs with in the same platform.

The silicon core process is based on an SOI wafer with a silicon film thickness of 305 nm. This thickness enables improved performance of passive devices as compared to the former 220 nm technology [36]. A modular approach is used to build the process flow that supports various sets of devices. Multi-level silicon patterning module allows the fabrication of waveguide with different slab heights, leading to different optical characteristics, which can be mixed inside the same die. A DUV 193 nm lithography mask level defines the most critical patterns. Up to eight levels of implantation are available in order to define the various type of lateral PN-based phase modulators. Modulation of up to 64 Gb/s has been demonstrated with this core silicon process [37]. Selective Germanium epitaxy is used to form the absorbing section of the device. The integrated photodiode is based on a SiGeSi architecture leading to a better light confinement compared to a full-Ge device [38]. A second optical layer made of SiN is integrated on top of the silicon. This layer can be used to design specific SiN-based devices or hybrid SiN/Si devices [39]. A two metal level BEOL is available with an integrated heater for thermal wavelength tuning of devices. Figure 2(a) presents the cross section of the overall platform.

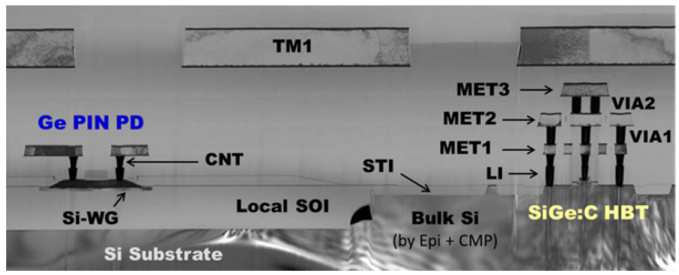

Fig. 3. Cross-section of IHP's EPIC technology platform (image of the first generation EPIC technology with 30 GHz photo detector). Locally reconstructed bulk Silicon by using epi+CMP enables frontend-of-line integration approach of SiGe electronics with state-of-the-art SOI-based photonics.

InP-based epitaxial layer can be integrated on top of the silicon layer of LETI's platform. Wafer or die bonding is available depending on the level of integration needed. Post-bonding fabrication is performed without downsizing the initial SOI wafer and using "CMOS-friendly" processes and materials allowing the large-scale integration of III-V based device on the mature silicon photonic platform (see Fig. 2 (b)).

The PDK supporting this platform proposes two device libraries containing a large set of devices to address O-band and C-band applications. The technology is accessible through the broker CMP (https://mycmp.fr/) with two MPW runs/year (without III-V integration) and has a TRL of $\geq$7.

The current focus of developments is on optimized hybrid laser designs taking into account the new capabilities offered by the CMOS compatible processes. Technology transfer to LETI's 300 mm fabrication line is ongoing. Advanced EIC/PIC integration solutions based on 50 μm pitch micro-bumps are available for dedicated customers and projects. Furthermore, TSV integration on silicon photonic platform is under development. The overall platform is becoming versatile enough to address more than telecom/datacom applications. Application diversification is a crucial issue for the sustainability of the silicon photonics. New markets such as advanced computing, 3D sensing or cryptography can be targeted with LETI's silicon photonics platform.

C. IHP's Monolithic Electronic-Photonic Platform

The goal of IHP's monolithic electronic-photonic integration platform is to deliver the integration of the basic components of electro-optic transceiver (i-e, modulator, driver, amplifier, photo-detector,..) on a single chip, which has SiGe *Hetero-Junction Bipolar Transistors* (HBTs) and PICs. IHP uses 200 mm SOI wafers with 220 nm guiding layer thickness on 2 μm BOX for a platform providing monolithic *Electronic-Photonic Integrated Circuits* (EPICs). The platform uses DUV (KrF) and i-line 250 nm CMOS-baseline technology. The technology has a mixed electronic-photonic frontend with five metal layers at the backend (three thin and two thick) and co-integration with high-performance HBTs as shown in Fig. 3.

The technology is developed for C- and O-band applications and has a TRL of $\geq$7. IHP's high performance BiCMOS technology SG25H5-ePIC is available to academic and industrial users in MPW mode through Europractice IC. IHP also provides

direct access to its technology through dedicated engineering runs. Key building blocks in IHP's EPIC technology are:

(i) nano-waveguides (etch depth 220 nm, 120 nm, 70 nm) with loss between 1-3.5 dB/cm, (ii) *Standard Single Mode Fiber* (SSMF) compatible 1D grating couplers with a typical insertion loss of 4.5 dB, (iii) MMI based splitters/combiners (1×2, 2×2, 4×4), (iv) Carrier dispersion based phase shifters (lateral PN, lateral PIN), (v) linear lateral PN with $V_\pi L = 2.8$ V.cm and 1.2 dB/mm @-1 V, (vi) thermal phase shifters, (vii) Waveguide coupled Germanium PIN detectors with responsivity = 0.9 A/W (internal), OE-S_{21}3dB > 60 GHz, dark current <200 nA @ room temperature, -2 V, (viii) HBTs with $BV_{CEO} = 1.65$ V, $f_T = 220$ GHz and $f_{max} = 290$ GHz [12], [40], [41]. Figure 3 shows the cross section of IHP's EPIC technology.

Recently, IHP's technology has been used to demonstrate a novel Mach-Zehnder modulator that is monolithically integrated with drivers in a photonic BiCMOS technology. The MZM consists of two 6 mm long parallel phase shifting elements. They are divided into 16 segments that are based on waveguide diodes and utilize the carrier dispersion effect to induce phase changes. The overall V_π of the modulator is 3.9 V at 1 V reverse bias and a fiber-to-fiber optical loss of 18 dB. The modulator driver is monolithically integrated with the modulator. The combined electro-optical S_{21} spectrum of the driver and modulator exhibits a slow roll-off with 3 dB and 6 dB bandwidth of 11 GHz and 36 GHz, respectively. The monolithically integrated modulator with a driver is used to demonstrate data transmission of net 300 Gb/s over 120 km SSMF. [42].

The PDK of the technology is developed for Cadence as well as TexEDA with fully featured electronic PDK, fundamental optical cells, electronic-photonic *Design Rule Check* (DRC), photonics-enabled LVS and script-based filler generation. Moreover, the PDK provides parametric building blocks and optical circuit simulation (optical S-Parameter + transient) using IPKISS. The upcoming features of the technology include higher performance HBT module integration, low-loss edge coupling and on-chip polarization management. In the long-term, IHP is striving to provide an integrated laser source on its EPIC platform. Regarding hybrid integration of other platforms, IHP collaborates with commercial partners. Solder bumping and copper pillars are available with 120 μm and 70 μm pitch, respectively. As for the photonic-electronic integration roadmap, IHP plans to provide co-integration with HBT performance of f_t/f_{max} of 300/500 GHz in the mid-term future.

D. VTT's Thick-SOI Platform

The foundation for VTT's Thick-SOI technology platform is the Micronova clean room facility where the first silicon photonics components were designed in 1997, and fabricated a few years later. Today, the main technology platform is based on 3 μm thick SOI where light is almost fully confined inside the Si core. The combination [43] of single-mode rib waveguides and multi-mode strip waveguides offers a unique combination of low losses ($\sim$0.1 dB/cm), dense integration (bend radii 1–30 μm) and small polarization dependence in effectively single-mode PICs. In addition to fully passive components, also thermo-optic phase modulators, plasma dispersion modulators and Ge photodiodes have been developed. Compared to the performance of similar devices in sub-micron SOI, the performance of passive and thermo-optic components is often better, while the bandwidth of high-speed active components is much lower (well below 10 GHz).

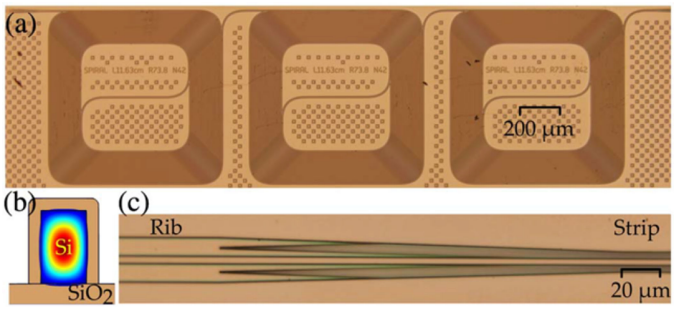

Fig. 4. (a) Top view of a 35 cm long waveguide spiral. (b) Simulation of the fundamental mode for the 3 μm $\times$ 1.875 μm silicon strip waveguide. (c) Rib-to-strip converter for coupling to the fundamental mode [47].

Silicon photonics has become the most important driver for VTT to develop the Micronova clean room facility. 3 μm SOI forms the basis for silicon photonics research and related small-volume manufacturing in Micronova. Continuous platform development covers TRL range 1–9. There is additional development on 12 μm SOI for optical interposers between SSMF arrays and PIC chips.

VTT offers up to two MPW runs/year in 3 μm SOI. Dedicated runs and other R&D services from design and process development to hybrid integration, packaging and chip/wafer level testing are carried out for customers around the world. They range from small university groups to large-scale companies. Contract manufacturing in Micronova is offered by VTT Memsfab, a separate company within the VTT group. Also, technology transfer and IP licensing are available. VTT provides direct access to its technology platform (www.vtt.fi/siliconphotonics).

The key building blocks in MPW technology are single-mode rib waveguides ($\sim$0.1 dB/cm), multi-mode strip waveguides ($\sim$0.15 dB/cm including bends), rib-strip converters (<0.05 dB) [43], Euler bends (<0.01 dB for >20 μm radius) [44], TIR mirrors (0.1–0.3 dB), thermo-optic phase modulators (<0.01 dB, >10 kHz, <25 mW/π), PIN modulators (>1 MHz, <5 mW/π), MMI couplers (0.1–0.2 dB), Mach-Zehnder interferometers, echelle gratings (1–4 dB), *Arrayed Waveguide Gratings* (AWGs) (2–5 dB) and dry-etched I/O facets with anti-reflection coatings ($\sim$0.5 dB coupling loss to lensed fibers). Dedicated runs also include up-reflecting mirrors with either 55° or 45° mirror angle (0.5–2 dB) and Ge photodiodes (<10 GHz). Hybrid integration mounts (with end-fire coupling) can be fabricated for various optoelectronic chips that are obtained either from the customer or from other service providers.

One key capability of the thick-SOI platform is to realize long and low-loss waveguide spirals in ultra-small footprint (see Fig. 4). They can be used to measure precisely the propagation loss of the waveguides and they have been used, for example,

to demonstrate demodulators for phase-shift-keying [45], Faraday rotation [46] and *Instantaneous Frequency Measurement* (IFM). In particular, IFM has been demonstrated in collaboration with the University of Sydney and the results were reported in [47]. The 35 cm long waveguide spiral used in this demonstration is shown in Fig. 4 and it allowed to efficiently harness Kerr non-linearity and to demonstrate the first on-chip four-wave mixing-based IFM system. Achieved measurement bandwidth was 40 GHz and the frequency estimation error (root mean square) was as low as 0.8% of the full bandwidth.

Design support for 3 μm SOI includes software-independent documents (platform overview, process description, design instructions and design rules) and software-specific PDKs for both Synopsys (up-to-date) and IPKISS (older version), as well as layer/technology setup files for KLayout and a GDSII example file with some model designs for key building blocks.

VTT is planning to add up-reflecting waveguide mirrors (45°) and Ge photodiodes as basic building blocks in future MPW runs. These enable wafer-level testing, VCSEL integration and on-chip power/signal monitoring. The present Au-Au thermal compression bonding will be complemented with solder-based flip-chip bonding to support a wider variety of optoelectronic and electronic chips to be hybrid integrated on 3 μm SOI. In VTT's long-term vision, the plan is to extend the MPW offering to also include athermal multiplexers, fast modulators/photodetectors (>25 GHz), monolithic isolators/circulators and wafer-level (or chip-scale) packaging.

The most important functionalities that are frequently requested by the customers and not yet offered in the open access 3 μm SOI platform are modulators and photodiodes with high bandwidth. These should reach at least >25 GHz and preferably >40 GHz. Different concepts for these are being developed in public-funded projects and some work has been done in industrial projects. Other frequently asked functionalities are low-loss coupling to large arrays of standard SM fibers with passive alignment and low-loss (1–2 dB), athermal multiplexing, polarization splitters, polarization rotators, isolators, circulators and various light sources. Some of these have already been demonstrated, but none of them is yet mature enough to be included as a standard building block in MPW runs.

E. AMO's Silicon Photonics Platform: Full Custom Rapid Prototyping Services

AMO provides a rapid prototyping silicon photonics platform for passive and active devices based on SOI substrates. Process flows are individually adaptable to the customers needs (etch depths, cladding thickness etc.). The main fabrication line is based on 150 mm SOI wafers and includes passive photonic devices with low-loss cladding options and up to four different implantation steps, up to two metal layers including i.e. heaters and contacts (see Fig. 5). The devices can be either optimized for O- (1310 nm) or C-band (1550 nm). The photonic layer is highly customizable as its fabrication is based on electron-beam lithography. Active devices can be realized in a Mix & Match approach, i.e., high-resolution photonic layers are defined with e-beam and larger feature sizes for implantations, vias or metal

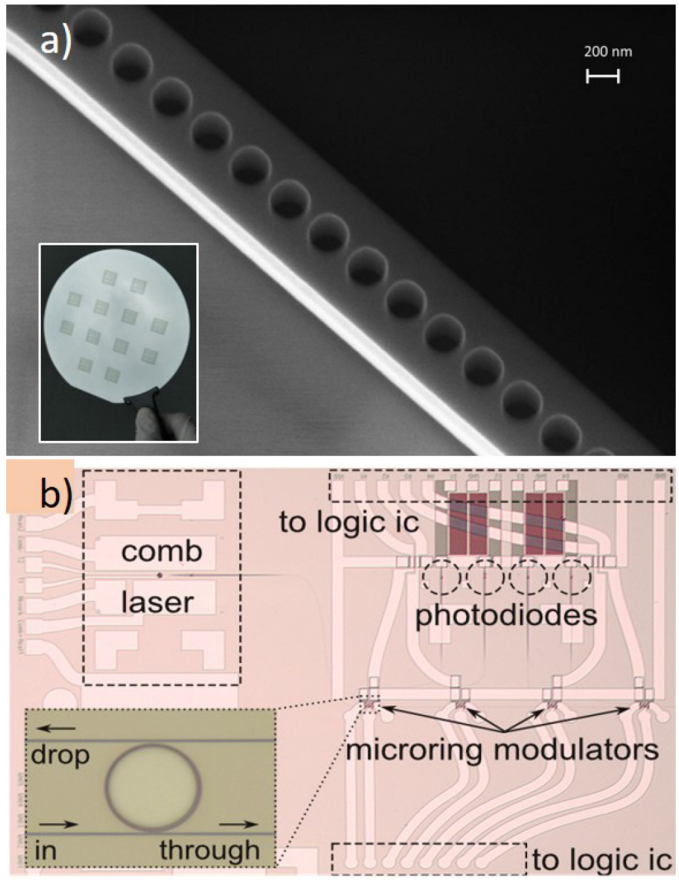

Fig. 5. AMO's Full Custom Silicon Photonic Rapid Prototyping Platform: Flexible process flows; (a): High resolution photonic device layer (inset: finalized photonic wafer before dicing). (b) transmitter module for active optical cable application.

are defined with projection lithography via i-line stepper. The silicon platform reaches TRL of up to 7 on full-wafer prototyping for ICT devices like transceivers [48], lab on a chip sensors or for hybrid integration of novel materials (i.e. graphene [49], [50]). AMO provides direct access (www.amo.de) to its silicon photonics technology platform and provides support in design and process flow to the end-users.

AMO's standard components are fabricated on SOI wafers with 220 nm top silicon layer on 3 μm BOX. Passive building blocks are waveguides (strip, rip, slot), grating couplers, ring resonators, Mach Zehnder interferometers, directional couplers and spot size converters. Waveguide losses for strip waveguides lie between 0.5 dB/cm and 1.5 dB/cm depending on dimensions and cladding. Grating couplers have losses of around 2.5 dB (cladding dependent).

AMO is specialized in advanced prototyping targeting new device concepts and fabrication methods. High-speed transmitter modules have been fabricated [48], see Fig. 5(b), as well as ring resonator based 16 $\times$ 1 packaged MUX/DEMUX for optical networks [51], high-speed graphene photodetectors [49] and many more. Device development resulted in ultra-efficient silicon-based modulators with record low efficiency-loss products $V_\pi L * \alpha$ [52]. This is enabled by mixing the standard

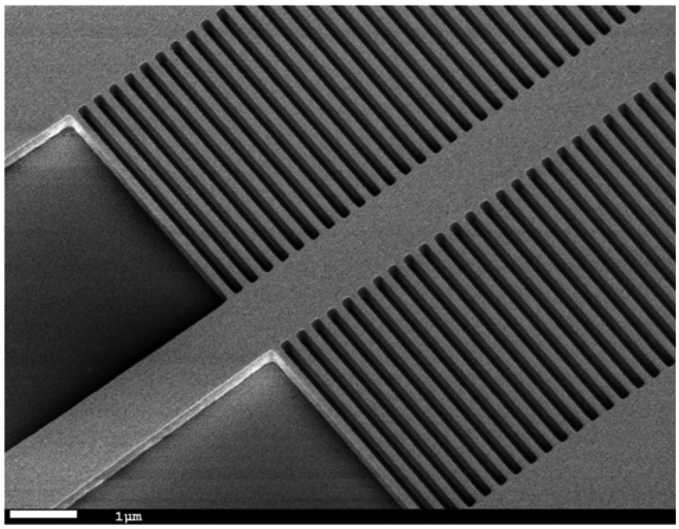

Fig. 6. A suspended waveguide for mid-infrared applications using CORNERSTONE's silicon photonics technology.

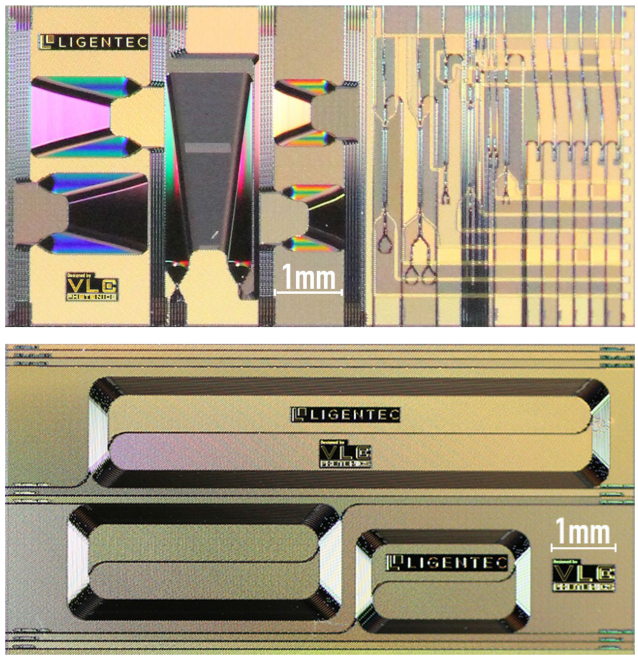

Fig. 7. Two chips examples from LIGENTEC. The upper chip shows five compact AWGs (left) and PDK building blocks with heaters for 1550 nm operation. The lower chip shows spirals with losses below 0.05 dB/cm used as compact delay lines.

fabrication processes for waveguides etc. with novel implantation strategies and by combining process simulation and fabrication results.

In the future, AMO is striving to develop more efficient fiber to chip coupling options. This is key to broaden the fields of application of the silicon photonics technologies. New features may also be introduced through research contracts due to the high flexibility of the pilot line. Specific process steps can be realized to obtain targeted device performance, as AMO can develop the corresponding technology.

On a medium to long-term timescale efficient packaging technologies are necessary to bring the revolution of integrated photonic devices into more market segments. AMO is active to develop devices and platform interfaces which enable effective packaging in the future.

F. Cornerstone: Versatile Wafer-Scale Prototyping

CORNERSTONE is a rapid prototyping MPW capability that utilizes industrially-compatible tools (e.g., deep-UV lithography), to enable seamless scaling-up of production volumes, whilst also retaining device level innovation capability using high-resolution lithography (e-beam) and versatile processes. The TRL 5 technology platform is a collaboration between the Universities of Southampton, Glasgow and Surrey in the UK, with the majority of the processing taking place in the Optoelectronics Research Centre's cleanrooms at the University of Southampton, where a 248 nm Nikon Scanner is installed. Lower TRL opportunities are also available for researchers and innovators to test experimental designs. Presently, CORNERSTONE offers three different SOI platforms (220 nm Si / 2 μm BOX, 340 nm Si / 2 μm BOX and 500 nm Si / 3 μm BOX), enabling a plethora of applications including telecommunication, mid-infrared sensing (see Fig 6) etc. The unique hybrid processing (DUV projection lithography and e-beam lithography) capability renders the CORNERSTONE platform attractive to both academia and industry and can mimic advanced industrial processes.

CORNERSTONE is an open-access technology, which offers up to six MPW calls per year. In addition to that, dedicated fabrication batches are also available on demand. CORNERSTONE provides direct access to its technology platform through the CORNERSTONE website: www.cornerstone.sotonfab.co.uk.

Utilizing patented self-alignment processing technology, the CORNERSTONE team have designed silicon carrier depletion modulators with data rates of beyond 56 Gb/s [53], [54]. With four implant layers, three Si etch depths and metallization steps, these designs are available in the active device MPW calls. Additionally, more frequent passive, or passive-with-heaters, MPW calls enable the fabrication of complex silicon photonics circuits [55], with single-mode rib waveguide propagation losses as low as 2.5 dB/cm, and using the hybrid high-resolution e-beam lithography layer, high-efficiency grating couplers with insertion losses $<$1 dB [56]. The CORNERSTONE PDK is available using Luceda's IPKISS platform.

Additional capability will be added to the CORNERSTONE platform as it matures via other research projects within the consortium. Consequently, CORNERSTONE is continually adding more functionality for designers to exploit e.g. Ge photodetectors and silicon nitride.

The vision of the CORNERSTONE platform is to offer designers device level innovation capability using industrially compatible processes, at a rapid turn-around and an affordable cost. CORNERSTONE strives to introduce the latest research into its MPW capabilities by transferring technology currently under development as part of the significant number of ongoing research projects within the CORNERSTONE consortium.

III. Silicon Nitride Technology Platforms

SOI is the most prominent material system for silicon photonics PICs. However, it is not transparent for wavelengths below 1.1 μm and above 4 μm. The success of SOI and the emergence of applications operating at visible and very-near-infrared wavelengths triggered a growing interest in SiN-based "silicon photonics". SiN has a moderately high index contrast as compared to SOI. As a result, SiN-based silicon photonics out-competes SOI in the performance of passive devices in terms of propagation loss. Also, the thermal sensitivity and nonlinear properties of SiN outperform those of SOI. Even though low-speed active functions such as heaters are available in open-access SiN-platforms, they lack monolithically integrated high-speed devices, such as modulators and detectors, and thus rely on the integration of other materials for demonstrating these functions. Typically the turnaround time of SiN-based MPW takes up to three months from design submission to the delivery of chips. Generally, rapid-prototyping fabrication services take shorter turnaround time than the CMOS pilot lines.

In the next sub-sections, SiN-based open-access platforms offered by various European institutes and companies are discussed.

A. Ligentec's Thick SiN platform

LIGENTEC is a SiN photonics foundry. The Ligentec process is based on an all-nitride-core technology and designed from the bottom-up for photonics and modularity. In the all-nitride-core, most of the optical mode energy is in the waveguide material, which reduces loss ($<$0.1 dB/cm) and makes small bending radii ($<$10 μm) possible. There are two processes available: the AN800 for the IR and the AN150 for visible and near-infrared wavelengths. Both processes are complemented by modules extending the integrated functionality. Those modules are (i) M1 for metal-based heaters, (ii) LoCA for local window opening facilitating sensing and bonding applications (sub-nm flatness for bonding area), (iii) X2 for multi-level nitride integration ($<$20 nm overlay accuracy), realizing true 3D photonic circuits and (iv) ExSpot a spot converter for single mode fiber coupling with 0.5 dB loss per facet. All-nitride-technology is using optical grade LPCVD SiN and oxide cladding materials. LIGENTEC is using DUV stepper technology for 150 nm applications in combination with etch techniques developed to improve the optical losses of the waveguides. LIGENTEC is capable of providing TRL 8-9 prototyping and low-volume fabrication services and has a fabrication partner to address high-volume customers.

LIGENTEC is an open-access foundry offering its all-nitride-core technology in MPWs and dedicated runs. Access is provided directly through LIGENTEC or through VLC Photonics, a strategic partner and a technology broker. In MPW runs both processes AN150 and AN800 are offered, but X2 and ExSpot modules are only available in dedicated runs. Main application areas are quantum and nonlinear integrated photonics, high-power LiDAR, bio-sensing as well as microwave photonics, datacom and laser metrology.

Key building blocks include the standard passive components such as ring resonators with Q-factors well above 1 Million (loaded), splitters with high accuracy, Mach-Zehnder interferometers, mode converters for SMF fibers or customized mode field diameters and 4-channel arrayed waveguide gratings with a footprint of only 1mm^2. Heaters are used for tuning of resonances of the resonators and phase modulation of Mach-Zehnder interferometers with efficiencies for a π-phase shift of around 100 mW. In addition to that, LIGENTEC offers the LoCA module, which enables cladding opening for accessing the evanescent field of the SiN waveguide for bonding or sensing applications.

Recently, a *Chip Scale Optical Resonator Enabled Synthesizer* (CORES) showed frequency synthesis with PIC components [57]. Several PIC components, ranging from laser, passive components and detectors are used to dial in the frequency of a tunable laser with the precision of less than one Hz. A LIGENTEC chip was used to generate a THz frequency comb in combination with an interposer function to integrate other materials such as Lithium Niobate and to connect different PIC components [58]. It has a first thick SiN circuit where high Q resonators enable nonlinear frequency generation [59]. On the same chip, the light is transferred to the second layer of thinner SiN, where the signals are routed to different outputs. Additionally, a bonding window is etched to allow for evanescent field coupling between the SiN and the bonded material. Heater elements could still be integrated for tuning.

Both LIGENTEC processes, AN800 and AN150, have a PDK. The PDK for the AN800 is designed for operation at 1550 nm, while for AN150 is designed for VIS-NIR operation. The PDKs are implemented in Synopsys and Luceda IPKISS, whereas DRC file is available in Mentor Graphics Calibre. Both PDKs are updated frequently with extended measurement data.

The integration of active elements with a low-loss platform is one of the most commonly required functionalities. The most common request is the integration of a light source and detection. LIGENTEC is planning to address this in the future with the inclusion of active elements. A second demand is for modulation using low power and compact footprint devices. The combination of speed, power, size and phase shift losses (including insertion) is a challenge that LIGENTEC addresses.

B. LioniX International TriPleX Platform

Since 2001, LioniX International commercially offers the SiN-based platform called TriPleX. The main characteristics of the platform are the ultra-low loss, broad wavelength range of operation (400 nm - 2350 nm) and the possibility to adapt the mode properties on the chip. The TriPleX waveguide platform is based on LPCVD processes and comes in several cross sectional types, optimized for specific applications [60]–[62].

The cross sections use one (single stripe) or multiple layers of LPCVD Si_3N_4 to create waveguides with different properties. The single stripe cross section finds general application in fiber-mode matching at the edges of the chip, or in ultra-low loss waveguides. The Symmetric-, Asymmetric Double stripe (SDS, ADS) as well as the box-shape cross sections have a moderate high index contrast allowing bend radii down to a few 10 s of μm. The SDS and ADS are optimized for one polarization, whereas

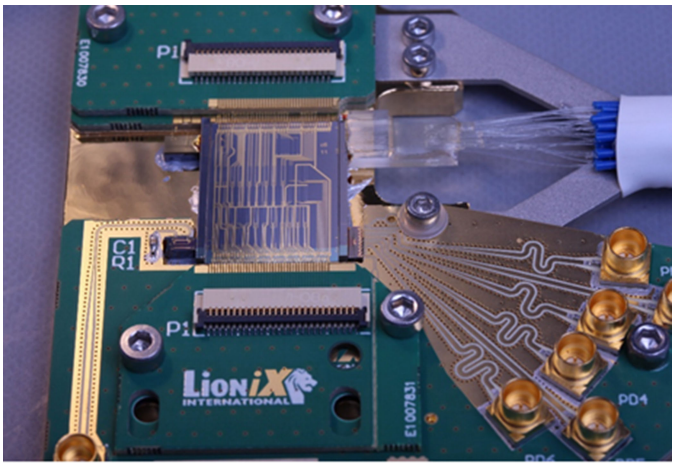

Fig. 8. Commercial example of TriPleX waveguide technology: Integrated Optical Beam Forming network showing hybrid integration of TriPleX and InP elements into an MWP module for satellite communications.

the box-shape is optimized for both polarization states. Finally, the buried TriPleX structure allows for thick waveguide layers and is used when high confinement is needed, for example in non-linear applications [60]. A key capability of the TriPleX technology is the tapering process to convert between different cross sections. For example, to taper from the ADS, allowing tight bends on chip, to the single stripe that is optimized for fiber coupling. LioniX offers the TriPleX waveguides on 100, 150 and 200 mm wafers, depending on the quantity needed. The ADS structure has a typical propagation loss of 0.1 dB/cm for $\lambda = 1550$ nm. For the single stripe record low losses of 0.1 dB/m have been demonstrated. [62].

The TriPleX waveguide platform is offered via dedicated runs as well as via open-access MPWs and can be accessed directly or via several brokers (i-e, JePPIX and PIX4life [63]). The platform is part of the vertically integrated offer of LioniX for product development as well as production runs, where design, manufacturing and assembly are integrated. Also, the MPW offering has a strong focus on assembly, for example by the characterization package that allows for easy assembly of a chip manufactured in an MPW.

The work-horse cross section at this moment (ADS) has a typical propagation loss of $\sim$0.1 dB/cm. On-chip, the bend radius is as small as 25 μm, capable for micro-ring resonators. Fiber-to chip coupling sections are optimized to have $<$0.5 dB per facet in-coupling loss. Along with design rules, templates to optimize packaging and standard building blocks such as directional couplers, y-splitters and thermo-optic phase elements, the MPW also offers a tunable laser module (tunable over 40 nm, $>$1 mW output power) as a PDK building block whereby the user receives an assembled module including the InP integration.

TriPleX is used in a broad range of applications ranging from life science, tele- and datacom, quantum technology, to food and health [60]. A good demonstrator of the capabilities is the *integrated Optical Beam Forming Network* (iOBFN), shown in Fig. 8, for *Microwave Photonic* (MWP) systems [61]. This iOBFN is fully RF-in RF-out due to the hybrid assembly of lasers, photo-diodes and modulators. The tunable phase elements for the long delays are made in the TriPleX technology. The low-loss silicon-nitride waveguides combined with the InP sections are enabling this application.

For the MPW, a full PDK is available on the Synopsys Software and well as VPI Photonics platform. It contains the validated building blocks and design templates and rules for assembly of the chip. When one of the TriPleX technologies are used and not offered via MPW, an internal PDK library is used to support the customers in a first time right design.

The TriPleX waveguide technology is a mature silicon-nitride platform that is serving several industrial customers. The platform is continuously improved, both by adding new basic building blocks (like AWG, or MMI) as well as by technology improvements. The most recent is the development of a new actuator principal, based on the stress-optic effect using piezo material (PZT) that has been introduced to dedicated runs. It is expected to be offered through MPW mode as well. The main advantage of PZT actuator is the large reduction in power consumption of the actuators from tens of mW down to several μW per actuator.

The TriPleX waveguide platform, especially combined with hybrid integration of InP active elements is set to address many upcoming applications. The main challenge is the scaling of the assembly of photonic modules. The market will keep pushing the technology for lower losses, lower power and lower assembly costs. Novel markets, especially in the visible domain, require a different approach (market not used to working with chips), as well as improved assembly techniques as the shorter wavelength range requires an increased fabrication accuracy. The vertically integrated offer containing the TriPleX platform addresses these upcoming demands.

C. Imec's BioPIX PECVD SiN Platform

imec started in 2012 with the development of a SiN photonic platform named BioPIX. A PECVD SiN material with low losses in the visible and near-infrared range of the electromagnetic spectrum has been developed. Its low autofluorescent properties and the prospect of an ultra-high waveguide density by leveraging small mode sizes and very tight bending radii make this platform ideally suited for bio-applications, e.g. biosensing and DNA sequencing [64], [65]. In addition, the low-temperature deposition method (PECVD) used, makes this platform fully compatible with the BEOL of CMOS circuits. The latter enables monolithic integration of photonic circuits directly on top of CMOS wafers containing e.g., CMOS imagers or electronic circuits enabling more innovative life science applications, e.g., on-chip spectrometers [66], [67].

The BioPIX platform has further matured during the PIX4life project, which is a European funded pilot initiative for SiN photonics together with the accompanying supply chain focusing on visible light applications for life sciences. There are two flavors of the BioPIX platform, which are readily available: i.e., the BioPIX300 and BioPIX150. BioPIX300 is targeting wavelengths above 650 nm with a SiN core thickness of

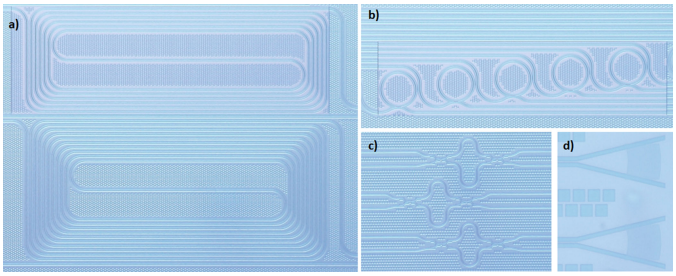

Fig. 9. The BioPIX platform gives the opportunity for components such as (a) spiral waveguides and (b) ring resonators to interface with biological samples through the use of the open-clad module, while also providing high performance standard components such as (c) compact Mach-Zehnder Inteferometers and (d) grating couplers for vertical interfacing, down to 388 nm wavelength on the BioPIX150 platform.

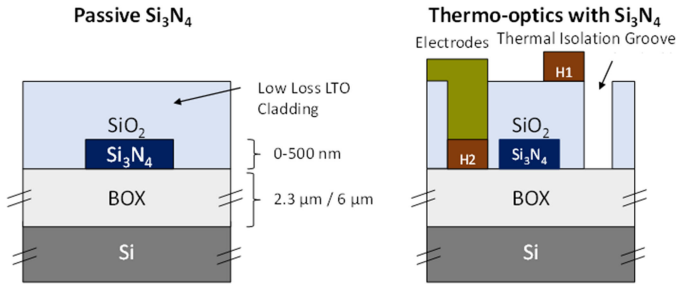

Fig. 10. AMO's Full Custom Rapid Prototyping Platform for silicon nitride photonics: left: Passive devices with customized Si3N4 waveguide dimensions. Right: Thermo-optical devices can be built either with metal heaters on top of the low-loss cladding (H1) or next to the waveguide (H2). Thermal isolation grooves improve the power budget for the heaters.

300 nm whereas the BioPIX150 is meant for wavelengths between 450 nm to 700 nm with a SiN core thickness of 150 nm, all fabricated on 200 mm wafers. The current status of the technology is estimated to match a TRL of 7. Figure. 9 gives an overview of a selection of components of the BioPIX PDK.

imec offers the BioPIX platform through dedicated wafer runs under bilateral agreements. Also, the BioPIX platform is accessible since 2018 through the PIX4life pilot line by means of MPW runs. The MPW service is offered at subsidized cost to external industrial and academic users aiming to launch new products in the life science area. The announcements of these runs and all necessary information for the customers can be found on the PIX4life website [63], [68].

PIX4life has enabled a portfolio of building blocks which is validated and available for the users in the respective PDK libraries of the platform. For example, various building blocks for shallow and deep etched waveguide layer have been fabricated and thoroughly tested. For each run, *Process Control Monitoring* (PCM) structures were implemented and measured using an automated wafer scale probe station. Building blocks are, but not limited to, rib and strip waveguides, grating couplers [69], evanescent couplers, splitters, MMIs, AWGs and ring resonators. Moreover, the imec BioPIX platforms offer a module where the top oxide cladding is removed selective to the SiN waveguides, in order to expose the bare SiN core material.

Further to those standard passive building blocks, thermo-optic modulators, top metallization and edge coupling modules are currently under development. All the information regarding the basic building blocks performance, design, layer nomenclature, stack description with process variations are available within the PDK. The PDK of the BioPIX platform is part of the photonic design software packages offered by Luceda Photonics and Synopsys. A technology handbook including layer and stack descriptions and basic performance values of the process control monitoring structures is provided to the designers as well, especially for those who do not work with the above mentioned software packages.

To demonstrate the success of the technology, two demonstrators have been fabricated based on the BioPIX300 platform technology within the context of PIX4life. The first demonstrator is the on-chip *Optical Coherence Tomography* (OCT) imaging system for ophthalmology applications. This demonstrator is designed and developed by the industrial partners of PIX4life consortium and is intended for their future OCT-products. New process modules such as thermo-optic modulators and edge couplers are incorporated in the circuitry of the OCT chip. The second demonstrator developed by the PIX4life consortium is a multi-degree of freedom or multi-DoF sensor for liquid or gas sensing applications. One of the target applications for this demonstrator is sweat analysis. This sensor is predominantly employing the clad opening module of the BioPIX technology.

To realize a prototype, PIX4life focuses on light integration options and general packaging solutions. More importantly, recently PIX4life intensified its collaboration with the PIXAPP pilot line for assembly and packaging (www.pixapp.eu). The aim is to integrate the necessary metallization steps and alignment structures on the BioPIX platform in order to allow smooth and easy packaging of the PICs within the PIXAPP pilot line.

In addition to packaging challenges, a challenge that is not tackled within the PIX4life pilot line, is the surface activation or pre-treatment for life science applications. For example, biosensing applications require an anti-fouling or bio-specific chemistry. These specific surface conditions should not alter during packaging, assembly or storage. However, the current photonic assembly and fabrication houses are not equipped for this. Furthermore, in the longer term, especially for the life science industry, it will be necessary to integrate photonic chips not only with electronics but also with microfluidics. The challenge will be the integration and assembly of all these components on a small footprint in a cost-effective way.

D. AMO's Silicon Nitride Photonic Platform: Full Custom Pilot Line Services

Recently, AMO has established a rapid prototyping SiN platform offering passive devices and actives, which are based on thermo-optic effect. Photonic devices in this platform are fabricated via projection lithography (i-line stepper) on 150 mm wafer equipment. The ultra-low loss platform uses Si handle wafers with 6 μm thermal oxide and a top layer of LPCVD SiN (see Fig. 10). On top of the waveguide layer, a specially

developed low-loss cladding is applied. Low-loss switches can be built by adding heaters to the design.

Key building blocks of the SiN platform are waveguides for 1550 nm and 800 nm as well as grating couplers for these wavelengths. Waveguide losses at 1550 nm are ∼0.1 dB/cm (cladding dependent). Directional couplers enable the precise functionality of Mach Zehnder interferometers for switches. The thickness of the waveguide layer can be customized from ∼50 to 500 nm. TRL 6-7 is reached within this platform. AMO provides direct access to its SiN platform and provides support in design and process flow to the end-users.

The SiN platform has been used to demonstrate *Synthetic Aperture Radar* (SAR) applications [70], plasmonic sensors [71] and integrated perovskite lasers [72], [73]. Variable optical attenuators, using graphene as active material, demonstrate the platform functionality at 855 nm [70]. Recently, true-time delay control of an optical beamforming network has been realized based on this platform [70]. This can be used for array antenna systems for SAR applications. Long waveguide lengths of up to meter-scale can be utilized, which open the field of routing applications for efficient switches. With the help of plasmonic materials, highly integrated sensors with high-sensitivity were built [71]. Moreover, the first integrated perovskite lasers have been realized on top of AMO's SiN waveguides. The low-loss platform also enables integrated quantum photonic components.

AMO is investigating efficient fiber to chip coupling techniques as the availability of broadband and low-loss I/O is key to widen the range of applications. Further developments for AMO's SiN platform target the availability of active devices by integration of novel materials onto the platform.

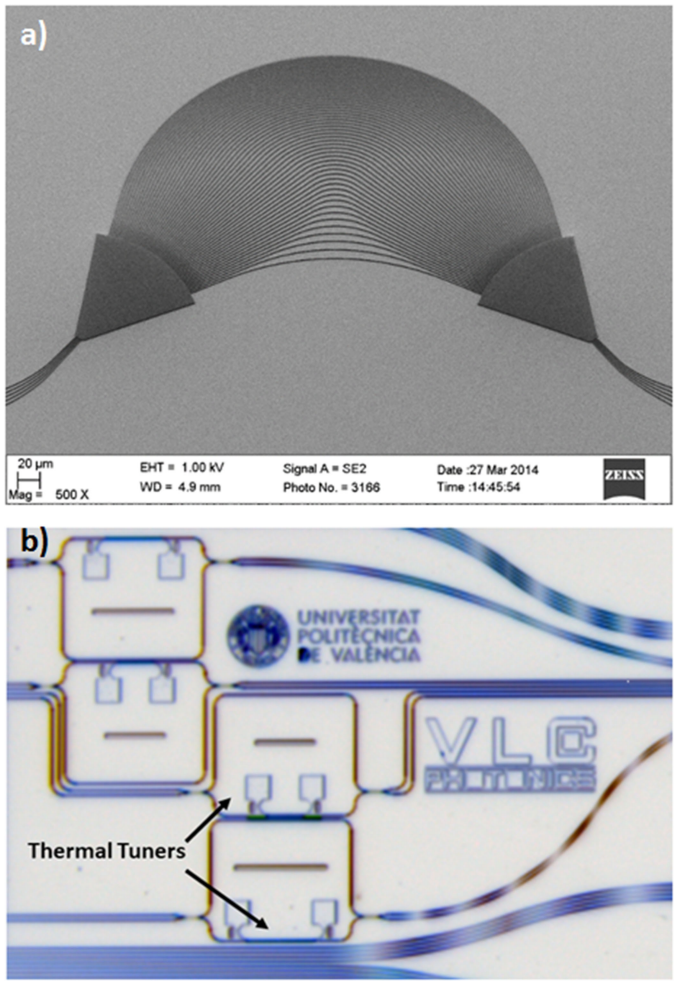

Fig. 11. (a) Arrayed waveguide grating, and (b) thermal tuners as an example of available components in the IMB-CNM platform.

E. IMB-CNM SiN Platform

The IMB-CNM is a moderate confinement SiN photonics integration platform aiming at covering a wavelength range from 400–3700 nm for photonic integrated applications such as biophotonics, tele/datacom and sensing (TRL≥7) [75]. The photonic platform runs in the Integrated Micro- and Nanotechnology clean room hosted by the IMB-CNM (CSIC) parallel to a standard CMOS line. The infrastructure has 1500 m^2, with Class 100 (ISO5) and Class 1000 (ISO6) areas.

SiN waveguide structures are defined with CMOS compatible fabrication equipment. The process makes use of 100 mm (4 inch) Si wafers. The guiding cross sections for NIR wavelengths (C-Band) comprise three geometries: rib 150/300 height, ridge and mini-ridge having 300 and 150 nm thick Si_3N_4 core layer, respectively. Figure 11 (a) shows an example of basic building blocks used. For the visible wavelength range, a rib cross section with a small rib height were used as basic waveguide structure. For both technologies, process technical features include thermo-optic tuners (Cr/Au) for optical modulation and selective area trenching for development of evanescent sensors. Figure 11 (b) shows a thermo-optic tuner developed within the platform. For the visible range, the waveguide basic structure comprises a 2.0 μm thick BOX grown on a silicon substrate by thermal oxidation. On top of the BOX layer, a SiN layer deposited via by LPCVD, with a thickness of 150 nm, forms the propagation core. To work under single mode and enhance the confinement a rib waveguide is used. The technology includes the sensing well definition level for direct interaction with the media in order to do the measurements.

The IMB-CNM SiN platform offers open-access in MPW mode and provides design support for design submissions. IMB-CNM is accessible directly or through VLC-Photonics. Two standard die sizes are available: M (5.0 × 5.0 mm) and L (10.0 × 5.0 mm). At least 20 copies of each die are delivered to the users to be used as proof of concept for research or industrial prototypes.

The technology provides low-loss shallow waveguides with 0.3 dB/cm, deep waveguides for sharp bending with <50 μm radius, 1 × 2 and 2 × 2 MMI couplers with arbitrary splitting rations, tunable Mach-Zehnder and Sagnac interferometers Arrayed Waveguide Gratings with custom channel count and wavelength spacing/FSR, Echelles Gratings, ring resonators with Q-factors up to 1 Million, etc [76].

A key demonstration of IMB-CNM platform is the implementation of a field-programmable photonic arrays in a SiN chip [77]. The demonstrator employed an MPW run in the CNM platform to make a low-loss physical implementation of their

novel concept. The circuit comprises multiple tunable Mach-Zehnder Interferometers arranged in a hexagonal mesh that will allow implementing multiple optical functionalities by exploiting the reconfiguration capabilities of the circuit by thermal tuners.

A PDK is available for the Synopsys Software platform, containing all the technology related information automatized for the design, simulation and layout of the user components, and the guidelines to submit contributions to the platform.

New process modules are under development to enable expansion of the platform from visible to mid-infrared wavelengths, increasing the functionality of the photonic integrated circuit to cover the biosensing and molecular spectroscopy applications. The modules are based in the experience gained by fabricating interferometric biosensors [78] and PICs for nanoscopy purposes working in the visible range [79].

There is on-ongoing research to design and demonstrate SiN membrane waveguide technology for broadband operation (λ range 0.4–6.7 μm).

IV. Long Wavelength Silicon Photonics Platforms

In 2006, Soref proposed to expand the Si photonics technology to the long-wave infrared region, advocating that the co-integration of group IV photonics with appropriately designed III-V heterostructures, could be effectively translated to the Mid-IR wavelength band [3–12 μm] to obtain fully integrated optical devices [80], [81]. The applications addressed by these technologies include free-space data communication, optical countermeasures, IR imaging of biological tissues, spectroscopy and many others. However, the most mature field of use is the detection of traces of chemicals in gaseous, liquid or solid phases. Due to its high absorption, silicon oxide is not allowed in this wavelength band. CEA-LETI has developed a technology platform for PIC fabrication based on SiGe materials on 200 mm Si wafers. For applications in the 3–8 μm range, the waveguides are composed of a SiGe40% core surrounded by Si cladding. In the 8–12 μm range, the waveguides are composed of a pure epitaxial Ge surrounded by SiGe cladding [82]. The TRL is around 5 to 6. VTT has also demonstrated low-loss (0.1–0.5 dB/cm) operation in both 4 and 11 μm thick SOI waveguides at 3.4 μm wavelength. Absorption in silicon oxide has been avoided by using an air cladding (see Fig. 12).

The technologies are accessible through the European MIRPHAB pilot line via the website http://www.mirphab.eu/ and the broker CMP. It is an open access service with a focus on industrial users. Dedicated runs of a limited number of wafers are used for specific prototyping. Based on a design rule manual for each technology, the design can be optimized for each application.

For gas sensing applications with a need for combining different sources, many AWGs with a high number of inputs have been designed and produced. As an example, we report here results @ 4.5 μm with SiGe/Si technology. Basic passive devices (lines, bends, and splitters with Multi-Mode Interferometers) were first characterized in order to verify the quality of fabrication. The waveguide loss was measured by cut-back method using spirals

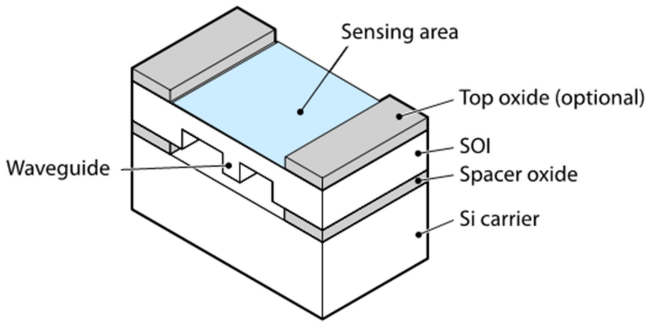

Fig. 12. Illustration of a Thick-SOI waveguide for mid-infrared sensing applications.

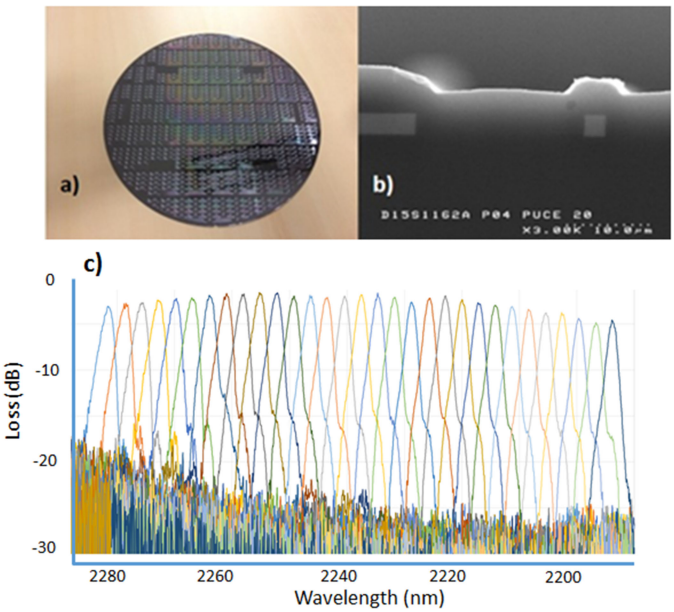

Fig. 13. (a) 200 mm SiGe/Si wafer for mid-IR PICs. (b) Cross section of the fabricated waveguides. (c) Transmission response of 31 channels of the AWG operating at mid-IR wavelengths.

waveguides [83] and is ~0.3 dB/cm. The Arrayed Wave Guide AWG is designed with 17 outputs and 35 input waveguides. The AWG exhibited a low-loss normalized transmission (−1.6 dB insertion loss) with a crosstalk below −12 dB (see Fig. 13). The maximum shift from channel spacing measured for the AWG central output was $\Delta\sigma_{input22} = 0.13$ cm^{-1}, which is a 4 % variation from the designed 2.94 cm^{-1} channel spacing.

Under the MIRPHAB and REDFINCH EU projects, these technologies are in permanent evolution in order to address many other application fields. Especially the introduction of other materials could give more versatility. For example, supercontinuum in the MIR could have an interest in spectrometers.

V. Evolution of the European Silicon Photonics Ecosystem

Silicon photonics draws its value proposition from the ability to demonstrate cheap and compact photonic *System on a Chip* (SoC). A mature technology platform with high TRL is

one element to demonstrate high-density photonic SoC using silicon photonics. Equally important are Electronic-Photonic Design Automation (EPDA) tools for the design of photonic SoCs, and advanced packaging and assembly tools/techniques to test them. In the last few years, the European silicon photonics ecosystem has consolidated to offer a complete supply chain to transform a design idea into a functional integrated photonic system. On the design side, the interoperability between physical level simulation tools, circuit level simulation tools, system-level simulation/emulation environments and electronic design tools has increased. Similarly, for the packaging and assembly aspects, a broad range of solutions have emerged. This includes techniques for fiber to chip coupling or PIC to PIC coupling, DC/RF electrical interfacing with PICs, assembly of electrical ICs and photonic ICs, handling of thermal and mechanical issues for packaging, and standardised test protocols. The above-mentioned packaging and assembly solutions for small volumes are provided by the PIXAPP packaging pilot lines. The pilot lines also provide scale-up routes towards larger volume silicon PIC packaging and assembly [6], [85].

VI. Summary

Open-access of silicon photonics is of vital importance to enable the uptake of this technology by industry. The silicon photonics open-access model emulates the proven methodology used by electronics. In Europe, various types of open-access silicon photonics technologies are offered to address the needs of different market sectors. The maturity of the European open-access platforms enables routes for scalable volume manufacturing of PICs.

Appendix

The TRL of open-access silicon photonics platforms discussed in this paper are defined by using the below defined criteria. The definitions of these TRLs are determined by translating the TRL definitions outlined by the European Commission [84].

- *TRL 1, 2 and 3:* not applicable
- *TRL 4:* PIC process flow successfully developed and demonstrated in a laboratory environment, typically with research-oriented tools
- *TRL 5:* PIC process flow successfully developed in an environment with manufacturing-grade tools or wafer-level prototyping tools
- *TRL 6:* PIC process flow successfully and reproducibly demonstrated (with a yield acceptable for prototyping) in an environment with manufacturing-grade tools or wafer-level prototyping tools
- *TRL 7:* Prototyping (including MPW-based prototyping or dedicated full-wafer prototyping) of market-relevant products by means of a PIC process flow that has been successfully and reproducibly demonstrated (with a yield acceptable for at least prototyping) in an environment capable of manufacturing or wafer-level prototyping
- *TRL 8:* PIC process flow qualified with respect to manufacturing requirements (yield, turn-around-time, quality assurance) in an environment capable of manufacturing
- *TRL 9:* PIC process flow used for competitive manufacturing at least at low and/or high-volume level

Hereby the following definitions are used for various open-access modalities:

- *MPW-based prototyping:* up to 100 chips per order.
- *Prototyping:* typically one to a few wafers per order.
- *Low-volume manufacturing:* up to 50 wafers per order.
- *Medium-volume manufacturing:* up to 500 wafers per order.
- *High-volume manufacturing:* beyond 500 wafers per order.

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Graham Reed is currently a Professor of silicon photonics and Group Leader. He joined the University of Southampton, Southampton, UK, in 2012 from the University of Surrey, Guildford, UK, where he was Professor of Optoelectronics, and was Head of the Department of Electronic Engineering from 2006 to 2012. He is a pioneer in the field of silicon photonics, and acknowledged as the individual who initiated the research field in the UK. He established the Silicon Photonics Research Group at the University of Surrey in 1989. The first silicon photonics company in the world, Bookham Technology, Inc., was founded by Reed's Ph.D. student, Dr. A. Rickman, and adopted the research developed in the Group. The Silicon Photonics Group has provided a series of world leading results since its inception, and is particularly well known for its work on silicon optical modulators. He has authored or coauthored more than 500 papers in the field of silicon photonics. Prof. Reed is a regular invited and contributing author to the major silicon photonics conferences around the world. He has served on numerous international conference committees. He is currently a member of five international conference committees.

Georg Winzer received the Dipl. Ing. degree in electrical engineering from the Technical University Berlin, Berlin, Germany, in 2012, and is currently working toward the Ph.D. degree. Starting in 2006, he worked with the center for Hochfrequenztechnik-Photonic at Technische Universität Berlin on layout and measurement of photonic integrated circuits. Since 2012, he has been with IHP Microelectronics, Frankfurt, Germany, where his research interests include the design and layout of PIC and EPIC devices, high-speed O/E device characterization, and the setup of a photonic design-kit.

Stefan Lischke received the B.Sc. and M.Sc. degrees in physics with specialization in semiconductor technology from the Technical University Brandenburg, Cottbus, in 2005 and 2007, respectively, and the Ph.D. degree in physics from the Technical University Berlin, Berlin, Germany, in 2017. He is currently a Researcher with the Silicon Photonics Group within the Technology Department of IHP—Leibniz-Institut fr innovative Mikroelektronik, Frankfurt, Germany. His current work is focused on Germanium photo detectors and the integration of photonic devices into IHP's photonic BiCMOS technology. He was the recipient of the several Best Paper Awards.

Lars Zimmermann was born in Germany. He received a higher education (undergraduate) from Friedrich-Schiller University, Jena, Germany, Brunel University London, London, U.K., and TU Delft, Delft, The Netherlands, and the Ph.D. degree from IMEC, Leuven, Belgium, in 2003. He moved to Belgium for his postgraduate studies at Katholieke Universiteit Leuven. In Leuven, he was affiliated with IMEC where he worked for five years. His scientific work at IMEC dealt with the development of extended short-wave infrared detector arrays and sensor assembly processes. In 2004, he moved to TU Berlin. In Berlin, he worked for five years on silicon-based optical motherboard technology, realizing early hybrid assemblies of silicon waveguides with lasers, semiconductor optical amplifiers, and detectors. In 2008, he moved to IHP, the Leibniz Institute für innovative Mikroelektronik. At IHP, he directs the silicon photonics activities. In 2018, he re-joined TU Berlin where he is currently a Professor in the field of silicon photonics. He is also a Team Leader Silicon photonics at IHP, coordinating the cooperation with TU Berlin in the field of Silicon photonics within the frame of the Joint Lab Silicon Photonics. His current work is focusing on high-performance photonic-electronic integration for optical communications and for nonlinear optical signal processing.

Dieter Knoll received the Diploma degree in physics from the Technical University of Chemnitz (the former Karl-Marx-Stadt), Chemnitz, Germany, in 1974, and the Ph.D. degree in applied physics from the Academy of Sciences of the GDR, Berlin, Germany, in 1988. From 1974 to 2017, he has been with IHP in Frankfurt, Germany, where he was engaged in research on the fabrication of silicon-based devices and circuits. He is currently a consultant in the field of photonics integration. His research interests included npn-SiGe-base and SiGe:C-base bipolar transistors, pnp bipolar transistors, BiCMOS technology, and Si photonics.

Douwe Geuzebroek received the Ph.D. degree in electrical engineering from the University of Twente, Enschede, The Netherlands, at the Integrated Optical MicroSystem Group on a topic of applying integrated optical microring resonators in telecommunication networks. He is currently with the VP Marketing and Sales at LioniX International. He has more than 15 years of experience in integrated photonics and its applications, ranching from R&D to product development stages. He has a strong interest in matching the technical aspect of a technology to the needs of the market. In 2005, he joined LioniX BV as a Design Engineer and Project Leader focusing on microring resonators and other integrated optical telecommunication devices and was actively involved in the startup of XiO Photonics in 2008. As VP Marketing and Sales at XiO Photonics, he supported the development of the waveguide technology for visible light applications and the introduction of this technology in several products. He participated in several research projects both national and European. Currently, as VP Marketing and Sales at LioniX International, he is involved in the acquisition of new commercial and research projects for photonic integrated modules in life science, metrology, and telecommunication applications.

Arne Leinse received the Ph.D. degree in the integrated optical microsystems group from the University of Twente, Enschede, The Netherlands, in 2005. He is currently active in integrated optics for more than 15 years. Hereafter, he joined LioniX BV where he was involved in the invention and development of the TriPle platform from the beginning. He has been involved from the original concept until the exploitation and (co)authored more than 100 articles in the last years. He has been active as a Vice-President of LioniX BV in the last years and since the establishment of LioniX-international in 2016 active in the role of Chief Commercial Officer.

Michael Geiselmann received the degree in physics and engineering from the University of Stuttgart, Stuttgart, Germany, the graduate degree from the Ecole Centrale Paris, France, in 2008, and the Ph.D. degree from the Institute of Photonic Sciences, Barcelona, Spain, in 2014. He joined the Laboratory of Prof. Kippenberg at EPFL, Lausanne, Switzerland, where he advanced frequency comb generation on integrated silicon nitride chips towards applications. He was leading several international research projects. In 2016, he cofounded LIGENTEC. As a Managing Director, he is responsible for strategy, sales, and business development. He coauthored more than 18 publications and over 20 conference contributions.

Michael Zervas received the B.S. and M.S. degrees in applied mathematics and applied physics from Athens Technical University, Athens, Greece, in 2005, and the M.Sc. degree in micro and nano technologies for integrated systems, joint master's degree received by the Ecole Polytechnique Federale de Lausanne (EPFL), Lausanne, Switzerland, Institut National Polytechnique de Grenoble, Genoble, France, and Politecnico di Torino, Turin, Italy, in 2007, and the Ph.D. degree from the Department of Electrical Engineering, EPFL, under the supervision of Prof. Leblebici in the area of nanofabrication, in 2013.

From 2007 to 2010, he was with Oerlikon, first as a Management Trainee and later as a Strategic Procurement Manger, Singapore for Oerlikon Solar (two years). He was with IBM from 2012 to mid 2013 under CMOSAIC Project as an Research Associate and with the Intel from 2013 to 2014, as a Process Engineer for the 14-nm node. After rejoining EPFL, as a Scientist in mid 2014, he cofounded LIGENTEC, Lausanne, Switzerland, in 2016, where he is advancing the technology development of silicon nitride based integrated circuits.

Hilde Jans received the Ph.D. degree in chemistry from the Catholic University of Leuven, Leuven, Belgium, in 2010. She is a Senior Researcher with the Experimental Bio-Photonics Team of the LSI Department. Her main activity is to link the (bio-) application to the technology under development in the team. Since 2011, her focus is on Raman spectroscopy applications as she is involved in many project, both bilateral and European projects.

Andim Stassen received the B.S. degrees in physics and molecular biology and genetics from Istanbul Technical University, Istanbul, Turkey, and the M.S. degree in nanoscience and nanotechnology from Catholic University of Leuven, Leuven, Belgium, in 2010. In the same year, she joined Life Science Technologies Department at imec. She is currently working as a Process Integration Engineer for life science applications and she is responsible of the SiN photonics platform development.

Carlos Domínguez received the B.S., M.S., and Ph.D. degrees in chemistry from the Universidad Complutense of Madrid, Madrid, Spain, in 1980, and 1985, respectively. He became a member of the scientific staff at the Instituto de Microelectrnica de Barcelona (IMB-CNM, CSIC) in 1986. Since 2002, he has been a Research Professor. In 1992, he founded the Chemical Transducers Group within the institute, having today 28 researchers and technicians, and has been recognized as a Technological Transfer Center by the Catalan Government. He is a member of the Spanish Royal Society of Chemistry, the Committee of Optoelectronics and Integrated Optics of the Spanish Optical Society, and a member of the International Committee of Ibersensor. Also a member of the Association EPIC (European Photonic Industry Consortium) Technology Platform Photonics21, and former member of SECPhO Technology Cluster (Cluster of Southern Europe Photonics and Optics). He is involved in materials and process development for new transducers and sensor devices, authored or coauthored around 165 papers in this area. He is currently working on the development of an integrated optical technology based on silicon and silicon compounds for (bio)-chemical sensors and broadband telecommunications applications.

Pascual Muñoz was born in Valencia, Spain, on February 7, 1975. He received the Ingeniero de Telecomunicacion degree and the Ph.D. degree in photonics from Universitat Politecnica de Valencia (UPV), Valencia, Spain, in 1998 and 2003, respectively. In 1999, he served as 1st Lieutenant in the Spanish Airforce, while working as IT consultant for AIME Instituto Tecnologico. He is currently an Associate Professor with the Departamento de Comunicaciones, and a Researcher with the Institute for Telecommunications and Multimedia Applications, both at UPV. He runs a consolidated research line, started in 2005, on prototyping Photonic Integrated Circuits (PICs) in a technology agnostic fashion, where PICs are designed in the best suited technology (Silicon-On-Insulator, Indium Phosphide, Silica on Silicon, Silicon Nitride amongst other) for each application. He has been involved in several European Commission funded projects, being coordinator for integration on InP within the NoE IST-EPIXNET. He has authored or coauthored more than 40 papers in international refereed journals and more than 60 conference contributions. He is a member of the Technical Programme Committees of the European Conference on Optical Communications and the European Conference on Integrated Optics. He was the recipient of the VPI Speed Up Photonics Award in 2002 for innovative Fourier optics AWG with multimode interference couplers modeling, by Virtual Photonics Incorporated and the IEEE COMMUNICATIONS MAGAZINE. He was also granted the IEEE/LEOS Graduate Student Fellowship Program in 2002. He was also the recipient of the extraordinary doctorate prize from UPV in 2006. From his research line, he cofounded the UPV spin-off company VLC Photonics in 2011, where the PIC design know-how, expertise and tools have been transferred, and he served as CEO from 2011 to 2013. He is a Senior Member of the OSA.

David Domenech was born in Alfafar, Valencia, Spain. He received the B.Sc. degree in telecommunications from the Escuela Politecnica Superior de Gandia, Valencia, Spain, in 2006, the M.Sc. degree in technologies, systems and networks of communication from the Universidad Politecnica de Valencia, Valencia, Spain, in 2008, and the Ph.D. degree in photonics from the Universitat Politecnica de Valencia within the Optical and Quantum Communications Group in 2013. He has been involved in several national and international research projects. He has authored or coauthored more than ten papers in international refereed journals and more than 20 conference contributions. He was the recipient of the Intel doctoral student honor programme award in 2012 in recognition for his work during his Ph.D. He is a Cofounder and CTO of the spin-off company VLC Photonics, devoted to the design of photonics integrated circuits in multiple integration technologies.

Anna Lena Giesecke received the Diploma degree from Leibniz University, Hannover, Germany, and the doctoral degree in physics from Heinrich-Heine University, Dsseldorf, Germany. She joined AMO GmbH in 2013 and is the Head of the nanophotonics group. She has been working in the research fields of ultrafast laser sources, plasma physics, and photonic integrated circuits based on silicon and silicon nitride as well as optoelectronic devices. One of her current research interests is the integration of light sources into dielectric platforms.

Max C. Lemme received the Dipl.-Ing. and Dr.-Ing. degrees in electrical engineering from RWTH Aachen University, Aachen, Germany. He is currently a Professor of electronic devices with RWTH Aachen University and the Director of AMO GmbH, Aachen. His current research interests include electronic, optoelectronic, and nanoelectromechanical devices and sensors made from novel materials like graphene and related 2-D materials, Perovskites or phase change materials and their integration into the silicon technology platform.

Roel Baets received the M.Sc. degree in electrical engineering from UGent in 1980 and a second M.Sc. degree from Stanford in 1981, and the Ph.D. degree from UGent in 1984. He is currently a Full Professor with Ghent University (UGent) and is part-time associated with IMEC. From 1984 till 1989, he held a Postdoctoral Position with IMEC. Since 1989, he has been a Professor with the Faculty of Engineering and Architecture of UGent where he founded the Photonics Research Group. From 1990 till 1994, he has also been a part-time Professor with Delft University of Technology and from 2004 till 2008 at Eindhoven University of Technology. He has mainly worked in the field of integrated photonics. He has made contributions to research on photonic integrated circuits, both in III-V semiconductors and in silicon, as well as their applications in telecom, datacom, sensing, and medicine. Web of Science reports more than 600 publications with an h-index well over 60. As part of a team of eight professors he leads the Photonics Research Group. With about 90 researchers this group is involved in numerous (inter)national research programs and has created six spin-off companies. The silicon photonics activities of the group are part of a joint research initiative with IMEC. He has led major research projects in silicon photonics in Europe. In 2006, he founded ePIXfab, the globally first Multi-Project-Wafer service for silicon photonics. Since then ePIXfab has evolved to become the European Silicon Photonics Alliance. He is also the Director of the multidisciplinary Center for Nano- and Biophotonics (NB Photonics) at UGent, founded in 2010. He was a cofounder of the European M.Sc. programme in Photonics. He is an ERC grantee of the European Research Council and a Methusalem grantee of the Flemish government. He is a Fellow of the IEEE, of the European Optical Society, and of the Optical Society. He is also a member of the Royal Flemish Academy of Belgium for Sciences and the Arts. He has been a recipient of the 2011 MOC Award and of the 2018 PIC-International Lifetime Achievement Award. He is Director-at-Large with the Board of Directors of The Optical Society.