

Thermally Tunable Quantum Cascade Laser With an External Germanium-on-SOI Distributed Bragg Reflector

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Abstract—Quantum cascade lasers (QCLs) are essential components for mid-infrared optical spectroscopy. Currently, widely tunable QCLs are using an external diffraction grating to tune the laser wavelength. In this paper we present a compact tunable QCL that is thermally tuned by a distributed Bragg reflector (DBR) implemented on a Germanium-on-SOI (Ge-on-SOI) waveguide circuit. The 5.1x μm wavelength laser, operating in pulsed mode at room temperature, is continuously tuned over 50 nm.

Index Terms—Quantum cascade lasers, distributed Bragg reflector, Germanium-on-SOI, mid-infrared.

I. INTRODUCTION

MID-IRRED spectroscopy is a highly discriminatory technique used for chemical analysis of gases, liquids and solids. The mid-infrared spectral region (2–20 μm) covers the fundamental vibrational transitions of many important molecules. This gives the mid-infrared region an advantage over the transitions at near-infrared and visible wavelengths, which mostly correspond to overtones and hence have orders of magnitude lower absorption cross section compared to the fundamental transitions [1]–[4]. In addition, molecular spectra in the mid-infrared are less densely arranged, allowing for selective spectroscopic detection of a large number of molecules, while near-infrared and visible spectra in general consist of overlapping bands that may be difficult to resolve [5].

QCLs are semiconductor lasers based on resonant tunneling and optical transitions between electronic levels within the conduction band of a multi-quantum well structure. As a result, the wavelength of the emitted light is determined by the thickness of the wells and barriers and can be tailored by band-gap engineering. QCLs allow for high optical output power in continuous

wave operation at room temperature [6]–[9]. Moreover, QCLs can be designed with a broadband gain medium, with full widths at half maximum of more than 200 cm^{-1} [10], enabling wide wavelength tunability.

Wavelength tuning currently mostly relies on combining a quantum cascade (QC) gain chip with an external grating, which provides wavelength-selective feedback to the laser and defines its emission wavelength. External cavity quantum cascade lasers (EC-QCLs) are widely tunable but are cumbersome and complex to build. They require well-aligned external optical components including a rotating diffraction grating for tuning, and a highly precise rotation mechanism that is prone to instabilities [11]. The implementation of a MEMS-based tunable diffraction grating partly overcomes these issues [12], however the assembly process remains cumbersome. In this paper we propose implementing the wavelength selecting external cavity on a silicon photonic chip in order to replace the external rotating grating. Whilst QCLs integrated on silicon waveguide circuits through wafer bonding have been demonstrated [13], these demonstrations were limited to non-tunable laser structures, with measured output peak power ~ 20 mW. Although papers show laser diode wide tuning by an external cavity on a silicon chip with the gain chip integrated through butt-coupling, flip-chip integration or wafer bonding [14], [15], this is the first time a QCL is employed, thereby paving the way to miniaturized widely tunable sources in the mid-infrared, without any moving parts which improves the stability, compactness and robustness of the system. The combination of silicon-based photonic integrated circuits (PICs) and efficient mid-infrared QCLs capable of operating at room temperature [6] are therefore expected to enable low-cost and compact mid-infrared optical sensors [16], [17].

Due to the high absorption of SiO_2 in the mid-infrared [18], the traditional silicon-on-insulator (SOI) photonic integration platform used at telecom wavelengths is limited to an operation wavelength of 4 μm [19]. In order to fully exploit the mid-infrared wavelength region, multiple silicon-based platforms have been proposed for the implementation of mid-infrared PICs beyond 4 μm using silicon as the guiding material, some of which rely on a suspended silicon membrane [20] or a silicon-on-sapphire layer stack [21]. However, using silicon as the waveguide core material limits the wavelength range of operation to about 8 μm . A number of devices have also been demonstrated on a graded index Silicon-Germanium (SiGe) waveguide

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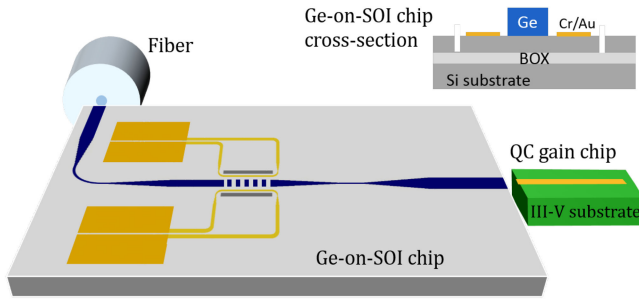


Fig. 1. A thermally tunable external cavity QCL without any moving parts: The rotating grating is replaced by a tunable DBR integrated on a Ge-on-SOI chip.

platform [23], as well as on Ge-on-Si and Ge-on-SOI platforms at wavelengths beyond $4 \mu\text{m}$ [24]–[28], with the potential of covering a broader wavelength range, ultimately limited by the transparency window of germanium ($1.6\text{--}14 \mu\text{m}$). While low propagation losses have experimentally been demonstrated on the graded index SiGe platform [29], the relatively weak index contrast leads to large bending radii and consequently a large PIC footprint. The Ge-on-Si platform benefits from a simple fabrication process and a strong index contrast. Unlike the Ge-on-Si platform, the Ge-on-SOI stack has an additional SiO_2 layer, which allows for more efficient integrated thermo-optic phase shifters [30] as the silica layer acts as a thermal insulation layer or as a sacrificial layer. On this platform, the Si undercladding of the Ge waveguide is thick enough to prevent overlap of the Ge waveguide mode with the underlying oxide, preventing excessive losses from the highly absorbing oxide at these wavelengths. In this paper we realize a thermally tunable QCL using a Ge-on-SOI wavelength selection/tuning element. The design that is used for this purpose is shown in Fig. 1. The QC gain chip is coated with a high reflection (HR) coating on one side, while the other facet has an anti-reflection (AR) coating which enables the laser cavity to be formed between the HR facet and a thermally tunable Ge-on-SOI DBR for the wavelength selection. Two symmetrical heaters on the two sides of the grating are used for thermal tuning. In this paper we demonstrate a 50 nm continuously tunable DBR-QCL operating in the $5.1 \mu\text{m}$ wavelength range. In this wavelength we can find absorption lines of acetylene, formic acid, ammonia and many other compounds of interest [5].

II. QUANTUM CASCADE GAIN CHIP CHARACTERISTICS

The active region of the QC gain chip used in our work, is based on a GaInAs/AlInAs lattice grown on a InP substrate [8]. The maximum operation temperature, room-temperature maximum peak power per facet, and room-temperature slope efficiency of the QCL are improved by using a slightly-diagonal transition between the initial and the final electron state in the active region and the introduction of AlAs blocking barriers [9]. The ridge waveguide is $10 \mu\text{m}$ wide and 3.5 mm long. Light is emitted from the cleaved front facet of the waveguide coated with a broadband $\text{SiO}_2/\text{Si}/\text{SiO}_2$ AR coating. The laser structure is mounted epi-side up on a heat sink. A small ($50 \mu\text{m}$) overhang

of the gain chip from the heat-sink is implemented to enable the butt coupling of the gain chip to the silicon PIC.

III. WAVEGUIDE CIRCUIT DESIGN AND SIMULATIONS

The DBR is implemented on a Ge-on-SOI waveguide platform consisting of a $2 \mu\text{m}$ thick germanium waveguide layer on a $3.2 \mu\text{m}$ silicon bottom cladding on top of a $2 \mu\text{m}$ thick SiO_2 layer. In order to get a narrow reflection bandwidth and hence a spectrally pure emission, a partially etched grating is needed. However, there are two limitations that come into play: on one hand, the shallower the grating, the longer the grating structure needs to be for a given reflectivity, which means that a longer grating section needs to be temperature tuned, increasing the power dissipation of the heater. Secondly, there is the issue of the control of the etch depth. The etching rate of our dry etching recipe is around 25 nm/min , including a dead-time in which no etching occurs. Therefore, shallow etched gratings are harder to control. We found that a 50 nm etched grating is a good compromise between grating strength and controlled fabrication. Heaters are deposited on both sides of the grating (on the silicon undercladding) to enable thermal tuning (Fig. 1). The laser cavity is formed by the III-V gain chip HR facet and the DBR, while the output waveguide of the PIC is used to direct the light off the silicon chip. The input and output waveguides on the silicon chip are positioned under 90° to avoid direct light coupling from the gain chip to the fiber (Fig. 1). A TiO_2 quarter-wavelength anti-reflection coating is deposited on both facets of the Ge chip - the facet facing the III-V gain chip and the facet facing the fiber.

A. Gain Chip - Ge-on-SOI Waveguide Coupling

Both the gain chip ridge waveguide and the Ge input waveguide are $10 \mu\text{m}$ wide. While the width of the Ge input taper could be selected to allow maximum overlap with the mode of the gain chip, the thickness of the Ge layer was fixed to $2 \mu\text{m}$ on our platform which limits the maximum butt-coupling efficiency, as the $1/e^2$ width of the quantum cascade mode intensity profile along the fast axis (perpendicular to the III-V stack) is about $3 \mu\text{m}$. From Fig. 2a, showing the sensitivity of the coupling efficiency to a misalignment of the gain chip along the fast axis and slow axis of the gain chip, we can see that due to the geometry of the cross-sections of the two waveguides, the alignment along the fast axis is more sensitive than the alignment along the slow axis.

For the optimal alignment along the fast and slow axis, we have simulated the butt-coupling efficiency between the gain chip and the Ge-on-SOI chip with and without AR coating on the two facing facets as a function of the gap between both chips. The simulations are performed assuming perfect one-layer AR coatings for the two layer stacks at $5.1 \mu\text{m}$ wavelength. In Fig. 2b we see that while the coupling efficiency for perfect butt-coupling between the chips is higher in the case without AR coatings (attributed to the finite thickness of the AR coatings and the associated diffraction loss), the coupling efficiency is less sensitive to the gap between both chips when AR coatings are present. This is due to the Fabry-Perot effect caused by

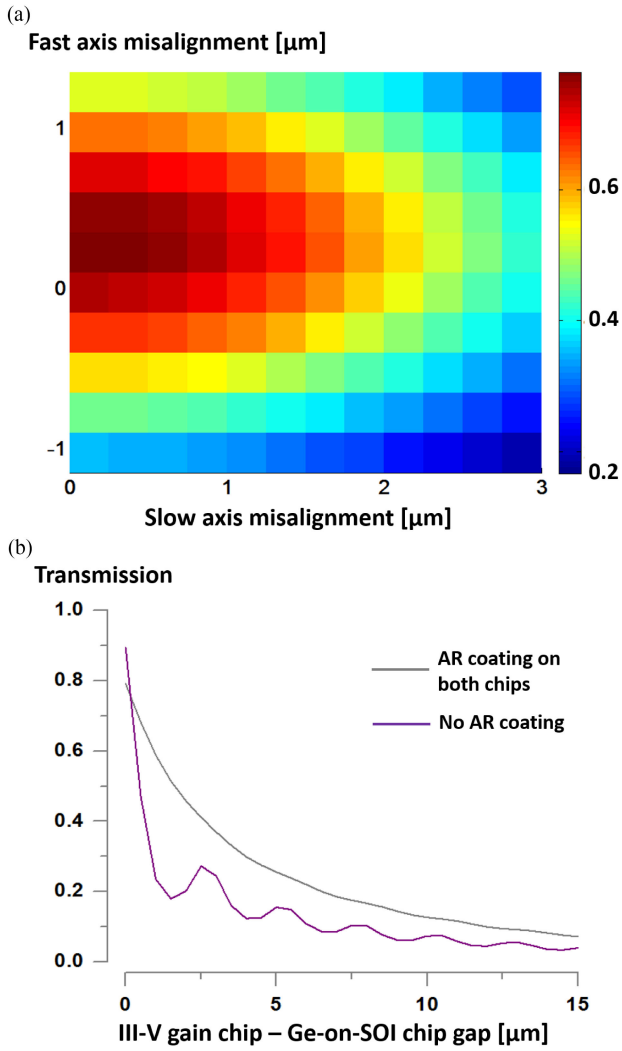


Fig. 2. A simulation of the impact of misalignment along the fast and slow axis between the III-V active region ridge waveguide and the Ge-on-SOI input waveguide on the coupling efficiency (a). For optimally aligned waveguides, the coupling efficiency as a function of the gap between the waveguides (b).

reflections at the interfaces in the case without AR coatings. The maximum butt-coupling efficiency of the chips with AR coatings is 80% with 3 dB less coupling for a gap of 2.5 μm between the two chips, while maximum coupling without AR coatings is 90% with already 3 dB less coupling for a gap of 0.5 μm .

B. DBR Design

The distributed Bragg reflector grating is etched 50 nm in the 10 μm wide Ge waveguide. The Ge waveguide is then tapered down to a short single-mode waveguide section serving as a transversal mode filter, followed by tapering up to a 10 μm waveguide for optimal overlap with the gain chip mode. Using wider waveguides also helps to reduce the intra-cavity losses. Single mode waveguide (typical loss of 3–5 dB/cm [24]) is used only in the short transversal mode filter section and bends. The tapers are 350 μm long linear tapers. The grating

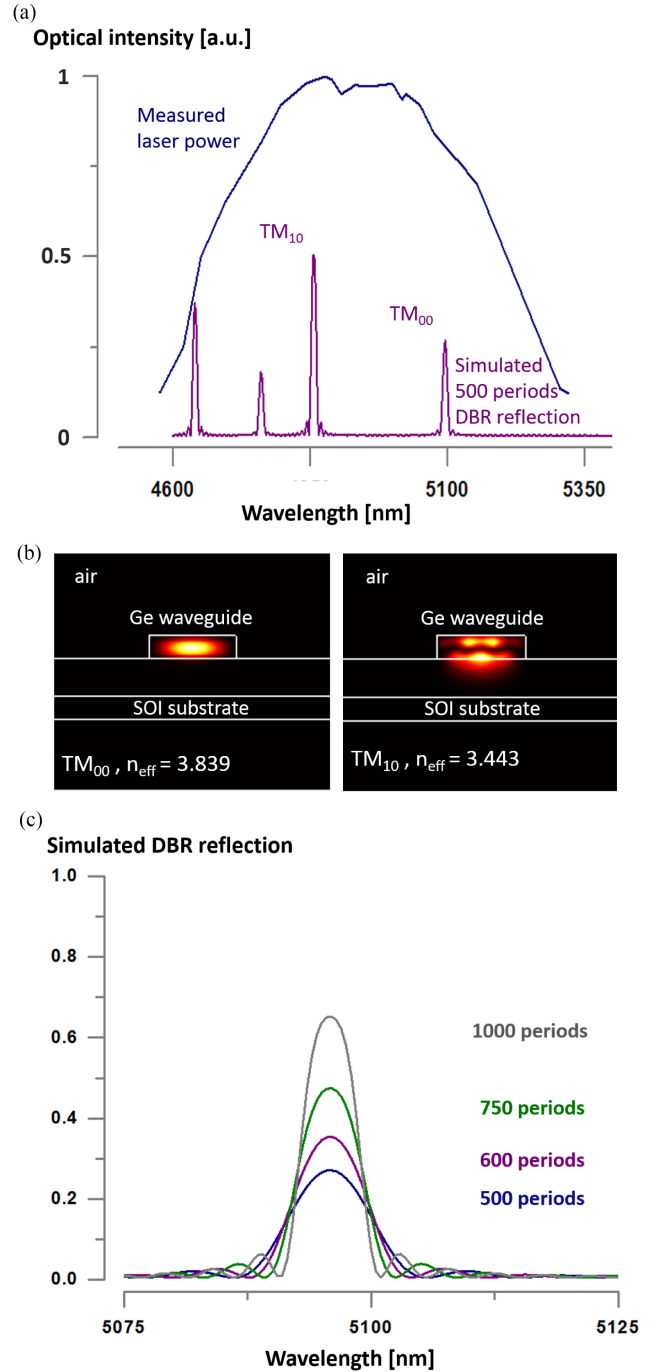


Fig. 3. (a) A measurement of the laser power vs. emission wavelength in an EC-configuration (Littrow type) and a simulation of the DBR reflectance when the fundamental TM mode is exciting the waveguide. (b) field distribution of the fundamental TM₀₀ mode and the TM₁₀ mode. (c) DBR reflectance as a function of the number of grating periods.

period is set to 660 nm with 60% duty cycle (tooth to period ratio). The simulation of the DBR reflectance when the TM₀₀ fundamental mode is exciting the grating is shown in Fig. 3a for a 500 period long grating together with the measured laser power. The laser power vs. emission wavelength was measured in an EC-configuration (Littrow type) at laser currents well above threshold. Close to threshold, where we performed our

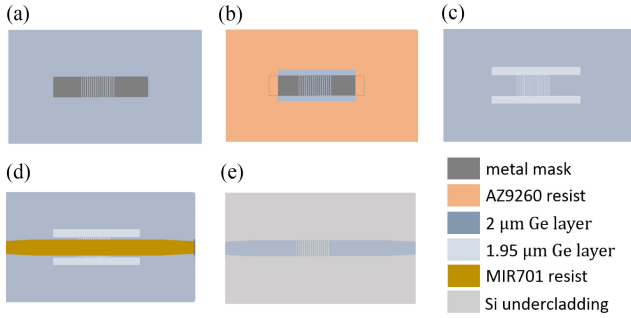


Fig. 4. The waveguide circuit fabrication consists of one combined e-beam/contact lithography followed by a partial etch step (a–c) to define the grating, and a contact lithography followed by a full etch to define the waveguides (d, e).

measurements, the gain bandwidth will be smaller. A strong reflection to the TM_{00} mode can be observed around $5.1 \mu\text{m}$ wavelength. At shorter wavelengths strong reflections to higher order modes are present, as is indicated in Fig. 3a. However, since these modes do not couple efficiently to the gain chip waveguide mode, they can be neglected when studying the laser operation. The first two modes of the $10 \mu\text{m}$ wide Ge-on-SOI waveguide, TM_{00} and TM_{10} are simulated at $5.1 \mu\text{m}$ wavelength and displayed on Fig. 3b. The dependence of the grating reflection on the number of grating periods is plotted in Fig. 3c. The FWHM of the grating reflection is about 5 nm .

IV. DEVICE FABRICATION

A combination of electron-beam lithography and optical lithography is used to define the Ge-on-SOI waveguide circuit, comprising a 50 nm deep etch for the grating and a $2 \mu\text{m}$ deep etch for the waveguide structures. In the first step we use a positive e-beam resist (AR-P 6200.09) to define the grating by a Ti/Cr (5 nm and 50 nm thick respectively) metal mask through a lift-off process (Fig. 4a). Since we are using positive e-beam resist, prior to etching the rest of the chip is protected by a thick AZ9260 resist (Fig. 4b). The grating is etched 50 nm in a CF_4/H_2 plasma after which the photoresist is stripped and the metal mask is removed using HF (Fig. 4c). The e-beam write field is $500 \mu\text{m}$ by $500 \mu\text{m}$, which allows accommodating the entire grating, up to 750 periods, in a single write field and hence avoids stitching errors inside the grating. The waveguides are defined by contact lithography with MIR701 resist (Fig. 4d) and subsequently etched in a $\text{CF}_4/\text{SF}_6/\text{H}_2$ plasma (Fig. 4e). The remaining photoresist is removed by O_2 plasma, followed by an acetone and isopropylalcohol rinse.

Next, Cr/Au heaters are defined at both sides of the grating using an image reversal lithography with Ti35 resist and lift-off (Fig. 5b). The Cr/Au (100 nm and 10 nm respectively) heaters are deposited directly on the silicon undercladding by electron beam evaporation. The same type of lithography followed by a lift-off step is used to deposit 700 nm thick Au contacts by sputtering. The buried oxide layer in the substrate prevents efficient heat sinking into the Si substrate, which enhances the efficiency of the heaters. To better thermally isolate the heaters

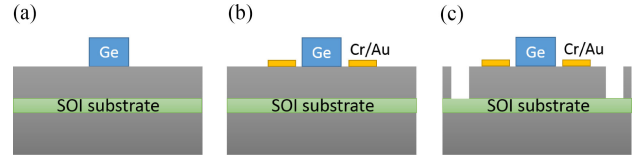


Fig. 5. Heaters are deposited directly on the silicon undercladding in proximity of the grating (a, b). A silicon etch step is performed to confine the heat laterally (c).

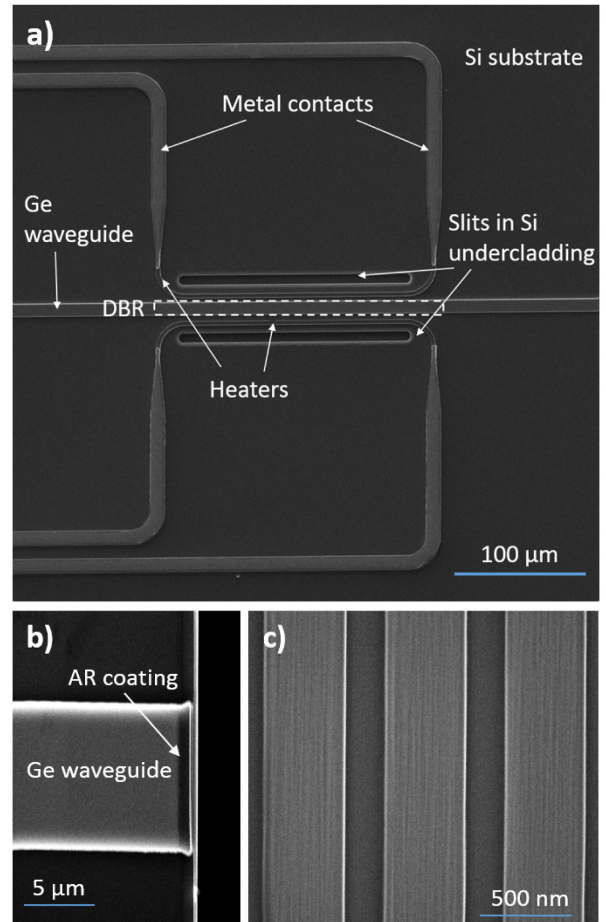


Fig. 6. SEM images of the fabricated Ge-on-SOI chip: the DBR structure with heaters (a), Ge facet with AR coating (b) and a zoom-in on the grating (c).

laterally and further improve their efficiency, we additionally etch through the Si undercladding layer to reach the SiO_2 in the vicinity of the heaters (Fig. 5c). For this AZ9260 photoresist and a $\text{CHF}_3/\text{SF}_6/\text{O}_2$ plasma is used. After etching, the remaining photoresist is again removed by a O_2 plasma treatment, followed by an acetone and isopropylalcohol rinse.

After the circuit definition and the heater deposition the sample is lapped down to $350 \mu\text{m}$ thickness to allow for a better cleave. After cleaving, a TiO_2 625 nm thick anti-reflection coating is deposited by electron beam evaporation on both facets of the circuit.

SEM images of the final device are shown in Fig. 6, where the grating with the double heater structure is shown in figure

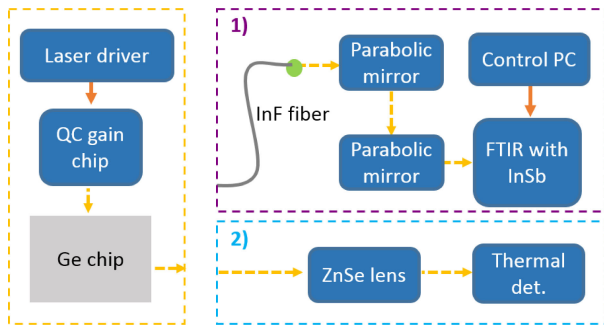


Fig. 7. The measurement setup consists of a fixed block on the left - the light source, and two detection blocks that are interchangeable. Detection block 1) measures the optical spectrum with an uncalibrated detector while block 2) has a calibrated thermal detector.

Fig. 6a, while the AR-coated facet and a close-up on the grating pitch are displayed in Fig. 6b and c.

V. MEASUREMENT SETUP AND RESULTS

The measurement setup is schematically shown in Fig. 7. The QC gain chip used a dedicated driver allowing operation in pulsed mode (100 kHz repetition rate, 1 μ s pulse duration). The gain chip is mounted on a cooling stage and the temperature is fixed at 20 °C. The gain chip is butt-coupled to the Ge-on-SOI chip, which is mounted on a separate translation stage. The heaters on the Ge-on-SOI chip are actuated by a Keithley current source (not shown in Fig. 7). For device characterization we used two different schemes. The first option is to use an InF single mode fiber to take the signal of the Ge chip to a FTIR with an uncalibrated InSb detector, which allows us to monitor the emission spectrum. The second detection scheme comprises a ZnSe lens AR coated for 3–5 μ m wavelength and a calibrated thermal detector that allows for power monitoring.

The thermal tuning is demonstrated in Fig. 8. The measurement is done in pulsed regime, at 100 kHz with 1 μ s pulse duration. The bandwidth of the spectra corresponds to the bandwidth of the reflector. We assume that the lasing wavelength is tuned over the bandwidth of the DBR by the power dissipated in the gain chip within one current pulse (approximately 30 W (2 A \times 15 V)), due to the change of the gain spectrum and longitudinal mode position during the pulse. In CW operation, we would not expect this wide lasing bandwidth. We achieved 50 nm of continuous tuning starting from 5107 nm, for a heater tuning power between 0 and 1.5 W. Because the DBR is etched in a 10 μ m slab waveguide the tuning efficiency is only 0.033 nm/mW. In our previous work [24], we measured the thermo-optic tuning efficiency of resonant filters to be about 0, 5 nm/K in the 5 μ m wavelength range. 50 nm tuning therefore implies a 100 K temperature increase of the filter. It is expected that the tuning efficiency could be improved by defining the DBR in a single-mode waveguide and using side-corrugated gratings, thereby achieving a wider tuning range. Another way to improve the tuning efficiency is to confine the heat by undercutting the BOX to improve the thermal resistance of the grating [30]. The bandwidth of the measured spectra (5 nm) corresponds to

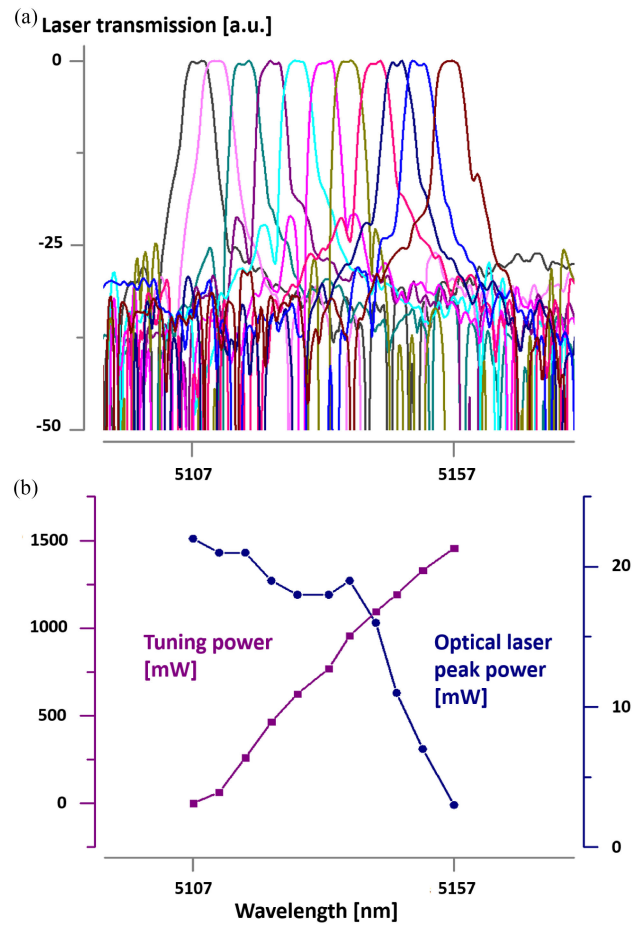


Fig. 8. Thermal tuning over 50 nm of the quantum cascade laser using a Ge-on-SOI feedback circuit (a). The tuning power dissipated in the heaters and the associated peak optical power in the Ge waveguide (b).

the simulated bandwidth of the DBR reflector. The quantum cascade gain chip current density was kept constant at 5.48 kA/cm² in this experiment, which corresponds to 1.92 A. The maximum peak optical power is 22 mW, while there is more than 10 mW of peak power for the first 40 nm of tuning. The side-mode suppression is >20 dB. The strong decrease of the emitted power after 5130 nm wavelength is attributed to the misalignment that occurs during the measurement, as the Ge-on-SOI chip is heated using the micro-heater. Due to the dimensions of the waveguide cross-section and the gain chip mesa (2 μ m and 3 μ m in vertical direction), the measurement is highly sensitive to misalignment and it is difficult to maintain alignment over longer period of time. This issue should be resolved when the QC gain chip is flip-chip integrated on the Ge-on-SOI chip.

Current - Peak power plot is shown in Fig. 9. The lasing threshold is 1.61 A. In this measurement, the laser operated without heater bias, so at 5107 nm. Variations in the threshold as a function of the wavelength could be observed. However, these are mostly attributed to temperature-induced misalignment between the two chips during the measurement. This misalignment causes excess losses in the laser cavity and increases the threshold of the laser. Below the threshold, a QCL is a

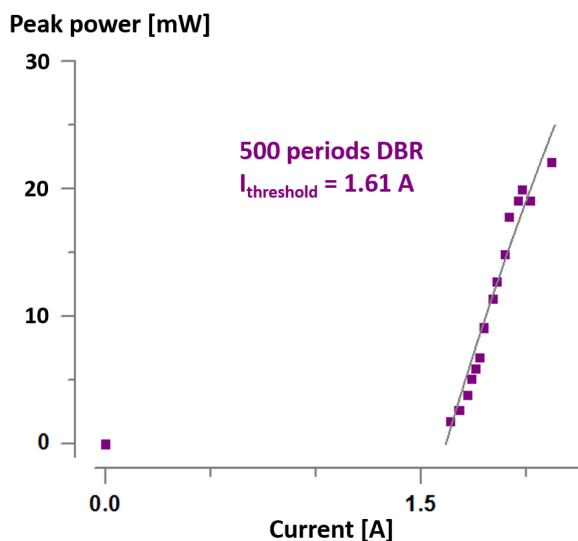


Fig. 9. Current - Power characteristic recorded for the laser with 500 periods DBR.

very inefficient light emitter (much worse than classical diode devices). This, combined with the fact that the thermal detector used had quite high noise floor (~ 0.1 mW), no meaningful measurements could be done below threshold.

VI. CONCLUSION

This paper demonstrates a proof-of-principle EC-QCL based on a QC gain chip butt coupled to a Ge-on-SOI DBR. The laser is thermally tuned over 50 nm. While there is definitely room for improvement in terms of device performance, we believe the combination of QC gain chips and silicon-based waveguide circuits for wavelength selective feedback (as well as implementing other functionalities on the chip) will enable the miniaturization of mid-infrared laser systems. While the current demonstration relies on two separate chips, the flip-chip integration of the quantum cascade gain chip on the silicon photonic integrated circuit is within reach. To improve the tuning range, the DBR filter can also be replaced with e.g. Vernier filters as we recently demonstrated in [24].

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