INVITED PAPER

Open-Access Silicon Photonics: Current Status and Emerging Initiatives

Silicon photonic devices are usually fabricated in large foundries that serve multiple customers. Silicon photonics takes advantage of these open-access silicon electronics foundries. This paper discusses this ecosystem and its evolution.

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ABSTRACT | Silicon photonics is widely acknowledged as a game-changing technology driven by the needs of datacom and telecom. Silicon photonics builds on highly capital-intensive manufacturing infrastructure, and mature open-access silicon photonics platforms are translating the technology from research fabs to industrial manufacturing levels. To meet the current market demands for silicon photonics manufacturing, a variety of open-access platforms is offered by CMOS pilot lines, R&D institutes, and commercial foundries. This paper presents an overview of existing and upcoming commercial and noncommercial open-access silicon photonics technology platforms. We also discuss the diversity in these open-access platforms and their key differentiators.

KEYWORDS | CMOS; foundry; multiproject wafer (MPW); open-access; photonic integrated circuits (PICs); photonic manufacturing; silicon photonics.

I. INTRODUCTION

Silicon photonics is a technology which implements high-density photonic integrated circuits (PICs) with complex functionality using process technology of a complementary metal–oxide–semiconductor (CMOS) electronics fab. Leveraging the existing CMOS infrastructure makes silicon photonics very well positioned to fabricate low cost, high yield, small form-factor, and low-power PICs and, at the same time, scale to large commercial volumes [1]–[3]. The above-mentioned definition of silicon photonics holds for a variety of material systems. To name a few, this includes different types of silicon-on-insulator (SOI), silicon nitride-on-insulator (SiN), germanium-on-insulator, germanium-on-silicon (GOS), germanium-on-SOI, GOS nitride, and silicon-on-silicon nitride-on-silicon. Since all these material systems can use well-established CMOS processing methodologies and infrastructure for densely integrated PICs, they can be considered as different flavors of silicon photonics, but to date the SOI platform has been the most prominent of these material systems both in terms of technological maturity and commercial use.

The last decade has seen the transformation of silicon photonics from a promising research field to a commercial success, mainly driven by the needs for large volumes of high-speed links for datacenters, metro communication, and telecommunication. However, the first conceived applications of silicon photonics were for sensing applications, such as fiber gyroscopes [4]. Nevertheless, variable optical attenuators (VOAs) for passive optical networks (PONs), developed and commercialized by Bookham Technologies in 1997 (with the technology later taken up by Kotura and afterward by Mellanox), were one of the first silicon photonics products to be actually commercialized [4]. Building up to the dot-com boom (and subsequent bust) in the early 2000s, silicon photonics was being considered as a technology that could address the demands of emerging tele/data communication applications. The bursting of the dot-com bubble did little to reduce that expectation but had an obvious negative effect on the investment climate for silicon photonics. It is only

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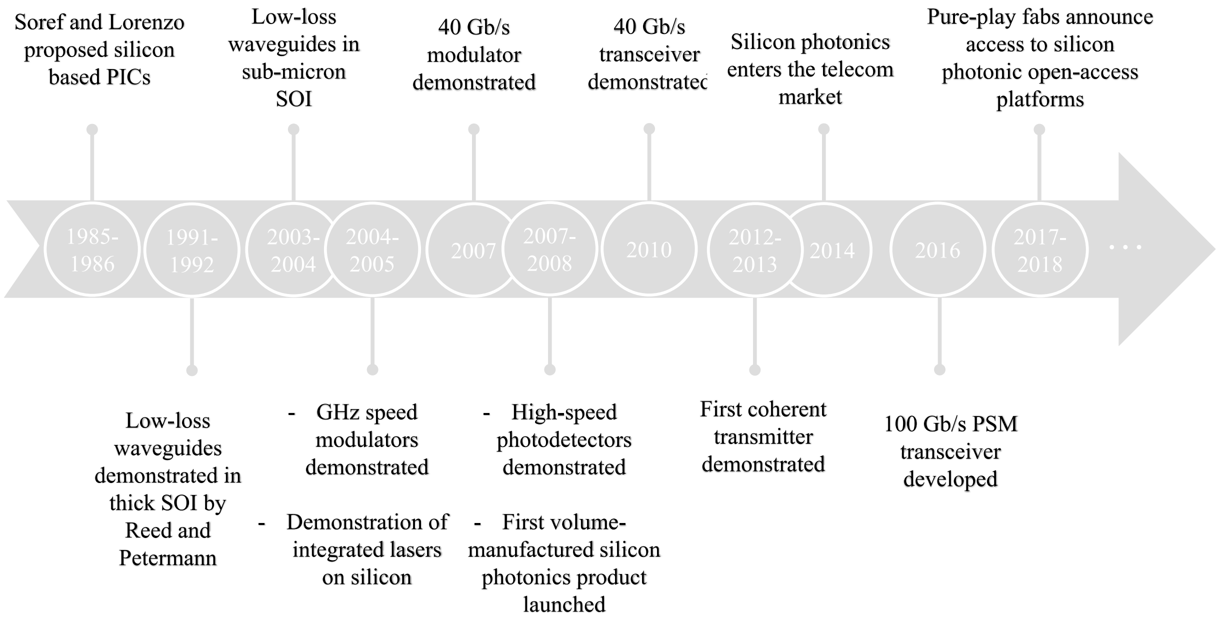

Fig. 1. ***Timeline of some of the major milestones in the field of silicon photonics.***

in 2007 that we see transceivers for datacenter communication, developed by Luxtera, to appear on the market and become a volume-manufactured silicon photonics product [5], [6]. In 2012, Cisco, which is one of the largest networking companies, acquired silicon photonics company Lightwire and started introducing silicon photonics solutions in their products, such as CPAK 100GBASE fiber modules, and in 2014, Acacia Communications brought silicon photonics into the commercial telecommunication market, launching coherent silicon photonics modules for intradata center communication and long-haul dense wavelength division multiplexing (DWDM) links. In 2016, chip manufacturer Intel, which has been building its silicon photonics technology for over a decade [7], [8], launched a 100-Gb/s parallel single-mode fiber 4-lane transceiver for cloud and data center applications. Inphi announced, in 2017, to offer interdatacenter 100G PAM4 DWDM silicon photonics optical engine. Fig. 1 summarizes some of the major technical and commercial milestones achieved in the field of silicon photonics in the last 30+ years. The above-mentioned milestones and in Fig. 1 are just a few examples of the many milestones accomplished by the field of silicon photonics, too numerous to report here completely.

Over the years, there has been a manifold increase in the number of fabless silicon photonics chip and system vendors serving the data center transceiver market. Consequently, in 2017, the silicon photonics transceiver market growth has outpaced the total optical transceiver market by a significant margin [9], [10]. Furthermore, the traction of the technology platforms is stimulating a diversification in the application space: extensive R&D initiatives and startup companies worldwide are betting on silicon photonics for a wide range of applications, such as sensing and biophotonics [11]–[13], light detection and ranging (LiDAR) for automotive industry [14], [15], neuromorphic computing [16]–[18], machine learning [19], [20], quantum information processing [21], [22], and many more.

Fig. 2 shows a simplified representation of the evolution silicon photonics manufacturing, which has gone through in the last several years. The manufacturing process is crucial to the success of silicon photonics, but the capital investment cost for CMOS fabrication infrastructure sets a limit to the number of actors who can fabricate such devices. Similar to the ecosystem of CMOS electronics, we can identify three types of manufacturers; integrated device manufacturers (IDMs) are vertically integrated and have their own infrastructure to manufacture silicon

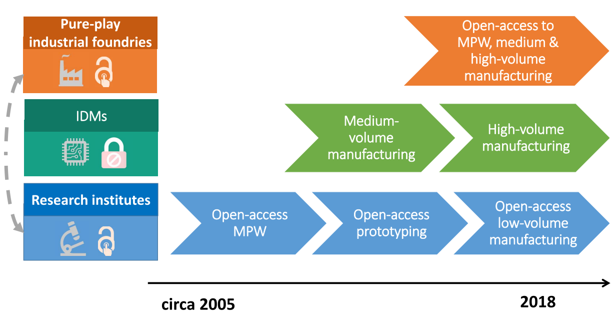

Fig. 2. ***Simplified representation of the evolution of silicon photonics open-access platforms provided by the research institutes and the pure-play fabs for different volumes of manufacturing. The evolution of the proprietary platforms developed by IDMs is also represented. It must be noted that in some cases, the IDMs also provide access to their technology platforms through bilateral contracts with third parties. The gray dashed line represents the collaboration to transfer the manufacturing process from R&D institutes to commercial pure-play fabs.***

photonics chips for their own products. In stark contrast, pure-play foundries have an open-access manufacturing process, where the fabs offer PIC manufacturing services that can be used hands-off by third party external users/clients, such as fabless companies. The notion "open-access" does not mean that the manufacturing services are free of cost to the end users, but rather that the fab imposes little or no restrictions to fabricate PICs for third parties. This is contrary to other areas of commerce, where open access implies that there is no cost to the end users (for example, open-access publications). Anticipating a growing demand for silicon photonics PIC manufacturing, such pure-play foundries [Advanced Micro Foundry (AMF), GlobalFoundries, TowerJazz, and others] have emerged in recent years to offer open-access silicon photonics technologies [23] to cater various manufacturing volumes. The third type of manufacturer is the CMOS pilot line at an advanced (public or private) research institute [24]–[32]. They offer open access to their platforms, which includes multiproject wafer (MPW) fabrication, and this has allowed these institutes to continuously improve their technology offering, to a point where the high technology readiness level (TRL) of their platforms has enabled them to offer low-volume manufacturing of silicon photonic chips through bilateral contracts. In some cases, the R&D institute/pilot line uses the same process flow as a commercial fab to ease the transfer of manufacturing process from R&D institutes to commercial fabs. Consequently, an entire ecosystem of companies providing PIC design support, equipment, and services for packaging, testing, and assembly of PICs is very rapidly materializing, supporting fabless companies engaged in silicon photonics product development [33]–[35].

This paper gives an overview of the current status of the open-access silicon photonics technologies and their access model. We draw parallels with the CMOS electronics ecosystem that has similar models but for much larger manufacturing volumes. The diversity of open-access silicon photonics technologies and its impact on economy-of-scale is discussed. Recent improvements in the design methodologies for PIC design and initiatives toward high-volume manufacturing are also discussed. It is to be understood that silicon photonics is a rapidly evolving technology in a continuously changing economic landscape, implying that the specific details about the current manufacturing platforms will likely be outdated soon. However, the trends, which we discuss in this paper, are likely to hold for the foreseeable future. It is important to mention that the discussion presented in this paper is based solely on publicly accessible information not only peer-reviewed articles but also information about the open-access platforms publicized by their providers.

II. ECONOMY OF (WAFER) SCALE FOR A STANDARDIZED PLATFORM

A standardized silicon photonics platform (also termed "generic integration platform" [36]) is one for which the manufacturing volumes are sufficiently large to establish and maintain a mature process flow. Such a platform has to offer a set of basic passive and active photonic functions, making it suitable for different applications and even for future performance scaling. This is required to offer the standardized technology as an open-access platform in a fabless model, where the end-user has to adhere strictly to the process and design rules defined by the fab. These rules typically prohibit the end-user to change key platform features, such as the material stack, critical dimensions (CDs), number of etch levels, doping concentrations, and so on.

Leveraging existing and well-established CMOS manufacturing technology and infrastructure has catapulted silicon photonics to the forefront of photonic integration technologies. However, the manufacturing volumes needed to meet even today's largest volume applications for PICs are meager (by several orders of magnitude) when compared to the manufacturing volumes of CMOS electronics. A typical CMOS fab processes up to tens of thousands of wafers per month. In contrast, the current total silicon photonics market requires up to few tens of thousands of wafers per year [37]. Considering this disparity, it makes perfect economic sense to capitalize on existing CMOS fabs with established processes, rather than making excessive capital investments for building dedicated fab infrastructure for silicon photonics. Apart from the technological differentiators, this is one fundamental economic reason that distinguishes silicon photonics from competing PIC technologies based on the III–V semiconductor, dielectrics, polymers, and so on.

Fig. 3 shows the approximate chip cost/mm^2 for a standardized silicon photonics technology in a CMOS fab, which is close to being fully loaded with CMOS electronics manufacturing. The cost curve is based on inputs provided by various fabs providing prototyping and/or manufacturing services for silicon photonics PICs. Here, the term prototyping refers to volumes of less than 1000 chips, whereas volumes of less than 100 000 chips are classified

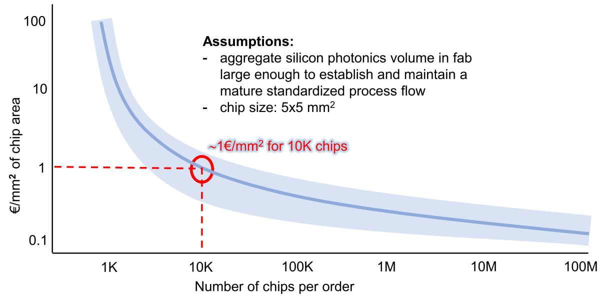

Fig. 3. ***Chip cost per mm^2 for silicon photonics chips in a CMOS fab, shared with nonphotonics use. The cost curve assumes that the silicon photonics volume in the fab is large enough to establish and maintain a mature process flow offering passive and active building blocks. Data are collected from the members of ePIXfab—The European Silicon Photonics Alliance (http://epixfab.eu).***

as medium volume. It is important to highlight that the above-mentioned volume definitions are valid only for PIC manufacturing, as any existing volume manufacturing of PICs lies well within the low-volume bracket of CMOS electronics manufacturing. The cost curve assumes a chip area of 25 mm^2. It accounts for the infrastructure for a complete silicon photonics process flow, including specific capital expenditures to set up the dedicated process for germanium growth needed for the fabrication of photodetectors in a CMOS fab.

The cost/mm^2 of chip area in Fig. 3 is estimated for standardized platforms supporting either monolithic or hybrid integration with electronics. Moreover, the chips considered comprise both active and passive photonic building blocks. The cost curve shows that for 10 000 chips, each mm^2 of chip area costs only 1€ (or 1$, given that these numbers are based on order-of-magnitude calculations). This contradicts directly the gross misunderstanding that silicon photonics is viable only for very large volumes. For up to 1000 chips, the cost is calculated by considering MPW fabrication, which is a cost-effective mechanism for the prototyping of a small number of PICs [38]. The fabrication cost of 10 000 chips is calculated by considering a full lot comprising 25 200-mm wafers (the number of chips on 300-mm wafers is roughly double, so still within the same order of magnitude). It must be noted that the cost of packaging is not considered in Fig. 3. Furthermore, it is assumed that the fabrication has a high yield due to the high maturity of the technology platform.

III. DIFFERENT FORMS OF OPEN-ACCESS SILICON PHOTONICS PLATFORMS

As mentioned in Section I, there is a variety of material systems that fulfils the definition of silicon photonics, which is the ability to use existing CMOS infrastructure for the implementation of complex photonic functions and systems on a chip. In Sections III-A–III-D, a brief description is provided for today's most prominent flavors of silicon photonics. This section only discusses those flavors of silicon photonics that are already or will be available in an open-access mode. In the current landscape, most material systems are developed for optical communication applications in C- and O-bands with wavelengths between 1300 and 1600 nm. Platforms for visible and mid-IR wavelengths are also developed on some of the material systems mentioned in the following, but those developments are still marginal, as compared to the developments made for the telecommunication wavelength range.

A. Silicon-on-Insulator

SOI is the most mature silicon photonics material platform. It relies on silicon (with a high refractive index) as the waveguide core material, surrounded on all sides by a silicon dioxide (glass) cladding. This gives a 41% index contrast, which is defined as $(n_{\text{core}}^2 - n_{\text{clad}}^2)/(2 \times n_{\text{core}}^2)$, in the telecommunication window. SOI can again be subdivided in two classes, namely, submicrometer SOI and thick SOI. The classification of submicrometer SOI and thick SOI is based on the thickness of the silicon guiding layer (i.e., the device layer of photonic components) and not the thickness of the buried thermal oxide (BOX). For thick SOI, the guiding layer is typically larger than 1 μm, whereas for submicrometer SOI, the guiding layer thickness is well below 1 μm. For both classes of SOI used in silicon photonics, the BOX layer is usually thick enough to prevent the leakage of optical signal into the substrate. Another distinction the two have is their current wafer size. Unlike thick SOI, submicrometer SOI is available in wafer size of 200 mm (8 in) or more.

1) Submicrometer SOI: In terms of economic activity, wafer volume, and number of actors in the fabrication field, submicrometer SOI is by far the dominant flavor of silicon photonics and is often considered as a synonym for the entire field. Open-access submicrometer SOI platforms provide the most complete set of passive and active integrated photonic functions, including waveguides, splitters, filters, high-efficiency grating-based fiber-chip couplers enabling wafer level testing, phase-shifters, (high-speed) modulators, and (high-speed) photodetectors. For submicrometer SOI platforms, the waveguide layer is typically only few hundred nanometers thick to ensure single-mode operation of the slab waveguide. The waveguide width is typically between 400 and 1000 nm, and the tight confinement of the optical field in a submicrometer SOI platform allows for waveguide bends of a few micrometers. For example, single-mode strip waveguides in 220-nm SOI allow for a minimum bend radius of $\sim$5 μm. Such a small bend radius enables dense integration of waveguide functions on submicrometer SOI platforms.

Over the years, a variety of platforms have emerged with different thickness of the guiding silicon layer [24]–[28], [30], [31], [39]–[44], all with thicknesses of a few hundred nanometer. Even with this variation, SOI with a 220-nm core thickness has become a kind of de facto standard, and it is being used by a majority of the fabs. Originally, this value of silicon thickness was chosen because of its commercial availability in SOI wafers, and it provided a waveguide layer that supported exactly one guided slab mode for both TE and TM polarization at wavelengths between 1.5 and 1.6 μm. This helped in maintaining single-mode operation in PICs. Moreover, SOI stacks with 310-, 340-, and 500-nm waveguide thickness have been adopted to facilitate laser integration on SOI [45]–[48] and explore mid-IR applications [49]–[52].

The high optical confinement of submicrometer SOI also brings along certain difficulties; the silicon waveguide devices are extremely sensitive to nanometer-scale dimensional variations [53], [54]. The consequences of this sensitivity are higher waveguide loss, backscattering [55], [56], and spectral shift in interferometric [57] and resonant devices [58], [59]. The propagation losses in submicrometer silicon waveguides can be minimized with thicker and wider waveguides. For example, by using 500-nm-thick SOI, waveguides losses of a few decibels per meter are possible to enable applications that require long delay lines, high-Q resonators, narrow filters, and so on [60]. Given that every fabrication process introduces some variability at the nanometer-scale (interwafer, intrawafer, interdie, or intradie, both systematic and random), this variability is a fundamental challenge of the submicrometer SOI platforms [61]. However, smart design strategies have been a topic of active research to make fabrication tolerant submicrometer SOI PICs [62], [63]. Another consequence of the high optical confinement in submicrometer SOI waveguides is the onset of two photon absorption (TPA) at power levels of few tens of mW and higher. TPA not only introduces nonlinear propagation losses in submicrometer SOI waveguides but also leads to free-carrier absorption-induced loss and index change. Beyond wavelengths larger than 2.2 μm, the effect of TPA is drastically reduced [64]. This makes submicrometer SOI structures ideal for implementing nonlinear optical devices at these longer wavelengths [49], [65], [66].

2) Thick SOI: For the so-called thick SOI platforms, the waveguide layer is typically thicker than 1 μm. Silicon photonics started with the demonstration of low-loss waveguides on thick SOI platforms [67]–[69]. Importantly, this platform offered one of the first and the longest lasting silicon photonics product in the form of a VOA for PONs [4].

The single-mode condition for thick SOIs waveguides is only met for rib-waveguides with a specific aspect ratio of waveguide width and height [69]. Slab and strip waveguides in the thick SOI are invariably multimode (at least at telecommunication wavelengths), but it is possible to keep light in their fundamental mode using adiabatic rib-strip conversion structures [70]. The larger mode field leads to increased optical confinement inside the Si core, making thick SOI waveguides less sensitive to dimensional variation, surface roughness, and polarization [71], [72]. It also allows them to handle much higher optical power (even >1 W) before nonlinear effects kick in and to extend the operating wavelength to the mid-IR [75]. Thick SOI waveguides generally have low propagation losses ($\sim$0.1 dB/cm) and weak backscattering, making them especially suitable for high-performance passive functionalities [29], [74]. The most common SOI thickness is 3 μm, which is also available in open-access [73].

Due to their weak lateral index contrast, the bend radius for rib waveguides in thick SOI is in the mm-scale, which does not support dense integration. Therefore, total internal reflection (TIR) mirrors [76] and Euler bends in multimode strip waveguides [77] have mostly replaced rib waveguide bends in thick SOI. With them, the typical bend radius in thick SOI is now ranging from 1 to 50 μm [77], which makes also thick SOI suitable for very dense integration. The Euler bends have very low loss for both polarizations (<0.1 dB/bend even for a few micrometers radius) and have enabled implementation of polarization independent devices with compact footprint for optical communication [78] and microwave photonics applications [79]. Unlike submicrometer SOI, where high-speed modulation and detection functions are monolithically integrated, open-access thick SOI platforms typically rely on flip-chip-like integration to provide these functions [80]. Nevertheless, low-speed modulation of optical signals in the kilohertz and megahertz range is available in open-access thick SOI platforms [29], [81]. High-speed modulators and photodetectors have been reported using thick SOI in [82]–[84], but they are currently not offered by open-access platforms. Input and output coupling for thick SOI waveguides is typically implemented via endfire coupling or upreflecting mirrors.

The main limitations in thick SOI technology relate to the large topography of the wafers. This makes it more difficult to realize high-speed active components, to precisely control the waveguide dimensions, and to use high-resolution lithography for narrow waveguide features. Due to the high topography, thick SOI PICs are typically fabricated in older generations of CMOS electronics fabs or in microelectromechanical systems (MEMS) fabs, rather than the state-of-the-art CMOS fabs.

B. Monolithic Silicon Photonics-Electronics Cointegration

Due to the potential compatibility of silicon photonics with the well-established industrialization methodologies used in CMOS technologies, there has been a significant thrust for monolithic integration of silicon photonics with electronics [85]. The additional parasitic capacitance and inductance of wire-bonds or microbumps used by the hybrid electronic-PIC (EPIC) platforms [86]–[89] are minimized by the front-end-of-line integration of photonic components with electronics [30], [90]. Monolithic EPICs have a potential to meet the stringent power dissipation and aggregate throughput demands for short-to-long-range photonic interconnects [30], [44], [90].

Various demonstrations of monolithic EPICs have been reported [5], [27], [30], [41], [44], [91]–[96]. These implementations are carried out on different types of material platforms, such as bulk CMOS wafers [41], [91], sub-100-nm SOI [30], [44], [93], and 220-nm SOI platforms [27]. Moreover, various technology nodes, such as 90-nm CMOS [94], 65-nm CMOS [92], 45-nm CMOS [93], 28-nm CMOS [97], and 250-nm BiCMOS [96], [98], are used for the implementation of monolithic EPICs.

These solutions can be categorized into two approaches. In one approach, the transistor process development is completely decoupled from the photonic process development. This approach provides the opportunity to optimize the performance of photonic building blocks, as reported in [5], [44], [91], and [94], where bulk CMOS or sub-100-nm SOI platforms are used. As an example, the sub-100-nm SOI platform demonstrated in [44] and [94] provides passive and active functions in the C-band. Similarly, on bulk CMOS platform, in [41], [91], and [97], photonic functions are defined on the polycrystalline silicon layer grown on the locally thicker silicon oxide isolation trenches of the transistor. This platform provides tight bending radius for waveguides, and the optical propagation loss in the O-band is 20 dB/cm when both active and passive devices were defined on the same wafer. An implementation on 220-nm SOI platform, where optical device modules were inserted in the baseline BiCMOS flow, is reported in [27]. In this approach, bulk silicon regions on the SOI substrate are defined for the monolithic integration of high-speed electronics and photonics using 250-nm BiCMOS technology.

The second approach does not deploy any change in the existing CMOS electronics process flow to demonstrate photonics functions. This approach is also known as "zero-change" silicon photonics [30], [93] and typically uses a sub-100-nm SOI platform. As an example, in [30] such a "zero-change" silicon photonics platform is demonstrated on a partially depleted SOI providing active and passive photonics functionality with tight bending radius and low waveguide loss for the C-band after locally removing the silicon substrate under the buried oxide layer, which is not thick enough to prevent optical leakage into the substrate.

C. Silicon Nitride

The lower wavelength limit of SOI transparency is $<$1.1 μm, corresponding to the bandgap of silicon. This implies that SOI is not a viable material system for applications operating at visible and very-near-infrared wavelengths. However, inspired by the success of SOI, there has been a growing interest in recent years to extend the wavelength range of "silicon photonics" to the visible domain using silicon nitride (SiN) as a waveguide material. SiN-based silicon photonics [99]–[102] has a transparency window that goes from $\sim$0.4 μm all the way up to mid-IR wavelengths of 4 μm. SiN technologies can be categorized on the basis of the deposition method used (PECVD and LPCVD) [100], [103], [104], [106]–[110]. The PECVD platforms exhibit higher waveguide losses at the 1.55-μm telecommunication band but do not require processing steps at temperature beyond 450 °C, which is an asset for certain process flows and applications. For applications operating at 1.55-μm, LPCVD-SiN is typically used. Because there is no TPA in SiN, much higher power densities than in submicrometer SOI can be supported, and the lower loss waveguides (with lower phase errors) make it easier to create high-quality filter circuits [111], [112].

SiN provides moderately high index contrast, which is 3.5 to 4.5 times less than that of submicrometer SOI in the telecommunication window. This leads to reduced loss and an order of magnitude weaker backscattering for the SiN-based waveguides [101], [113]. As compared to submicrometer SOI platforms, SiN has $\sim$5 times lower temperature sensitivity [101]. This means that SiN is a better suited platform for applications in which the temperature sensitivity may be an issue, but where active temperature control is not desirable. At the same time, the low temperature sensitivity of SiN leads to a higher power dissipation for tunable devices using the thermo-optic effect. Similar to SOI, we can identify trends toward thin and thick SiN core layers. Typically, thick SiN layers are exploited to develop high-power silicon photonics PICs [114]. This diversity of layer thickness is enabled by the flexible PECVD or LPCVD process used for the deposition of SiN layers. This contrasts with the SOI case, where the SOI wafer provider will only manufacture wafers of a specific layer thickness if there is a sufficient demand for it.

D. Germanium-Based Silicon Photonics

The 220-nm SOI with 2-μm BOX has a transparency of up to 2.9 μm [115], whereas this transparency reaches 3.8 μm for SOI with 400-nm guiding silicon layer thickness [50], [116], [117]. For the former, the transparency is limited by the substrate leakage while for the latter, the transparency is limited due to the onset of absorption in the buried oxide layer of SOI. Approaches such as the implementation of suspended SOI strip and slot waveguides are developed to extend the transparency range further into the mid-IR wavelengths [118]–[121].

GOS provides a moderate-vertical-contrast waveguide system with a transparency window in the mid-IR range of 2–8 μm [117], [122]–[125]. Though Germanium itself is transparent up to $\sim$14 μm, the silicon cladding starts absorbing at $\sim$8 μm and beyond. This makes it a suitable silicon photonics material systems for on-chip spectroscopic systems for gas and liquid sensing, monitoring of air or oil quality, control of engine emissions, free-space communication, and LiDAR systems [117], [122], [126]. Apart from GOS, there has been a variety of other germanium-based mid-infrared technology platforms, such as germanium-on-SOI [127]–[129], GOS nitride [130], $Si_{(1-x)}Ge_x$-on-silicon [131], and suspended germanium [132], [133].

Fig. 4 gives an overview of the various single-mode waveguide cross sections possible with the different flavors of silicon photonics platforms discussed earlier. The submicrometer SOI and SiN platforms support fully etched strip waveguides, deep and shallow etched rib waveguides, and slot waveguides. Specialized geometries for waveguides, such as Box-shell, are also available in the SiN-based silicon photonics [104]. Both submicrometer SOI and SiN material systems support different types of claddings (i.e., air and oxide). Thick SOI supports only rib waveguides with different cladding types, whereas germanium-based mid-infrared platforms typically support air-clad waveguides of strip, rib, and slot types. Fig. 5 shows the transparency range of SOI, SiN, and GOS material

Waveguide Type	Single Mode Waveguide Cross-sections	Sub-micron SOI	Thick SOI	SiN	Ge-based mid-infrared material systems
Strip	Air	✓	⊠	✓	✓
		✓	⊠	✓	⊠
Rib	Air	✓	✓	✓	✓
		✓	✓	✓	⊠
Slot	Air	✓	⊠	✓	✓
Box-shell		⊠	⊠	✓	⊠

Fig. 4. ***Typical cross sections of single-mode waveguides supported by the different variants of silicon photonics platforms. In many cases, the air cladding is replaced by a silica cladding, which creates a less fragile waveguide (less susceptible to dust).***

systems and the corresponding applications linked to optical transparency windows of these material systems.

E. Need for Standardization in Silicon Photonics

Each fab requires developing a standardized technology with an established and mature process flow to provide manufacturing of silicon photonics PICs. If more fabs adopt the same standard, fabless companies will have more supplier options, which reduces the costs and the risks for the silicon PIC design. However, in the current landscape of silicon photonics technologies, there is no single standard technology, rather each fab has defined its own standard technology. This helps them to maintain fewer processes, which results in reduced cost for a foundry.

Due to the high index contrast of the material system, dimensional control is important [31], [54], [57]. For example, the process control in terms of waveguide width and height required for wavelength selective devices in submicrometer SOI devices is more stringent than for CMOS electronics. Standardization in the process flow provides stability and repeatability in the device performance for large manufacturing volumes. Moreover, it helps in gauging variance in key device performance parameters [24], [31]. A well-understood and stable device performance is crucial to develop complex photonic integrated systems on a chip.

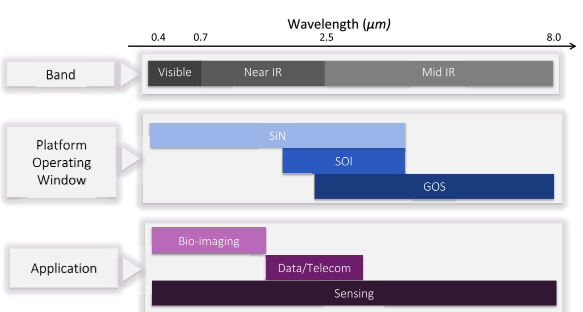

Fig. 5. ***Different forms of silicon photonics operating from visible to mid-IR wavelengths to provide integrated photonics solutions for bioimaging, optical communication, and sensing.***

F. Value of Diversity in Silicon Photonics

A single standardized technology platform is not necessarily capable of addressing the requirements for various applications in the very wide range of market sectors where PIC technology can potentially bring new value [134]. This means that while standardization is a must for the above-mentioned technical and economic reasons, so is the diversification. This is not something that is unique to silicon photonics. Again, we can draw the comparison with electronics, where CMOS is the most dominant technology, but which comes in a variety of nodes with different performance and price points. On top of that, there is a diversity for targeting specialized markets, such as high-power electronics, ultrahigh frequency RF electronics, ionization radiation resistant (rad-hard) electronics, and so on.

The degree of material diversity in silicon photonics enables a situation where technology platforms complement one another. Such a diversity not only prevents monopoly of one technology platform but also develops a sense of competition between technologies and makes them agile for evolution. As an example, Fig. 6 provides a qualitative comparison of submicrometer SOI (left), thick SOI (middle), and SiN-based (right) silicon photonics platforms. One can observe the complementarity of SiN (right Fig. 6) and submicrometer SOI (red lines in left Fig. 6). SOI complements SiN by providing compact form factor PICs through its small bending radius, high-efficiency fiber-chip coupling by using grating/edge couplers, and active functionalities, such as high-speed photodiodes and detectors. On the other hand, SiN provides lower loss waveguides, broad transparency window for visible, NIR and mid-IR applications, ability to deal with hundreds of milliwatts CW power, and reduced backscattering due to its lower index contrast than SOI.

Table 1 lists the type of material stacks used by various open-access silicon photonics technologies and their key technical differentiators. Moreover, it is also possible to combine elements of different platforms together. The manufacturing flexibility of SiN layers makes it possible to integrate SiN layers into the SOI platforms [108], [110], [135]–[138]. In such a platform, passive components demanding low loss and high fabrication tolerance are defined on the SiN layer [139], [140]. Functions, such as modulators and photodiodes, are then defined in the Si layer.

Along with the platform diversity, there is a diversity in infrastructure needed for silicon photonics. Most of the submicrometer SOI platforms use 200- or 300-mm wafers. For NIR applications on submicrometer SOI, the desired feature sizes or CDs can be delivered by 130- or 90-nm CMOS pilot lines and foundries. However, due to the high index contrast of submicrometer SOI, the required accuracy corresponds more to a 40- or 65-nm CMOS technology

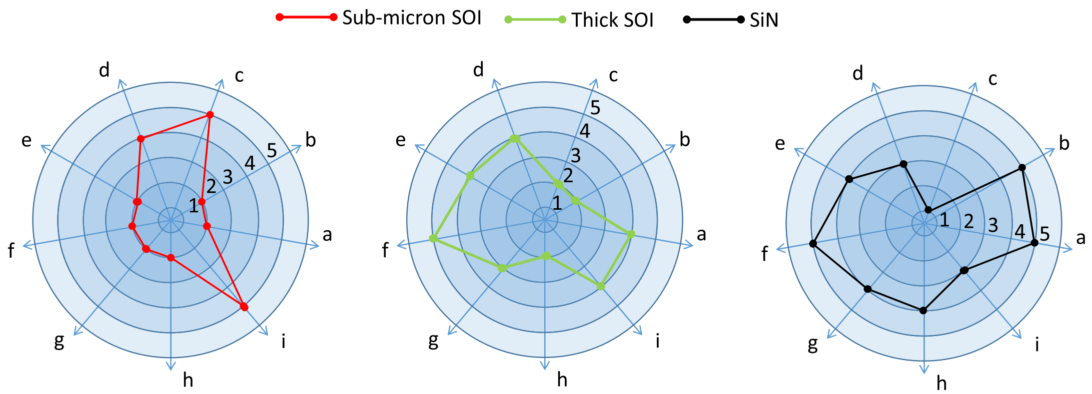

Fig. 6. ***Qualitative representation of the current status of submicrometer SOI (in red), thick SOI (in green), and SiN (in black) on a scale of 1–5 (5 is better). Submicrometer SOI complements SiN in providing compact form factor PICs through its small bending radius, high-efficiency IO by using grating/edge couplers, and active functionalities, such as high-speed photodiodes and detectors. On the other hand, SiN provides low-loss waveguides, a broad transparency window for visible, NIR and midIR applications, the ability to deal with hundreds of milliwatts CW power, and reduced backscattering due to its lower index contrast than SOI. Thick SOI is known to provide lower propagation loss, lower backscattering, and high-power operation but does not provide high-speed active functionalities. (a) Propagation loss. (b) Layer stack flexibility. (c) Active functions. (d) Efficient IO. (e) Backscattering. (f) High-power operation. (g) Transparency. (h) Thermal sensitivity. (i) Bend radius.***

node. These nodes already make use of the high-end 300-mm manufacturing equipment, such as immersion lithography, do not yet require expensive techniques, such as double/triple patterning. Still, the processing cost on 300-mm wafers at these nodes is considerably higher than that of older CMOS nodes on 200-mm wafers. Yet, for mid-infrared PICs the scaling—with wavelength—of photonic structures to larger dimensions relaxes the fabrication tolerances for submicrometer SOI and GOS-based PICs. Due to the relaxed tolerances of moderate index contrast material systems (i.e., SiN, GOS), the platforms on these material systems demand less advanced lithography and etching infrastructure, making them more cost-effective in certain volume manufacturing cases. As a result, wafer sizes of 100, 150, and 200 mm are still prevalent today for these platforms.

In the current landscape of open-access technologies, there is a clear scope for a moderate number of diversified platforms. The sustainability of these platforms depends on whether there is sufficient market for each platform. Therefore, there is a "sweet spot" in terms of standardization and diversity. It is still an open question how this sweet spot will evolve and which silicon photonics platforms will prove to be sustainable.

IV. SILICON PHOTONICS OPEN-ACCESS MODEL

A. Access Models

One of the key mechanisms behind the economic success of silicon electronics is the open-access model, where fabless companies can have chips fabricated in commercial foundries that provide standardized fabrication platforms. This separation of design and product development on one hand and fabrication on the other hand has acted as a multiplier in economic activity with hundreds of thriving fabless companies for every foundry [34], [141], [142]. It is a win–win formula, lowering the investment for fabless companies and generating profitable volumes for the foundries. In the silicon electronics ecosystem, the open-access foundry model can perfectly coexist with vertically integrated IDMs that benefit from a tight integration of product know-how and their own proprietary fabrication processes.

Given the many parallels between silicon photonics and silicon electronics, the open-access foundry model (or fabless model) can stimulate a similar growth in fabless PIC-based product development. Open access is a model that offers fabrication services to third parties, i.e., to external users/clients outside a technology consortium. Open access is facilitated through an ecosystem providing appropriate support services and tools, such as design software, packaging, and testing [34], [143]–[145].

Open access is not the only possible access model to fabrication technology. We already mentioned IDMs with vertically integrated fabrication and product development, but it is also possible for fabless companies to access foundry capabilities on a bilateral or multilateral basis, codeveloping proprietary flavors of a foundry's technology platform. This is a model that has yielded some of the most visible successes in silicon photonics [37], [38], [90], [146]. These are models that we also find in electronics and other custom semiconductor platforms, such as MEMS. Fig. 7 gives a schematic representation of different access models for PIC-based product development.

Given that a fabless/foundry ecosystem should address the largest possible application space, the versatility of silicon photonics open-access technology platforms and the ease of their access are of paramount importance. This

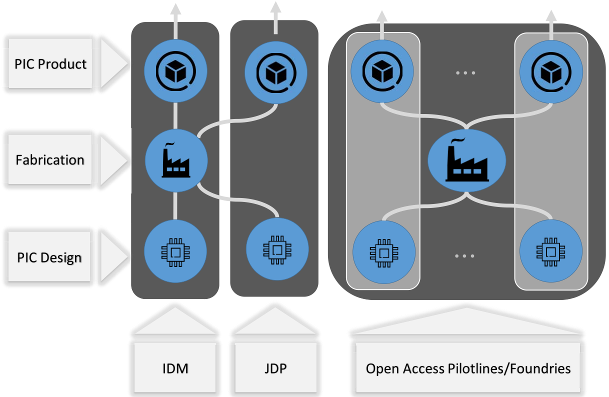

Fig. 7. ***Schematic of three prominent access models for PIC manufacturing. The first column represents vertically integrated IDMs. They internally control the entire process from chip design to production. Fabless companies can have joint development programs with IDMs as represented in the second column. The third column shows different end users submitting their PIC designs to open-access silicon photonics pilot lines/foundries for their product development.***

allows fabless companies to develop innovative products and evolve seamlessly from prototyping to small-volume manufacturing and possibly all the way to high volume manufacturing [141]. Like in electronics, this will also require a certain diversity in the technology offerings, allowing product developers to pick the platform best suited for their application.

B. Open-Access Workflow

In an open-access model, it is important for all parties involved that fabless companies find their way to a suitable foundry as easily and as affordably as possible. For electronics, this was given a boost through the creation of the MPW service MOSIS in 1981 [23], [34], [143]–[145], later mirrored by Europractice IC in Europe [147]. For silicon photonics, ePIXfab—a joint initiative by imec (Belgium) and Commission pour l'Energie Atomique-Laboratoire d'électronique des technologies de l'information (CEA-LETI) (France), operated from Ghent University (Belgium)—pioneered a similar access mechanism for silicon photonics through MPW service since 2006. By 2011, the open-access silicon photonics technologies of IHP and VTT Technical Research Centre of Finland were also offered by ePIXfab.[1]

A similar initiative, named Optoelectronic Systems Integration in Silicon (OpSIS), was launched in 2010 from the University of Washington and the University of Delaware [38]. While the initiative did not sustain beyond 2015, it was vividly successful in providing design support for researchers in silicon photonics and organization of multiple MPW runs through fabs, such as BAE Systems CMOS fab and the Institute of Microelectronics (IME), Singapore [37], [38]. Recently, a new initiative called the American Institute for Manufacturing integrated Photonics (AIM Photonics) has emerged. It is currently engaged in establishing an ecosystem supporting the complete silicon photonics product development (from design to prototype to pilot or mid-scale wafer and package manufacturing) using the 300-mm fab at The State University of New York Polytechnic Institute and packaging facilities in Rochester, NY, USA [148], [149].

Various other initiatives, which provide open-access silicon photonics technologies to end users have also emerged. For example, the Photonics Electronics Technology Research Association (PETRA), Japan, and the Electronics & Telecommunications Research Institute (ETRI), South Korea, provide access to the end users in these respective countries. Similarly, other countries have developed open-access technologies to address the demands of local and/or global end users.

When an end-user wants to access PIC fabrication technology, the first challenge is to determine whether the silicon photonics technology will meet the system specification and which technology flavors from a diverse pool of foundries are most suitable. In many cases, an end-user product developer does not have the internal technical know-how to make this platform selection, let alone kick-start the design of a full-custom complex PIC. As with custom electronics, this creates a space for photonic design houses and brokers that can support the end-user in his choice of technology.

After the selection of technology, the open-access process makes it possible to get started on a practical design without the need for complex bilateral discussions. Open-access foundries provide access to process design kits (PDKs) after signing a standard design kit license agreement with the fab. In a case, where the PIC design is outsourced to a design house, a similar nondisclosure agreement is usually signed with the design house.

The PDK provided by the foundry is the interface between the designer and the technology [150], [151]. It contains sufficient technical details of the technology to enable the designer to create either full-custom layouts or custom circuits. A PDK is typically compatible with specific design tools and is always foundry-specific. Unlike with electronics, where there is some standardization of the content of PDKs, there is, yet, no standardized blueprint for photonics PDKs. In its simplest form, it contains layer description associated with a process step and critical dimensions that define the design rules for the process steps. More advanced versions of PDKs also contain the followings:

1) component libraries with their parametric cells and their layouts [either actual layouts or intellectual property (IP)-protected black-boxes];

[1]Since 2015, the MPW services offered by ePIXfab have been transferred to Europractice IC Service. ePIXfab has transformed itself into the European Silicon Photonics Alliance, with the majority of the European open-access silicon photonics fabs as its members, and continues to promote silicon photonics science, technology, and application through fabless models (http://epixfab.eu).

2) technology handbooks describing different technology steps and process variability statistics, a design rule manual, and a component library handbook providing statistics about their performance;
3) design rules enabling the designer to match the critical dimensions and density of the design with the capabilities of the fab concerning mask preparation, lithography, and chemical–mechanical polishing. These design rules are often embedded in a deck for the design rule checking (DRC) software.

Recently fabs and design tool developers have started codeveloping calibrated compact model libraries (CMLs) for the PDKs of their respective open-access technologies. The CML is meant to improve the accuracy and reliability of PIC designs by enabling the designers to accurately simulate and optimize the performance of complex PIC designs before fabrication [152], [153]. In the future, such CMLs will be an integral part of PDKs. Furthermore, the fabs have also been striving to include the 3-D capable layout-versus-schematic (LVS) checking and the capability to run cosimulation with electronics ICs [61].

C. Open-Access Modalities

Generic open-access technologies are available in different modalities, depending on the phase of the product development:

1) multiproject wafer (MPW);
2) dedicated engineering runs;
3) preproduction, low- and high-volume manufacturing.

For the proof-of-concept and early stage R&D, MPW shuttle runs are ideally suited. MPWs play an instrumental role in catalyzing the field of silicon photonics by providing low-cost access to start-ups, small/medium enterprises, and low-capital companies to test their design ideas using a standard process flow of different fabs offering open-access technologies [33], [34], [142]. MPW helps the designers to gauge the capabilities available in a technology. In MPWs, several users share the design area and share the mask and fabrication cost. Typical design sizes for each user consume few tens of square millimeters with a typical cost of a few kilo-euros for passive PICs to a few tens of kilo-euros for PICs with advanced functionalities of modulation and photodetection [147]. In this stage, the end-user typically receives few dozens of chips. The designer has the freedom to make the design using custom components from his own component library and a component library of the fab PDK. The IP of the user is preserved by ensuring that the designs of the user are not visible to any other user sharing the same design reticle.

In many cases, the fab provides access to MPW prototyping services through a technology broker. Due to the very low-volume nature of the MPW service, fabs collaborate with technology brokers who aggregate the designs of the end users. Moreover, they support the end users by providing access to PDK for the fab, relevant design tools, and undertake layout verification by DRC. A technology broker can provide support for multiple technology platforms from different foundries. Table 1 lists some of the most prominent open-access silicon photonics platforms offered by various CMOS pilot lines, research institutes, and industrial fabs.

On average, each foundry offering MPW shuttles provides three to six runs in a year. In most cases, the MPW access is provided by research fabs. These fabs typically have a long fabrication cycle due to the limited capacity of their infrastructure. Typically, the turn-around time for a design with full process flow (e.g., passives and actives) takes 9–12 months. If the design has only passive devices, then this time is typically 4–6 months. These long production cycles prohibit the rapid-learning desirable during the early research, development, and prototyping phase of the product development. To circumvent this very issue, rapid prototyping services for silicon photonics have emerged. In some cases, these prototyping services are compatible in terms of processes, specifications, design flow, and design rules with the technology offered by an MPW fab. The typical turn-around time for a rapid prototyping service is few weeks, whereby an end-user gets 1–10 chips by paying a cost comparable to an MPW run through a fab. Most rapid prototyping platforms provide passive functions only, but in a few cases, they offer the complete process flow comprising both active and passive functions. Table 1 lists the few prominent platforms available in rapid-prototyping mode.

Typically 50%–70% of end-user designs in an MPW are based on user-defined custom building blocks [150]. Before moving to early prototype dedicated production runs, typically, an end user requires multiple tape-out iterations to optimize custom-designed building blocks and reach the performance specifications. This cycle of design optimization is not only time consuming but also has a significant economic cost. An alternative is to go for a dedicated engineering run directly. In such tape-outs, the same process flow as for MPW shuttles is used, but a user can get more wafers and more design space. While expensive, they provide the end users with an opportunity to put large custom building block design sweeps to optimize the overall PIC design with potentially fewer iterations.

Silicon photonics technology accessible via MPW has a fixed process flow with typically a high level of maturity (TRL level 6 and beyond). The platform is generic in the sense that slight variants of the same process flow may be used for diverse applications. Despite the generic nature of open-access technology, in many cases, this process flow is incapable of delivering the desired performance specifications. In addition, when moving from R&D to commercialization, a generic platform might still fall short of the functional performance specifications of a PIC through design optimization only. Both cases demand a customized process flow, which may involve new process development through dedicated engineering runs. Various iterations are carried out to achieve maturity for the cus-

Table 1 Prominent Open-Access Silicon Photonics Technology Platforms Offered by Various Fabs, Their Technology, and Access Mechanism

Foundry	Platform	Technology	Access	Waveguide Layer Thickness (nm)	Wafer Size (inch)
			RAPID PROTOTYPING SERVICES		
AMO	thin SOI SiN	e-beam	Direct	220, 340	6
Applied Nano Tool	thin SOI	e-beam	Direct	220, 300	6
CNM/VLC	SiN	e-beam	Direct	300	4
Cornerstone	thin SOI	248 nm	Direct	220, 340, 500	8
LIGENTEC	SiN	-	Direct	up to 2500	4/6
			CMOS PILOT LINES & RESEARCH INSTITUTES		
AIM (SUNY)	thin SOI	-	MOSIS	-	12
	SiN	-		-	12
CEA-LETI	thin SOI Ge/SiGe	193 nm	CMP	310 up to 3000	8 8
IHP	SiGe BiCMOS	248 nm	Europractice	220	8
IMEC	thin SOI SiN	193 nm	Europractice Direct	220	8 8
IMECAS	thin SOI	-	SPP	220	8
INPHOTEC	thin SOI	e-beam	Direct	220	6/8
Sandia Lab	thin SOI	-	Direct	240	
VTT	thick SOI	UV	Direct	3000	6
			INDUSTRIAL FABS		
AMF(former IME)	thin SOI SiN SiN-on-SOI	248/193 nm	Direct†	220, 340 - -	8 8 8
CompoundTek	thin SOI	193 nm immersion	Direct	-	-
Global Foundry/IBM	thin SOI	193 nm immersion / 248 nm	MOSIS, Direct, TAPO	sub-100 nm	8/12
SilTerra	thin SOI	-	Direct	-	8
SMIC	Thin SOI	-	Direct	340	8
ST Micro§	thin SOI	193 nm	Direct	310	12
TowerJazz	thin SOI	193 nm	Direct	-	8
TSMC	thin SOI	-	-	-	12
LioniX	SiN	UV	Direct	flexible	-

†CMC Microsystems (Canada) brokers MPW services to Canadian universities and industries.
§ST Micro platforms is accessible via bilateral contracts

tomized processes, which makes the turn-around time of such dedicated engineering runs longer than is the case with MPW. The end users are provided with a customized PDK with agreement on the design rules and design layers making these runs more flexible. Typically, a customized dedicated engineering run costs 10× more than an MPW participation.

Once the PIC design has reached a certain maturity, the silicon photonics product development requires preproduction engineering runs. During these runs, the process repeatability is established to ensure a predictable process flow. During this phase, corner lots are run as a critical validation step to determine the worst case estimate of the system functional performance specification. Such lots are important for defining the ideal process conditions for low- or high-volume manufacturing. Manufacturing volumes of a few hundreds to a few thousands of wafers per year are considered to be low volume for PIC manufacturing. As today most open-access technologies are offered by R&D fabs, this is the only volume bracket that can be addressed, as these R&D fabs generally do not have a capacity for medium- or high-volume production. However, R&D fabs may have agreements where the end users can translate the process developed in an R&D lab to commercial fabs providing medium- and high-volume manufacturing. This process transfer requires matched geometries (i.e., minimum feature size), a similar performance of building blocks, including the performance variability, matched PDK and associated device models, and migration of other parts of the supply chain (e.g., assembly). ST Microelectronics, though an IDM, is one of the first foundries to provide access to its technology platform for volume manufacturing through bilateral contracts [146]. Other foundries with the capacity for high-volume manufacturing, such as GlobalFoundries and TowerJazz, have also announced to launch open-access silicon photonics platforms. Moreover, in 2017, TSMC developed a through-silicon-via-enabled silicon photonics platform in a 300-mm foundry. This platform has demonstrated the state-of-the-art performance for various passive and active building blocks [90].

Table 1 provides a nonexhaustive list of institutes and foundries providing (or in the process of providing) open-access silicon photonics technologies. In the early days, the fabs chose 220-nm SOI as the substrate for their platform development [24], [25], [27], [31], [41]. More recently, silicon photonics open-access platforms based on 310-nm SOI [26], [40], 500-nm SOI [154], and SiN-and germanium-based mid-infrared platforms have also emerged. The technology, access mechanism, and wafer size used are also listed in Table 1. Table 1 will likely evolve considerably in the next years.

D. Recent Open-Access Silicon Photonics Technology and Ecosystem Developments

1) Process Technology: Advances in process technologies for silicon photonics platforms have resulted in their improved performance. These improvements resulted in demonstrating passive devices with lower loss, superior spectral accuracy, and higher reproducibility. Performance of active devices has also benefited from the evolved processing technology, whereby different types of efficient modulators and photodetectors operating at high-speed are demonstrated [24]–[28], [31], [32], [155]–[160]. As a result of advances in the process technology, open-access fabs have consolidated their platforms by offering new process modules, such as very low-loss waveguides [155], [156], high-speed modulators [161]–[166], integration of efficient electrooptic materials in a silicon photonics process flow [173], [174], multilayer SiN on Si [108], [110], [135]–[138], and broadband fiber-chip-fiber couplers [167]–[172], [175].

Most applications of PICs require that a light source supplies the chip with either a clean optical carrier (laser) or broadband light. A variety of approaches are pursued to bring III–V and SOI-based silicon photonics together [176]–[178]. Demonstrations are reported to reach the ultimate solution of a monolithically integrated quantum-well or quantum-dot III–V laser source in silicon photonics [179]–[185]. Currently, the most mature solutions are provided by hybrid or heterogeneously integration of quantum well or quantum dot laser source with silicon photonics PICs [183], [186]–[188]. Open-access platforms are actively engaged in developing the wafer-scale integration of light-sources on silicon PICs. Wafer-scale integration is required to preserve the cost advantage of silicon photonics. A recent demonstration of wafer-scale heterogeneous integration of light-sources is reported in [189]. An incumbent technology that can provide wafer-scale integrated laser sources is microtransfer-printing (μTP) [190]. Other open-access technology consortia, such as AIM Photonics, are also exploring the development of integrated laser solutions, including quantum dot-based wafer-scale epitaxially grown laser sources within their silicon photonics technology platform [148], [149].

To gauge the process stability and capability of the PIC platforms offered by the open-access fabs, methodologies and infrastructure for platform performance tracking are developed by monitoring the key dimensions for each processing step [24], [191]–[193]. Furthermore, infrastructure for wafer-scale end-of-line optical, electrooptic, and electrical testing using automatic setups is set up to determine device performance [31], [90], [194].

2) Design Tools: Open-access technologies only make sense in combination with a design infrastructure that enables platform users to design their own devices and structures. We can identify two essential parts of the design infrastructure: design/simulation tools and PDKs. A number of design tools for PICs have emerged in the past two decades [151]. At first, they supported the designer in generating complex layout features for photonic components, which are often much more complicated than those for electronics. Photonics requires curvilinear waveguides and custom all-angle geometries, while typical electronic layouts are based on simple rectangular features. The resulting geometries can be simulated using electromagnetic solvers, which can be quite computationally heavy.

Today, photonic design is gradually migrating to the circuit level [151]; instead of defining and simulating every individual geometry, a photonic circuit is constructed of building blocks and connected with waveguides. Each building block has an efficient compact model that is used to calculate the response of the entire circuit. This is similar to electronic circuit design, where the compact models are defined in SPICE or VerilogA. Photonic models can also be defined in VerilogA [195] or in a model for a specialized photonic circuit simulator. Such circuit-level design, which starts with a schematic and circuit simulation and only then implements the circuit as an actual layout, can scale up to designs of much larger complexity. In addition, circuit-level design allows the user to focus on the added value of his application, rather than redesigning low-level functional building blocks.

Circuit design requires a library of components that can be connected together into a circuit. For each technology platform, fabs supply a PDK that contains a standard component library for essential functions, such as waveguiding, splitting, crossing, modulation, detection, and fiber coupling. Until recently, these component libraries consisted of simple layouts that a designer could reuse at the circuit level, but the PDK libraries are now gradually populated with compact models for the building blocks, enabling designers to verify the circuit function in simulation.

Most photonic design tools are available as commercial software. Unfortunately, at this point, there is only limited interoperability between the tools of different vendors, even though some collaboration and standardization activities are emerging [196]. This also extends to the integration of photonic design tools and electronics design automation (EDA) tools, as we see EDA vendors gradually supporting photonic design [197], [198].

Because high-contrast silicon photonics components are so geometry sensitive, it is important that the effects of the fabrication process are taken into account at the design stage. Design-for-manufacturability techniques that originated in electronics are now being adapted and extended for photonics. This includes litho-friendly design [199], tolerant circuit design [63], use of optical proximity corrections [200], and tiling to control pattern densities [201].

To obtain a first-time-right design, an effective verification strategy is needed. This consists of two steps: DRC ensures that the laid-out design can actually be fabricated, while LVS tests extract the functional circuit from a layout and compare it to the original design intent, including simulation of the extracted circuit. Robust layout verification flows have also been under development to ensure that both the mask fabrication and silicon processing will not be affected by the inclusion of designs that are not qualified [61].

The landscape of design tools and PDKs is rapidly evolving with new capabilities for designers being released every few months. This is needed because a low-threshold design experience is a direct enabler to open-access technology.

3) Packaging: The packaging of silicon photonics chips is of critical importance both at the prototyping and the manufacturing level. Efforts have been made in standardizing the packaging processes to reduce the cost of packaging and to improve the reliability issues associated with optical and electrical interfaces to silicon photonics chips. Passive and automated packaging schemes are developed to cut the cost associated with photonics packaging [202]. Similar to PIC layout design rules, there have been efforts to develop packaging design kits and packaging design rules for cost-effective packaging of silicon photonics chips, their thermal management, integration with electronics, and assembly of off-chip light sources. Recently, the open-access PIC Assembly and Packaging Pilot Line PixAPP has been established in Europe to provide end users easy access to the packaging of PICs. Similar initiatives are emerging in other continents. For example, the open-access platform of AIM Photonics [148] and the one from Sandia National Laboratories are combined with chip scale assembly and packaging service.

4) Emerging Silicon PIC Prototyping & Manufacturing Initiatives: The success and impact ePIXfab created by pioneering open-access silicon photonics technologies acted as a blueprint for various other players. A growing number of initiatives, including opSIS and A*STAR IMEC, have taken up the same model and compounded to its success, building a much broader and active community engaged in PIC-based research and development. Though OpSIS has ceased and ePIXfab handed over its brokering role to Europractice and CMP, the ePIXfab members (IMEC, CEA-LETI, IHP, and VTT), and A*STAR IME continue to consolidate their respective technologies by the inclusion of new process modules and enhancing their TRLs.

Recent years have seen numerous new initiatives by CMOS pilot lines and public/private research institutes to provide open-access silicon photonics technologies. For example, in Europe, the pilot lines PIX4Life providing PIC prototyping/manufacturing for life-science applications and MIRPHAB for mid-IR applications have surfaced. A*STAR IME, which is a pioneering Asian institute providing open-access silicon photonics, has started a spin-off AMF in 2017 to provide manufacturing of silicon PICs using the processes and technology developed by A*STAR IME. In Japan, the PETRA initiative, in South Korea, the Electronics and Telecommunications Research Institute, and in China, IMECAS have started providing silicon PIC platforms to their domestic end users. In North America, Sandia Research Laboratories and AIM Photonics have made progress to develop and offer silicon photonics platforms. Anticipating a demand for high-volume PIC-manufacturing, CMOS pilot lines and research institutes have developed routes for high-volume manufacturing through commercial fabs. Moreover, commercial fabs have developed silicon photonics PIC platforms and started offering them to third-party end users.

V. CONCLUSION

Open access of silicon photonics technologies, initially offered by CMOS research institutes, has played an instrumental role in making it a mainstream photonic integration technology. Thanks to the continuous consolidation of the technology platforms offered by CMOS pilot lines and research institutes, low-volume manufacturing of silicon photonics PICs is already happening. The number of fabless companies envisaging silicon photonics products and requiring the manufacturing of their products is rapidly increasing. With this clear trend in market growth and looming demand for high-volume manufacturing by fabless companies, pure-play foundries have started offering open-access silicon photonics technologies for prototyping as well as manufacturing at low- and high-volume level.

The potential penetration of silicon photonics into market sectors beyond optical communication further augments the growth of silicon photonics. The flavor of silicon photonics geared toward visible wavelengths and mid-infrared wavelengths, respectively, has emerged to address life-science and sensing applications. There are cases where the different flavors of silicon photonics compete with each other, making the technology more agile for evolution, and there are cases where these flavors complement each other to strengthen silicon photonics against competing technologies. Since silicon photonics is also viable at moderate volumes, many of the existing silicon photonics flavors may grow industrially even if they target specialized applications.

The developments made by the open-access technology platforms have galvanized the silicon photonics ecosystem. A mature and complete supply chain from design to packaging and testing is imminent. ■

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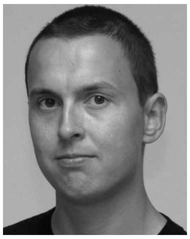

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