Expanded-Beam Through-Substrate Coupling Interface for Alignment Tolerant Packaging of Silicon Photonics

N. Mangal[1, 2, *], J. Missinne[2], G. Roelkens[3], J. Van Campenhout[1], G. Van Steenberge[2], B. Snyder[1]

[1]*imec, Kapeldreef 75, Heverlee B-3001, Belgium*

[2]*Centre for Microsystems Technology, imec and Ghent University, Technologiepark-Zwijnaarde 15, Ghent B-9052, Belgium*

[3]*Photonics Research Group, Ghent University-imec, Ghent 9000, Belgium*

**Author e-mail address: nivesh.mangal@imec.be*

Abstract: We demonstrate an alignment tolerant through-substrate coupling interface by combining an optimized downward-directionality grating on a silicon photonic chip with a hybrid integrated polymer lens, generating a collimated beam at λ=1310nm for more than 600µm.

OCIS codes: (250.5300) Photonic integrated circuits; (050.1950) Diffraction gratings; (200.4650) Optical interconnects; (220.3620) Lens system design

1. Introduction

The increase in growth of internet data traffic has resulted in an increase in the performance requirements of data centers. The role of silicon photonics for short-reach interconnects is promising owing to its advantages in scaling, bandwidth, density and power efficiency [1]. In order to overcome cost-limiting factors that create challenges for its adoption, solutions in the domain of photonic packaging and 3D integration with CMOS are needed [2].

Efficient VCSEL-based optical coupling interfaces have been designed in the past using microlenses to enable laser-to-fiber coupling [3,4]. An alignment tolerant interface is a key enabler to drive down the costs of photonic packaging, as the usage of active alignment adds significant cost and assembly time overhead in the scheme of overall integration. Keeping that in perspective, we have demonstrated hybrid integration of polymer microlenses onto the substrate of a silicon photonic chip to achieve collimation of output beams (Fig. 1a). A collimated beam coupled out of a photonic chip has the potential to not only enable alignment-tolerant coupling to on-package and on-board waveguides, but can also be applied in the domain of sensing and imaging.

2. Design

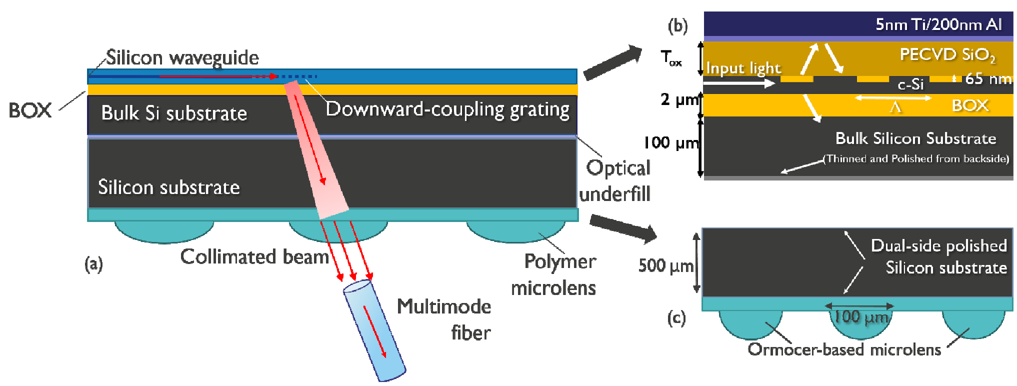


Fig. 1 A cross-section schematic of (a) Hybrid integration of polymer microlenses with the downward-directionality grating couplers through the substrate of a photonic chip, (b) SOI grating coupler (Λ=490nm, fill-factor=0.5) with a metal reflector on top of a 2 µm thick top oxide and (c) Ormocer-based microlenses fabricated on one side of the dual-side polished silicon substrate.

The hybrid-integrated photonic chip and microlens assembly comprises a 100 µm thinned and backside-polished silicon photonic chip and a separate polymer microlens array on a polished silicon substrate. The photonic chip has grating couplers fabricated on the top side that couple light from a waveguide to a beam oriented slightly off-normal in the downward direction through the SOI wafer substrate (Fig. 1a). Previously, upward-coupling diffraction grating couplers have enabled wafer-scale testing of SOI photonic circuits [5]. By depositing a Ti/Al metal reflector on the oxide cladding above such gratings, a coupler with a mixed directionality can be modified to realize a dominant downward directionality by exploiting constructive interference (Fig. 1b). The optimum oxide thickness between the grating and the metal reflector to achieve this constructive interference is given by $t_{ox} = m.(\lambda/2).\cos\theta/n_{ox}$, where m is an integer. Based on this calculation, the optimum thickness of 2 µm for a wavelength of 1310 nm was verified using Synopsys RSoft 2D finite-difference time-domain (FDTD) simulations (Fig. 2a).

Microlenses were designed to be fabricated on a separate dual-side polished silicon substrate (Fig. 1c). The thickness of this substrate was chosen to be 500 µm in order to sufficiently expand the beam, which increases the distance over which the final beam is collimated. In order to collimate the diverging beam from the downward-coupling grating, a spherical microlens was designed using a ray-trace model in Zemax. The far-field divergence of the output of the grating coupler, as determined from the 2D-FDTD simulations, was incorporated in the ray source of the model. The 4.06° chief ray angle of the beam in silicon was also derived from the FDTD far field. The ray-trace calculations for this wavelength indicated that the optimal value of radius of curvature is 145 µm and lens diameter is 100 µm. Fig. 2b and 2c illustrate collimation of the beam over a distance of more than 600 µm. Thus, the

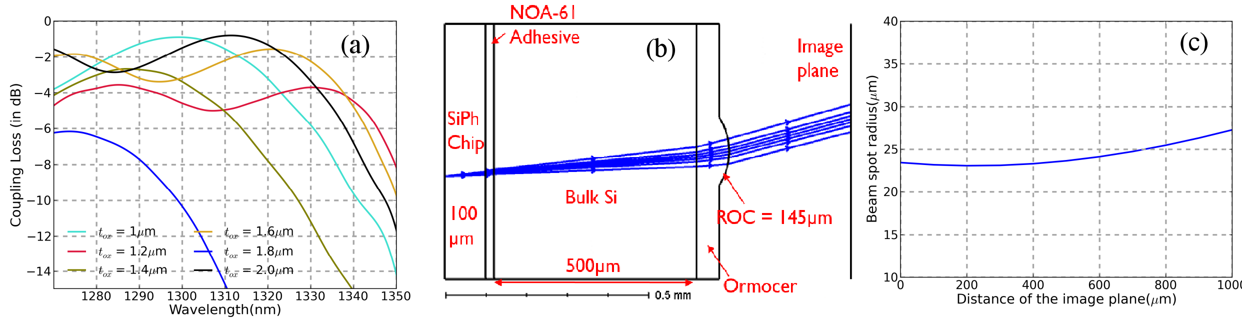


Fig. 2(a) The coupling efficiency of a grating coupler with a metal reflector is maximum for an oxide thickness of 2 µm, (b) Ray-trace model of the chip-lens integrated system and (c) Evolution of the spot radius of a Gaussian beam as it propagates from the apex of the lens (z=0).

simulations indicate that the outcoupled beam from the integrated assembly is highly tolerant to misalignment in the optical axis at the coupling interface for on-package or on-board optics.

3. Fabrication & Assembly

The photonic dies used in this packaging experiment were fabricated in imec's 200 mm wafer-scale silicon photonics pilot line [6]. A sample chip was subsequently processed further at die-level to apply metal reflectors above the output grating couplers. The die was then thinned to a total thickness of 100 µm and a 170 nm Si_3N_4 antireflection coating was applied to the bottom surface. A 40° angled polished fiber fixed in a Si V-groove was actively aligned to an input grating coupler from the top side of the die, which was itself mounted on a die-support frame, and the fiber and the photonic die were subsequently packaged with a UV-cure photopolymer (NOA-61) [7]. For the fabrication of microlenses, UV-based imprinting of Ormocer material was used to form microlenses on a silicon substrate [8]. The master stamp was made on glass using the conventional photoresist reflow technique after which a negative was made using a foil, which was later utilized for imprinting the lenses on the final silicon substrate [9]. These microlenses were then actively aligned with the output grating coupler through the photonic chip substrate with the aid of an IR camera. The bonding between the thinned photonic chip and microlens substrate was also performed using NOA-61 (Fig. 3).

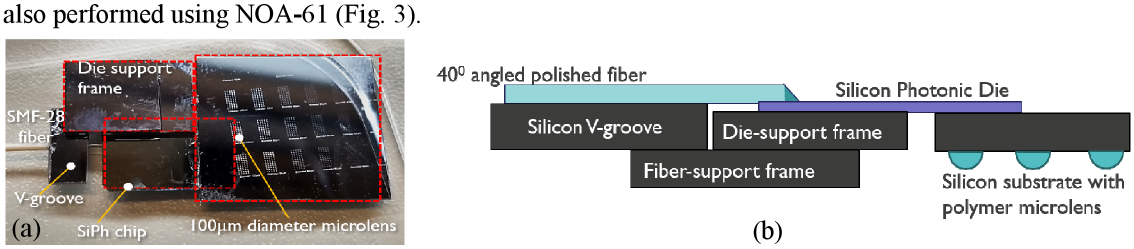
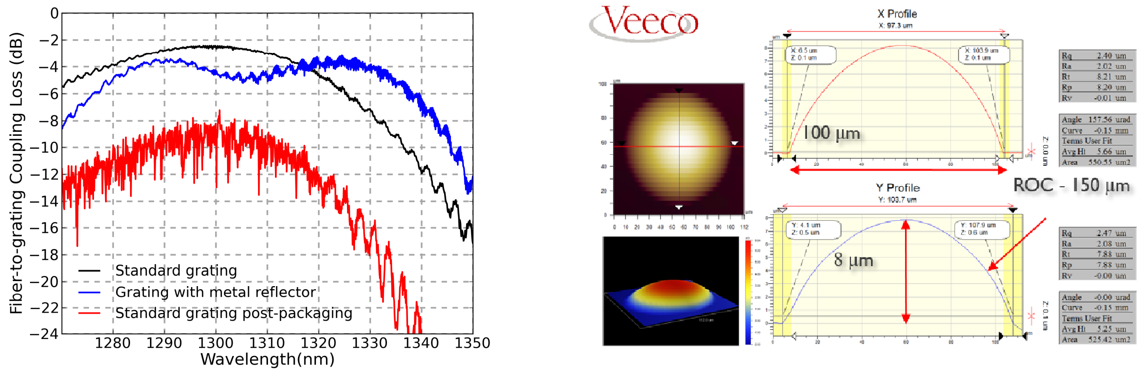


Fig. 3(a) Image of the actual demonstrator as viewed from the side of microlens and (b) Cross-section of the assembled demonstrator.

4. Measurements & Results

The coupling efficiency spectrum to SMF-28 fiber of the standard top-coupled shallow-etched grating coupler without a reflector is compared before and after packaging to that of the same grating with a metal reflector and measured from the bottom of the chip instead (Fig.4a). The high loss due to packaging using angled polished fiber is attributed to improper roll-alignment during packaging.

The surface profile of a 100 µm diameter fabricated microlens was measured using a Dektak profilometer. The measured radius of curvature of 150 µm was close to what was required from the optical model (Fig. 4b).



(a) (b)

Fig. 4(a) The fiber-to-grating coupling loss comparison of a standard grating coupler before and after packaging and (b) The microlens height = 8 µm, diameter = 100 µm and radius of curvature = 150 µm obtained through 3D surface profile measurement using Dektak profiler.

The optical output from the integrated assembly was coupled into a 0.2 NA multi-mode fiber. The fiber was retracted from the apex of the lens a fixed distance along the optical axis and then a lateral scan of the fiber was performed. This was repeated for several points at fixed steps. The 1/e^2 width of the aligned power profile was then compared with the longitudinal distance to determine the degree of collimation of the beam. The minimal variation between the scans performed at successive distances from the lens indicate that the beam achieves near collimation over the measured range (Fig. 5a and 5b).

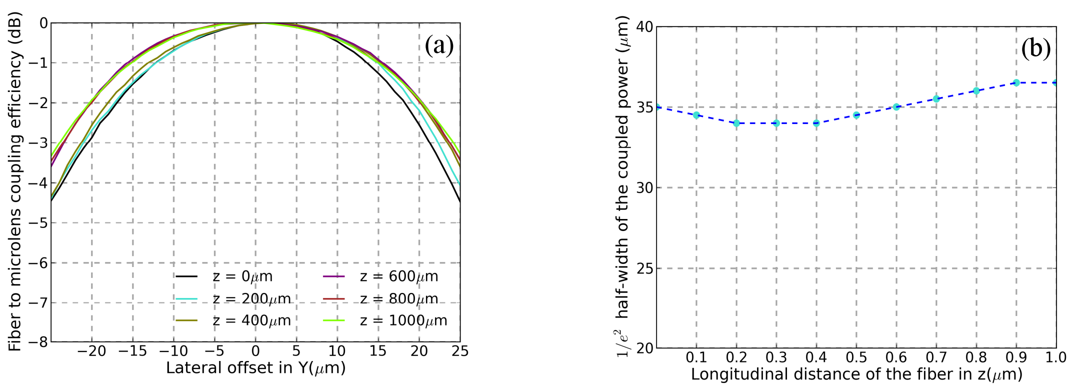


Fig. 5(a) Normalized fiber-to-microlens coupling efficiency vs. lateral offset of a 0.2NA multimode fiber and (b) 1/e^2 -width of the coupled power into the fiber,as it is retracted away from the microlens.

5. Conclusion

We have demonstrated hybrid integration of 100 µm diameter microlenses onto the substrate of a silicon photonic chip to obtain an alignment tolerant coupling interface that is collimated over a distance of more than 600 µm. This measured distance correlates well with the value obtained using ray-tracing simulations. The described approach can also be extended with reactive-ion etching to fabricate microlenses directly at wafer-scale on the substrate of silicon photonic chips in the future. This work was supported in part by imec's Industry-Affiliation R&D Program on Optical I/O.

6. References

[1] T. Tekin et al., eds. *Optical interconnects for data centers*. Woodhead Publishing, 2016.
[2] I.M. Soganci et al, Optics express 21.13 (2013): 16075-16085.
[3] V.Bardinal et al. Adv.in Optical Technologies, (2011).
[4] C. Levallois et al. Photonics Europe. Vol. 6992. 2008.
[5] D. Taillaert et al., Optics letters, 29(23), 2749-2751, 2004.
[6] P. Verheyen, et al., Integrated Photonics Research, Silicon and Nanophotonics (pp. IW3A-4), OSA, 2014.
[7] B. Snyder et al., IEEE Transactions on Components, Packaging and Manufacturing Technology, 3(6), 954-959, 2013.
[8] S.M. Kim et al., J. Phys. D: Appl. Phys. 36 2451-6, 2003.
[9] D. Daly et al., in Measurement Science and Technology 1.8 (1990): 759.