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III/V nano ridge structures for optical applications on patterned 300 mm silicon substrate

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We report on an integration approach of III/V nano ridges on patterned silicon (Si) wafers by metal organic vapor phase epitaxy (MOVPE). Trenches of different widths (≤500 nm) were processed in a silicon oxide (SiO_2) layer on top of a 300 mm (001) Si substrate. The MOVPE growth conditions were chosen in a way to guarantee an efficient defect trapping within narrow trenches and to form a box shaped ridge with increased III/V volume when growing out of the trench. Compressively strained InGaAs/GaAs multi-quantum wells with 19% indium were deposited on top of the fully relaxed GaAs ridges as an active material for optical applications. Transmission electron microcopy investigation shows that very flat quantum well (QW) interfaces were realized. A clear defect trapping inside the trenches is observed whereas the ridge material is free of threading dislocations with only a very low density of planar defects. Pronounced QW photoluminescence (PL) is detected from different ridge sizes at room temperature. The potential of these III/V nano ridges for laser integration on Si substrates is emphasized by the achieved ridge volume which could enable wave guidance and by the high crystal quality in line with the distinct PL. *Published by AIP Publishing.* [http://dx.doi.org/10.1063/1.4961936]

Silicon photonics is a rapidly growing field of research, combining the advantages of the mature silicon (Si) microelectronic technology and of optical data transmission.[1,2] Having a low-cost integration scenario for an efficient laser diode on the Si substrate is the key to fully profit from optoelectronic integration circuits (OEICs). The main obstacle is that Si is a poor light emitter due to its indirect electronic band structure; therefore, other active materials with high optical gain have to be transferred to the Si substrates. Many different approaches are under investigation, which can be divided into two main routes: (1) Hybrid integration such as wafer- or chip-bonding,[3–7] which allows for the best choice of laser material and device structure but is very likely a complex and expensive process flow. (2) Monolithic integration such as the direct epitaxial growth of laser materials on Si.[8–15] A monolithic approach could lead to a collective integration process flow with CMOS, which is highly scalable and cost-efficient. But it suffers from the formation of misfit and threading dislocations (TDs) due to the lattice mismatch between Si and most of the potential active materials. Although a clear reduction in dislocation density has been reported in literature, the remaining defect density still limits the device lifetime.[16,17] The integration of quantum dot lasers is a promising approach, as it seems to degrade less rapidly under the presence of non-radiative defects.[18,19] Hetero-epitaxial growth of GaNAsP/GaBP based laser diodes lattice matched on Si circumvents the formation of misfit dislocation (MD) but bears other challenges due to the complexity of the involved unknown material systems such as dilute nitrides and borides.[20] Up to now, the remaining defect density in the active material system was always preventing a sufficient laser diode lifetime in the monolithic integration approach.

In this paper, we discuss a III/V laser integration approach on (001) Si, which is based on aspect ratio trapping (ART)[21,22] in narrow oxide trenches starting with a V-shaped Si surface. A high aspect ratio allows for an efficient defect trapping whereas III/V nucleation on the {111} facets of the V-shape avoids the formation of anti-phase domains.[23,24] The high potential of ART has been demonstrated in various recent publications.[15,25,26] However, in the present work we want to benefit maximally from the ART by growing in very narrow trenches while still achieving a high III/V material volume for a sufficient modal gain by growing out of the trenches under the conditions that lead to clearly broadened III/V ridges. Pseudomorphically strained InGaAs/GaAs multi-quantum wells (MQWs) were deposited on the box shaped GaAs ridges on top of a patterned 300 mm Si wafer. High crystal quality and distinct photoluminescence (PL) have been observed, emphasizing the potential of these III/V nano ridges for laser integration.

The epitaxial growth was performed by metal organic vapor phase epitaxy (MOVPE) in a 300 mm deposition chamber applying group-V and -III precursors such as tertiarybutyl arsine (TBAs), trimethylindium (TMIn), triethylgallium (TEGa), and trimethylgallium (TMGa). Based on a standard STI (shallow trench isolation) process flow, Si trenches of different widths and lengths were realized in a 300 nm thick SiO_2 layer on the exact (001) oriented 300 mm Si substrates. The trench structures investigated in this work have a length of 10 μm, whereas the width varies from 20 nm to 500 nm. Trenches with the same dimension are grouped as arrays within 600 μm × 600 μm fields. The ratio of the Si trench surface versus the total area is kept between 9% and 10%. V-shape formation and exposure of {111} facets before epitaxial growth were achieved by a tetramethylammonium hydroxide

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(TMAH) wet-etch process. More details about the Si wafer treatment before deposition and a general introduction to the GaAs integration approach by MOVPE are published in Ref. 27. For the current structures, we applied a two-step GaAs monolithic deposition process. The GaAs nucleation layer was grown at 360 °C with TEGa, whereas the main layer growth inside as well as outside the trench was performed at 580 °C with TMGa. Chosen V/III ratios were 70 and 15, respectively. The InGaAs quantum well (QWs) were also deposited at 580 °C with a V/III ratio of 18.

The photoluminescence (PL) was carried out on a micro-PL set-up. The excitation wavelength of 532 nm from a continuous Nd:YAG laser was focused as a circular spot, 200 μm in diameter, on the sample within one array of identical trenches for each measurement. The pumping power was around 30 mW. The PL signal was detected by a thermoelectric-cooled InGaAs detector after passing a high-pass filter at 650 nm to cut off the excitation signal. Transmission electron microcopy (TEM) was performed using a Titan (FEI) microscope operating at 300 kV, whereas a Helios (FEI) focused ion beam (FIB) was used for the sample preparation and lift-out. Spin-on-carbon (SOC) and electron beam deposited platinum (e-Pt) were used as a capping layer.

A low temperature seed is important to ensure a 2-dimensional GaAs nucleation layer on the {111} facets and at the same time to avoid the formation of planar defects such as stacking faults and twins. Growth at high temperature guarantees better GaAs crystal quality and enhances misfit defect nucleation and TD gliding, which are essential for full relaxation. The silicon oxide (SiO_2) trench sidewalls lead to an efficient defect trapping. TDs lying in planes perpendicular to the STI walls are easily confined. Also, TDs running in lattice planes parallel to the trench orientation can be trapped, if these defects glide along the {111} planes such as 60° misfit dislocation preferably do. Due to the inclined angle of these {111} planes towards the vertical trench wall, each {111} plane will finally hit an oxide wall, if the aspect ratio is high enough. In the same way, planar defects on {111} planes parallel to the trenches are trapped. Only planar defects lying in planes perpendicular to the trenches will never be blocked. Therefore, it is of key importance to avoid the formation of stacking faults and twins from the beginning by an optimized seed layer and sufficient pre-cleaning of the Si surface, whereas the nucleation of misfit- and threading dislocations should be initiated as deep as possible in the trench, close to the Si surface, to benefit from a high aspect ratio.

Under the chosen growth conditions, all trenches defined by the mask pattern were filled uniformly with GaAs. Since the deposition was continued after reaching the trench top, a clear box shape formation was observed along each trench. The original V-shape given by the Si surface disappears due to reflow of the GaAs seed layer during the temperature ramp to 580 °C. In addition, the growth rate on the upwards oriented Ga-rich {111} planes is the highest under the chosen MOVPE conditions. Therefore, these $(111)A$ and $(\bar{1}\bar{1}1)A$ facets vanish during growth and the ridge shape is finally dominated by the (001) top surface, the {110} side facets, and the As-rich $(11\bar{1})B$ and $(\bar{1}\bar{1}\bar{1})B$ facets at the ridge bottom, which all have a lower growth rate.[28] Figure 1 shows the scanning electron microscopy (SEM) images of GaAs box shaped ridges. The basic rectangular shape evolution is the same for narrow and wide trenches while the total volume and ridge height are defined by the trench width. It is also important to emphasize that the ridge courses are very straight and uniform with flat surfaces in all directions, which is essential for realizing a waveguide with low light scattering losses.

Reciprocal space maps (RSM) indicate (not shown here) that these GaAs ridges are completely relaxed; thus, the (001) GaAs box surface provides the strain-free lattice constant of GaAs, which is used as a buffer for the pseudomorphic growth of compressively strained InGaAs MQWs. In order to achieve efficient PL and high modal gain, a three-time InGaAs/GaAs QW structure with about 19% In was grown on these GaAs ridges.

The InGaAs QWs are clearly noticeable in HAADF-STEM (high-angle annular dark-field scanning transmission electron microscopy) images, see Figure 2. The top-left picture is a cross-section of the full device ridge while the top-right image provides a higher magnification of the QW region. The straightness of the QWs becomes very obvious in the transverse HAADF-STEM section along the trenches, bottom picture in Figure 2 (the GaAs inside the STI trenches has a slightly different contrast, because some STI material was also cut out during the fib (focused ion beam) lamella preparation). Energy-dispersive X-ray measurements (EDX) confirm the In content of about 19% for QWs grown on the 100 nm wide trenches.

The thicknesses of the QWs on the (001) surface are 9.9 nm, 8.9 nm, and 7.7 nm counting from the bottom to the

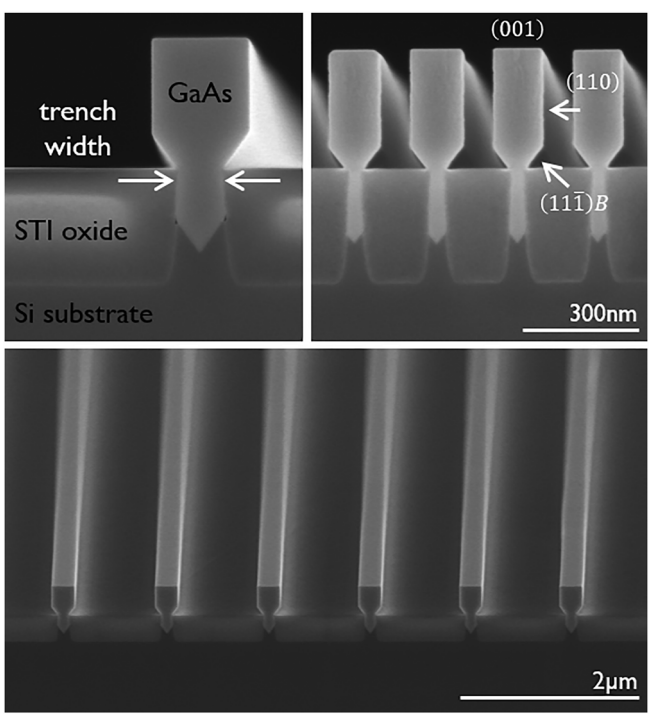

FIG. 1. SEM pictures of box shaped ridges integrated on STI-patterned Si wafers. Top left: Cross-section of a 100 nm wide trench. Top right: Cross-section of 20 nm wide trenches. Bottom: inclined top-view of a 100 nm trench array. The facet nomination is the same for the GaAs growth in narrow and wide trenches.

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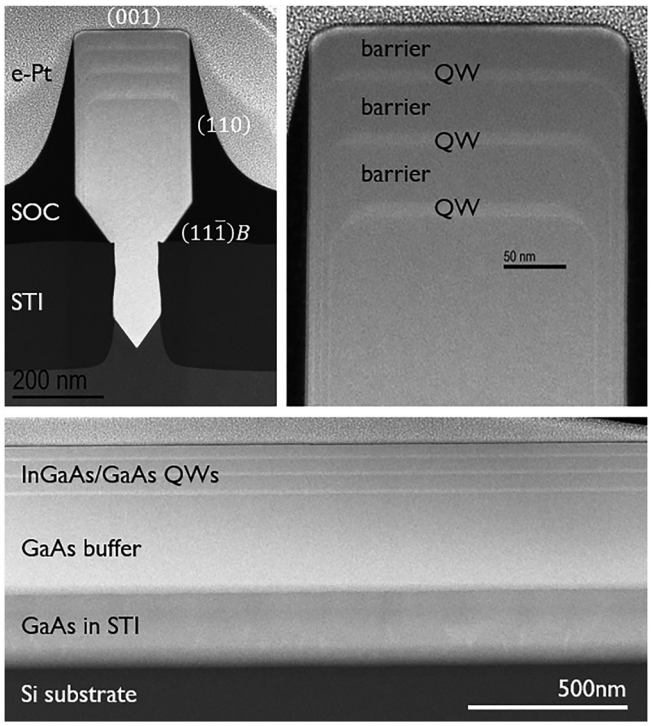

FIG. 2. HAADF-STEM pictures of a box shaped GaAs ridge with three InGaAs QWs. Top left: Cross-section of the full ridge. Top right: Higher magnification of the QW region. Bottom: Transverse section along the trench. The GaAs inside the STI shows a slightly different contrast because some STI oxide was cut out during sample preparation.

top, although the growth time per QW was kept constant. The deposition time of the last three GaAs barrier layers was also fixed but it is very obvious in Figure 2 (top-right) that the thickness is decreasing going from the bottom of the structure to the top. A closer look at the magnification in Figure 2 reveals that InGaAs is also deposited around the corners on {111} facets and higher index crystal planes. At the same time, the InGaAs layer thickness decreases continuously along the edges and converts into a uniform and very thin (<2 nm) layer on the two {110} box side walls. Nevertheless, the main active InGaAs material is provided by the uniform QWs on the (001) plane with lateral dimensions of more the 160 nm.

The III/V material supply for a given deposition time, coming from the gas phase as well as from loading effects on the STI mask, is distributed around the full box surface at which the growth rate on the top (001) surface still dominates the ridge evolution. The increase in total surface over time leads to a clear reduction in the growth rate with rising box size. This strong correlation between the effective (001) growth rate and the total ridge size requires well-adjusted MOVPE process conditions for the full device stack, which is possible once the growth rates are defined. In addition, the side wall deposition leads to a very good lateral carrier confinement reducing non-radiative recombination channels at the QW side surfaces and is therefore desirable. Especially the evolving decrease in InGaAs thickness at the lateral ends of the QWs will lead to higher quantized electronic states, which induces an injection and repulsing of electrons and holes in the InGaAs layer at the box edges towards the centered QW region with constant layer thickness and lower energetic states. The InGaAs layer of less than 2 nm thickness on the {110} side walls is too thin to hold bonded states with an efficient radiative recombination rate.

The fact that ART leads to a very efficient defect trapping in 100 nm wide trenches was confirmed by investigating high resolution HR-TEM and bight field BF(002) images in cross-section looking at several trenches as well as along a 5.5 μm long transverse ridge lamella. All threading dislocations (TDs) are well confined inside the STI trench. No indication of any misfit and threading dislocations was found above the STI level or close to the MQW region. Only three planar defects such as micro twins are visible in a 5.5 μm long transverse section, see Figure 3.

The complete blocking of TDs within the trench region is a very important achievement towards laser integration with sufficient lifetime. The impact of planar defects on the device performance might be less than for TDs; nevertheless, a further reduction in density is wanted. The formation of planar defects can have various sources. In our case, we suspect that twins or stacking faults are caused either by a non-optimal GaAs seed layer or by residuals and contamination on the Si surface due to a non-perfect cleaning procedure.

In order to have a first feedback about the optical properties of the QWs, room temperature PL measurements were carried out looking at different trench widths. A clear emission peak between 1000 nm and 1050 nm can be observed from all structures except for the 500 nm trench width. The photon emission from the MQWs is several orders of magnitude higher in intensity than the signal from the doped Si substrate around 1140 nm. Figure 4 contains a selection of PL spectra in log-scale. Some spectra show a weak high-energetic shoulder around 980 nm, which could be related to radiative recombination from higher quantized states. For

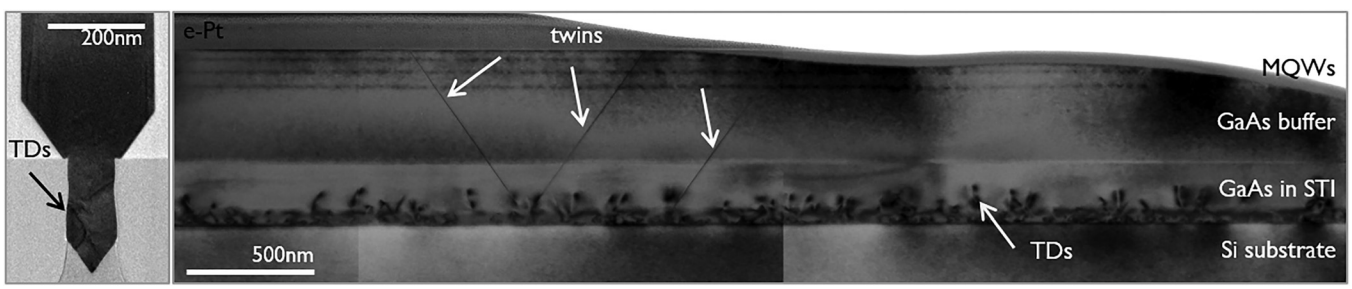

FIG. 3. Left: Cross-section HR-TEM of the GaAs buffer. Right: Combined BF(002) images of a transverse section along the trench. The vertical lines visible in the Si substrate are caused by the image combination. Threading dislocations are clearly visible by the dark blurred contrast, whereas planar defects such as micro twins cause a straight dark line in ⟨111⟩ directions.

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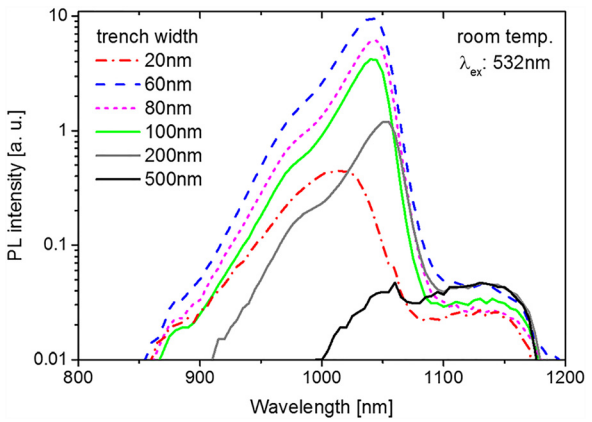

FIG. 4. Room temperature PL spectra from different trench widths in log-scale.

the widest trench size, the QW-PL is still recognizable but very weak. With a reducing trench width, the corresponding PL intensity increases up to 60 nm wide trenches before going down again for 20 nm wide trenches. But even for the narrowest trench width of 20 nm, the PL intensity from the QWs is still very pronounced, see Figure 4. Comparison of the PL intensity has to be treated very carefully due to the following reason: The total III/V ridge volume on top of the trenches as well as the periodic arrangement of each trench within an array varies; therefore, the absorption of the pump light will differ in each structure leading to different excited carrier densities. In addition, the changing ratio of surface area over ridge volume for each type of trench will have a big impact on the effective carrier concentration in the QWs considering that non-radiative recombination processes at surface states are in competition to the radiative recombination in the active material. Although it is difficult to judge about the overall impact of these uncertainties, it is very likely that the decrease in PL intensity towards wide trenches is linked to an increase in TD density. The aspect ratio of trenches wider than 100 nm is quite low, leading to an insufficient defect trapping. Hence, the remaining defect density in the ridge material of wider trenches could cause high carrier losses. The intensity decline towards narrow trenches could be related to a disproportional rise in ridge surface area or less pump light absorption.

The shift in PL-peak position can be explained by a change in In concentration or in QW thickness for the different trenches, inducing an energetic shift in the quantized states. Both effects are very likely to occur because the MOVPE growth behavior on top of the ridge is very complex. Further investigation is necessary to evaluate both explanations.

The PL line width of the 100 nm wide structure is about 38 meV for the chosen experimental conditions. TEM investigation of the 100 nm wide trench structure revealed that the QW thickness is not constant but varies. This variation in QW width will have an impact on the PL line width of a single MQW stack due to contributions from different quantized states. This QW thickness variation seems to be the strongest for the 20 nm trenches, since the PL line width is clearly broadened in comparison with the others. However, the origin of this broadening can be easily avoided by adjusting the growth time for each QW.

In conclusion, we have introduced an approach towards the integration of III/V nano ridge lasers based on the selective area growth in narrow trenches by MOVPE. TEM investigation confirms a very efficient defect trapping in GaAs inside the trenches, whereas the GaAs ridge on top of the trenches is completely free of threading dislocations. Only a few planar defects are still present. The growth of pseudomorphically strained InGaAs/GaAs MQWs with 19% In on top of these fully relaxed GaAs ridges leads to a pronounced PL peak around 1040 nm, which emphasizes the potential for optical application. Despite the narrow trench dimension, the grown out III/V ridge has reached a volume suitable for wave guidance (various publications of laser devices with comparable dimension can be found in literature, e.g., Refs. 15, 29, and 30). Currently, optimized nano ridge structures with an increased GaAs volume and a confining InGaP cap layer to reduce carrier losses due to surface recombination are under investigation. First, SEM inspections have revealed that the ridge volume was scaled up by a factor of 2, which clearly improves the light field confinement. All these achievements point towards the realization of first nano ridge laser diodes in the near future.

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