Selective Epitaxial Growth of III-Vs on Patterned 300 mm Si Substrate

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Abstract— Emerged more than a decade ago, silicon photonics has been widely recognized as the best integration platform for various applications of optical data transmission, mainly due to its direct compatibility with CMOS infrastructure and its very compact size. While most of the required building blocks have been demonstrated, the key functionality of light generation has become the most challenging task, and the co-integration of other materials becomes essential. III-V material is the dominating material platform for active optoelectronic devices. The introduction of III-Vs on a silicon photonics chip has been widely explored by using bonding technology, and great achievements have been made. Nevertheless, bonding technology has its own limitations, e.g., the relatively high cost, the incompatibility with CMOS, the low yield, etc. Therefore, integration of III-Vs on silicon by epitaxial growth can be the optimal solution, as long as the huge lattice constant and polarity difference between the two materials can be effectively overcome.

In this report, we present the selective growth of InP and InGaAs on patterned 300 mm (001) silicon substrate. CMOS compatible processes were carried out to form nano-scale SiO_2 trenches on silicon, and the defect-trapping effect of the narrow trench dramatically reduces the defect density of the III-Vs selectively grown inside and outside of the trench. To address the polar/non-polar interface obstacle for high quality growth, a unique design of the III-V/Si interface shape and also an optimized nucleation procedure was developed. Micro-PL measurement results show almost defect free III-Vs on silicon has been achieved. It is also interesting to find that the In content of InGaAs material grown on the intermediate InP buffer layer changes and hits the 1550 nm window by optimizing the trench width.