193nm immersion lithography for high performance silicon photonic circuits

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ABSTRACT

Large-scale photonics integration has been proposed for many years to support the ever increasing requirements for long and short distance communications as well as package-to-package interconnects. Amongst the various technology options, silicon photonics has imposed itself as a promising candidate, relying on CMOS fabrication processes.. While silicon photonics can share the technology platform developed for advanced CMOS devices it has specific dimension control requirements. Though the device dimensions are in the order of the wavelength of light used, the tolerance allowed can be less than 1% for certain devices. Achieving this is a challenging task which requires advanced patterning techniques along with process control. Another challenge is identifying an overlapping process window for diverse pattern densities and orientations on a single layer.

In this paper, we present key technology challenges faced when using optical lithography for silicon photonics and advantages of using the 193nm immersion lithography system. We report successful demonstration of a modified 28nm-STI-like patterning platform for silicon photonics in 300mm Silicon-On-Insulator wafer technology. By careful process design, within-wafer CD variation (1sigma) of <1% is achieved for both isolated (waveguides) and dense (grating) patterns in silicon. In addition to dimensional control, low sidewall roughness is a crucial to achieve low scattering loss in the waveguides. With this platform, optical propagation loss as low as ~0.7 dB/cm is achieved for high-confinement single mode waveguides (450x220nm). This is an improvement of >20 % from the best propagation loss reported for this cross-section fabricated using e-beam lithography. By using a single-mode low-confinement waveguide geometry the loss is further reduced to ~0.12 dB/cm. Secondly, we present improvement in within-device phase error in wavelength selective devices, a critical parameter which is a direct measure of line-width uniformity improvement due to the 193nm immersion system. In addition to these superior device performances, the platform opens scenarios for designing new device concepts using sub-wavelength features. By taking advantage of this, we demonstrate a cost-effective robust single-etch sub-wavelength structure based fiber-chip coupler with a coupling efficiency of 40 % and high-quality (1.1x105) factor wavelength filters. These demonstrations on the 193nm immersion lithography show superior performance both in terms of dimensional uniformity and device functionality compared to 248nm- or standard 193nm-based patterning in high-volume manufacture platform. Furthermore, using the wafer and patterning technology similar to advanced CMOS technology brings silicon photonics closer toward an integrated optical interconnect.

Keywords : Silicon photonics, WDM devices, waveguides, fiber-chip couplers

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1. INTRODUCTION

Next-generation silicon photonics transceivers will require the integration of ultra-low-power active devices with ultra-low-loss passive devices enabling wavelength-division multiplexing (WDM). A major challenge in the manufacturing of such devices is the extreme sensitivity of the device and waveguide properties (phase and amplitude transfer control) on the cross-sectional dimensions and sidewall quality of the employed photonic wire and rib structures, which results in poor device uniformity across a die or a wafer [1]. Recently, there have been works reported on high-resolution pattering for silicon photonic circuits by using advanced CMOS technology [2-4]. Since it is early days, the performance reported so far are on-par with 200mm based toolset. In this paper, we demonstrate that by using advanced CMOS process technology with 300mm pattering toolset performance and device can be improved by an order of magnitude.

2. LITHOGRAPHY CHALLENGES

Patterning of silicon photonic circuits bring new challenges compared to CMOS, in particularly for lithography. The two main challenges for lithography are, firstly, diversity in device geometry, where a ring resonator is defined by a combination of an isolated line, which is ~450 nm and a semi-isolated trench of ~140 nm. Another example of such diversity is photonic crystal devices, where one would need an isolated line and dense holes. Though the CDs, at least in the present example do not call for advanced patterning platform the specification on the dimensional accuracy and tolerance is demanding. Silicon photonic devices are very sensitive to small cross-section dimensional variation, roughly 1nm variation in CD would shift the spectral response of the device by 1nm. Hence a platform that can deliver such a high degree of uniformity is needed. Though active tuning can be employed, it is desired that the CD variation is kept to a minimum to reduce power spent on tuning the non-optimal devices. In addition, line edge roughness on the waveguides both high and low-frequency components of roughness directly affect the optical propagation loss in the waveguides by scattering along the edges of the patterned silicon. The loss in the optical power has a direction implication on the power penalty of the systems, hence the loss has to be controlled, particularly where energy efficiency is crucial.

3. PROCESS FLOW

The devices were fabricated in 300 mm photonic-SOI wafer that has 220 nm of crystalline silicon device layer on top of a 2000 nm thermal oxide (BOx). The patterning process for silicon photonic circuit was developed by modifying 28- nm shallow-trench isolation (STI) process. The pattern on the photomask is transferred into silicon using 193-nm immersion lithography and a dry etch process. For functional devices we used two etch levels, 220-nm for waveguide and waveguide based devices and 70-nm for light-chip coupling gratings. Figure xx shows fabrication result of different photonic devices in silicon.

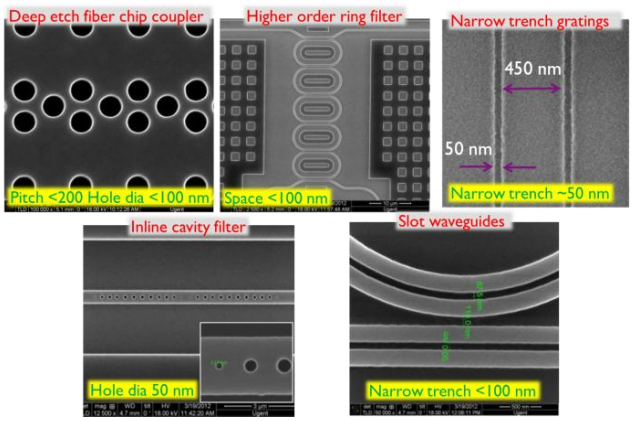

Figure 1 Different silicon photonic devices fabricated in300 mm SOI wafer using the 193 nm immersion and dry etch process.

4. PATTERNING RESULT SUMMARY

4.1 CD Uniformity

Wafer-scale uniformity of the target CD is monitored after lithography and dry etch and strip process. The CDs are measured using top-down CDSEM. Figure 2 shows the variation of a 450 nm waveguide during the pattering process. We observe a 3σ of 2.34 nm and 7.95 nm after lithography and finally pattering respectively, which is >50% improvement from 193nm dry lithography based pattering in 200mm pattering tool set (

Table 1) . As mentioned earlier regarding multitude of patterns in one pattering step, we were able to pattering 80nm trenches in 450 nm/80 nm line-space-line structure with high degree of uniformity (

Table 1).

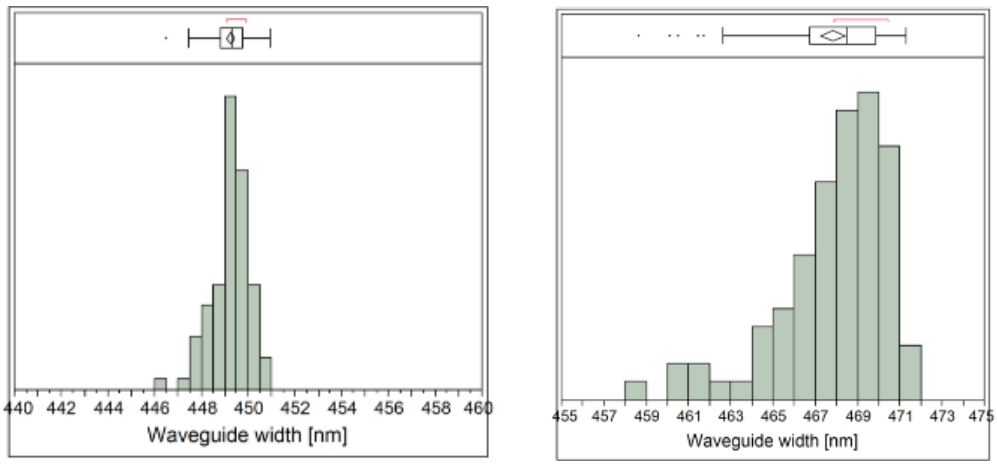

Figure 2 CDU of a 450 nm wire waveguide after lithography(left) and etch(right) over a 300mmm wafer.

Table 1 CDU comparison of a 450 nm wire waveguide between 200mm and 300mm pattering tool sets

Patterning platform	**450 nm photonic wire**		**80 nm space in 450/80 nm line/space**	
	After Lithography 3σ [nm]	**After dry etch 3σ [nm]**	**After Lithography 3σ [nm]**	**After dry etch 3σ [nm]**
200mm 193nm dry litho/Dry etch	7.05	2.34	NA	NA
300mm 193immersion litho/ Dry etch	17.25	7.95	5.39	5.95

5. DEVICE RESULTS

We present there type of devices to demonstrate the advantages of using 193immersion based 300mm pattering toolset platform for silicon photonic circuits; waveguides for demonstrating pattering quality with respect to sidewall roughness, photonic crystal nano-cavity and fiber-chip coupler for demonstrating complex device pattering and wavelength selectrive devices for within-device and within-wafer CD control.

5.1 Propagation loss

We use three types of waveguides to demonstrate the loss performance: (1) single-mode photonic full-depth etched wires, (3) shallow etched ridge waveguide with single mode bend sections and (3) slot waveguide. The propagation loss in these waveguides is mainly attributed to light scattering off the etched sidewalls. Therefore, losses are a direct qualification of the patterning process quality. To assess the propagation loss, we fabricated single mode spiral photonic wire (450nm) ,ridge (700nm) and slot waveguide (260nm rail width, 100nm slot width). Each waveguide comes in 4 lengths (1, 2, 4 and 7cm) from which the propagation loss is extracted by a linear fit. The bend radius of wires and slot waveguides was 10µm and 20µm respectively for photonic wire and slot waveguides. Spiral ridge waveguide was built using straight ridge section and 4µm photonic wire bend attached by a transition waveguide as shown in Figure 5. While the wire and slot waveguides are fully etched (220nm), ridge waveguide is 70 nm shallowly etch.

In the C band, we measure an average propagation loss of 0.7 dB/cm for 450 nm wide wire waveguides with oxide side-cladding (Figure 3). The error margin on individual data point is <0.02dB. To our knowledge, this is the lowest loss reported for fully etched single-mode silicon wire. The waveguide losses are verified across the 300mm wafer with 3-σ variation of 0.12dB/cm and a range of 0.12dB/cm (Figure 3). This represents over 50% improvement as compared to the best single-mode waveguide reported loss on a 200mm platform and 30% better than the best loss demonstrated with e-beam technology.

For slot waveguides, we measure a propagation loss of 2dB/cm at 1550nm (Figure 4), while with the 200mm platform, a similar type of waveguide geometry yields a loss of between 10-15dB/cm. This is a direct consequence of low sidewall roughness on fully etch waveguides.

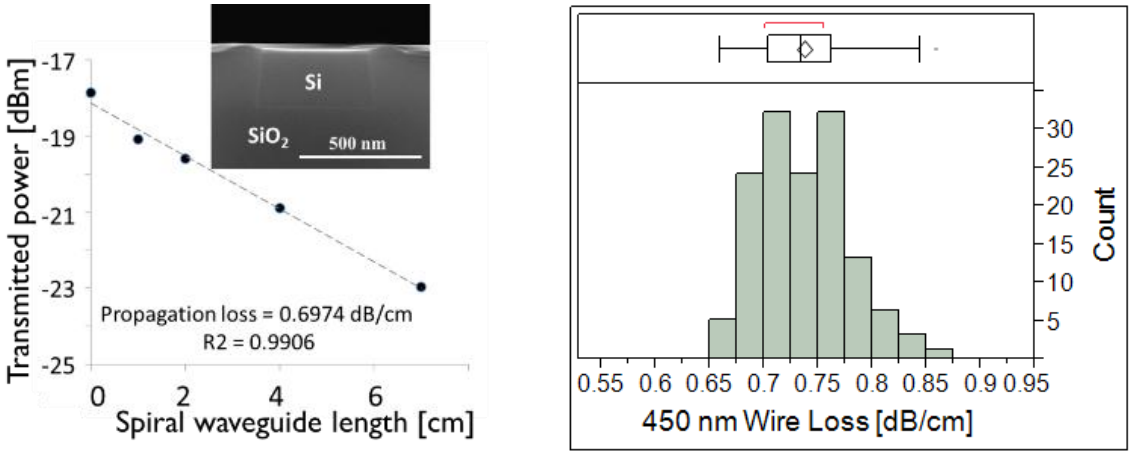

Figure 3 Propagation loss of a 450 n wide photonic wire waveguide and uniformity over a 300 mm wafer.

Figure 5 shows the propagation loss and bend loss of a compact ridge waveguide. We measured a propagation loss of 0.12dB/cm and a total bend loss of 0.01 dB/bend. The propagation loss of the single mode ridge waveguide due to reduce sidewall interaction with the propagating mode has considerably low loss compared to wire waveguide, which is in line with the expected trend. Though low-loss ridge waveguides alone require large radius to make a 90 degree bend, hence using wire waveguide with transition enables compact yet low-loss waveguide circuit.

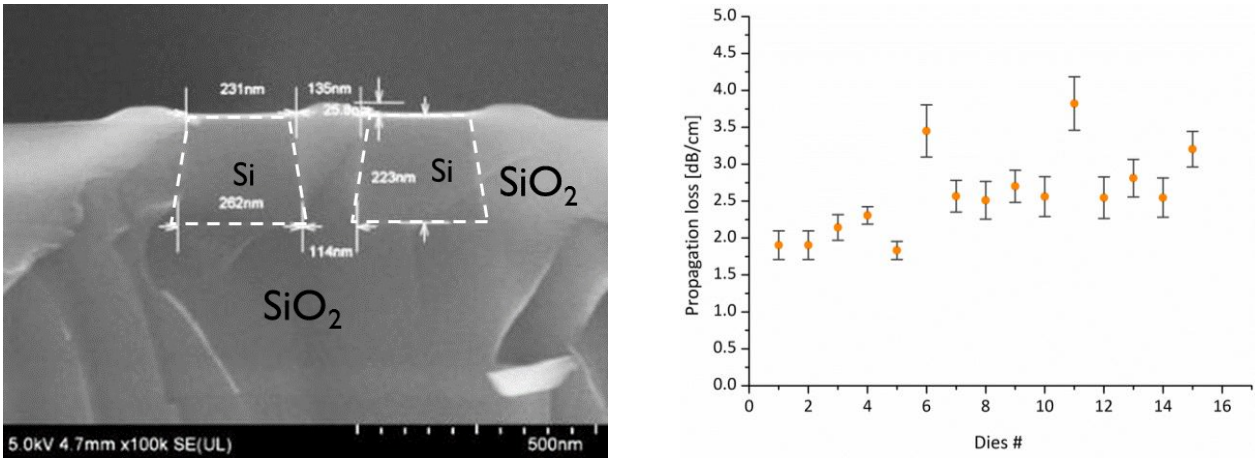

Figure 4 (Left)Cross-section view graph of a slot waveguide with respective dimension and (Right) Propagation loss of the slot waveguide over a 300mm wafer with cross-section dimensions shown in the view graph.

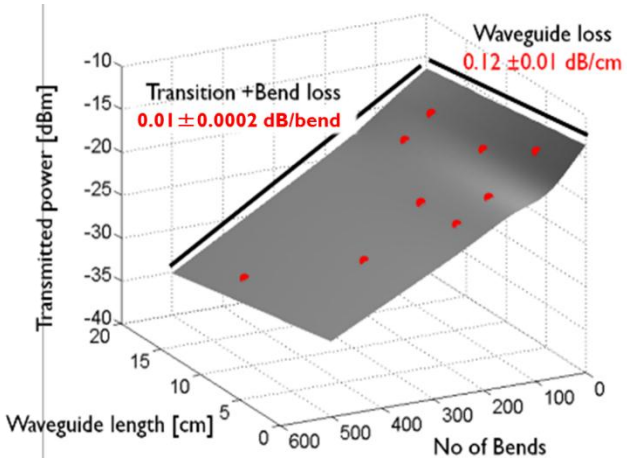

Figure 5 (Left) Schematic of a compact ridge waveguide bend with wire waveguide and transition. (Right) Propagation and bend loss extraction(at 1550 nm band) from a 2D plan fitting of measured transmitted power.

5.2 Complex device patterns

We use two photonic crystal based devices as an example of complex pattering demonstration; photonic crystal (PhC) based fiber-chip coupler and 1-D photonic-crystal based high-quality factor nano-cavity. Both devices are challenging in their own right, PhC based fiber coupler used sub-wavelength grating, where the pitch of the PhC is ~220 nm with a fillfactor of 68% of which results in gap of ~70 nm between the holes. Figure 6 shows the SEM image of a fiber coupler implement using PhCs. Unlike standard line/space grating based fiber coupler implementation, this type of implementation brings in a key advantage of manufacturability, where the silicon is completely etch till the box, which is use a etch-stop layer removing etch depth based non-uniformity. Figure 6 shows measured coupling efficiency to a single-mode optical fiber, we measured an efficiency of 40% against 30% with standard implementation [5]. The efficiency is comparable to the previous demonstration with e-beam technology [6].

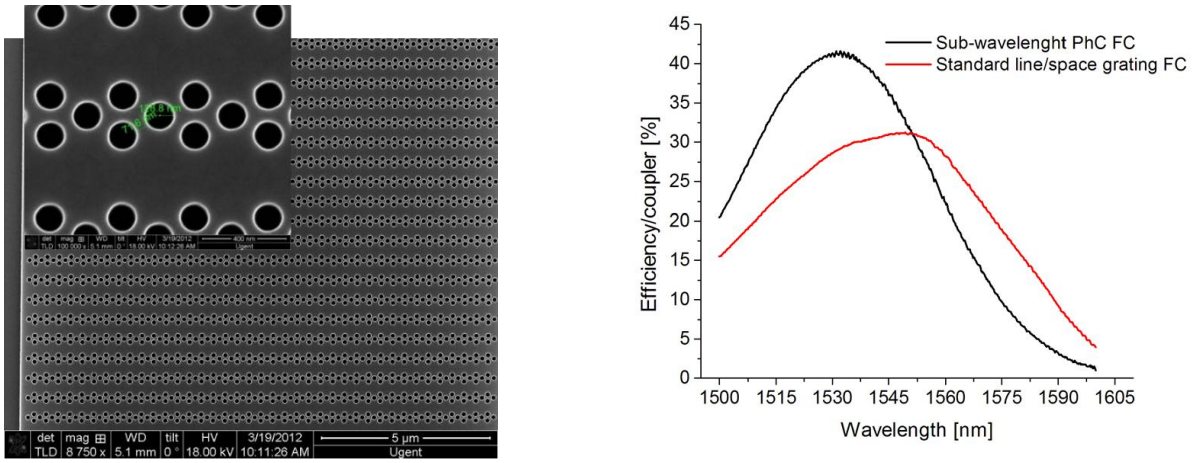

Figure 6 (Left) top-down SEM image of a photonic crystal based fiber-chip coupler and (left) coupling efficiency of a coupler compared with a standard line-space based coupler.

PhC cavities have been investigated intensively during recent years; they can strongly confine light in a small volume enabling high-quality factor. These types of cavities are interesting for a wide spectrum of application, including high-speed modulators. Despite their advantages reliable, large-scale fabrication still remains a challenge as they require

tighter specification on the CD control. Using 193nm immersion pattering, we were able to fabricate and demonstrate for the first time a 1-D PhC cavity on a photonic wire waveguide (Figure 7). The PhC was chirped to reduce reflection, which makes the pattering even more challenging as they need hole diameters <70 nm, in this particular case hold diameter of 50 nm was achieved. Designs with varying PhC dimension was fabricated and optically characterized. Figure Figure 7 shows optical characterization of cavity modes from different designs, and the inset shows the expected wavelength from the design. High Q-factor in correspondence to a predictable wavelength demonstrates patterning fidelity and accuracy, which has never demonstrated with a high-volume manufacturing process.

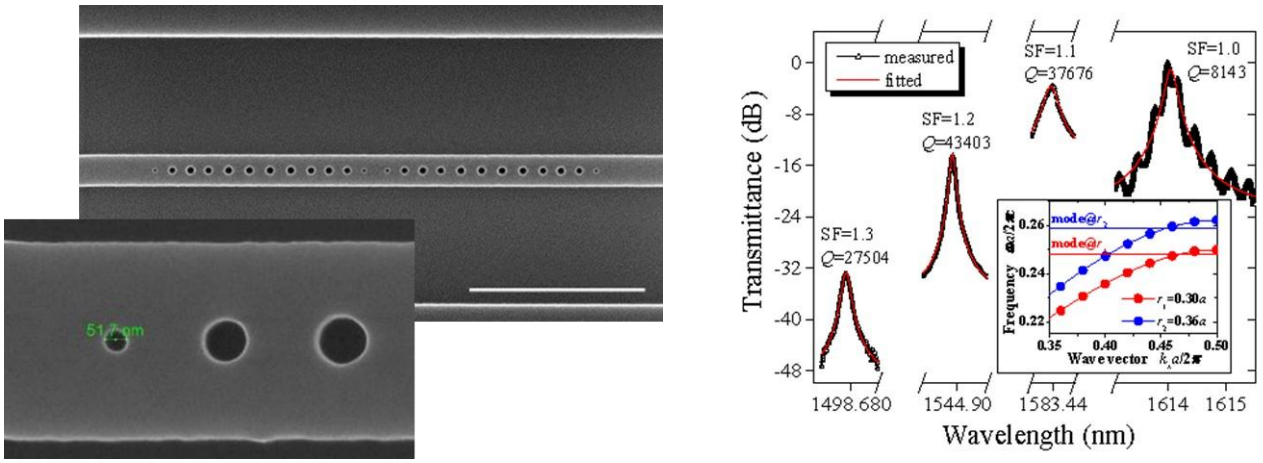

Figure 7 (left) Top-down SEM of a 1D photonic crystal cavity with chirped holes and (left) optical characteristics of nano-cavity with varying PhC dimensions. SF-scaling factor of PhC design

5.3 CD control

Wavelength selective devices are an essential component in a photonic circuit for wavelength division multiplexing and de-multiplexing (WDM). There are a variety of devices that one can use for WDM; however, all of them are very sensitive to small dimension variation as mentioned earlier. Not only, for device match, dimensional variation also impacts a single device such as an Arrayed Waveguide Grating (AWG). AWGs use delay arm preferably using photonic wires to make them compact, any device in the wide of the waveguide along the delay arm will result in phase error, which will translate to channel crosstalk in device performance. In practice, the waveguide with is widened to circumvent this issue, typically 800nm instead on 450nm. We fabricated two types of designs one with 800 nm waveguides and the other with 450 nm. Figure 8 shows schematic of an AWG and the two different implementation. Optical characterization of the devices showed no difference between an 800 nm and 450 nm wide delay arm suggesting low phase error or good CD control of the waveguide within a device.

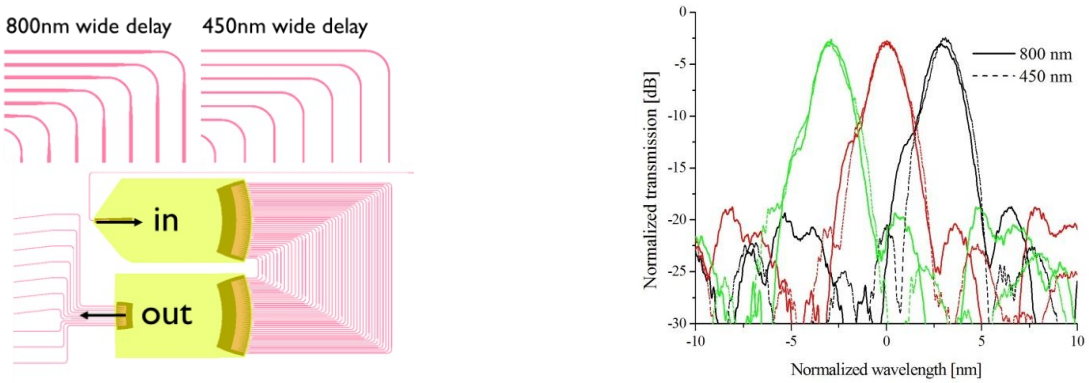

Figure 8 Normalized transmission spectrum of 3 adjacent channels from 8X400 GHz AWGs with 450 nm an 800 nm delay arm wire width

6. SUMMARY

In this paper, we presented key technology challenges faced when using optical lithography for silicon photonics and advantages of using the 193nm immersion lithography system. We report successful demonstration of low-loss and highly uniform single mode wire, slot and ridge waveguides using a modified 28nm-STI-like patterning platform for silicon photonics in 300mm Silicon-On-Insulator wafer technology. In addition, by taking advantage of high resolution patterning we demonstrated photonic crystal based fiber-chip coupler and cavities. Furthermore, CD control of wavelength selective device showing superior phase error control has been demonstrated. These demonstrations clearly indicate that 193immersion based 300mm patterning platform for silicon photonic brings silicon photonic closer towards an integrated optical interconnect technology.

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