Planar Concave Grating Demultiplexers on an InP-Membrane-on-Silicon Photonic Platform

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Abstract—We present measurement results of a 0.25 mm^2 footprint eight-channel planar concave grating demultiplexer fabricated in a 300-nm-thick InP membrane adhesively bonded to silicon. The measured cross-talk between the different channels of the device is better than −18 dB, while the insertion loss is 2.8 dB. The power non-uniformity between the channels is 1.2 dB.

Index Terms—Demultiplexing, diffraction, gratings, nanophotonics, indium phosphide.

I. INTRODUCTION

IN THE past decades, the complementary metal-oxide-semiconductor (CMOS) industry has brought our society to the Information Age, by miniaturizing electrical circuit boards, and mass-producing them at very low cost. However, electrical wiring has now become so dense that signal delay and power consumption threaten to prevent further miniaturization. A solution proposed to overcome this bottleneck, is the use of optical on-chip interconnects. Thanks to their high refractive index contrast, photonic membranes can integrate very small optical devices into high-density, low-power photonic integrated circuits (PICs) suitable for integration on top of CMOS chips, and they are able to transport data more efficiently than electrical wiring [1].

One of such membrane photonics platforms, the silicon-on-insulator (SOI) platform, has received wide attention, and has been used to demonstrate various compact and high-quality photonic devices, as well as low-loss waveguides [2], [3]. Lasers and optical amplifiers on SOI are realized by heterogeneous integration of III-V gain materials [4]. A III-V-based membrane platform, like the InP-Membrane-on-Silicon (IMOS) platform [5], can integrate both active, and passive components in a single layer, thereby simplifying the fabrication process of PICs on CMOS. Recently, several low-power consumption active devices, including electrically-pumped lasers [6] and switches [7] have been

demonstrated in III-V-based membranes, as well as a number of high-quality passive components, including power splitters, ring resonators [5], an ultrasmall polarization converter [8], and waveguides with measured propagation losses as low as 0.4 dB·mm^{-1} [7], [9]. Another important function required for future on-chip optical interconnects is wavelength (de)multiplexing. A low-footprint four-channel arrayed waveguide grating (AWG) demultiplexer in an InP-based membrane has been reported [10], with measured insertion losses of 6 dB and a cross-talk of around −10 dB. In this letter, we report the fabrication of a 0.25 mm^2 footprint eight-channel demultiplexer in InP membrane with 2.8 dB insertion loss and −18 dB cross-talk, based on a planar concave grating (PCG).

II. DESIGN

A PCG demultiplexer (also referred to as Echelle grating, or etched diffraction grating) functions by combining the high dispersion of a large period grating, with the focusing power of a concave mirror. As shown in Fig. 1(a), the light coming from the input waveguide spreads in an unetched free-propagation region (FPR) and reaches the PCG, where it is simultaneously reflected and diffracted by the grating corrugation, and re-focused by its curvature. Due to the inherent dispersion of the grating, different wavelengths are diffracted in different directions, and can therefore be collected separately by several output waveguides placed on the so-called Rowland circle (see [11], for more detail on the design and behavior of PCG demultiplexers).

In this work, we designed an eight-channel PCG demultiplexer for transverse-electric (TE) polarized light, with a central wavelength of 1550 nm, and a channel spacing of 4.0 nm. For characterization purposes, the input and outputs of the PCG demultiplexer are connected to grating couplers [cf. Fig. 1(e)], via single-mode photonic waveguides (300 nm × 420 nm core) and linear tapers. Grating couplers are a commonly used solution to couple light efficiently from cleaved fibers into membrane photonic chips and vice versa [12]. Finally, in order to reduce the insertion loss of the device, the transition between waveguides and the FPR is optimized using deep and shallow etching [cf. Fig. 1(d)], and the reflectivity of the PCG's facets is maximized using distributed Bragg reflectors (DBRs) [13]. According to eigenmodes expansion simulations [14], a six-period DBR with 350 nm period, 50% filling factor, and 250 nm etch depth can provide above 90% power reflection in the 1520 nm to
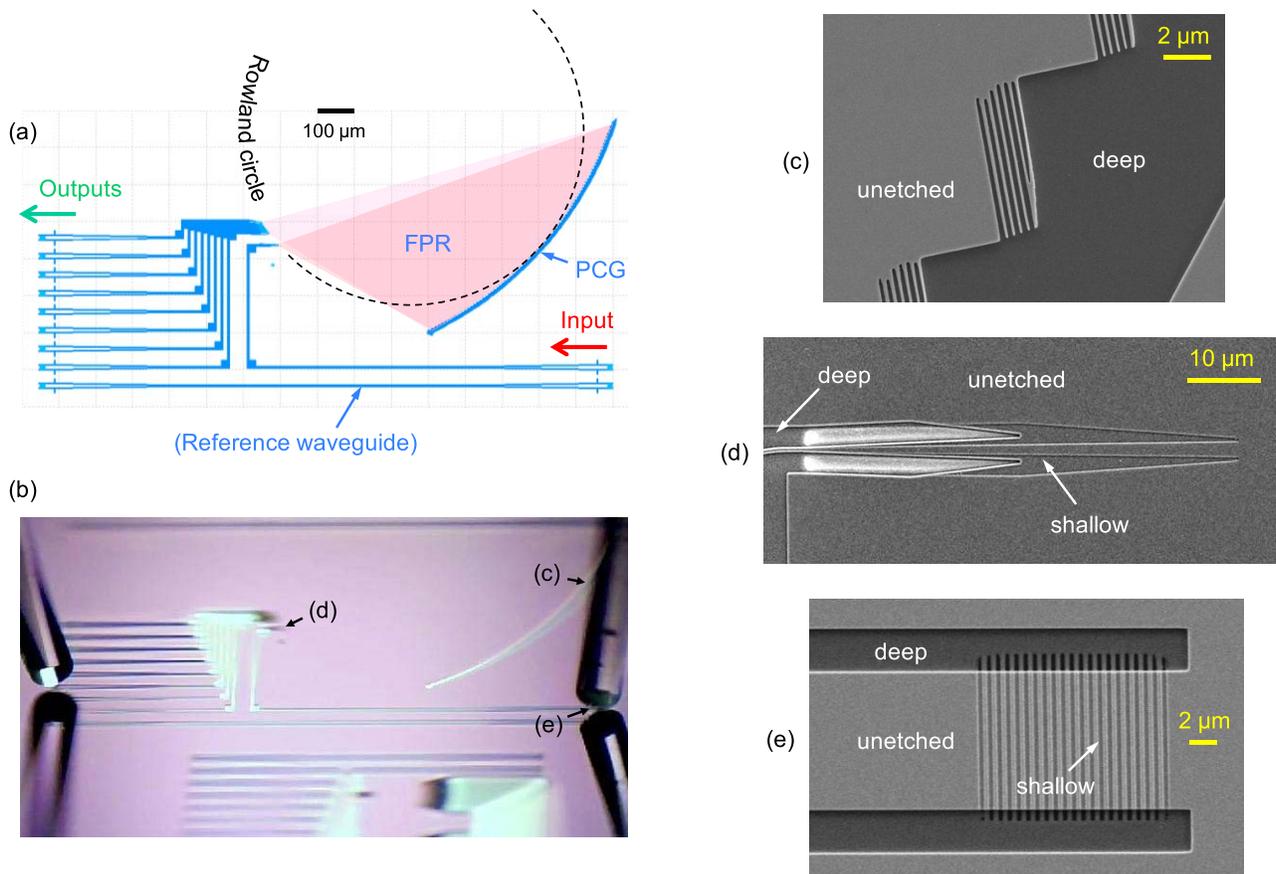
Fig. 1. (a) Layout of the presented demultiplexer. (FPR = free-propagation region, PCG = planar concave grating.) (b) 45° aerial view of the fabricated device, as seen during the measurements. (c–e) Scanning electron microscopy (SEM) images of a distributed Bragg reflector (DBR) facet of the PCG (c), the waveguide-to-FPR transition of the input waveguide (d), and a grating coupler used to couple light from a cleaved fiber into the chip (e).

1620 nm wavelength range. One of the fabricated DBRs can be seen in the SEM picture of Fig. 1(c).

III. FABRICATION

Like other devices demonstrated on the IMOS platform [15], the presented PCG demultiplexer is fabricated in a 300 nm InP membrane after the latter has been bonded to a silicon carrier wafer, following the bonding scheme described in [16].

The membrane is prepared by growing a two-layer stack (InGaAs–300 nm/InP–300 nm) on an InP substrate. The 300 nm InP layer is the future membrane, whereas the InGaAs layer will be used as an etch-stop layer during the InP substrate removal that immediately follows the bonding. A 2-inch silicon carrier wafer is cleaned and covered with a 1.5 μm thick SiO_2 layer to optically decouple the future InP membrane from the silicon. Subsequently, a die (4 mm $\times$ 6 mm, in this work) is cleaved from the previously mentioned InP epitaxy and flip-chip bonded to this silicon/SiO_2 carrier wafer, using a 50 nm thick DVS-BCB (divinylsiloxane-bis-benzocyclobutene) adhesive layer [cf. Fig. 2(a)]. The InP substrate and the 300 nm thick InGaAs etch-stop layer are then removed successively by selective wet etching (using 4HCl: $1H_2O$, and $1H_2SO_4$: $1H_2O_2$: $10H_2O$ respectively), leaving the 300 nm thick InP membrane bonded on the Si/SiO_2

carrier wafer, ready for the patterning of photonic devices [cf. Fig. 2(b)].

The presented PCG demultiplexer is fabricated in this membrane using two e-beam lithography (EBL) steps, to define consecutively deeply (250 nm) and shallowly (120 nm) etched regions. First, a 50 nm thick SiN layer is deposited on the membrane by plasma-enhanced chemical vapor deposition (PECVD), and a layer of e-beam resist (ZEP520A) is spin-coated on top of it [cf. Fig. 2(c)]. The first EBL step is then used to define simultaneously the PCG itself, the trenches around the access waveguides [cf. Fig. 2(d)], and local markers to which the second EBL can be precisely aligned. The exposed pattern is transferred from the ZEP520A layer to the SiN layer using a CHF_3–O_2 reactive ion etching (RIE) process, and subsequently from the SiN layer to the InP membrane, using a CH_4–H_2 RIE process [cf. Fig. 2(e)]. Note that a 50 nm footing is left in these deeply etched regions, to prevent under-etching of the SiO_2 cladding, during the subsequent SiN removal in buffered hydrofluoric acid. In order to define the shallowly etched regions (waveguide-to-FPR transitions and grating couplers), the SiN layer is then replaced by a fresh one, and the same EBL procedure is repeated [cf. Fig. 2(f)], albeit with a shorter etching time in the final InP RIE etching. Once all the structures are fabricated, the SiN layer is removed, and a 300 nm thick SiO_2 over-cladding
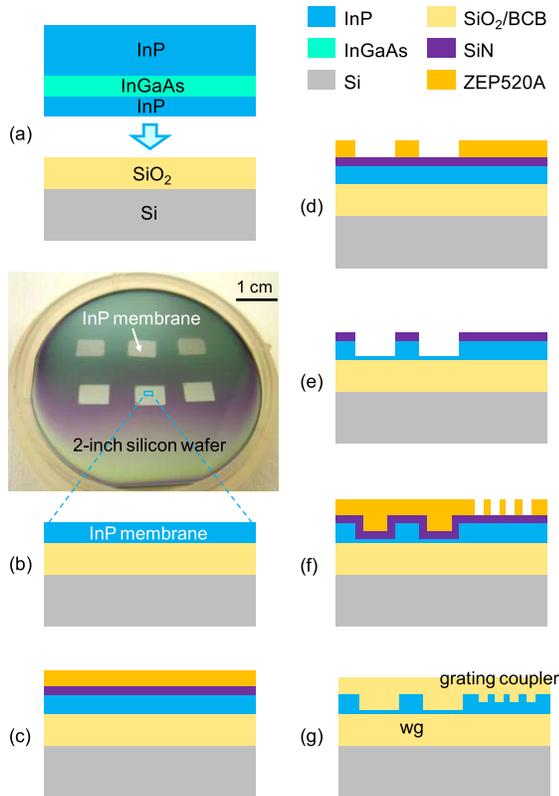
Fig. 2. (a–g) Process-flow used to fabricate the IMOS PCG demultiplexer (wg = waveguide). (b-inset) Photograph of six InP membranes bonded simultaneously on a 2-inch silicon wafer, one of which was used to print the PCG demultiplexer.
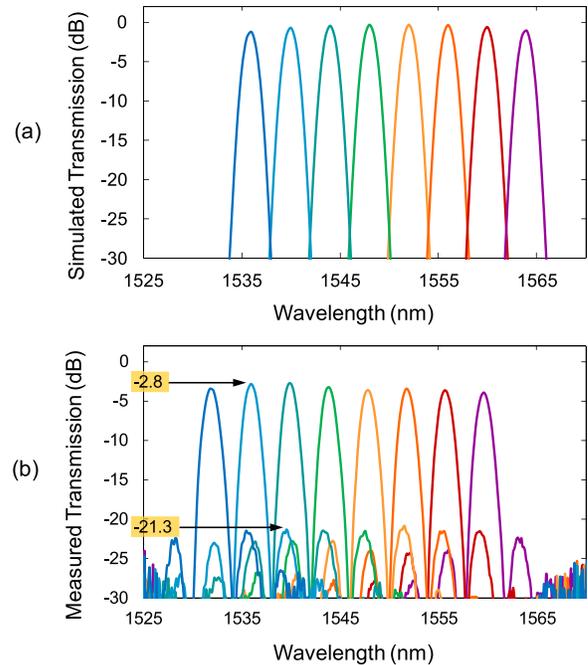

Fig. 3. (a) Designed transmission spectrum of the PCG demultiplexer presented in this letter. (b) Measured transmission spectrum of the fabricated device. (Axes scales in both graphs are identical to facilitate comparison.)
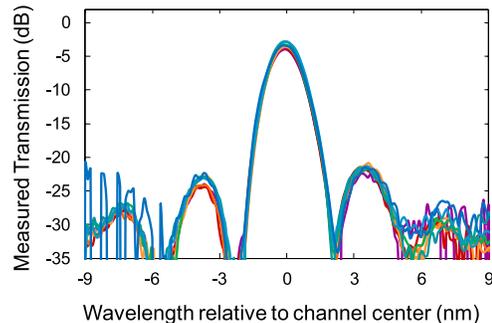

Fig. 4. Superimposed transmission spectra of the fabricated PCG demultiplexer's eight channels, showing a very good overlap and a maximum transmission power non-uniformity of 1.2 dB.

is deposited on the membrane [cf. Fig. 2(g)], to make the membrane more symmetric in the vertical direction, and to reduce the effect of sidewall roughness on waveguide losses [7].

IV. CHARACTERIZATION

In order to assess the performance of the fabricated PCG demultiplexer, the light of an amplified spontaneous emission source covering the C-band (1530 nm to 1565 nm) is fed into the device's input. The spectrum of the light collected by each of the device's output ports is then recorded using an optical spectrum analyzer (OSA), and normalized to the spectrum of a reference waveguide [cf. Fig. 1(a)], fabricated next to the PCG demultiplexer. Fig. 3 shows both the designed (a), and the measured (b) transmission spectra of the device. In the measured spectrum, each channel's central lobe matches very well the predicted Gaussian shape. The channel spacing of the measured device (3.96 nm) is close to the designed value of 4.0 nm. The spectrum is blue-shifted by 4.1 nm with respect to the designed spectrum, and the insertion losses (2.8 dB) are higher than the value predicted in our simulation (0.2 dB). The shift is caused by a deviation of the membrane thickness from the design value [17]. The extra insertion loss arises due to fabrication imperfections in the PCG's DBRs, including trench width variation, roughness, e-beam proximity effects [cf. DBR micrograph in Fig. 1(c)], and to a lesser extent, non-verticality [13]. Furthermore, each channel of

the measured spectrum presents sidelobes on both sides of the central transmission peak, which can best be seen when superimposing the eight output channels of the device, as in Fig. 4. These sidelobes are caused by a degradation of the PCG imaging quality due to phase noise, which has been shown to originate from membrane thickness non-uniformities on the order of 0.05 nm [17], as well as from the DBRs fabrication imperfections described above. However, the transmission level in these sidelobes does not exceed −21.3 dB, meaning that the cross-talk figure for our device is better than −18 dB. Finally, the power non-uniformity between the transmissions of the different channels is below 1.2 dB.

V. CONCLUSION

In this letter, we demonstrate the first PCG demultiplexer fabricated on an InP-based photonic membrane platform.

The device shows 2.8 dB insertion loss, 1.2 dB channel non-uniformity and −18 dB cross-talk. Being realized in an InP membrane, the device is suitable for integration with active devices in InP-based membranes on silicon platforms.

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