III-V/Silicon First Order Distributed Feedback Lasers Integrated on SOI Waveguide Circuits

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Abstract *Heterogeneously integrated III-V-on-silicon first order distributed feedback lasers utilizing an ultra-thin DVS-BCB die-to-wafer bonding process are reported. A novel design exploiting high confinement in the active waveguide is demonstrated. 5 mW output power coupled to a silicon waveguide, 40 dB side mode suppression ratio and continuous wave operation up to 60°C is obtained.*

Introduction

Silicon photonics is clearly becoming an enabling technology for the realization of integrated optical transceivers for optical interconnect applications. The key component that is difficult to realize in this technology however is the laser source. Such a source needs to provide single wavelength emission with milliwatt level optical output power and should be able to operate at elevated temperatures. A monolithically integrated laser would be the ultimate solution, and a substantial body of research is geared towards the implementation of germanium lasers [1]. However, the performance of these sources does not yet match the typical performance of a III-V semiconductor laser diode. Therefore, several research groups focus on the heterogeneous integration of III-V semiconductor layer stacks on silicon waveguide circuits. This can be realized through either molecular wafer bonding or adhesive wafer bonding [2]. Several single-wavelength laser types have been demonstrated in literature, including distributed Bragg reflector lasers [2,3] and distributed feedback lasers [2,4]. These laser structures typically use a hybrid laser waveguide geometry, where the bulk of the optical power is concentrated in the silicon device layer, while the tail of the evanescent mode feels the gain from the multi-quantum well gain region. In this paper we report on distributed feedback lasers integrated on a silicon waveguide circuit, where the bulk of the optical mode is concentrated in the III-V waveguide layer and the mode tail overlaps with the silicon device layer, in which the first order quarter wave shifted Bragg grating is implemented. This gives rise to higher modal gain, but necessitates the use of a spotsize converter to efficiently couple the laser emission to the underlying silicon waveguide circuit.

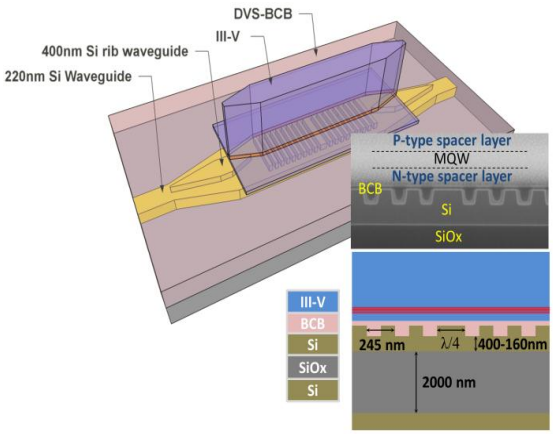

Fig. 1: Schematic of the heterogeneously integrated first order distributed feedback laser presented in this work

Device Design

The device design is schematically depicted in Figure 1, showing the III-V thin film laser mesa bonded onto a silicon waveguide circuit using an adhesive bonding layer (DVS-BCB). The silicon waveguide circuit consists of a 400 nm thick crystalline silicon device layer that is used to define the quarter wave shifted first order distributed feedback grating structures (180 nm deep etch) and to allow realizing an efficient spotsize converter between the III-V device layer and the silicon device layer. After the laser emission is coupled to the 400 nm silicon device layer a second spotsize converter structure is

used to couple to a 220 nm thick device layer thickness, since this device layer thickness is emerging as a standard in different silicon photonics foundry services and allows the implementation of high performance passive and electro-optic functionality. In order to obtain a high efficiency power transfer between the III-V device layer and the silicon waveguide layer, a piecewise linear taper structure was implemented in both layers, where the III-V taper first quickly (L= 35 µm) tapers from the laser mesa width of 3 µm to 0.9 µm, after which a second linear taper of 180 µm long tapers down to a III-V taper tip width of 500 nm. At the same time the silicon waveguide structure underneath tapers from 300 nm to 1000 nm over 180 µm length. The III-V layer stack that is used for the device demonstration consists of a 200 nm thick n-InP contact layer, two 100 nm thick InGaAsP separate confinement heterostructure layers (bandgap wavelength 1.17 µm), 6 InGaAsP quantum wells (6 nm thick, emission wavelength 1.55 µm) surrounded by InGaAsP barriers, a 1.5 µm thick p-InP top cladding and a 100 nm p++ InGaAs contact layer. The confinement factor of the optical mode in the 6 quantum wells is 9.3 %. Since the taper is implemented in the same epitaxial layer stack as the laser mesa it also needs to be electrically pumped in order to prevent excessive absorption in the spot size converter.

Device Fabrication

The silicon device wafer fabrication was carried out in a CMOS pilot line on 200 mm SOI wafers. Three etch steps were used (180 nm deep, 70 nm deep and 220 nm deep) for the definition of the waveguide structures. The 70 nm etch depth is used to define the fiber-to-chip grating coupler structures. After waveguide etching, a SiO2 top cladding was applied, after which chemical mechanical polishing was used to planarize the wafer. The III-V layer stack was bonded onto the silicon device layer using a 100 nm thick DVS-BCB adhesive bonding layer, after which the InP substrate was removed [4]. The laser mesa was defined using i-line contact lithography and wet etching. The required 500 nm III-V taper tip widths were successfully obtained this way. After etching through the multi-quantum well layers, the n-type contacts were defined, the mesa is passivated and p-contact metallization is applied. A scanning electron microscopy picture of the fabricated taper tips is shown in Figure 2.

Device Characterization

First order quarter wave shifted devices with a

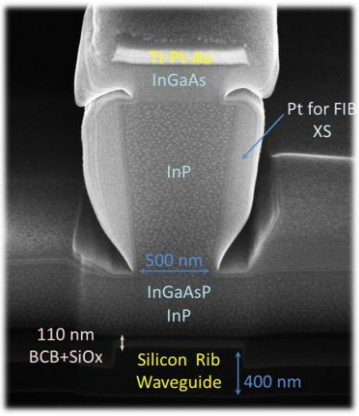

Fig. 2: Scanning electron microscope picture of the III-V semiconductor taper tip realized using i-line lithography and wet etching.

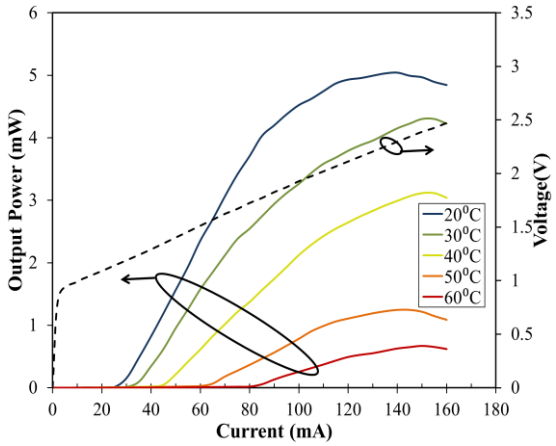

Fig. 3: Laser L-I-V characteristics.

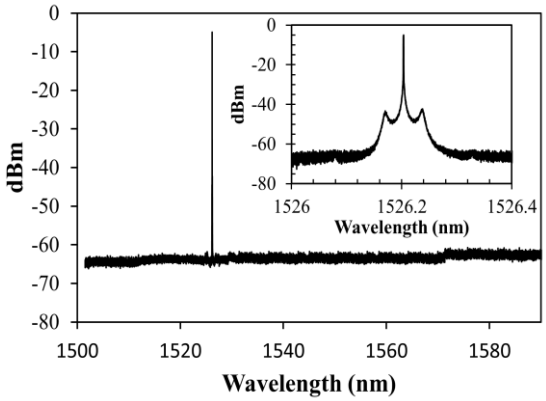

Fig. 4: The laser emission spectrum.

grating period of 245 nm and a total grating length of 600 µm were characterized. For a 100 nm DVS-BCB bonding layer thickness the grating coupling strength is simulated to be 20 cm^{-1}. The laser device characterization was carried out from room temperature up to 60°C. The resulting L-I-V curves are shown in Figure

3, illustrating continuous wave operation up to 60°C and over 5 mW optical output power coupled to the silicon device layer. The laser threshold is 29 mA at room temperature and the external differential efficiency is 0.072 A/W. The series resistance of the laser is 9 Ω. The laser spectrum is shown in Figure 4. More than 40 dB side mode suppression ratio was obtained. The laser linewidth was characterized using a delayed self-heterodyne measurement setup using 22.5km of optical fiber. Typical laser linewidths of 1 MHz are obtained. This shows that these devices have satisfying characteristics to be used in silicon-based transceiver technology.

Conclusions

In this paper we presented first order distributed feedback lasers heterogeneously integrated on a silicon device wafer. While currently the silicon device layer only contains passive optical functionality, one can envisage connecting arrays of such distributed feedback lasers to a bench of silicon optical modulators and wavelength multiplexers to realize a high aggregate bitrate silicon photonics transmitter module.

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