Comparison of Silicon Ring Modulators With Interdigitated and Lateral p-n Junctions

Marianna Pantouvaki, *Member, IEEE*, Hui Yu, Michal Rakowski, Phillip Christie, Peter Verheyen, Guy Lepage, Nele Van Hoovels, Philippe Absil, and Joris Van Campenhout, *Member, IEEE*

***Abstract*—We present a rigorous comparison between Si ring modulators based on interdigitated and lateral p-n junctions. A detailed Si ring modulator model is derived, which is used to fit and benchmark the measured modulation performance of both ring modulators. At 10 Gb/s and 1 $V_{\rm pp}$ drive swing, the interdigitated ring modulator is found to exhibit a superior extinction ratio at low insertion loss as compared to the lateral ring modulator, at the expense of a higher capacitive load. Design improvements are proposed to obtain 25-Gb/s operation with similar extinction ratio and low insertion loss in future devices. Such devices are attractive to enable power-efficient scaling of optical interconnects to 400 Gb/s and beyond.**

***Index Terms*—Optical interconnections, optical transmitters, ring modulators, silicon photonics.**

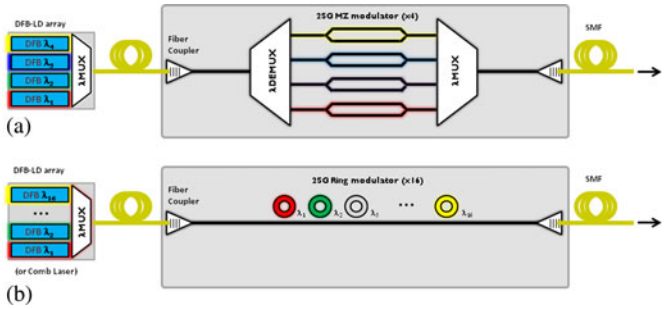

Fig. 1. (a) MZ-based silicon photonics 100G transmitter. (b) Ring-based silicon photonics 400G transmitter.

I. Introduction

THE CONTINUOUS growth of internet traffic is imposing major challenges on system interconnects in high-performance computing systems and data centers, with respect to bandwidth density, power consumption, and cost [1], [2]. Optical interconnects based on single-mode (SM) optics and fibers are increasingly being considered for use in such systems, as the reach and the high bandwidth density of SM-based links may be required for enabling continued scaling of data centers both in terms of capacity and footprint. Several implementations for next-generation, SM-based 100 Gb/s Ethernet optical modules for the short-to-medium range (<2 km) are currently being proposed and evaluated [2]. One implementation comprises the wavelength-division multiplexing (WDM) of four wavelength channels, generated by an array of four distributed-feedback laser diodes and individually modulated at 25 Gb/s using Mach–Zehnder (MZ) modulators, as illustrated in Fig. 1(a). Photonic integration technology will be essential to sufficiently reduce the fabrication cost of these optical modules. Silicon photonics technology is highly attractive in this respect, as the passive optical components such as the fiber couplers and WDM filters, as well as the 25 Gb/s MZ modulators and Ge-based photodetectors can be cost-effectively integrated on a single wafer using existing CMOS infrastructure and integration processes [4], [5].

Further interconnect scaling will be needed beyond the 100 Gb/s optical modules currently under development, eventually targeting 400 Gb/s and 1 Tb/s optical interconnects in the next 5–10 years. Such high-bandwidth electro-optic interfaces will have to operate at power efficiencies on the order of 1 pJ/bit or better, combined with a high number of WDM channels (e.g., 16 or more), each modulated at 25 Gb/s or higher. Obtaining these power efficiencies will require ultimate device optimization along the full optical link to reduce the overall WDM link energy budget and optical loss [6]. By minimizing the insertion loss (IL) of each optical component as well as the overall power penalty (PP) across the link, the required laser power for operation can be reduced, thereby reducing overall link power consumption.

At the transmitter side, modulators operating at 25 Gb/s and above should be designed with maximum extinction ratio (ER) and lowest IL, using CMOS compatible voltages of preferably 1 V peak-to-peak ($V_{\rm pp}$), in order to reduce driver circuit complexity while staying within the energy budget of substantially less than 1 pJ/bit. Silicon ring modulators have demonstrated high-frequency operation at voltages <2 V, while at the same time having a smaller footprint and smaller dynamic power consumption as compared to MZ modulators [7], [8]. In addition, ring modulators can be cascaded along the same bus waveguide for modulation of different wavelengths in a WDM system, without the need for additional WDM multiplexers and demultiplexers, as illustrated in Fig. 1(b). This can further reduce the link footprint, IL and thus overall power consumption. Obviously, these benefits will only be obtained provided that the thermal stability of the rings can be guaranteed, which

Manuscript received June 1, 2012; revised August 31, 2012; accepted October 23, 2012. Date of publication November 20, 2012; date of current version April 3, 2013. This work was supported by Interuniversity Microelectronics Centre's Core Partner Program.

M. Pantouvaki, M. Rakowski, P. Christie, P. Verheyen, G. Lepage, N. Van Hoovels, P. Absil, and J. Van Campenhout are with the Interuniversity Microelectronics Centre (imec), Kapeldreef 75, Leuven 3000, Belgium. M. Rakowski is also with the Catholic University Leuven, Leuven 3000, Belgium (e-mail: pantouvm@imec.be; rakowski@imec.be; christie@imec.be; verheyen@imec.be, lepage@imec.be; vhoovels@imec.be; absilp@imec.be; jvcampen@imec.be).

H. Yu is with the Photonics Research Group, Department of Information Technology and Center for Nano- and Biophotonics, Ghent University, 9000 Ghent, Belgium (e-mail: hyu@intec.ugent.be).

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Digital Object Identifier 10.1109/JSTQE.2012.2228169

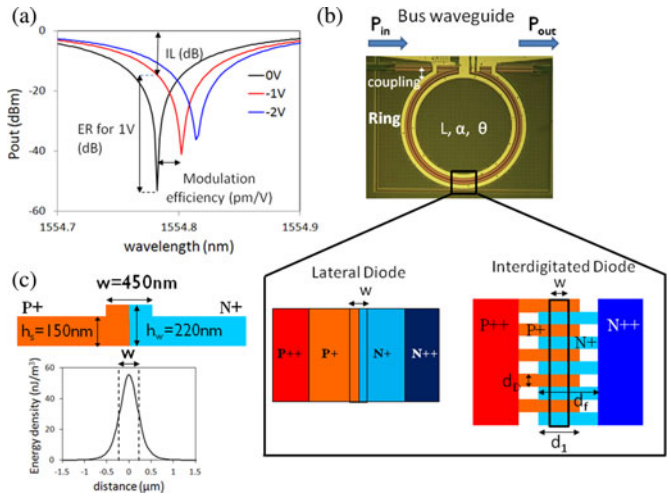

Fig. 2. (a) Typical transmission spectra of carrier depletion ring modulator for different applied bias. The ER, IL, and ME are indicated for 1 $V_{\rm pp}$. (b) Ring modulator schematic showing the lateral and interdigitated diode designs. (c) Ring waveguide cross section and mode distribution.

will require the implementation of power-efficient thermal control circuits [9].

Silicon ring modulators are typically using carrier injection in p-i-n diodes or carrier depletion in p-n diodes. Carrier depletion modulators combine low fabrication complexity and high speed, but they may suffer from weak modulation efficiency (ME), which results in low ER and high IL when driven with 1 $V_{\rm pp}$ swing. In order to improve the ME of carrier depletion modulators, the interdigitated diode design was recently theoretically proposed [10], [11]. By periodically exchanging p- and n-doped regions perpendicular to the waveguide, the overlap of the optical mode with the depletion region is increased, producing larger refractive index changes. Although interdigitated p-n junctions were recently demonstrated in both MZ and ring modulators [12]–[15], the direct comparison of their performance to lateral p-n junctions is still limited. In this paper, we present a detailed comparison of both diode implementations for ring modulators on the same fabrication platform. A comprehensive ring modulator model is presented in Section II, followed by extensive device characterization at 10 Gb/s in Section III. The results are subsequently fitted using the ring modulator model, and discussed in Section IV. Based on the calibrated device model, design improvements are suggested to enable modulators with similar performance at 25 Gb/s. Finally, conclusions are summarized in Section V.

II. Device Model

Fig. 2(a) shows an example of the transmission spectrum of carrier depletion ring modulators and its variation with applied voltage. Typical figures of merit that are used to describe the modulator response at system level are the extinction ratio (ER), insertion loss (IL), bit-rate (BR) and energy per bit ($E_{\rm bit}$). The extinction ratio for a given operating voltage change is the ratio ER $= P_1/P_0$ where P_1 and P_0 are the power levels when transmitting a 1 bit and a 0 bit, respectively, while the insertion loss is the loss introduced for a 1-bit. A schematic showing the ER and IL for 1 $V_{\rm pp}$ swing at the resonance wavelength is shown in Fig. 2(a). The maximum obtainable bit-rate is related to the 3-dB modulator frequency response $(f_{\rm 3dB})$, which is used to describe the modulator's high frequency limit. The frequency response can be related to the maximum obtainable bit-rate approximately as $f_{\rm 3dB} \approx 2{\rm BR}/3$. Finally, the power consumption of a modulator transmitting a nonreturn-to-zero bit sequence is described by the energy per bit, defined as [16]

$$E_{\rm bit} = C_d V_{\rm pp}^2/4 \tag{1}$$

where C_d is the junction capacitance and $V_{\rm pp}$ is the peak-to-peak voltage swing.

All of the aforementioned performance metrics have to be considered for a fair comparison of different modulator designs. They are defined by a set of physical parameters that describe the devices. For example, the extinction at resonance and the ring quality factor $(Q = \lambda_r/\delta\lambda)$ depend on the ring geometry, the loss in the ring, and whether or not the ring is critically coupled to the bus waveguide: the modulation efficiency, defined as the resonance wavelength shift per voltage [see Fig. 2(a)], depends on the p- and n-doping of the ring and on the diode design, while the modulation speed $(f_{\rm 3dB})$ is defined by the device capacitance, series resistance, and the Q-factor.

The diode designs considered here are shown in Fig. 2(b). The lateral diode design has a p-n junction parallel to the waveguide. The ring circumference is $L = 2\pi R$, where R is the ring radius. The height and length of the depletion capacitor in the lateral case are equal to the waveguide height h_w and to the ring circumference L, respectively. The interdigitated diode design has multiple p- and n-doped areas alternated perpendicular to the waveguide, comprising multiple p-n junctions along the ring. Here, the width of the p- and n-doped fingers (d_D) is chosen to be equal, d_f is the length of the p- and n-doped fingers, and d_1 is the p-n junction interaction length. If d_1 is larger than the waveguide width, the depletion capacitor of one p-n junction consists of three parallel capacitors: the waveguide core capacitor of height h_w and width equal to the waveguide width (w), and two slab capacitors of height equal to the slab height h_s and width $w_s = \frac{d_1 - w}{2}$ each. All of these components are taken into account here for calculation of the interdigitated ring capacitance.

The output spectrum of a ring modulator can be modeled by combining 1) transmission matrix equations to describe the coupling between the ring and the waveguide and the transmission through the bus waveguide and the ring, 2) p-n diode physics to describe depletion carrier changes, and 3) a confinement factor to account for the fraction of the optical mode that experiences the refractive index changes in the depletion region.

The transmitted power at the output of the bus waveguide in the absence of a drop port is given by [17]

$$P_{\rm out} = \frac{|t|^2 + \alpha^2 - 2\alpha|t|\cos(\theta + \varphi)}{1 + \alpha^2|t|^2 - 2\alpha|t|\cos(\theta + \varphi)} \tag{2}$$

where $t = |t|\exp(i\varphi)$ is the amplitude transmission through the bus waveguide with phase shift φ, $\alpha = \exp(-a_r L)$ is the ring round-trip loss, α_r is the modal propagation loss, L is the ring circumference, $\theta = \frac{2\pi n_{\rm eff} L}{\lambda}$ is the round-trip phase shift, and $n_{\rm eff}$ is the effective index of the ring waveguide.

In the presence of doping in the ring, changes in the effective index and absorption due to a change in applied voltage ΔV

can be described as

$$n_{\text{eff}} = n_{\text{eff}}^0 + \Delta \text{n}_{\text{eff}}(\Delta V) \tag{3}$$

$$\alpha_r = a_r^0 + \Delta\alpha_r(\Delta V) \tag{4}$$

where n_{eff}^0 and α_r^0 are, respectively, the effective index and absorption at the bias voltage of interest V_0. The modal changes Δn_{eff} and $\Delta\alpha_r$ can be related to the silicon refractive index (Δn_c) and absorption $(\Delta\alpha_c)$ changes via the confinement factor $\Gamma_{\Delta A}$ [18]

$$\Delta n_{\text{eff}}(\Delta V) = \Gamma_A(\Delta V)\Delta n_c = \frac{n_g}{n_{\text{Si}}}\gamma_{\Delta A}(\Delta V)\Delta n_c \tag{5}$$

$$\Delta\alpha_r(\Delta V) = \Gamma_{\Delta A}(\Delta V)\Delta a_c = \frac{n_g}{n_{\text{Si}}}\gamma_{\Delta A}(\Delta V)\Delta\alpha_c \tag{6}$$

where n_g is the group index, n_{Si} is the refractive index of silicon, and $\gamma_{\Delta A}$ represents the energy density confined in the differential depletion area $\Delta A(\Delta V)$

$$\gamma_{\Delta A}(\Delta V) = \frac{\iint_{\Delta A}\varepsilon|E|^2 dxdy}{\iint_{\infty}\varepsilon|E|^2 dxdy}. \tag{7}$$

It is well known that Δn_c and $\Delta\alpha_c$ have a power law dependence on changes of the electron (ΔN_e) and hole (ΔN_h) concentrations [19]

$$\Delta n_c = -1.62\times 10^{-28}\Delta N_e^{1.03} - 8.07\times 10^{-23}\Delta N_h^{0.81} \tag{8}$$

$$\Delta a_c = 6.77\times 10^{-27}\Delta N_e^{1.21} + 8.83\times 10^{-25}\Delta N_h^{1.11}. \tag{9}$$

In a symmetric p-n diode with acceptor concentration N_A equal to the donor concentration N_D, the change in free carrier concentration is $\Delta N = N_A = N_D = N_{\text{dop}}$, assuming full depletion. In that case we can define parameters f_N and a_N to combine the electron and hole contributions to the effective index and absorption changes within a linear approximation

$$\Delta n_c = f_N N_{\text{dop}} \tag{10}$$

$$\Delta a_c = a_N N_{\text{dop}}. \tag{11}$$

Equations (5) and (6) can now be written as

$$\Delta n_{\text{eff}}(\Delta V) = \frac{n_g}{n_{\text{Si}}}\gamma_{\Delta A}(\Delta V) f_N N_{\text{dop}} \tag{12}$$

$$\Delta a_r(\Delta V) = \frac{n_g}{n_{\text{Si}}}\gamma_{\Delta A}(\Delta V) a_N N_{\text{dop}}. \tag{13}$$

The change in depletion charge per unit length ΔQ is related to the change in depletion area ΔA according to

$$\Delta Q = qN_{\text{dop}}\Delta A = C_d\Delta V \tag{14}$$

where q is the electron charge and C_d is the depletion capacitance per unit length at bias voltage V_0. For the calculation of the depletion capacitance, the p-n junction is treated as a graded junction. The depletion capacitance is therefore given by [20]

$$C_d(V) = \frac{C_{j0}}{\left(1-\frac{V}{V_{bi}}\right)^m} \tag{15}$$

where $C_{j0} = \frac{\sqrt{q\varepsilon_{\text{Si}}N_A N_D}}{\sqrt{2(N_A+N_D)(V_{bi}-(k_B T/q))}}$ is the depletion capacitance per meter at zero bias, V_{bi} is the junction built-in voltage, ε_{Si} is the permittivity of silicon, and k_B is Boltzmann's constant. Typically, the grading factor m is 0.5 for an abrupt junction and 0.33 for a linearly graded junction. The modulation of the effective index and absorption coefficient can then be calculated from (12)–(15) as

$$\Delta n_{\text{eff}}(V) = \frac{n_g f_N}{qn_{\text{Si}}}\frac{\gamma_{\Delta A}}{\Delta A}C_d\Delta V \tag{16}$$

$$\Delta a_r(V) = \frac{n_g \alpha_N}{qn_{\text{Si}}}\frac{\gamma_{\Delta A}}{\Delta A}C_d\Delta V. \tag{17}$$

The modulation efficiency can then be estimated by

$$\text{ME} = \frac{\Delta\lambda}{\Delta V} = \frac{\lambda}{n_{\text{Si}}}\frac{\gamma_{\Delta A}}{\Delta A}\frac{f_N}{q}C_d(V). \tag{18}$$

Similarly, an expression can be derived for estimating the absorption at bias voltage $\alpha_r^0 = \Gamma_{\text{Si}}\alpha_N N_{\text{dop}}$, where Γ_{Si} is the confinement factor of the entire silicon waveguide.

Equation (18) shows that increasing the p-n junction capacitance can help increase the modulation efficiency, provided that the differential depletion area ΔA is implemented near the peak of optical energy density (high $\gamma_{\Delta A}$). This can be done by increasing the doping concentration N_{dop}. However, higher doping concentration will also result in higher modal propagation loss α_r^0, which will impose a limit on the maximum obtainable Q-factor, and as such on the ER and IL. Alternatively, the modulation efficiency can be enhanced by increasing the total depletion area ΔA within the optical field, which is pursued by the interdigitated diode design.

In addition, higher junction capacitance will affect the dynamic performance of the ring modulator. The frequency response of ring modulators depends on the cavity photon lifetime and the *RC* time constant and can be approximated by

$$\frac{1}{f_{3\text{dB}}^2} = \frac{1}{f_Q^2} + \frac{1}{f_{RC}^2} \tag{19}$$

where $f_Q = \frac{1}{2\pi\tau}$ is the frequency limitation due to cavity photon lifetime (τ) and $f_{RC} = \frac{1}{2\pi RC}$ is the *RC* frequency response of the modulator. The cavity photon lifetime depends on the Q-factor of the ring and is expressed as $\tau = \frac{Q\lambda}{2\pi c}$, where λ is the operating wavelength and c is the speed of light in vacuum. Consequently, a tradeoff exists between modulation efficiency and modulator speed.

III. Experimental Results

A. Device Fabrication

Modulators with lateral and interdigitated diode designs were fabricated on 200 mm silicon-on-insulator wafers consisting of 220 nm crystalline silicon and 2 um buried oxide. The 450 nm wide ring waveguides were defined by 193 nm lithography and etching 70 nm of silicon. This shallow etch allowed for the fabrication of the ring modulators during the same patterning steps as the fiber couplers, but it imposed a limit to the minimum size of the rings that was possible without significant waveguide bending loss. Here, a ring radius of 40 μm was used. After patterning the rings, the bus waveguides were defined $\sim$570 nm away from the rings. This was followed by p- and n-doping of the rings using boron and phosphorus implants, respectively, and targeting $\sim 2\times 10^{18}$ cm^{-3} peak concentrations at $\sim$110 nm depth into the waveguide. 248 nm lithography was used to form the desired

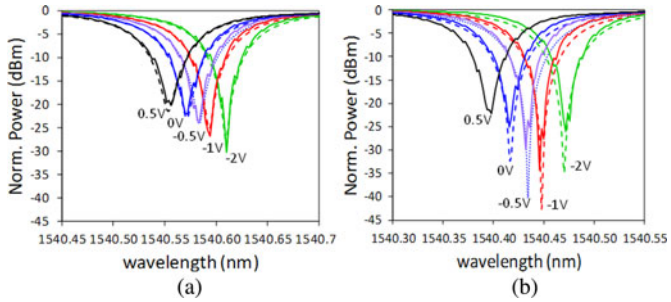

Fig. 3. Normalized transmitted power of ring modulators with (a) lateral and (b) interdigitated diode designs for voltages from 0.5 to −2 V. The dashed lines show the fitted spectra.

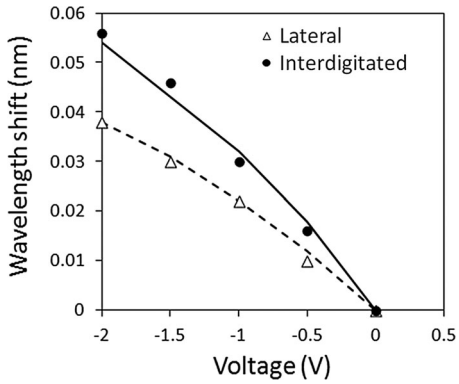

Fig. 4. Resonance wavelength shift versus voltage for interdigitated and lateral diode designs. The symbols are experimental data, while the lines show the modeled results.

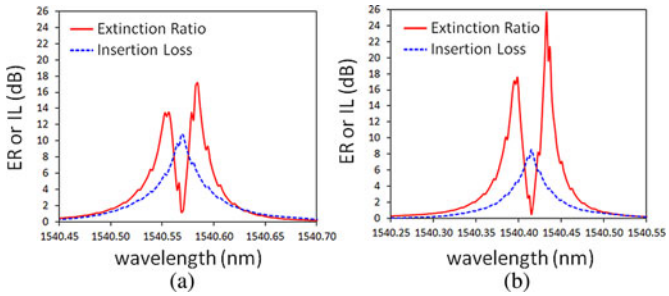

Fig. 5. Experimental ER and IL for (a) lateral and (b) interdigitated ring modulators for 1 $V_{\rm pp}$ voltage swing with 0 V bias.

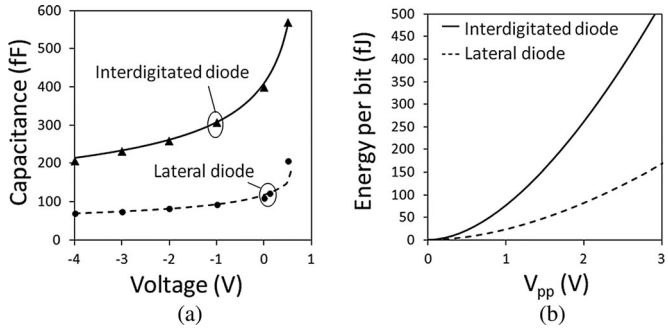

Fig. 6. (a) Capacitance–voltage measurements (symbols) and fitting (lines), and (b) energy per bit versus peak-to-peak voltage ($V_{\rm pp}$) for lateral and interdigitated diode designs.

implantation patterns. For the lateral diode design, the p- and n-doped regions were formed parallel to the waveguide, with the p-n junction region centered in the waveguide. For the interdigitated diode design, the p- and n-doped regions were alternated perpendicular to the waveguide with finger widths $d_{\rm D} = 300$ nm each. The length of the interaction region d_1 of the p-n junction was fixed to 1.8 μm to fully cover the guided optical mode [see Fig. 2(c)], while the length of the fingers was $d_{\rm f} = 3$ μm. P- and n-implants at 10^{20} cm^{-3} concentrations were placed 2 um away from the waveguide center to form the ohmic contacts. After an activation anneal at ∼1000 °C, the highly doped regions were silicided and contacted via standard CMOS 130 nm technology tungsten contacts. Finally, connections to the pads were formed by standard copper damascene processing.

B. Static Performance

Fig. 3 shows the normalized transmission spectra of ring modulators with lateral and interdigitated diode designs for applied voltages from −2 to 0.5 V. The total insertion loss off-resonance was <0.2 dB for both rings, while the back-to-back loss including fiber couplers and bus waveguide loss was 9 dB. The Q-factors of the rings, calculated from experimental data, were ∼15100 for the lateral and ∼16000 for the interdigitated diode design at 0 V bias. Both rings were close to critical coupling. The transmission spectra were fitted with the model presented in the previous section and the results are also shown in Fig. 3. The model resulted in power coupling coefficients 0.12 and 0.13 for the lateral and interdigitated diode designs, respectively. Similarly, the ring propagation loss was found to be 25.1 and 25.4 dB/cm for the lateral and interdigitated design, respectively, which is close to the value predicted by the model (24 dB/cm).

The resonance wavelength shift is plotted versus voltage in Fig. 4. Higher modulation efficiency is observed for the interdigitated diode design as compared to the lateral diode design. In particular, for a voltage swing from 0 to −1 V, the ME of the interdigitated diode design is 30 pm/V as opposed to 22 pm/V for the lateral diode design.

A more quantitative comparison of the two diode designs is shown in Fig. 5, where the static ER and IL are plotted for 1 $V_{\rm pp}$ swing. The maximum ER of the lateral diode design is 17.2 dB, corresponding to 6 dB IL. For the interdigitated diode design, the maximum ER of 25.7 dB corresponds to only 4 dB IL. Comparing the two designs at the same IL of 3 dB, the ERs are 4.7 and 12.7 dB for the lateral and interdigitated modulators, respectively.

Low-frequency capacitance–voltage measurements were performed at 100 kHz. Fig. 6(a) shows the experimental results, together with the capacitance values resulting from the fitting of Fig. 3. The interdigitated diode design results systematically in higher diode capacitance, as expected from the theory. The concept that led to this design is to induce larger refractive index changes by increasing the overlap of the optical mode with the depletion area, at the expense of higher depletion capacitance. A best fit to both the ring spectra of Fig. 3 and the ring capacitance–voltage curves of Fig. 6 resulted in grading factors of $m = 0.33$ for the lateral and $m = 0.38$ for the interdigitated diode design. Fig. 6(b) shows an approximation of the energy

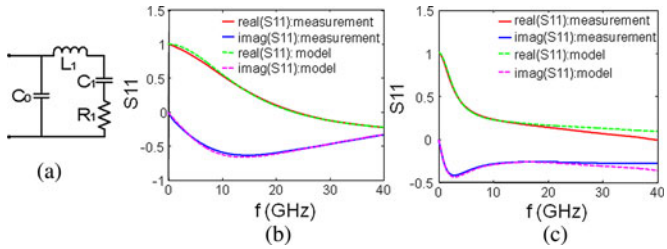

Fig. 7. (a) Circuit model and $S11$ measurements from ring modulators with (b) lateral and (c) interdigitated diode designs. The fitting to the measured data is shown by the dashed lines.

TABLE I
CIRCUIT MODEL PARAMETERS CALCULATED FROM FITTING TO EXPERIMENTAL $S11$ DATA

Diode design	C_0 (fF)	L_1 (pH)	R_1 (Ohm)	C_1 (fF)
Lateral	10	36	29	137
Interdigitated	40	19	76	450

per bit for the two diode designs, using the modeled capacitance of Fig. 6(a). The better ER and lower IL of the interdigitated diode design comes at the expense of higher energy per bit.

C. High-Speed Characterization

The small-signal high frequency response of the modulators can be studied by measuring the $S11$ and $S21$ parameters of the ring modulators. The $S11$ parameters were measured at 0 V bias in the frequency range from 100 MHz to 40 GHz. The results were fitted using the circuit model shown in Fig. 7(a), where C_0 is the pad capacitance, while R_1, C_1, and L_1 model the series resistance, capacitance, and inductance of the p-n diode, respectively. The inductance L_1 was included in the circuit model due to the relatively large size of these ring modulators. The $S11$ measurements together with the fitting are shown in Fig. 7. The extracted parameters for the circuit model can be found in Table I. The diode capacitance C_1 is more than three times higher for the interdigitated diode design as compared to the lateral design, in agreement with the low-frequency capacitance measurements of Fig. 6. The RF diode resistance R_1 is also higher for the interdigitated diode, indicating that device optimization should be done to avoid high frequency limitation due to this parameter.

In order to determine the electro-optical frequency response of the modulators, the $S21$ parameters were measured at 0 V using a network analyzer. Fig. 8 shows the results of these measurements. Frequency response 12.9 GHz and 4.9 GHz were measured for the lateral and interdigitated modulators, respectively.

Equation (19) can be used to determine which factor is predominantly affecting the frequency response of the devices. Table II shows the expected f_{RC} (assuming a 50 Ω driver impedance) and f_Q based on the experimental data from the lateral and interdigitated diode designs. While the lateral ring modulator is limited by both the cavity photon lifetime and the *RC* response, the interdigitated ring is dominantly limited by its *RC* response. To enable operation of the interdigitated modulator at high speed (>10 Gb/s), the *RC* time constant has to be reduced.

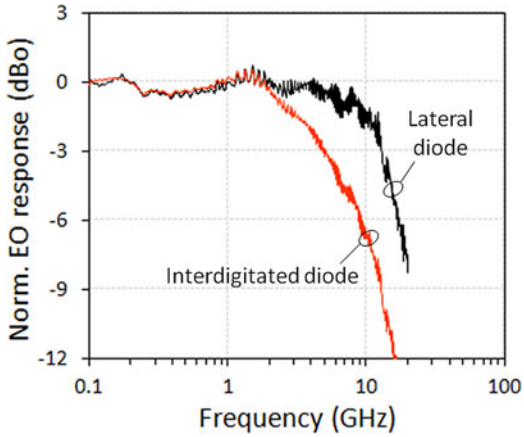

Fig. 8. Electro-optical $S21$ frequency response of ring modulators with lateral and interdigitated diode designs at 0 V bias.

TABLE II
FREQUENCY RESPONSE ANALYSIS

Diode design	f_Q (GHz)	f_{RC} (GHz)	$f_{3dB,exp}$ (GHz) (S21 measurement)
Lateral	13	14.8	12.9
Interdigitated	12.1	2.8	4.9

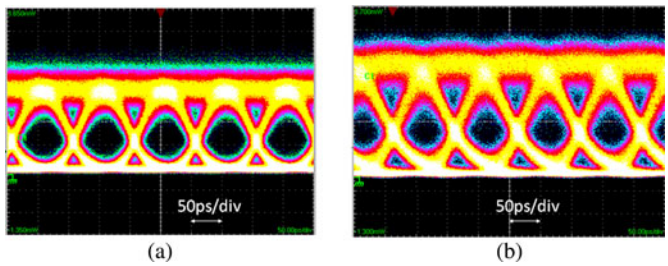

Fig. 9. Eye diagrams of (a) lateral and (b) interdigitated modulators at 10 Gb/s.

Large-signal high-frequency measurements were performed at 10 Gb/s to study the high-speed modulation performance of the lateral and interdigitated ring modulators. Measurements of the eye diagrams were done at 10 Gb/s using a nonreturn-to-zero pseudorandom bit sequence of $2^{15}-1$. The voltage was set to 1 and 0.7 $V_{\rm pp}$ for the lateral and interdigitated rings, respectively, at the output of the pulse pattern generator and it was applied on the devices via a high-speed unterminated ground-signal-ground probe. The dc bias was set to -1 V for both modulators, while the laser wavelength was set to give maximum ER in each case. After passing the modulator, the signal goes through an erbium-doped fiber amplifier (EDFA) and an optical filter of 0.6-nm 3-dB bandwidth, before being monitored by a 20 GHz optical oscilloscope. The EDFA gain is adjusted to give ~0 dBm on the oscilloscope. Fig. 9 shows the 10 Gb/s eye diagrams from the ring modulators with lateral and interdigitated diode designs. The eye diagram of the interdigitated modulator is suffering from horizontal eye closure due to the *RC* limitation of this device. However, it was possible to compare the dynamic ERs

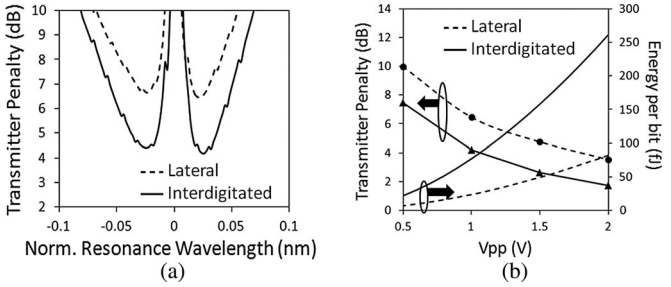

Fig. 10. (a) Expected transmitter penalty versus wavelength for lateral and interdigitated diode designs, calculated for 1 $V_{\rm pp}$ swing. (a) Transmitter penalty and energy per bit versus $V_{\rm pp}$ for lateral (dashed lines) and interdigitated (solid lines) diode designs.

of the two designs. ERs of 11.2 and 10.2 dB were measured at 10 Gb/s for the lateral and interdigitated modulators, respectively.

IV. Discussion

The experimental comparison of the interdigitated versus lateral diode design has shown that the interdigitated design can improve the modulation efficiency and extinction ratio of the rings, and lower the insertion loss, at the expense of higher capacitance. The higher capacitance corresponds to higher energy/bit consumption on the modulator and lower frequency response. Based on the estimated high-frequency capacitance (see Table I), and assuming modulation with 1 $V_{\rm pp}$ signal, the lateral and interdigitated diode designs require energies of $\sim$35 and $\sim$113 fJ/bit respectively.

Another figure of merit that is often used for link comparison is the power penalty (PP). The power penalty of a modulator with ER is defined as [21]

$$\mathrm{PP(dB)} = 10\log\left(\frac{\mathrm{ER}+1}{\mathrm{ER}-1}\right). \tag{20}$$

We can define the transmitter penalty (TP) as

$$\mathrm{TP} = \mathrm{IL} + \mathrm{PP}. \tag{21}$$

Fig. 10(a) shows a comparison of the TP introduced by the lateral and interdigitated diode designs, centered at the wavelength of minimum ER and maximum IL. The TP in Fig. 10(a) is calculated for 1 $V_{\rm pp}$ swing (from 0 to -1 V). It is shown that the interdigitated diode design can reduce the TP by $\sim$2.5 dB as compared to the lateral diode. The TP and energy per bit are plotted versus $V_{\rm pp}$ in Fig. 10(b). At 1 $V_{\rm pp}$, there is $\sim$55 fJ/bit additional energy penalty when using the interdigitated diode design, which corresponds to -2.6 dBm additional modulator power needed at 10 Gb/s. Both the reduction in TP and the increase in energy per bit should be included in a full-link analysis with interdigitated modulators. However, the existing interdigitated diode design is not optimized—improvements can reduce the modulator capacitance with small impact on other parameters, as shown in the following.

The results from the diode design comparison are summarized in Table III. In order to take advantage of the better extinction ratio and insertion loss of the interdigitated modulator, the design of this device should be optimized for minimum *RC* limitation in the frequency response.

First, we will consider the performance improvements that are possible in the interdigitated design of Fig. 2(b) without changing the waveguide geometry or the doping of the ring. In the present design, the length of the p-n interaction region d_1 per junction was 1.8 μm to fully cover the guided optical mode. However, from Fig. 2(c), it is observed that most of the optical mode is confined in the waveguide region. Since reducing the interaction region would reduce the capacitance, it is interesting to know what the impact of this would be to the modulation efficiency. Fig. 11 shows the simulated capacitance and modulation efficiency when the finger length d_1 is gradually reduced from 1.8 to 0.45 μm, which is the width of the ring waveguide. It is observed that while the modulation efficiency is reduced by only $\sim$2 pm/V, the junction capacitance is more than halved, to $\sim$170 fF. The nonlinear dependence of the modulation efficiency on d_1 is due to the dependence of the confinement factor on d_1 [see (18)]. Using the high-frequency resistance of Table I for the interdigitated diode design, it is found that for $d_1 = 0.45$ μm, the *RC* frequency bandwidth becomes $f_{\rm RC} =$ 7.2 GHz. For the same f_Q, this results to $f_{\rm 3db} = 6.2$ GHz.

TABLE III
Comparison of Measured Performance Metrics for Lateral and Interdigitated Modulators

Diode design	Max ER (dB)	IL at max ER (dB)	$f_{3dB,exp}$ (GHz)	E_{bit} (fJ/bit)	Min TP (dB)
Lateral	17.2	6	12.9	35	6.5
Interdigitated	25.7	4	4.9	113	4.2

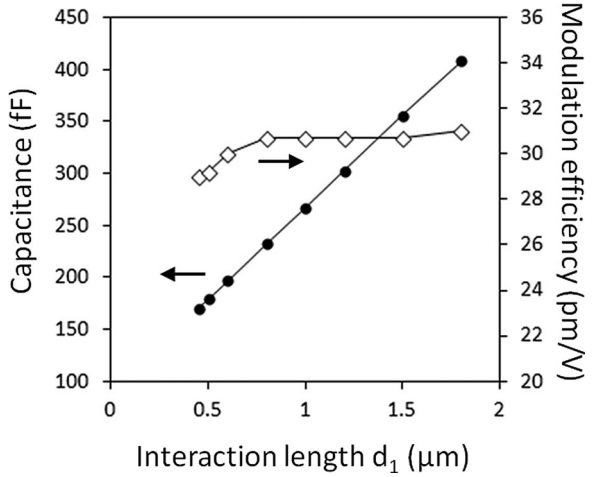

Fig. 11. Calculated junction capacitance and ME versus interaction length d_1.

Another drawback of the interdigitated design of Fig. 1(b) is the high series resistance compared to the lateral design (see Table I). This is because the current has to pass through 3-μm-long fingers of 300-nm width. If the interaction length is reduced to the waveguide region, the length of the fingers could also be reduced, bringing the highly doped contact areas closer to the waveguide and therefore reducing the series resistance (see, for example, [14]). A tradeoff exists between reducing the series resistance and increasing the waveguide loss when bringing the highly doped areas closer to the waveguide. However, series resistance values close to those for the lateral modulator should be possible. This would boost further the *RC* frequency bandwidth to $f_{\rm RC} = 11.6$ GHz and the device bandwidth to $f_{\rm 3dB} =$ 8.4 GHz. It is expected that this improved interdigitated device design would enable 12.5 Gb/s operation, while maintaining the

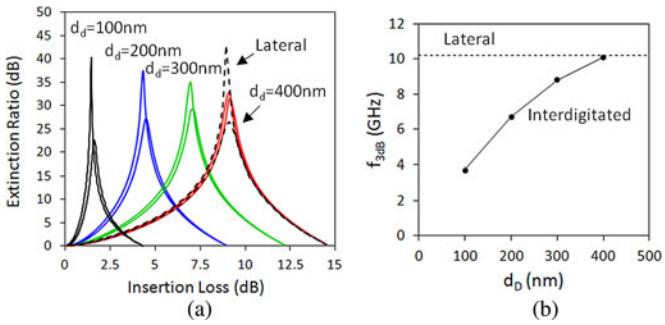

Fig. 12. (a) Calculated ER versus corresponding IL and (b) frequency response of interdigitated modulators, with variable finger width d_d.

high extinction ratio and low insertion loss of the interdigitated diode modulator.

To further explore the opportunities and limitations of the interdigitated design, we simulated the performance for variable finger width $d_{\rm d}$, from 100 to 400 nm. When varying $d_{\rm d}$, the total depletion area in the interdigitated modulator is changing, therefore affecting the modulation efficiency and frequency bandwidth of the device. The simulations were performed for finger interaction length $d_{\rm f} = 0.45$ μm and assuming almost critical coupling in all cases, yielding a Q-factor of $\sim$14000 in all cases. The results for 1 $V_{\rm pp}$ swing are shown in Fig. 12. A critically coupled lateral modulator reference is also shown for comparison. In Fig. 12(a), the extinction ratio is plotted versus insertion loss for different doping widths. In this plot, the performance is improving when the peak extinction ratio is moving to the left, toward lower insertion loss. Clearly, by reducing the finger width, the IL of the interdigitated modulators can be reduced significantly. The frequency response versus finger width is plotted in Fig. 12(b). The performance of the interdigitated modulator is matching the lateral design for a finger width of 400 nm, both in terms of ER/IL and of frequency response. When reducing the finger width below 400 nm, lower IL can be achieved at the expense of higher capacitance and lower frequency response. The higher capacitance that is responsible for this slow response will affect also the energy consumption of the device.

Finally, further improvement of the interdigitated modulator frequency response is possible if the ring radius is reduced and other parameters are optimized as follows: assuming that the slab height is reduced to 70 nm, a reduced ring radius of 10 μm would be possible. Keeping the finger width to 300 nm but doubling the doping concentration would increase the ring round-trip loss and reduce the Q-factor to 8000, resulting in $f_Q \sim 23$ GHz. Higher doping concentration combined with near-critical coupling would enable high ME ($\sim$60 pm/V). The smaller ring radius would result in $\sim$60 fF depletion capacitance with $\sim$4 dB TP at 1 $V_{\rm pp}$. If the series resistivity is maintained to the value measured experimentally on the lateral modulator ($\sim$7 Ω·mm), the resulting $f_{\rm RC}$ would be 15.3 GHz and $f_{\rm 3dB}$ $\sim$ 12.8 GHz, enabling operation of the interdigitated modulation at $\sim$20 Gb/s. However, the higher doping would reduce the series resistance. Operation at 25 Gb/s will be possible if the series resistance is reduced below $\sim$3.5 Ω·mm.

V. Conclusion

A detailed model based on the physical parameters determining the behavior of ring modulators with lateral and interdigitated diode designs has been presented. The model was used to fit and interpret static and dynamic measurements at 10 Gb/s on both diode designs. The interdigitated design exhibits higher extinction ratio at lower insertion loss, resulting in a reduction of the expected transmitter penalty by about 2.5 dB. Design optimizations were proposed to enable operation at >20 Gb/s and reduce energy per bit, while maintaining low transmitter penalty.

Acknowledgment

The authors would like to thank the efforts of Interuniversity Microelectronics Centre's 200-mm pline for their contributions to the device fabrication.

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Marianna Pantouvaki (S'99–M'03) received the Ph.D. degree in electronic and electrical Engineering from University College London, London, U.K., in 2004.

From 2003 to 2006, she was a Research Fellow in the Ultra-Fast Photonics Group, University College London, and a Visiting Researcher at the Centre for Integrated Photonics, Ipswich, U.K. In 2006, she joined Interuniversity Microelectronics Centre (IMEC), Leuven, Belgium, where she was involved in research on advanced Cu/low-k back end of line interconnects until 2010. In 2011, she joined the Silicon Photonics Group, IMEC, where she is currently involved in the development of high-speed transmitters for optical interconnects.

Hui Yu received the B.Sc. and Ph.D. degrees in electrical engineering from Zhejiang University, Hangzhou, China, in 2003 and 2008, respectively.

He is currently a Postdoctoral Researcher with the Department of Information Technology, Ghent University, Ghent, Belgium, where he is also with the Center for Nano- and Biophotonics. His research interests include the modeling, design, and fabrication of silicon active devices.

Michal Rakowski received the M.Sc. degree in electronic engineering from the Warsaw University of Technology, Warsaw, Poland, in 2006. Since 2011, he has been working toward the Ph.D. degree at the Catholic University Leuven, Leuven, Belgium.

In 2006, he was with the VLSI Engineering and Design Automation Division, Institute of Microelectronics and Optoelectronics, Warsaw University of Technology. In 2008, he joined Interuniversity Microelectronics Centre, Leuven, Belgium, where he was with Process Quality and Integration Group, working on electrical data analyzes and circuit measurements. His main research focus is on modeling optoelectronic devices and CMOS circuit designs for optical interconnect applications.

Phillip Christie received the Ph.D. degree in molecular electronics from the University of Durham, Durham, U.K., in 1985.

In 1986, he joined the faculty of the Department of the Electrical and Computer Engineering, University of Delaware, where his research was focused on design, modeling, and metrology of electronic and optical interconnect-limited computer systems. Following sabbatical years at the University of Southampton in 1997 and Philips Research in 2000, he joined Philips Research, Leuven, Belgium, in 2002, which later became NXP Semiconductors in 2006 with the spin-off of Philip's Semiconductor Division, where he was a Senior Principal Scientist in the process technology sector, with responsibilities for ultralow power CMOS development, design-technology integration, and strategic planning. In 2009, he joined Interuniversity Microelectronics Centre, Leuven, with responsibility for foundry technology assessment, tactics and strategy for small/medium businesses and fabless/fablite companies.

Peter Verheyen received the M.S. and Ph.D. degrees in electrical engineering from the Katholieke Universiteit Leuven, Leuven, Belgium, in 1996 and 2003, respectively.

He is currently a Senior Researcher with the Interuniversity Microelectronics Center (IMEC), Leuven, where he has been involved in studying advanced CMOS device concepts, the impact of strain on CMOS devices, and microelectromechanical system technology development. His current research interest is focused on CMOS compatible Si photonics technology.

Guy Lepage received the B.Sc. degree in chemistry from the Hoge Rega School, Leuven, Belgium, in 1999.

From 1999 to 2008, he was at Cytec, developing coatings for different applications. In 2008, he joined Interuniversity Microelectronics Centre (IMEC), Leuven, where he was involved in research on SiGe microelectromechanical system until 2011. Since 2011, he has been involved in the IMEC silicon photonics platform.

Nele Van Hoovels, photograph and biography not available at time of publication.

Philippe Absil received the Ph.D. degree from the University of Maryland, College Park, in 2000.

He is the Optical IO Program Director at Interuniversity Microelectronics Centre (IMEC), Leuven, Belgium, where since 2010, he has been responsible for the Silicon Photonics technology platform development. Before that, he spent seven years managing the Advanced CMOS Scaling Program at IMEC. In the early 2000s, he developed the passive photonics platform technology for Little Optics Inc., Annapolis Junction, MD. His doctoral work contributed to the early demonstrations of semiconductor microring resonators.

Joris Van Campenhout (S'02–M'07) received the Ph.D. degree from Ghent University, Ghent, Belgium, in 2007, for his research on hybrid, electrically driven microdisk lasers integrated on silicon-photonic waveguide circuits.

He is currently the Program Manager of the optical I/O industrial affiliation program at Interuniversity Microelectronics Centre (IMEC), Leuven, Belgium. This program targets the development of a silicon-based, scalable and industrially viable optical-interconnect technology to mitigate the I/O bandwidth bottleneck anticipated at the chip level in future sub 20-nm CMOS nodes. Prior to joining IMEC, he spent more than two years as a Postdoctoral Researcher at IBM's TJ Watson Research Center, Yorktown Heights, NY, where he investigated and developed silicon electro-optic switches for use in reconfigurable optical networks.

Dr. Van Campenhout is a member of the Optical Society of America.