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Mid-IR Photonic Integrated Circuits

A. Malik, 1,2 and G. Roelkens 1,2

Photonics Research Group, INTEC Department, Ghent University-IMEC,
 Sint-Pietersnieuwstraat 41, 9000 Ghent, Belgium
 Center for Nano- and Biophotonics (NB-Photonics), Ghent University, Belgium

The Mid-IR wavelength range is particularly interesting for spectroscopic sensing applications. Integration of Quantum Cascade Lasers with a photonic integrated circuit will pave the way for providing a tunable laser source along with a possibility of Lab-on-achip applications. A major challenge in realization of these devices is identification of a suitable waveguide platform. In this paper we will discuss the design and fabrication strategies of the possible waveguide platforms and will propose a generic concept of realizing a widely tunable integrated QCL using wavelength selective feedback elements implemented on a silicon photonic chip.

Introduction

The Mid-IR wavelength range is a region of interest for spectroscopic sensing applications. For sensing, it is well known that the gases in atmosphere show considerably high absorption peaks in this wavelength regime [1]. Also, it is known that the atmosphere has transparency windows in the Mid-IR regime of wavelengths [1] hence opening the possibility of free space communication.

A widely tunable integrated system in this range of wavelengths will allow realizations of lab-on-a-chip systems which can then be used in hand held applications. The advent of Quantum Cascade Lasers (QCL) in the previous decade has allowed for a light source based on epitaxially grown semiconductors in the Mid-IR whereas previously these wavelengths were accessible only by bulky sources like gas lasers. Present days QCLs allow the possibility of having a wide gain bandwidth [2] and their integration with photonic integrated circuits containing wavelength selective elements seems to promise a compact hand held system.

The very first challenge in realizing this kind of system is having a suitable photonic integrated circuit the details of which we discuss below.

Mid-IR waveguides - New platforms

For telecom wavelengths, Silicon on Insulator (SOI) is now a standard waveguide platform. There are several reasons behind this choice namely a large index contrast between Si and SiO₂, compatibility with CMOS pilot lines and the possibility for mass manufacturing. However, it is known that beyond 3.8 μm [3], the underlying SiO₂ starts absorbing heavily and hence it would not be possible to use SOI as the passive waveguide platform for Mid-IR applications.

Table 1: Table showing refractive indices and the transparency windows of different materials. [3]

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Fabrication of Mid-IR waveguides

Table 1 presents a list of mate-

rials with their refractive indices

and the transparency windows.

From this table we can identify

free standing Si, Ge on Si, Si

on Sapphire, Si on Chalcogenide

as possible candidates for an al-

ternate waveguide platform. SiN

has certain absorption bands depending on the growth conditions

and hence is not a very attractive

Although the waveguides for the Mid-IR wavelength range require new waveguide platforms, the requirements of minimum feature size is quite relaxed due to the fact that single mode width of waveguides is rather large when compared to waveguides for telecom wavelengths and hence these waveguides don't require complicated lithographic tools like e-beam lithography or DUV lithography and can instead be fabricated using a standard i-line lithography machine. Below we present the details for fabricating the different waveguides.

Free hanging Si

option.

Figure 1(a) shows the detailed steps required to fabricate a free standing Si waveguide. We begin with a SOI wafer (from Soitec) and first deposit a thin layer of alumina and then 300 nm of SiO₂ to act as hard mask. Then we pattern the SiO₂ layer using a photoresist mask and dry etching in a RIE system. The reason we use alumina in between SiO2 and Si is because SiO_2 is etched using a mixture of SF_6 and O_2 which also etches Si itself. Hence the alumina layer acts as an etch stop. Next we dip the sample for approximately 1 minute in a solution of CrO₃ and H₃PO₄ to remove the thin alumina layer. This dip will cause isotropic etching of alumina but since the oxide layer itself is dry etched, the mask profile is still anisotropic. Then we dry etch the waveguides in Si using a mixture of SF₆ and O₂ in a RIE system. As stated above, this mixture also etches the hard mask SiO₂ but the etching rate is rather slow (40 nm/min for SiO₂, while 300 nm/min for Si). After this we perform a dip in HF solution to remove both Alumina and SiO₂ layers.

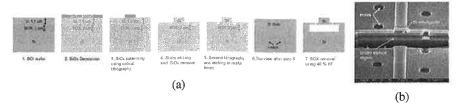


Figure 1: a) Schematic processing steps of a free standing Si waveguide and b) SEM cross section of such a waveguide

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After we have defined waveguides, next goal is to etch holes in the slab region such that we can access the underlying SiO₂. To do this we repeat the above mentioned steps once again and after these holes have been etched, we put the sample in HF solution such that it can etch the underlying oxide isotropically. Figure 1(b) shows the cross section of such a fabricated free standing Si waveguide.

Si on Chalcogenide

Fabrication steps for Si on Chalcogenide waveguides are summarized in the steps shown in figure 2(a). Again we begin with a SOI wafer and deposit a film of chalcogenide glass on it. Next we spin coat a layer of undiluted BCB on it and then bond it with a handle Si wafer. Then we remove the silicon and SiO_2 substrate by first performing grinding then dry etching and then wet etching in KOH and HF solutions. This then leaves us with Si on Chalcogenide bonded with a handle Si wafer on which we can further define waveguides via dry etching. Figure 2(b) shows the SEM image of Si on chalcogenide film bonded on a handle Si wafer. These chalcogenide films are deposited at the university of Southampton.

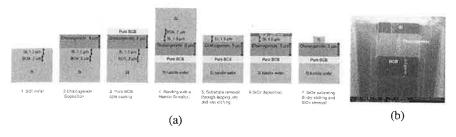


Figure 2: a) Schematic processing steps of a Si on Chalcogenide waveguide and b) SEM cross section of such a waveguide

Ge on Si

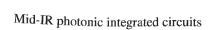
Compared to the above two waveguide platforms, Ge on Si waveguides have a straight forward fabrication procedure. Ge is grown epitaxially on a Si wafer in imec and we deposit a metal mask using negative lithography on top on Ge layer. We don't use a dielectric mask such as SiO_2 or Si_3N_4 because Ge is etched in CF_4 and O_2 plasma which etches these dielectrics at a faster rate than Ge itself. After dry etching Ge, we perform a dip in HF to remove the metal mask. Figure 3 shows a SEM image of such an etched Ge on Si waveguide.



Figure 3: Ge on Si waveguide

Widely tunable integrated QCL

A widely tunable integrated QCL on a photonic chip will pave the way for many novel and exciting applications. The presently available QCL systems work on the principle that feedback is provided through the movement of an external grating. This makes the



complete system bulky and not ideal for hand held and lab-on-a-chip applications. By integrating a processed QCL with a photonic chip, the wavelength selective feedback can be provided from the passive circuits for example by using ring resonators in various configurations and DBR mirrors. Also, the passive elements could be used for sensing applications by integration with microfluidics.

Figure 4 shows a generic scheme using which one could envisage a possible system where a processed QCL is integrated with a photonic chip using flip chip integration. For integrated telecom lasers,BCB bonding has been used widely but that seems less likely to work in case of QCLs as first of all QCLs are power hungry devices producing a lot of heat and BCB is a bad conductor and secondly BCB itself absorbs Mid-IR wavelengths.

Coupling to passive waveguide circuits

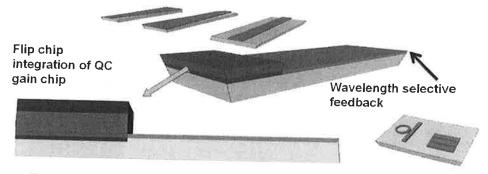


Figure 4: A schematic representation of an integrated QCL on a photonic chip

Conclusions

In this paper we have identified the certain possible alternate waveguide platforms for the Mid-IR wavelength range and have discussed their fabrication strategies. We successfully show the fabrication of a free hanging Si and Ge on Si waveguides and demonstrate a Si on chalcogenide film where waveguides could later be defined. In future we aim to characterize these waveguides and come up with the merits and demerits of each waveguide platform. We also present a generic idea to realize a widely tunable integrated QCL which could be interesting for lab-on-a-chip applications.

Acknowledgments

This work has been carried out in the framework of ERC-FP7-MIRACLE.

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Proceedings of the
2012 Annual Symposium of the
IEEE Photonics Society Benelux Chapter



















Editors

Marc Wuilpart, Christophe Caucheteur, Marilina Mura

29 & 30 November 2012 University of Mons Belgium ISBN 978-2-8052-0184-4 IEEE Photonics Society Benelux Chapter http://www.photonics-benelux.org/

University of Mons Faculty of Engineering Electromagnetism & Telecommunication Dpt.