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Advanced 300-mm Waferscale Patterning for Silicon Photonics Devices with Record Low Loss and Phase Errors

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We report on Si photonics devices fabricated on 300mm SOI substrates using 193-immersion lithography. Record low-loss of 0.7dB/cm with low phase-errors is obtained for 450-nm wide wire waveguides. We also demonstrate sub-wavelength grating fiber couplers with 42% coupling efficiency.

I. Introduction

Over the years, silicon photonics has matured from being a research interest to commercial reality. This is a direct consequence of leveraging CMOS based manufacturing technology for photonic functions. So far, 200 mm photonics-SOI is used for Si PIC manufacturing [1]. However, with the growing demand from a wide range of applications, such as datacom and biosensors, the need for complex device functionality and very precise dimensional control are becoming crucial. Transition toward 300 mm wafers technology brings many key advantages including access to state-of-the-art high-resolution mask technology and patterning tools/processes, which can potentially yield high pattern fidelity and superior dimensional uniformity.

In this paper, for the first time we demonstrate record low-loss waveguides, sub-wavelength photonic crystal fiber-chip couplers and high-resolution patterning in 300 mm SOI wafers fabricated using 45 nm mask technology, state-of-the-art 193 nm immersion lithography and an ICP-RIE process.

II. Device Design and Fabrication

A. Test device design

We use three photonic devices to demonstrate three key advantages of using a high-resolution patterning platform. Firstly, single-mode photonic wire and shallow etched ridge waveguides were designed to demonstrate loss performance. The wires were designed to be 450 nm wide and 220 nm high, while the ridge waveguides were 700 nm wide with an etch depth of 70 nm. Spirals waveguides of varying length (0.5, 1, 2, 4 and 7 cm) and a bend radius of 10 μm are used for propagation loss measurements.

Secondly, we designed sub-wavelength deep-etched fiber-chip couplers to demonstrate small features patterning capability using optical lithography. Grating based fiber-chip coupling is a versatile technique for coupling light in and out of a silicon photonic circuit [2].

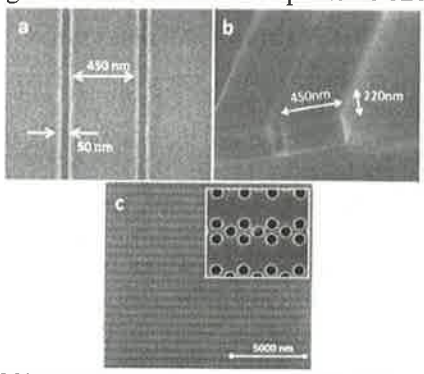

Fig. 1 SEM image of some of the structures from top left, 1a: 50 nm Trench patterning along with 450 nm photonic wire in photoresist, 1b: a section of direction coupler and 1c: sub-wavelength photonic-crystal fiber coupler.

Traditionally, shallow etch line/space patterning is used to create refractive index modulation, which requires shallow etching in addition to deeply etched wire patterning. In order to achieve the same degree of refractive index modulation, the low index can also be defined by using sub-wavelength deeply etched photonic crystal holes [3]. We have designed TE grating fiber couplers with a pitch of 660 nm with 50% duty cycle. The index modulation is achieved by photonic crystal of 220 nm pitch and 100 nm hole diameter in a triangular lattice configuration.

Finally, Arrayed Waveguide Gratings (AWG) are used to demonstrate linewidth uniformity within in a device. It is well known that the phase error caused by linewidth variation between the arms in an AWG results in higher crosstalk. In present day Si AWG designs, this is circumvented by increasing the wire widths in the delay arms [4]. We have designed two AWGs with different wire widths in the arms; 800 nm and 450 nm to compare the effect of phase-noise induced by linewidth non-uniformity. Both AWGs were designed to have 8 channels with 400 GHz channel spacing.

B. Fabrication

For the device fabrication, we used 300 mm SOI wafer with a 220 nm thick device layer on top of a 1000 nm buried oxide. A modified CMOS-type shallow-trench isolation module was employed for the waveguide patterning. After initial wafer cleaning, a pad oxide and SiN hard-mask layer are deposited and 220 nm deeply etched structures are patterned. The patterns are first

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defined in photoresist using 193 nm immersion lithography followed by 220 nm of Si etch using ICP-RIE selectively stopping on the BOx layer. Fig.1 shows a SEM image of some of the fabricated devices. After dry etching and resist strip, the patterned Si is covered with silicon dioxide followed by planarization using chemical mechanical polishing, where SiN is used as a stop layer to form a topography-free wafer surface. On top of the planarized surface shallow-etched patterns (70 nm) are defined using 193 nm immersion lithography, while the Si etch duration is tuned to reach a depth of 70 nm. The patterning process was aimed at achieving smooth sidewalls and good dimensional control both within a die and over the wafer.

III. RESULTS AND DISCUSSION

Optical characterization was done by coupling in light from either a broad-band SLED or a tunable laser operation in the C-band and the output is measured via an OSA or a photodetector respectively.

Fig.2 shows propagation loss spectrum of a 457 nm wide photonic wire and a 700 nm wide ridge waveguide. At 1550 nm, we measured a loss of 0.71 ± 0.05 dB/cm and 0.12 ± 0.01 dB/cm for the wire and ridge waveguide respectively. To our knowledge for this waveguide cross-section, this is the lowest loss reported for single-mode photonic wires and ridge waveguides fabricated either with e-beam or optical lithography. The low-loss behavior of the waveguides can be attributed to the optimized fabrication process technology.

Fig. 3 shows the efficiency of a deeply etched sub-wavelength grating fiber-chip coupler. The coupling efficiency was extracted from the measured transmission spectra of a 10 μm wide waveguide with two identical couplers and subtracting the loss from the setup which included connectors and polarization controller. Both input and output fibers were positioned at 10° normal to the sample plane. We have measured a coupling efficiency of 42% with a 1 dB bandwidth of 25 nm. The efficiency of the TE couplers agrees well with the efficiency for a similar device fabricated using e-beam [3].

Finally, Fig. 4 shows the transmission spectrum of three adjacent channels of an AWG with 450 nm and 800 nm wide waveguides in the delay arms. Both designs give similar filter characteristics. We measured an average insertion loss and crosstalk of 2.8 and 18.7 dB respectively for both the designs. Identical characteristics of these two designs clearly suggest that the phase error in the 800 nm wide design is the same as that of 450 nm. One of the main reasons for this is linewidth uniformity of the waveguides obtained from high resolution patterning and mask technology.

IV. CONCLUSION

For the first time, we have demonstrated Si photonic integrated circuit in 300 mm SOI wafer technology and patterning using state-of-the-art 193 nm immersion lithography and dry etch process. Using advanced patterning technology we have demonstrated record low-loss of 0.71 ± 0.05 dB/cm and 0.12 ± 0.01 dB/cm for 450-nm wide photonic wires and 700 nm wide ridge waveguides respectively. Furthermore, sub-wavelength photonic crystal based fiber-chip coupler with a coupling efficiency of 42% has been demonstrated. We also showed low-phase noise by comparing 800 nm wide and 450 nm wide delay wires in AWGs.

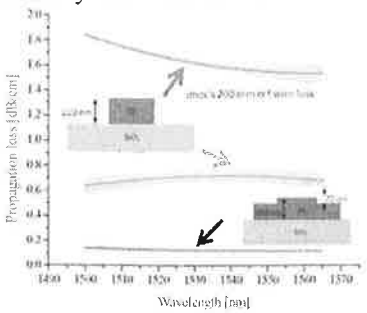

Fig. 2 Propagation loss of a 457 nm wide photonic wire (red curve) and a 700 nm wide ridge waveguide (black curve) in comparison with imec's 200 mm reference wire loss (black curve). The measurement error is indicated by means of grey band.

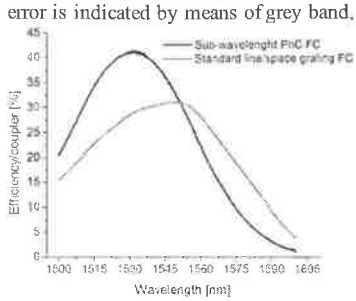

Fig. 3 Sub-wavelength fiber-chip coupler efficiency in comparison with standard line/space grating.

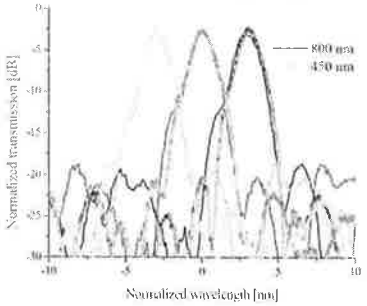

Fig. 4 Normalized transmission spectrum of 3 adjacent channels from 8X400 GHz AWGs with (—) 450 nm an (o) 800 nm delay arm wire width.

ACKNOWLEDGMENT

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