Compact Silicon Differential Receiver with Integrated Zero Biased Balanced Detection

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***Abstract*— We present an optimized differential receiver in silicon with a minimized footprint and balanced zero biased Ge photodiodes. The receiver integrates a delay-line with a 2x4 MMI 90 degree hybrid and two balanced photo diodes for DQPSK demodulation. Also a tunable power splitter is included for better balancing. Two receivers were tested, for 10Gbps and 20Gbps operation, and well opened eye-diagrams were measured.**

***Index Terms*— silicon photonics; coherent receiver; balanced detectors**

I. Introduction

THE differential-phase-shift-keyed (DPSK) modulation format exhibits several advantageous qualities [1]. It enables 3-dB improved receiver sensitivity with balanced detection, and has higher tolerance to nonlinear degradation compared with on-off keying (OOK). The detection of the phase at the receiver can either be implemented using coherent or differential (non-coherent) detection. A coherent receiver uses carrier tracking by phase-locked loops to estimate the absolute phase, while in differential encoded DPSK the information is in the phase transition and can be demodulated using a passive delay-interferometer. The simplicity of the differential detection and the elimination of a local oscillator (LO) and digital signal processor (DSP) makes differential detection advantageous for low cost links.

Mainly two designs of differential silicon receivers have been addressed in the literature, either using more standard Mach-Zehnder Delay-Line Interferometer MZDI [2-4] or by using micro ring-resonators [5]. Even though the size of the ring-resonator can be very compact the optimal performance is reached for an optimized Q-factor and at the same time maximized extinction ratio, which usually requires adding some tuning mechanism as in [6] and therefore increases power consumption and complexity of the receiver. The MZDI still seems to be the most used implementation in more complete systems such as presented in [2,4].

In this paper we demonstrate 5GBaud (10Gbit/s) and 10GBaud (20Gbit/s) operation using a very compact differential receiver for DQPSK demodulation. The receiver includes a tunable power splitter, a delay-line spiral, a compact 2x4 MMI 90 degree hybrid and two balanced germanium PDs.

II. Design and Optimization

The principle of operation of a differential demodulator using a MZDI is to superpose two adjacent bits using a delay-line (DL) and the intensity of the superposed signal can then directly be photo-detected converting the differential bit-transition into an intensity variation of the signal. In DQPSK modulation the four bits are coded as four different orthogonal phases.

The layout of the proposed structure is depicted in Figure 1, including a thermo-optically tunable MZI power splitter in series with a MZDI and a 90 degree hybrid. At the output the in-phase and quadrature signal are detected using two balanced PDs in *pinpin* configuration. In the following sections the implementation and optimization of each of these elements will be described.

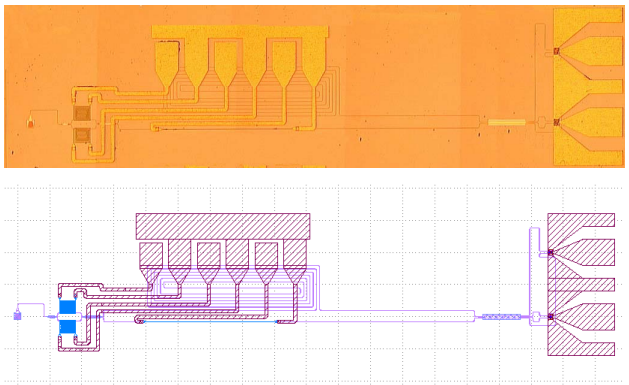

Fig. 1. Design of the differential receiver for DQPSK and 10G symbol rate; (upper) optical photograph of fabricated device, (lower) gds design. The receiver is assembled using 5 componentes, from left to right in the figure: Curved grating coupler, MZI tunable power splitter, delay-line interferometer, 90-degree hybrid and two balanced photo detectors.

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A. Curved grating couplers

The grating couplers are standard curved gratings [7]. Curved gratings are used in order to minimize the size of the chip since there will be no need to include spot size converters.

B. MZI tunable power splitter

To maximize the sensitivity of the receiver the output of the MZDI has to be balanced. To deal with the (potentially varying from run to run) loss in the delay-line, resulting in unbalanced behavior, we include a tunable power splitter at the input of the MZDI. If needed, we can now use micro-heaters to actively tune the input power, the propagation loss can then be compensated for by directing more optical power into the delay-line arm in order to have perfect balance at the output. The MZI switch is designed using two identical spirals which will optimize the footprint and the bandwidth of the device.

C. MZDI

Two different receivers with different delay-lines lengths were tested, including 5G and 10G symbol rates. The length for the 5G and 10G delay-lines are approximately 1.8cm and 0.9cm, respectively. On the one hand, we want to fold these delay-lines into spirals to have a maximum compactness of the receiver, on the other hand we want to minimize propagation losses. Even though 5 micron bend radius is considered close to loss-less we wanted to make sure no extra loss was introduced in the spirals. By using adiabatic bendings there is a smooth transition to the tight curvature and no loss is expected [8]. The 18 mm and 9 mm spirals have been folded to a minimal footprint occupying only 1.1 mm × 0.1 mm and 0.6 mm × 0.1 mm, respectively.

D. 90 degree hybrid

Instead of the more standard implementation of a DQPSK receiver with two parallel MZDI, each coupled to a 180 degree hybrid, here a single MZDI is used coupled to a 90 degree hybrid. This will both minimize the chip area by almost a factor of two as well as the number of active controls needed for tuning.

Here we use a 2x4 MMI design with shallowly etched multimode region. The device has a footprint of only 0.1 mm × 0.1 mm and exhibits a common mode rejection ratio (CMRR) better than −20 dBe and phase errors better than ±5 degrees in a 50 nm bandwidth [9].

E. Balanced Photodetectors

To have a 3dB increase in sensitivity of the receiver, balanced detection is used instead of single detection. We here use zero bias balanced detection and we can hence scale down the complexity and size of the receiver by excluding the need of a decoupling capacitor. Also, by using one single detector in a *pinpin* configuration, additional wire bonding or metal connections are eliminated since the signal is directly extracted from one single central pad. Here a lateral *pinpin* germanium balanced photodetector, only 10 µm long, is selectively grown at the end of silicon waveguides. The photodiodes used are comparable to the ones having a bandwidth above 10GHz for any negative voltage bias [10] , which clearly is sufficient for our application. The responsivity is measured to 1 A/W at 1550 nm using 0 to -2V bias with a dark current of 10nA.

III. Simulations

Figure 2 shows the simulated spectral response of the MZDI and the two balanced photodiodes using the transfer matrix method [11]. On the x-axis is the differential phase with respect to the two adjacent bits. The two curves are shifted exactly 90 degrees with respect to each other in order to obtain the four different states on the DQPSK modulation format. The states are marked in the figure as dotted vertical lines at the four different orthogonal phases at, -90, 0, +90, and +180 degrees.

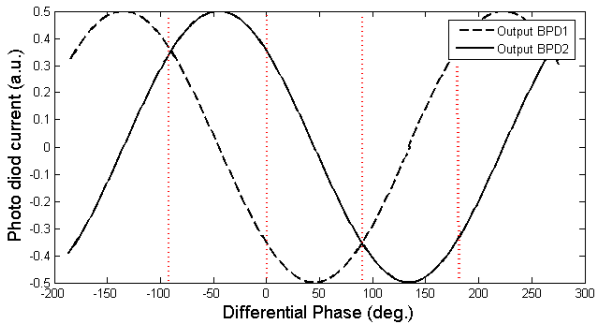

Fig. 2. The simulated output of the receiver. The two curves represent how the in-phase and quadrature detected current from the two diodes varies with the differential phase. The four different two-bits states are marked as dotted lines at -90, 0, 90, and 180 degrees, corresponding to [+1 +1], [-1 +1], [-1 -1], and [+1 -1], respectively.

IV. Fabrication

On SOITEC optical SOI with 220nm Si on 2µm BOX, the process starts with the deposition of 100nm High Temperature Oxide (HTO) on top of the silicon layer. The gratings and the waveguide arms are first patterned, followed by RIE silica etching with C_4F_8, which defines a hardmask. The silicon is then partially etched (65nm) with HBr and controlled by ellipsometry in order to define precisely the grating teeth depth. In the second lithography step, the gratings are protected by the resist and the remaining hardmask serves for the waveguides in a self-alignment process. Then a full silicon etch down to the box completes the waveguide fabrication. We then defined cavities for the selective epitaxial growth of Germanium. This is achieved by deposition of a silica layer which is etched at the end of waveguides. In order to achieve direct coupling, the silicon part of the cavities is etched down to 50nm on top of the BOX. Germanium was then selectivity grown in the cavities and CMP used to adjust the thickness around 300nm. The doped regions (N and P) of the lateral Ge photodetector are defined sequentially by ion implantation of Phosphorus and Boron. A 400nm thick SiO2 was deposited and a deposition and etching of 100nm of Ti/TiN defined the heaters. Then after deposition of 500nm of SiO_2 and two-step openings, the electrodes were defined by Ti/TiN/AlCu metal

stack deposition and Cl2 etching.

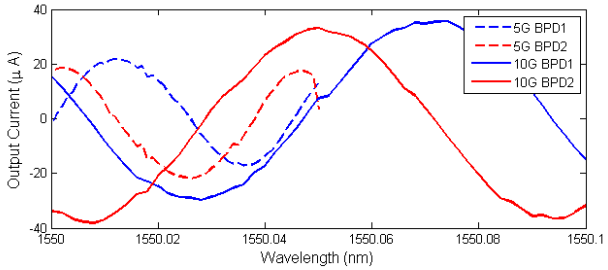

Fig. 3. Transmission spectra for the output current for the 5GHz (red lines) and 10GHz (blue lines) symbol-rate receiver. The solid and the dashed lines corresponds to the quadrature and in-phase outputs

V. Measurements and Experimental Results

Continuous-wave light was generated by an external cavity tunable laser. The light was coupled to the chip through the curved grating coupler using manual micro-positioners. A GSGSG probe with a 100μm pitch was used to measure the output current of the photo diodes. Figure 3 shows the measured transmission spectra for -3dBm input power. The spectra have excellent agreement with the expected behavior for a DQPSK receiver shown in Figure 2. For both the 5G and 10G receiver, the two outputs are perfectly 90 degree phase shifted with respect to each other. The lower output current from the 5G receiver is expected due to the longer delay-line.

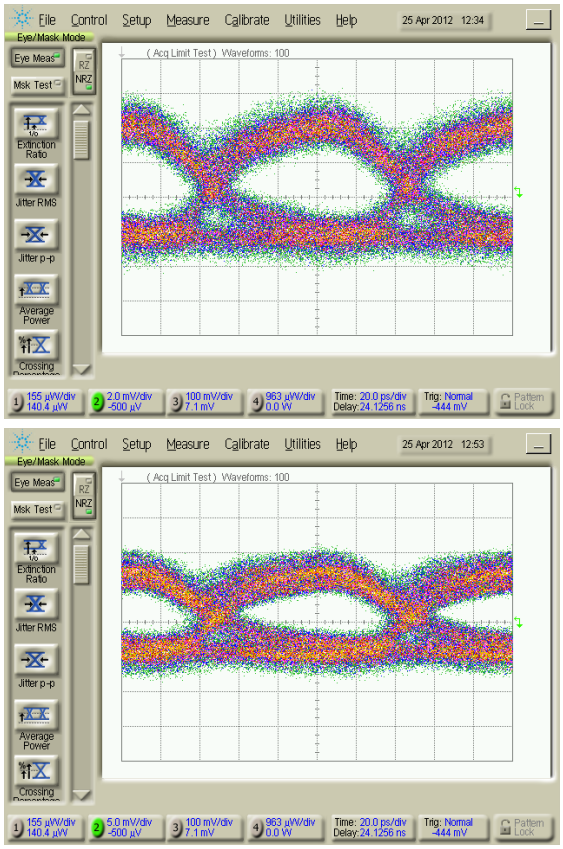

Fig. 4. Eye diagrams measured for the 20Gbps differential receiver. The upper and lower graphs correspond to the demodulated in-phase and quadrature signal.

To test the high speed behavior of the receiver an optical data stream was generated using a Lithium Niobate dual-drive modulator generating a DQPSK signal. The bit streams used were two decorrelated pseudorandom binary sequences (PRBS) with a pattern length of 2^{23}-1 at 10Gbps, generated by a bit pattern generator (SHF BPG 44E). At the output of the chip, the signal was extracted directly from the photodiodes using a GSGSG probe and fed to a Communication Analyzer (Infinium DCA-J 86100C). For an input power of 5.5dBm, Figure 4 shows well opened eye-diagrams of the two demodulated I and Q signals for 20Gbps operation.

VI. Conclusion

An optimized receiver for DQPSK transmission was demonstrated with a minimum footprint and with zero biased photo detectors. Each building block of the receiver is optimized for high performance, low loss and maximum compactness. The results demonstrate the compactness and high performance of a silicon DQPSK receiver.

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