Multiple die-to-wafer adhesive bonding for heterogeneous integration

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***Abstract*— A new process for bonding of III-V dies to processed silicon-on-insulator waveguide circuits using divynilsiloxane-bis-benzocyclobutene (DVS-BCB) was developed using a commercial wafer bonder. High-quality bonding, with ultra-thin bonding layers (< 60 nm) is demonstrated, which is suitable for the fabrication of heterogeneously integrated photonic devices, specifically hybrid III-V/Si lasers.**

Keywords: Adhesive bonding; heterogeneous integration; Silicon-on-Insulator (SOI)

I. INTRODUCTION

Silicon-on-insulator (SOI) is an emerging platform for photonic integrated circuits. It offers the potential for realizing low-cost and compact optical functions, since the standard complementary metal oxide semiconductor (CMOS) massive processing infrastructure can be used to process these optical components. Fabrication of light sources on this platform is still a big problem, due to silicon's indirect bandgap. Heterogeneous integration, achieved through the bonding of III-V semiconductor materials onto SOI, is the most promising approach to address this problem [1]. Commercial silicon and CMOS production is done on wafers with diameters of 200 mm and above, while III-V wafers used in photonics applications have typical diameters of less than 100 mm. Therefore, one-to-one wafer bonding between differently sized wafers is not an effective integration approach. Therefore, a cost-effective approach in heterogeneous integration requires small pieces of III-V material to be bonded on the SOI photonic wafer. We focus on a multiple die-to-wafer adhesive bonding process, where III-V dies are bonded to an SOI wafer using DVS-BCB as the bonding agent. In this paper, we describe a new adhesive wafer bonding process scheme that involves partial curing of the DVS-BCB prior to bonding and attaching the III-V dies to the SOI substrate at room temperature prior to curing in a vacuum atmosphere. An alternative method has been reported earlier, in which adhesive die-to-wafer bonding was demonstrated in a commercial wafer bonder [2]. In that method, spacers are used to keep the III-V die and SOI substrate separate prior to loading the stack in the bonding tool. In this new method no carrier is required to load the top wafer/die into the machine and no vacuum or heating is required prior to contacting the wafers in the bonding chamber. This 'cold bonding' method significantly simplifies the bonding preparation for machine-based multi-die scale bonding and it shows high yield for ultra-thin bonding thicknesses below 60 nm. This process was applied to achieve ultra-thin DVS-BCB bonding layers for the fabrication of several photonic devices, such as III-V/SOI lasers [3].

II. DESCRIPTION OF THE BONDING PROCESS

The bonding process was developed for multiple die-to-wafer bonding, as well as a single die bonding. A MicroTec Süss ELAN CB6L wafer bonder was used for the bonding experiments. The bonding process starts with the cleaning of the SOI substrate and III-V dies. The SOI cleaning is performed by dipping the substrate into a Standard Clean 1 (SC-1) solution heated to 70°C, for 15 min. After this, the DVS-BCB:mesitylene solution is spin-coated onto the SOI substrate. The SOI substrate is then baked for 10 min at 150°C, to let mesitylene evaporate, after which the substrate is slowly cooled down to room temperature. Finally, the SOI is mounted on a carrier wafer made of Pyrex glass. Meanwhile, prior to bonding, two sacrificial layers on the III-V die are removed by selective wet etching, which also removes particles and contaminants from the III-V die surface. The III-V die is then rinsed with DI water, dried and mounted on the SOI die. Since in the presented method the dies are contacted at room temperature, individual dies can easily be pick-and-placed onto the silicon target wafer. They can be aligned manually with an accuracy of 500μm without any extra tools or can be placed more accurately using a flip-chip machine. After that, the SOI substrate on its carrier wafer is mounted on the transport fixture and is loaded into the processing chamber of the wafer bonding tool. The chamber is pumped-down and heated to 150°C with a ramp of 15 °C/min for 10 min, while applying pressure on the III-V/SOI stack. The actual bonding pressure (the applied force per area of the III-V die) is kept in the range of 200 to 400 kPa. After keeping the pressure on the dies for 10 min at 150 °C, the temperature is increased up to 280 °C, with a ramp of 1.5 °C/min. Upon reaching 280 °C, the dies are kept at this temperature for 60 min in a N_2 atmosphere. After the curing, the bonded samples are cooled down (at 6-10 °C/min) and unloaded from the processing chamber. The InP substrate of the III-V die is then removed by selective wet etching, leaving a thin III-V film with the functional layers bonded to the SOI die, ready for further processing.

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III. DVS-BCB MULTIPLE DIE-TO-DIE BONDING RESULTS

In order to demonstrate the true potential of die-to-wafer bonding, 0.3cm^2 III-V dies were transferred to a quasi-planarized SOI die (fabricated in CEA-LETI), using the ultra-thin bonding recipe. The results are shown in Figure 1.

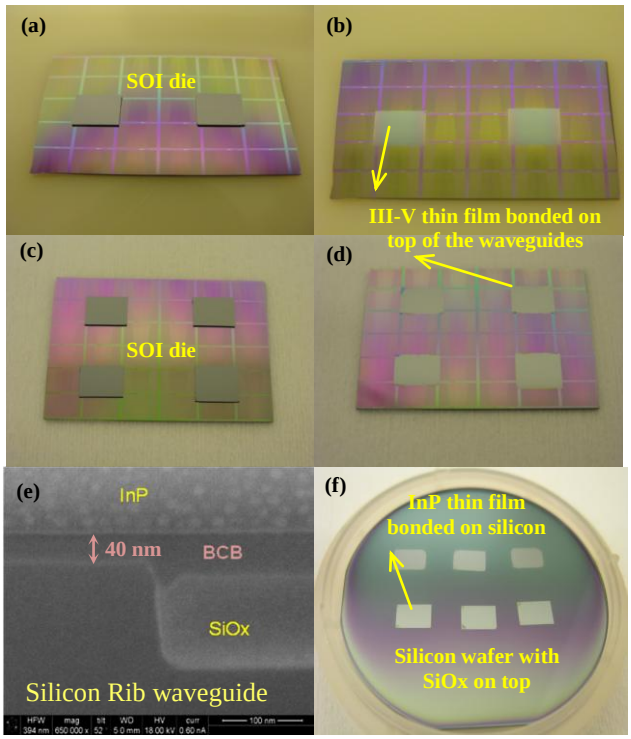

Figure 1. (a-b) two epitaxial 0.3 cm^2 III-V dies bonded on a planarized SOI die before and after the substrate removal process; (c-d) four epitaxial 0.3 cm^2 III-V dies bonded on a planarized SOI die before and after the substrate removal process; (e) SEM image of the bonding interface.(f) 6 InP-membranes (with the individual die area of 0.2 cm^2) bonded on a 50 mm silicon wafer.

The bonding quality was assessed by bonding six III-V dies to a 50 mm silicon wafer with 1.5µm-thick layer of SiO_x on the top. This bonding is usually used for InP-Membrane-on-Silicon applications [4] (see Figure 1f). The InP films were etched away using a wet etching solution to measure the thickness and uniformity of the DVS-BCB bonding layer. The results for the six dies bonding experiment are showing a good uniformity over the whole bonding area and a high reproducibility of the nominal bonding layer thickness. A DVS-BCB: mesithylene dilution of 1:8 (v/v) was used in the experiment, spin coated at 2500 rpm, resulting in an average bonding layer thickness of 60 nm, varying by +/- 5nm over all six dies.

In particular applications, there is a need for bonding different types of III-V dies on a single SOI die or wafer (e.g. a die containing laser epitaxy and a die containing photodetector epitaxy). Here we show that by applying the new bonding recipe, in combination with a graphite foil between the dies and the bonding head, four die bonding using 2 different epitaxial layer stacks (with about 50 µm difference in substrate thickness) can be achieved. This graphite foil is used to compensate for these thickness variations in order to distribute the pressure evenly over all dies during the bonding, as is illustrated in Figure 2. These differences in substrate thickness are difficult to handle using the classical bonding recipes while our new bonding process results in perfectly bonded dies.

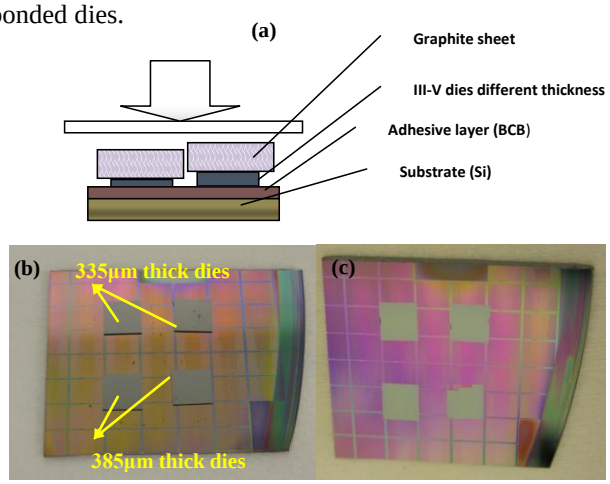

Figure 2. Bonding of four III-V dies, with different substrate thickness, on a planarized SOI die,using a graphite foil to compensate for the die thickness variations: (a) schematic; (b) before substrate removal; (c) after substrate removal.

IV. CONCLUSION

The 'cold bonding' method significantly simplifies the preparation process for machine-based bonding in a multiple die-to-wafer adhesive bonding procedure. The demonstrated DVS-BCB bonding layer thickness is very uniform and ultra-thin DVS-BCB bonding (<60 nm) can be achieved. Additionally, we developed the process for simultaneous bonding of multiple III-V dies with different thickness, suitable for the heterogeneous integration of different types of III-V components on a SOI photonic circuit.

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