How to bring nanophotonics to application – silicon photonics packaging

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Abstract: Fiber pigtailing and packaging of nanowaveguide circuits are key technologies to realize nanophotonic applications. Technical problems start with a large mode mismatch of nanowires and standard single-mode fibers, which requires innovative coupling structures for low coupling loss and for large alignment tolerances. Looking further ahead, solutions are needed that allow for wafer level optical device testing and also for reduced packaging costs. These are essential ingredients for making nanophotonics a truly competitive and large scale technology. In the following we shall present work that focuses exactly on such issues, covering a general evaluation of coupling techniques, silicon grating couplers, fiber array packaging of silicon nanophotonic circuits, and roads to reduced costs and generic nanophotonic packaging.

1. Introduction

Silicon photonics based on silicon-on-insulator (SOI) nanophotonic waveguides is a promising technology for integrated photonics due to unique properties of the ultra-high index contrast silicon waveguide systems, and due to the use of advanced microelectronics manufacturing technologies. The high index contrast of silicon nanowires allows for sharp waveguide bends with radii of just a few microns [Bogaerts_JLT05]. The footprint of silicon nanowaveguide devices is therefore strongly reduced compared to classical integrated optics. Still, a sufficiently large fraction of the guided light of nanowires is outside of the waveguide core in the evanescent field, making such waveguide structures also very promising candidates for sensing applications [DensmoreA_PTL06]. Furthermore, the exploitation of nonlinear properties of silicon in nanowaveguide structures shows strong potential for use in tele or datacom [Q.Lin_OEx07]. Last but not least, the use of common process tools and advanced SOI substrates make silicon nanowires a natural choice for integration with advanced microelectronics.

Despite such positive prospects there remains a major stumbling block on the way to nanophotonics applications - the issue of coupling light in and out of nanophotonic circuits by means of optical fibers. The major problem stems from the large mismatch in modesize of nanowires (~ a few hundred

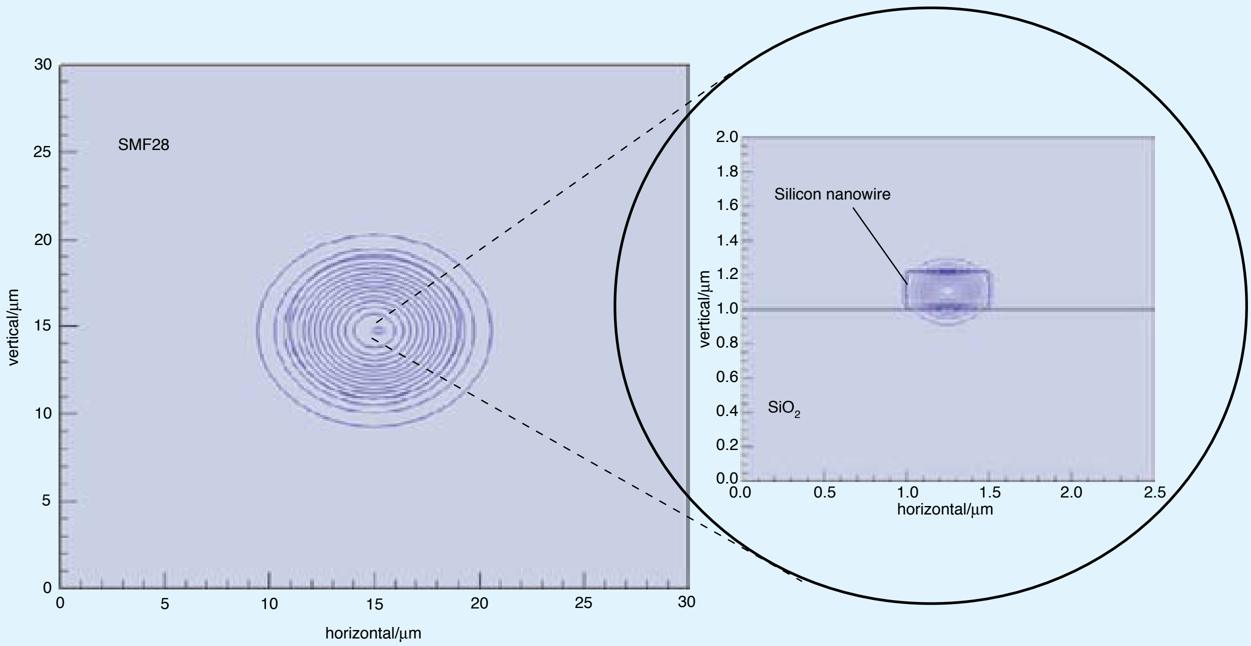


Figure 1. Intensity distributions (modesize) of a standard telecom fiber (SMF28) and a silicon nanowire (TE). Note the significant difference in scale. Without modesize adaptation techniques, coupling loss would be in excess of -16 dB.

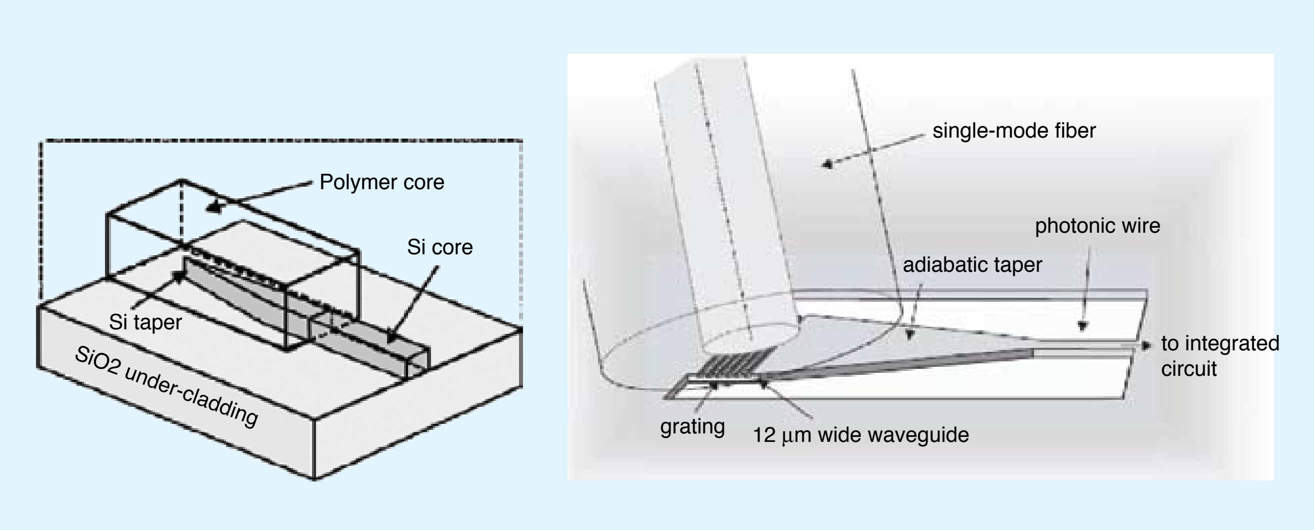


Figure 2. Lateral coupler (a) using spotsize conversion via inverse taper (from {Tsuchizawa_JSTQE05}). Vertical coupling via diffraction grating in the nanowaveguide (b).

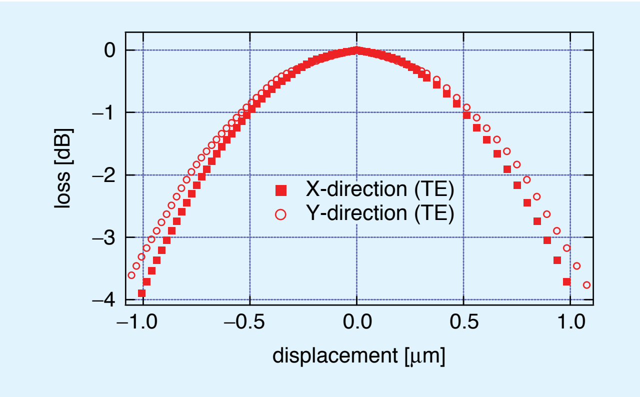


Figure 3. Example of fiber-chip coupling penalty for horizontal (X) and vertical (Y) displacement from the optimum position. Coupling between a 3 μm nitride box waveguide on SiO_2 and a 3 μm fiber spot. Penalty is 1 dB in both directions for a 1D-displacement of ±0.5 μm. The XY displacement tolerance for a 1 dB penalty is ±0.3 μm.

nanometers) and standard single mode fibers (SMF, ~ 10 μm), which is illustrated in Figure 1. Various spot-size converters and coupling schemes between the silicon circuits and fiber have been demonstrated, with losses down to below 1dB. However, most complex integrated circuits require a high optical 'pin-out'. Achieving high-yield, low-penalty coupling to arrays of fibers is still a challenge today.

Many solutions to overcome low efficiency coupling have been proposed and new work keeps appearing in literature. They follow in general one of the following two approaches:

- Lateral coupling (in plane)
- Vertical coupling (out of plane)

Both techniques require spotsize conversion. However, they differ in the dimension of spotsize conversion, i.e. whether they just deploy lateral spot-widening (1D-tapering) or true extension of the mode in the second dimension (2D-tapering). Lateral coupling implies 2D-spotsize conversion. Vertical coupling requires out of plane diffraction via gratings. Both schemes are depicted in Figure 2. Note that in case of nanowaveguide dimensions reflection is not efficient due to the diffraction limit.

Lateral and vertical coupling experiments have demonstrated low insertion loss. However, besides efficiency, other constraints can also limit the feasibility of a coupling approach. That will be clarified in the following by a brief overview of how lateral and grating coupler techniques are put to work. The next section will then provide a more detailed account of grating couplers that are certainly the most appealing interface to silicon photonics due to their availability in the front-end of line (FEOL) and their large modesize. We shall see later on that grating couplers are excellent means of wafer-level probing and pigtailing with single mode fiber (SMF) arrays.

Lateral coupling. Nanowaveguide taper-structures usually imply the fabrication of a sub-100nm nanotip and precise down tapering to that tip-size. Excellent control of critical dimensions (CD) is mandatory with such tapers. Matching the modesize of SMF is very difficult to achieve with a single taper structure. Therefore, the nanowaveguide mode is first expanded to an intermediate spotsize of ~ 3 μm and launched into a larger waveguide by means of the nanotip. The process is also referred to as mode conversion, because the spotsize at the nanotip matches the fundamental mode of the larger waveguide. In a second taper stage the spotsize is then adapted to SMF. Double taper structures are sensitive to process variations and quite elaborate in process design and development. Most 2D-tapers are therefore single-stage and limited in their modesize to approximately 3-4 μm. Efficient coupling to such mode diameters can be achieved by means of lensed fibers or high-numerical-aperture fibers (high-NA), but mechanical alignment tolerances remain substantially below 1 μm. This is illustrated for the coupling between a 3 μm waveguide and a lensed fiber with 3 μm spotsize (Figure 3).

Furthermore, tapering in the vertical direction requires dealing with substantial topography, so taper processing has its place naturally at the very back-end of line (BEOL). Lateral coupling also requires precise preparation of the edge of the die, either by polishing (if optically flat surfaces are required) or by precision grinding (if the distance to the edge of the die needs

Saturn's northern latitudes and the moon Mimas. Image from the Cassini-Huygens mission.

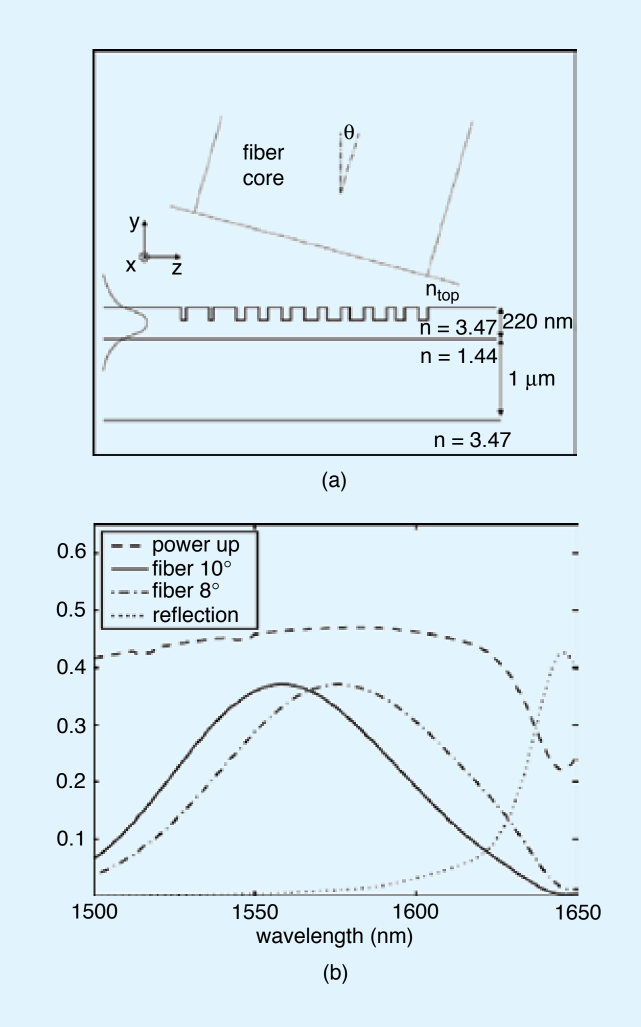


Figure 4. Cross section through single etch 1D-grating structure with non-uniform fill factor (a). Coupling characteristics of simple uniform 1D-grating structure (b). Depicted curves show upwards radiated power, coupling efficiency to the fiber and reflection at the waveguide grating interface.

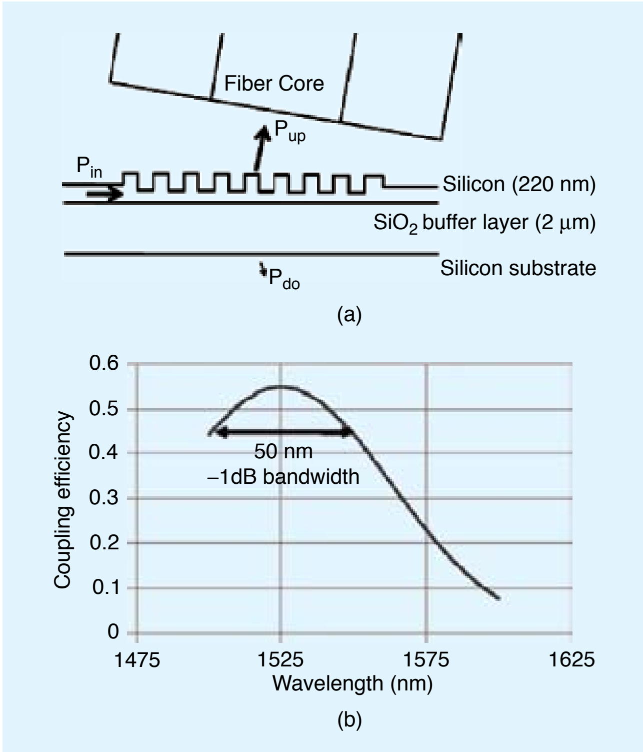


Figure 6. Grating coupler with silicon overlay to increase efficiency (a). Measured coupling efficiency of a grating coupler with overlay (b).

to be critically defined). A considerable process overhead should therefore be kept in mind when lateral coupling is considered.

Vertical coupling is achieved by means of second order grating structures. A more detailed account of grating couplers will follow in the next section. We shall limit this paragraph to a concise review of grating coupler properties as required for a first comparison with lateral couplers. The fabrication of gratings necessitates precise control over etch depth and etch profile. However, grating fabrication is fully compatible with FEOL processing. Gratings essentially act like a filter, exhibiting strong polarization dependence and limited bandwidth. The peak efficiency of simple grating couplers is rather low (-4.5 dB). Strategies have been devised and experimentally verified that overcome low efficiency and polarization dependence, though at the cost of additional process effort. Furthermore, grating couplers are fabricated by planar wafer-level processes, and do not require single die processing. They provide the capability of wafer level optical probing.

A comparison of lateral and vertical coupling from the point of view of fiber pigtailing is summarized in Table 1.

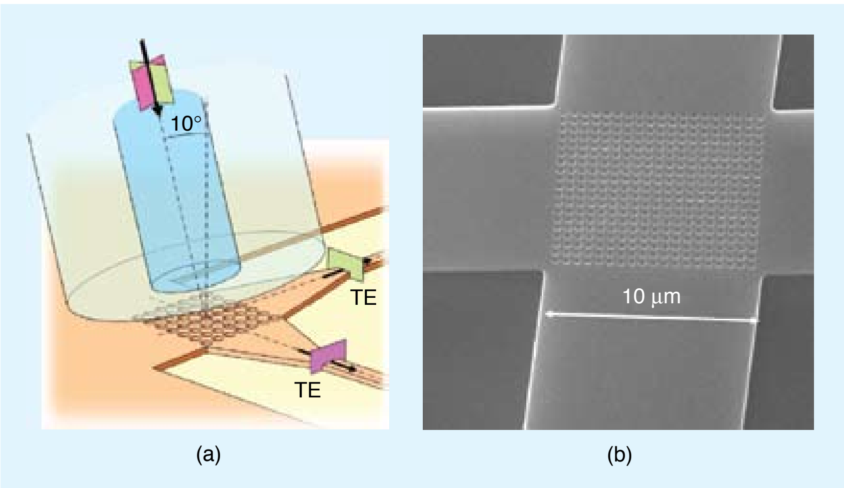


Figure 5. A 2D grating couples each of the two orthogonal states of polarization of the incoming light into a separate nanowire, thus implementing polarization diversity (a). Scanning electron microscope (SEM) image of 2D grating coupler with access waveguides (b).

2. Grating couplers

Coupling to silicon photonic wires through high-index contrast gratings is attractive because of the relaxed alignment tolerances compared to facet coupling. Grating couplers match standard single mode fibers.

Because of the high index contrast, the grating can be short (25 periods) and achieve a relatively large bandwidth.

Simple one-dimensional grating couplers with a uniform fill factor, etched into a broad waveguide, achieve a coupling efficiency of around 35% (-4.5 dB) with a 40nm 1dB bandwidth (per coupler) for a single polarization. Detuned gratings with a coupling angle of 8° to 10° are used in order to avoid back reflections. The alignment tolerance for a 1dB loss penalty exceeds ±1μm. A schematic cross section through a 1D-grating coupler structure is shown in Figure 4(a). Figure 4(b) depicts simulated coupling characteristics of a typical 1D grating with uniform fill factor. The total upwards coupled light exceeds the light coupled to the fiber due to mismatch of the respective far-field characteristics. There is also an angular dependence of the maximum coupling. The shift of the maximum of the reflection curve reveals the detuning of the grating. 1D gratings are optimized for TE polarization ([Taillaert06JJAP]). Experimentally measured coupling efficiencies match the simulation results.

	Lateral	Vertical
Coupling loss to SMF (butt fiber)	–7 dB (single stage) –1.5 dB (double stage)	–4.5 dB (standard grating) –1 dB (optimized grating)
Coupling loss to SMF (lensed fiber, incl. excess loss due to lens)	–1.5 dB (best) –3 dB (typical)	–
Coupling tolerances for 1dB penalty	±0.3 μm (single stage)	±1.0 μm
3 dB bandwidth	Broadband	60 nm
Polarization dependence	Weak	Strong (but can be solved with 2D grating and polarization diversity approach)
Suitable for multiple fiber I/O	No (due to small tolerances)	Yes

Table 1. Relevant properties of the major fiber coupling techniques to silicon nano-waveguides

In addition, a two-dimensional grating coupler simultaneously splits the two incident polarizations ([Taillaert03PTL]) and can be used in a polarization diversity scheme, which is schematically illustrated in Figure 5 (a). A real two-dimensional grating coupler is shown in Figure 5 (b). Simple 2D couplers achieve similar efficiency and bandwidth as one-dimensional couplers, but have reduced alignment tolerances in order to achieve polarization independent circuits.

The grating couplers can be optimized in various ways to improve the efficiency or size. Focusing couplers achieve the

Fiber #	1	2	3	6	7	8
Mismatch in y [µm]	–2.2	0.8	0.3	0.1	0.0	2.0
Mismatch in x [µm]	0.0	4.0	1.7	–2.5	–4.3	0.0

Table 2. Measured deviations of fiber positions within an eight fiber array. Only six fibers are included because fibers 4&5 are not used during the experiment. 1550nm CW light source (HP81553SM optical power (HP81532A)

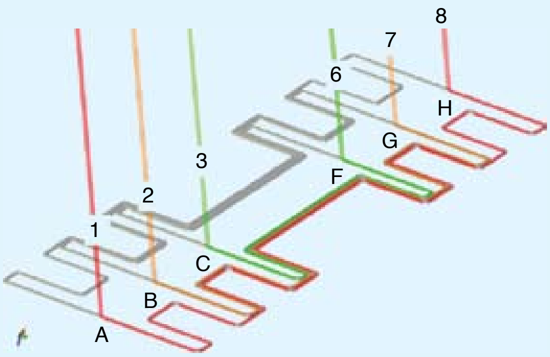


Figure 7. Schematic drawing of a grating coupler array designed and fabricated at IMEC. The grating couplers are interconnected by nanowaveguides (red, orange, green). Coupling loss and uniformity of the array coupling process can be determined from simple loss measurements between fibers 1/8 (AH), 2/7 (BG), and 3/6 (CF).

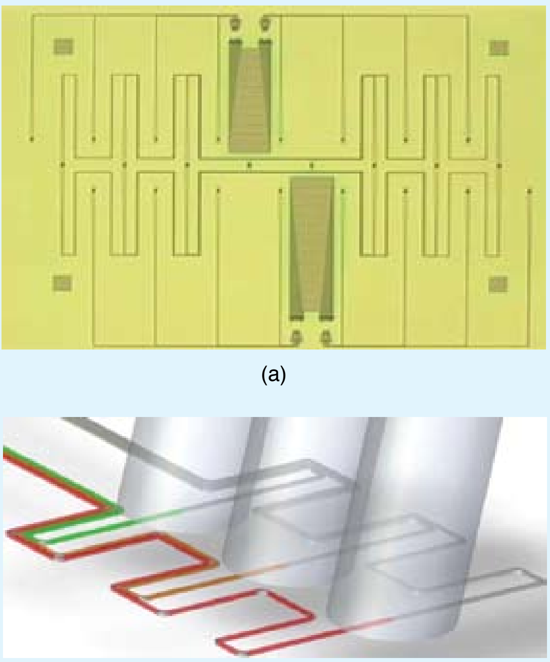


Figure 8. Photograph of Silicon on Insulator (SOI) chip (2.5mm x 1.7mm) with shortened grating coupler array (a). To illustrate the proportions of the coupling arrangement SMF fibers and grating pitch have been drawn to scale in (b). Nanowaveguides are still enhanced to increase visibility.

Transmission	1AH8	2BG7	3CF6
1 dB loss penalty at x-axis [µm]	±1	±1	±1.5
1 dB loss penalty at y-axis [µm]	±2	±1.5	±2
3 dB loss penalty at x-axis [µm]	±2.5	±2.5	±2.8
3 dB loss penalty at y-axis [µm]	±3.5	±3.5	±3.5

Table 3. Summary of alignment penalties

same efficiency on a much smaller footprint, as with the regular coupler one still has to taper down the broad waveguide [VanLaere07PTL]. By using non-uniform fill factors, lower coupling losses can be obtained and the efficiency can be further boosted by decreasing the vertical symmetry of the structure or adding bottom mirrors [Taillaert06JJAP]. With an overlay, efficient couplers can be obtained [Roelkens08APL]. Figure 6 (a) shows a grating with increased efficiency due to a silicon overlay (thickening). Such overlays have been realized by epitaxial overgrowth. The experimentally determined coupling efficiency of an overlay grating is plotted in Figure 6 (b). Here, the coupling loss is decreased to -2.5 dB.

The main benefit of coupling to vertically mounted fibers is for wafer-scale testing and characterization. By hovering fibers over the on-chip couplers, photonic integrated circuits can be tested in much the same way as standard electrical wafer-scale tests are done.

3. Fiber array packaging

Due to the extended usage of different multiplexing techniques, and due to the increase of functionalities which are integrated within a single photonic integrated circuit (PIC), the number of optical ports increases and multiple fiber I/O becomes more and more important. Today many different commercial fiber array solutions are available.

Tolerances of commercial fiber arrays. Limitations in case of commercial fiber arrays are related to their uniformity. Here extensive measures can be taken to minimize the tolerances related to the dimensions of v-shaped grooves for carriers of arrayed fibers. However most likely the fiber tolerances especially the variation within the fiber core and fiber cladding concentricity define the uniformity limits. The core-cladding concentricity tolerance is < 0.5 for SMF-28 fiber, so an alignment error below 1 per single fiber within a multiple fiber array can be manufactured. However, to understand the tolerances of presently available fiber arrays we investigated the actual alignment precision of a purchased fiber array.

By using a precise alignment system (PI F206) and a single mode fiber, the lateral deviations of a commercial fiber array (core of the fiber) from the ideal position was measured by scanning along the array with the optical probe and detecting the received signal as a function of the lateral position. The deviations of the positions of the respective fiber cores from the ideal are listed in Table 2, which shows that the total deviation from the ideal position could amount to more than what would be expected from the manufacturer's specifications. In this particular case the pitch deviated by 4 µm from the expected between fiber 1 & 8 (distance 1750µm).

Fiber array coupling. Recently, we carried out a study concerning generic fiber array interconnections for silicon photonics ([Tekin08_ECOC]). In course of this work we investigated the pigtailing penalty when coupling a commercially available fiber array to an SOI chip with an array of grating couplers. The SOI chip was manufactured for testing purposes at IMEC and carried 6 spare vertical grating coupler ports, which were shortened by nanowaveguides (Figure 7).

The sensitivity of transmission to the alignment between fiber array and SOI chip was investigated. The position of the SOI chip was varied and the transmissions through the ports AH, BG, and CF were measured, respectively. A photograph of the SOI chip is shown in Figure 8 (a). To illustrate the proportions between nanophotonic chip and fiber array, 3 fibers have been depicted to scale over the SOI chip in the drawing in Figure 8(b).

The measured alignment sensitivity for coupling between a grating coupler and a SMF is depicted in Figure 9. The key to successful fiber array coupling is a large alignment tolerance at each individual coupling point. The measured alignment tolerance of a waveguide grating coupler for a 1dB loss penalty is ±2µm. The measured sensitivity is summarized in the following Table 3. Hereto, 1 dB and 3 dB loss penalties in the lateral direction are provided.

The chip alignment is optimized by active alignment using the monitoring ports on the SOI chip. The position (x, y, z, and rotation) of the SOI chip was varied and the transmission through the ports AH, BG, and CF was monitored for optimized polarization state. After active alignment the chip is fixed by a UV-curing epoxy. The basic assembly configuration is depicted in Figure 10. No significant change in transmission signal was observed after the curing process. The generic fiber array based package without and with glob top encapsulation are depicted in Figure 11 and 12, respectively. The SOI chip is mounted face down on the fiber array.

The wavelength dependence of the transmission through shortened grating couplers was measured, where HP8168A was used as an ECL (external cavity laser). The transmission curves in Figure 13 have a comparable performance, and non-uniformity was ~ 1dB. We

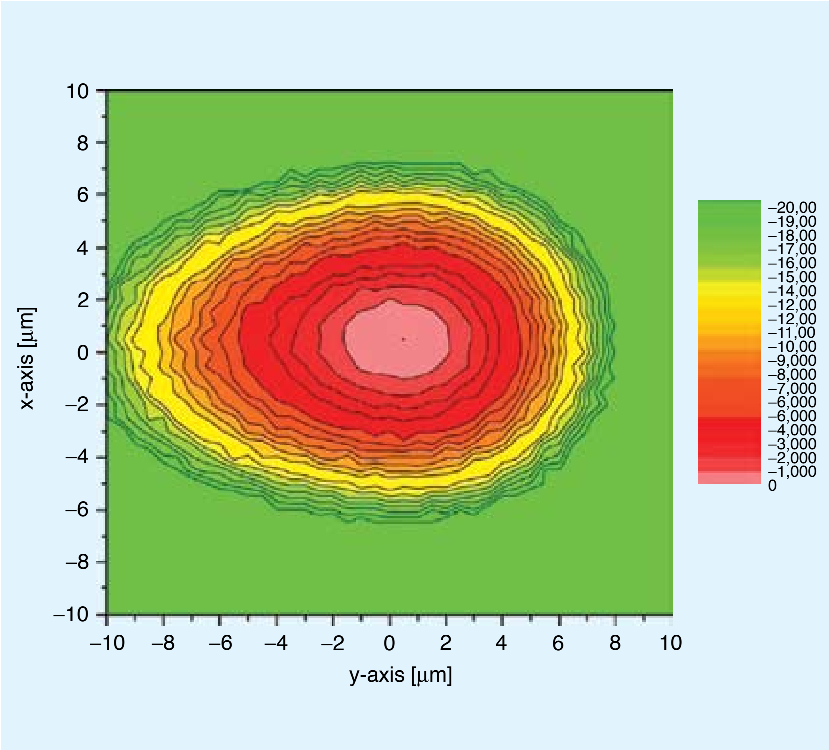


Figure 9. Experimentally determined penalty of coupling between SMF and standard grating couplers. A penalty of <1 dB can be achieved with an XY displacement accuracy of ± 1µm.

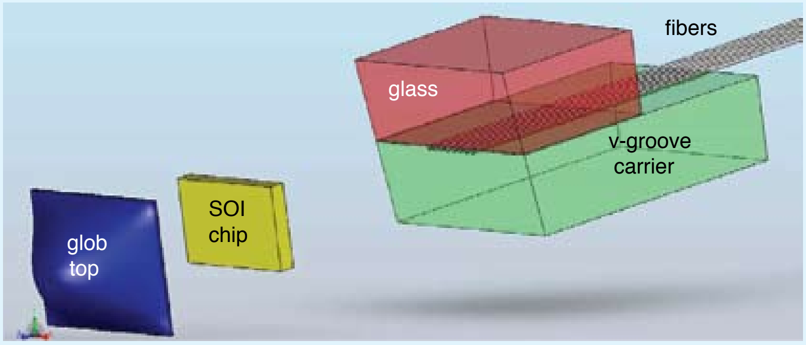


Figure 10. Schematic drawing of how a fiber array package is assembled. The mechanical support of the fibers stems from the v-groove base itself.

observed insertion loss of up to approximately -12 dB, with typical shape of grating coupler filter curves. The penalty due to multiple fiber pigtailing therefore amounts to ~ 1-2 dB.

4. Generic packages & outlook

As the optical 'pin-out' of silicon photonic chips increases, costs of optical fiber alignment increase even stronger. Therefore, for research and testing purposes, costs can be reduced to an affordable level only by standardization. Such is possible with a generic fiber pigtailing approach and a generic package for prototyping, by which the non-recurring costs can be spread over a large number of users. In this approach, the chip design is adapted to the package, rather than the other way round.

In that case, when IC designers make sure to keep to some fixed design rules for the placement and configuration of on-chip optical fiber couplers, the resulting chips can be pigtailed and packaged at much reduced cost.

In addition, silicon photonic IC's are going to get electrical contacts. A generic package approach for prototyping should therefore handle both optical and electrical pin-out.

Within the EU-funded ePIXnet Network of Excellence on photonic integration, the authors are working on such a generic package approach under the name of g-Pack. This work is collaboration between ePIXpack ([ePIXpack]), the packaging service platform, and ePIXfab ([ePIXfab]), the silicon photonic IC prototyping service. Both services were set up within ePIXnet. As a result, ePIXfab users will be able to have a number of their chips fiber pigtailed and packaged through ePIXpack for testing purposes. For low-frequency electrical I/O, the engineering cost is relatively small. Therefore, we focus first on the combination of optical fiber connections with DC or low-frequency (~1MHz) electrical contacts, such as for thermo-optic tuners or for switch-

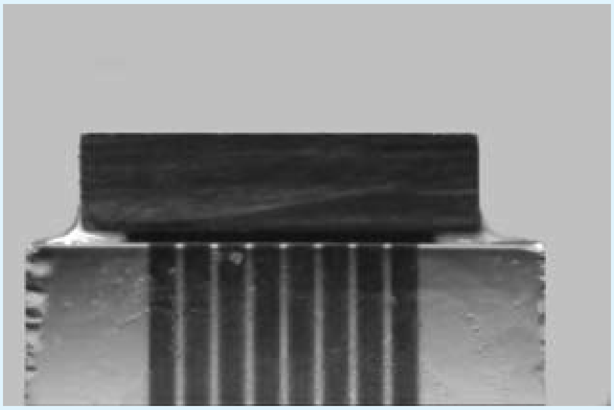


Figure 11. Photograph of the v-groove base with the mounted SOI die.

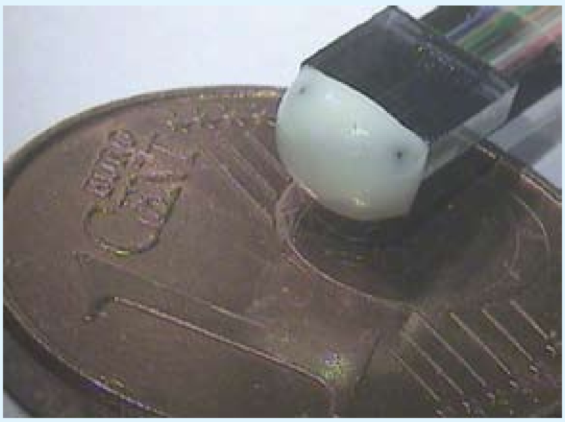
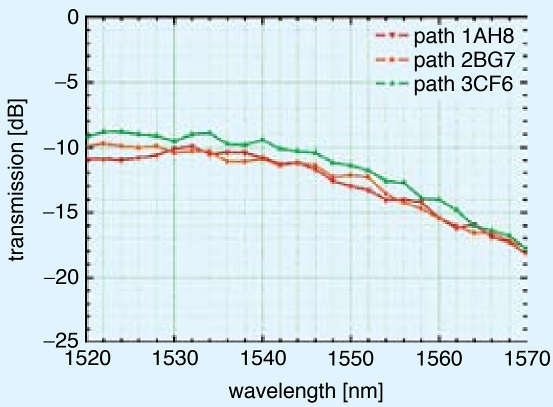


Figure 12. Photograph of the final fiber array package with glob-top protection. The solution is very compact due to the small scale of the nanophotonic die.



Figures 13. Transmission characteristics as measured on the fiber array package. Bandwidth is reduced due to the coupling via 2 gratings. Minimum loss of the couplers would be -9 dB, so a maximum penalty of 2 dB is incurred by fiber array pigtailing process. Uniformity is ± 1 dB.

es. In a later stage, an extension to RF is possible, for instance with a co-planar 50W non-impedance matched approach.

g-Pack is designed for vertical fiber couplers, with a fiber array up to 32 fibers. A first example with an eight fiber array is presently being elaborated ([Zimmermann08_GFP]). The schematic sideview is shown in Figure 14. The g-Pack approach makes use only of commercially available components such as the fiber array and the ceramic pin grid array carrier. The design matches a standardized SOI chip as manufactured by ePIXfab. All optical I/O is mounted along one side of the chip (West), whereas the electrical I/O pads are on the North and South sides, allowing for up to 65 pins. The topview of the g-Pack configuration is shown in Figure 15.

The work presented here has resulted from cooperations within the European Network of Excellence ePIXnet. The work will continue in the framework of the European funded integrated project HELIOS ([HELIOS]).

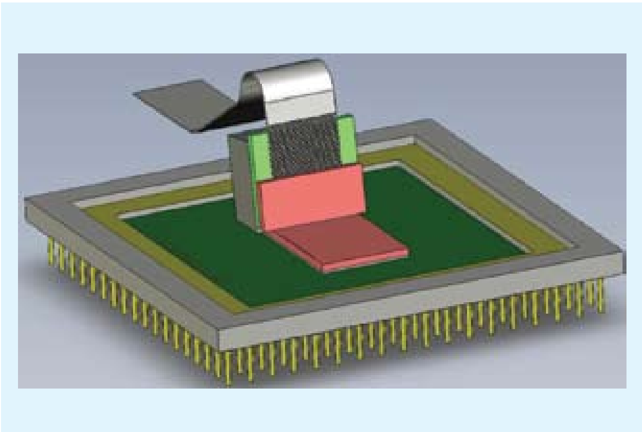


Figure 14. g-Pack, side view. The pin grid array carrier was chosen to provide a large number of DC connects & to comply with standard socket dimensions.

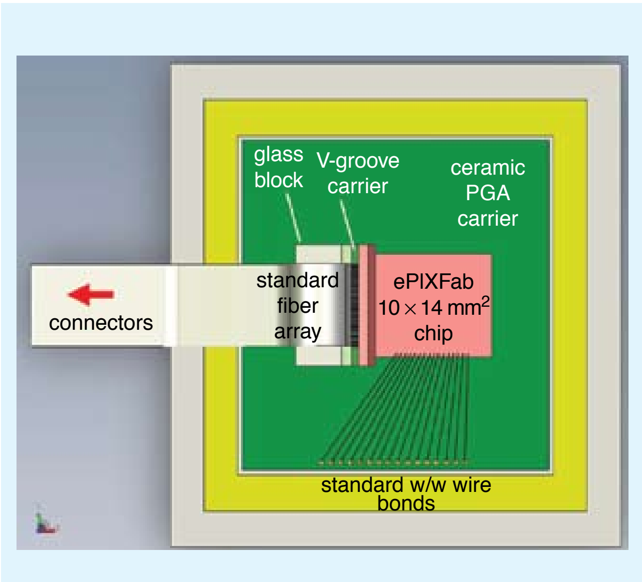


Figure 15. g-Pack, top view. The ePIXFab chip is optically coupled to a commercial fiber array (up to 32 fibers), while electrical connections are established via standard wire bonding techniques.

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