State of the art in optical interconnect technology

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***Abstract*—We review recent progress in opto-electronic components and circuits for optical interconnect networks based on a silicon based photonic wire technology. We discuss the transmitter part, the receivers and the integration with electronics.**

I. INTRODUCTION

The continued reduction in transistor feature sizes has led to a paradigm shift in advanced micro processor design. Instead of further increasing the clock speed and the number of transistors within a single processor, multiple cores, each comprising a smaller number of transistors, are now integrated on a single die. The main driver hereby is the increased power efficiency. However, as a result, on-chip and off-chip communication is becoming increasingly the bottleneck in sustaining the performance growth foreseen by the International Semiconductor Roadmap (www.itrs.net). A total data rate of 50-100TB/s is expected by 2015 and more than double that by 2022, with a maximum allowed power consumption of 0.1 to 1pJ/bit [1]. At this moment there is no known technology (neither using electrical connects, neither using other types of interconnects) that can fulfil this requirement. For that reason several groups worldwide are now investigating the possibility of using an optical interconnect network to replace off-chip interconnects and maybe even the long range on-chip interconnects. Although free space communication has been investigated intensively in the past almost all current work now focuses on guided wave solutions. Solutions using VCSEL arrays and multimode waveguides are rapidly maturing and may be introduced in the coming years for board level interconnects [2]. However, such solutions are not compatible with on-chip optical interconnect. Therefore, approaches using silicon nanophotonic waveguides as the optical backbone are now heavily studied. Different network topologies have been proposed, going from circuit switched networks [3] up to fully interconnected crossbar networks [4-7]. Nevertheless, the basic components from which these networks are built up are rather generic. In most cases wavelength division multiplexing is used for increasing either the capacity or the flexibility of the network. Therefore transmitters capable of generating data at multiple wavelengths, wavelength routing and switching circuits and wavelength selective detectors are required. In this paper we will review state-of-the-art for all these components. We will also discuss how these circuits can be integrated with electronic circuits.

II. PHOTONIC WIRING CIRCUITS

To reach a high bandwidth density the waveguides used to route the traffic should be as small as possible, allow for short bends and exhibit negligible crosstalk even when two waveguides are placed close to each other. To fulfill these requirements a high refractive index contrast between the waveguide core and cladding is required. Therefore most work now focuses on silicon waveguides (n~3.5, with n the refractive index) embedded within a SiO_2 cladding (n~1.5), which exhibits one of the highest refractive index contrasts currently available. Moreover, these circuits can be fabricated using tools available within standard electronics circuit fabrication lines. Fig. 1shows a top view of a spiral waveguide used for measuring propagation and bend losses. The inset shows the cross section of a waveguide. Fabrication typically starts from a silicon-on-insulator wafer having a 2μm buried oxide layer, which will serve as the bottom cladding, and a 220nm silicon waveguide layer on top. For patterning often ebeam lithography has been used [8, 9]. However, we have focused on the use of deep UV lithography because of its compatibility with mass manufacturing [10]. Next the pattern is transferred into the silicon layer using a dry etching process. The typical waveguide losses (for a 450nm wide, 220nm high single mode waveguide) vary from below 1dB/cm (using ebeam lithography [11]) to 3dB/cm and mainly originate from sidewall roughness. Bend losses are as low as 0.04dB per 90^o turn (2μm radius). For a centre to centre waveguide separation of 1.6μm, the crosstalk over a 1cm link is less than 20dB. We also reported waveguide crossings with <0.2dB loss per intersection and splitters with <0.1dB excess loss [12]. As an alternative for using crystalline silicon we also developed a process based on amorphous silicon. Standard amorphous silicon layers exhibits too high losses for practical use. However, by using a process optimized for passivating the dangling bonds, we could reduce the loss of standard strip waveguides down to 3.6dB/cm [13]. This is a low temperature process (<400C) so in principle such waveguides could be defined in the back-end (on top or between the metal layers) of electronic chip fabrication (see also section V). It is of course

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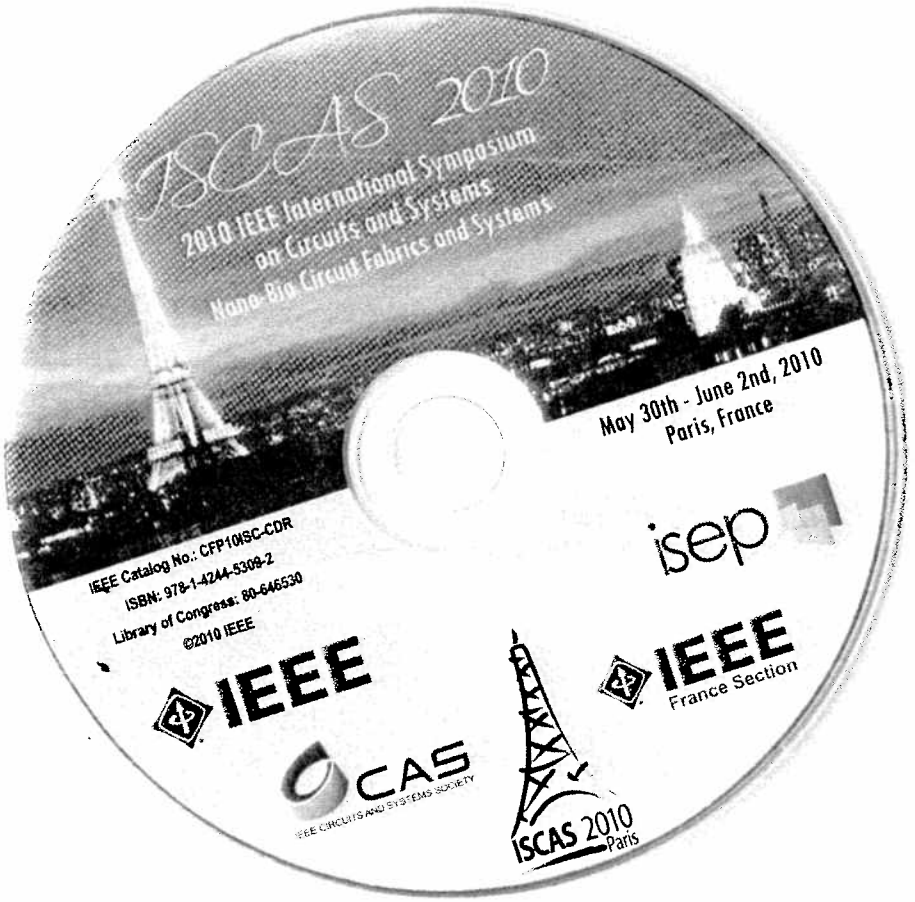
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important that the active components being developed are compatible with these circuits. This will be discussed in sections III and IV.

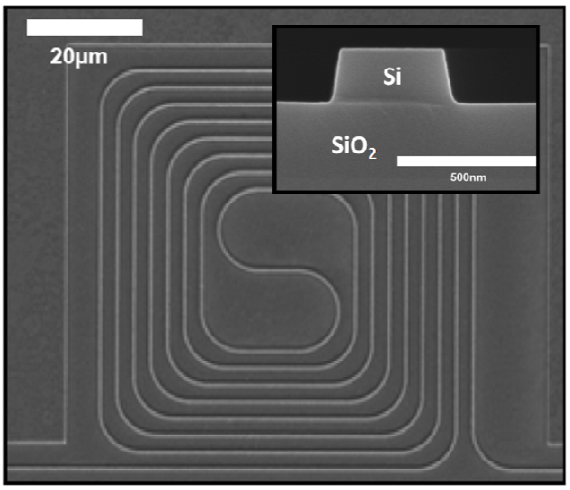

Fig. 1 Silicon on insulator photonic wire circuit (inset: waveguide cross section)(from [12]).

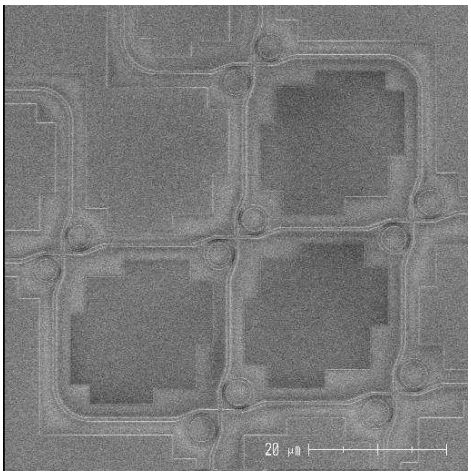

Fig. 2 Optical cross-connect (4x4) build up from individual resonator elements.

Using such silicon nanophotonic waveguides, complex optical filters and switching structures have been demonstrated. Fig. 2 shows a 4 x 4 optical cross-connect build up from individual resonator elements. Each element is tuned to a dedicated wavelength. Signals on this wavelength channel will be switched to the cross channel, while other wavelength channels will simply pass through. A major issue in developing these circuits is their sensitivity to global or local fabrication variations. A dimensional variation in the order of 1nm (0.2% of the line width) will already result in a total loss of the signal. We recently investigated this issue in detail and outlined the limits of the currently available lithography process [14]. In practice either active tuning or more tolerant designs will be required [15].

III. TRANSMITTER

In designing the transmitter for optical interconnect networks, two approaches have been pursued, either using an off-chip source in combination with an on-chip power distribution network and modulators or using on-chip microsources, which are directly modulated. We will shortly discuss both of them below.

A. Use off-chip source

Using an off-chip source avoids the need for implementing an on-chip source, which is arguably the most challenging component from an integration point of view. Also the associated heat management issues are circumvented that way. The drawback is that optical modulators are often large, or if resonant structures are used to reduce their size, they have to be aligned in wavelength to the external pump source. Further, the optical power distribution network may become too complex to handle in larger optical interconnect networks.

Several groups now have demonstrated all silicon modulators, compatible with the photonic wiring circuits discussed above. In most cases a pin-junction is introduced in the waveguide and the modulators work either in injection mode (largest effect but slower) [16, 17] or in depletion mode (smaller effect but faster) [18]. To reduce the length of the modulator, they are sometimes implemented under the form of a resonator, which reduces the useful optical bandwidth but also decrease the footprint considerably. Fig. 3 shows an example of such a modulator, implemented as a ring resonator with 12µm diameter [17]. Using this modulator, the authors demonstrated 3Gb/s data communication with 0.5V modulator voltage swing and a total energy consumption of 120fJ/bit. Modulator speeds up to 18GB/s for injection type modulators (with pre-emphasis) and 40GB/s for depletion type modulators has been demonstrated. The latter are still over one millimeter long though.

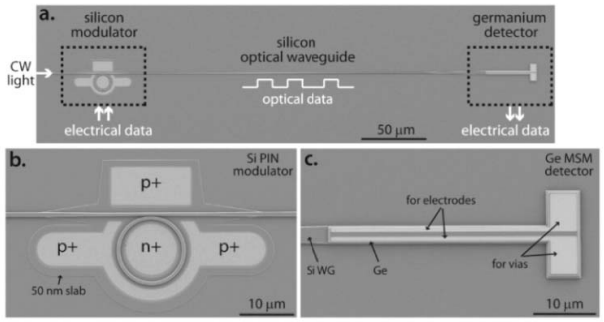

Fig. 3 Optical link with off-chip source, silicon modulator and germanium detector (from [19]).

B. *On-chip directly modulated sources*

As an alternative, people are now also pursuing the possibility of using compact directly modulated optical sources. Several approaches are being investigated. A large amount of effort has been put into the use of erbium, e.g. coupled to silicon nanocrystals [20] and recently, lasing from strained germanium was demonstrated [21]. However, the gain of these materials remains relatively low and the demonstrated devices require long (several mm) cavities and high pumping currents. Therefore, in our own work, we have focussed on the integration of III-V direct band gap semiconductor based devices on silicon, using wafer bonding approaches [22]. Thereby high quality InP-based epitaxial layers are bonded on-top of preprocessed silicon waveguides. Subsequently the substrate is removed and the optoelectronic devices are defined collectively using waferscale processes.

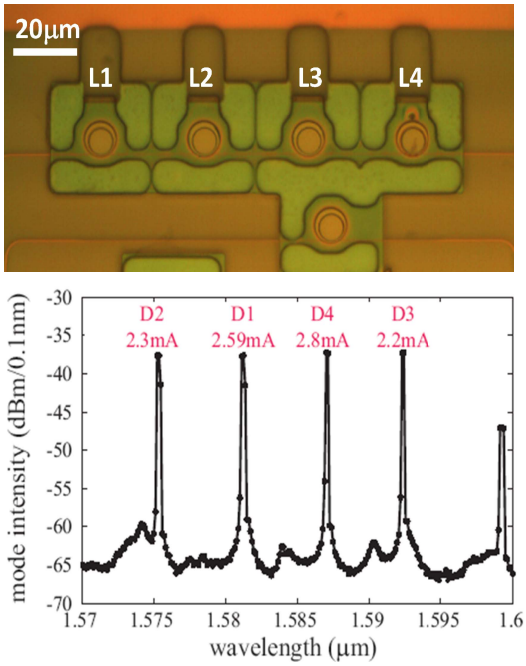

Fig. 4 Fabricated multiwavelength laser before metallization, composed of four MDLs on a single silicon bus waveguide. Spectra of multiwavelength lasers with 6 nm are also shown. The bias current of each MDL is indicated on the corresponding lasing peak (from [23]).

Using this heterogeneous integration technology we demonstrated electrically injected microdisk lasers coupled to a silicon nanophotonic waveguide exhibiting a threshold current of only 350µA, a diameter of 7.5µm and up to 200µW coupled into the underlying silicon waveguide [24]. By coupling multiple such lasers to a single bus waveguide a compact multiwavelength transmitter can be realized. This is illustrated in Fig. 4, which shows such a laser (before metallization) and the associated optical spectrum. Using these sources we also demonstrated direct optical modulation, all optical wavelength conversion, external modulation and all-optical switching [25].

IV. Detectors

Several groups now have demonstrated Ge-detectors integrated with silicon nanophotonic waveguides (e.g. see [17, 26, 27]), exhibiting high efficiency up to 1580nm, a capacitance of a few fF and acceptable dark current. The main challenge is the large lattice mismatch between silicon and germanium (4%). In [17] a GeOI-SOI wafer (Germanium bonded on insulator) was used to overcome this issue. Most groups however have adopted an epitaxial growth based integration process, using an optimized two step process, starting with a thin low temperature Ge buffer layer, followed by a high temperature active layer. Using such a process, in [26] a 42GHz pin photodetector was demonstrated with a 1A/W efficiency (size 15x3µm). At 1V reverse bias, the devices exhibited a dark current of 18nA.

V. Integration

Obviously the optoelectronic components have to be integrated intimately with suitable driver electronics and associated logic circuits. We have focused on integrating the photonic interconnect layer in the back end process, either using 3D-interconnect techniques or using low temperature amorphous silicon waveguides. This has the advantage that the fabrication process for the photonic layer and the electronics can be decoupled, leading to lower development costs and possibility for separate testing (in the case of 3D-integration). The relatively long distance from electronic driver circuits to the optics, through the metal layer stack, may lead to higher power consumption however and this has to be investigated in detail. This issue may be overcome by integrating the photonics layer directly in the front end [7]. However, in that case a lot of expensive floor space is used for the optic circuits. It also requires a redesign of the optical layer for each new generation of electronics.

VI. Conclusion

A lot of progress has been made in developing the basic components needed for an optical interconnect layer. Also a good understanding of possible network topologies has been build up. Nevertheless, still a lot of work needs to be done. In particular the power consumption of the transmitter and optical switches has to be further lowered. Also strategies for compensating fabrication inaccuracies and thermal drift without increasing power consumption have to be proposed. This will be the topic of our future work.

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