10de firw doctoraats-symposium

9 december 2009

Het Pand
Onderbergen 1
9000 Gent

UNIVERSITEIT GENT

FACULTEIT INGENIEURSWETENSCHAPPEN

Athermal SOI ring resonators by overlaying a polymer cladding on narrowed waveguides

Jie Teng

Supervisor: Geert Morthier

I. Introduction

With mature CMOS (Complementary Metal Oxide Semiconductor) fabrication technology, silicon based devices have the potential to provide highly compact circuits with low cost, multifunctionality and enhanced performance. However, the large temperature dependence of silicon material degrades the performance of silicon-based devices ($dn/dT=1.8\times10^{-4}$/°C). To stabilize the chip temperature to a constant level, external heaters or coolers have to be employed. This element takes extra space and reduces the power efficiency of the whole chip.

In this work, we introduce a simple way to suppress the temperature dependence of silicon based devices. The wavelength temperature shift of the silicon ring resonator is reduced to less than 5 pm/°C, almost 11 times lower than normal silicon waveguides.

II. Theoretical Analysis

A standard SOI (silicon on insulator) structure with a height of 220nm is used for designing the athermal waveguides (Figure 1). Polymer PSQ-LH with a large TO coefficient of -2.4×10^{-4}/°C and low loss at 1550nm is chosen as the cladding material. To obtain athermal silicon waveguides, the dimension of the silicon waveguide should be highly reduced to allow more light coming out of the core waveguides into polymer to use polymer's negative TO coefficient to counterbalance silicon's positive TO coefficient. The $d\lambda_m/dT$ of standard 500nm width SOI waveguides is near to +60pm/°C. By narrowing the width of SOI waveguides, $d\lambda_m/dT$ is reduced to zero and then becomes negative. From the theoretical calculation results, the ideal width for athermal silicon waveguide is around 306nm.

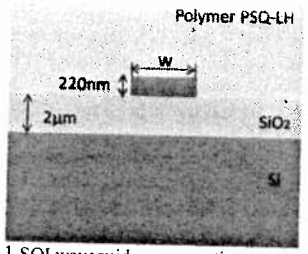


Figure 1 SOI waveguide cross-section structure

III. Fabrication & Measurement Results

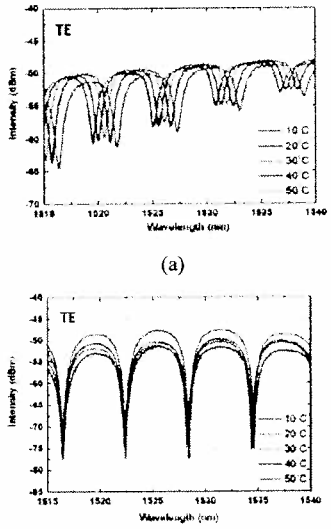
A. Fabrication

The narrow SOI waveguides in this paper are fabricated by deep UV lithography with standard CMOS fabrication technology. This technology offers both the required resolution and the throughput for commercial application. Simple racetrack ring resonators with different waveguide widths are fabricated as shown in Figure 2.

J. Teng is with Department of Information Technology Department (INTEC), Ghent University (UGent), Gent, Belgium. E-mail: Jie.Teng@UGent.be .

Figure 2 SEM pictures of fabricated ring resonators with a width of 350nm

B. Measurement results



(a)

(b)

Figure 3 Transmission spectrum of a ring resonator with width of 350nm at different temperatures (a) before overlaying a polymer cladding (b) after overlaying a polymer cladding (Width=350nm, Gap=180nm, L=2μm, R=15μm)

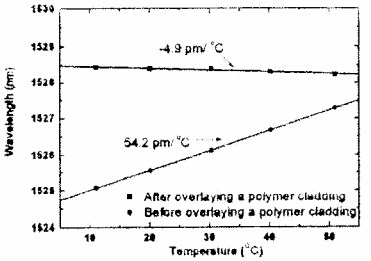


Figure 4 Linear fit of the wavelength versus temperatures

To measure the transmission spectrum at different temperatures, the sample is mounted on a heating system to accurately control the chip temperature. Figure 3 shows the measured transmission spectrum of a ring resonator (Width=350nm, Gap=180nm, L=2μm, R=15μm) for temperatures from 10°C to 50°C with an interval of 10°C. By linear fitting of one resonance wavelength at different temperatures, the wavelength temperature dependence $d\lambda/dT$ is extracted (Figure 4). As shown in Fig.4, the wavelength temperature dependence of the 350nm-width ring resonator is reduced from 54.2pm/°C to -4.9pm/°C after overlaying a polymer PSQ-LH cladding, almost 11times than normal SOI waveguides . The ideal width for the athermal ring resonator is found to be around 350nm, a little different from the theoretically calculated value of 306nm.

Acknowledgements

The fabrication of the SOI circuits was done by CEA-LETI through ePIXfab (www.epixfab.eu). Jie Teng acknowledges CSC scholarship and Ghent University BOF cofounding.