Heterogeneously Integrated SOI Compound Semiconductor Photonics

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Abstract *We present a review of recent progress in III-V on silicon heterogeneous integration technology. Both fabrication technology and devices are discussed.*

Introduction

Silicon has been shown to be an excellent material for realising compact photonic integrated circuits (PIC) operating in the telecom wavelength range (1100nm-1600nm). Crystalline silicon has very low intrinsic propagation losses and both large core fiber matched waveguides and extremely compact so-called photonic wire circuits have been demonstrated. Through carrier injection or depletion the real and/or imaginary part of the refractive index can be changed, allowing for switching and modulation of light. Since silicon is intrinsically transparent at these wavelengths, integration with other materials is required however for realizing efficient optical sources and detectors. The latter are now typically based on Ge, integrated with the silicon waveguides using heteroepitaxial growth techniques. Although being investigated intensively, these have had only limited success thus far for integrating compound semiconductors on silicon however, which is required for realizing compact light emitters and amplifiers. Therefore, several groups developed an alternative integration scheme, based on waferbonding technologies, which avoids the growth step but still allows for a process compatible with waferscale processing techniques. The latter is not only important from a cost perspective, but it also allows for accurate alignment of the active devices with respect to the underlying circuits. This paper reviews work of different groups in this field. In the following section the integration approach is described in more detail. Next, an overview of several fabricated devices is given.

Integration approaches

A classic approach in integrating III-V semiconductor devices with silicon (and silica) PICs is based on flip-chip bonding. In that case prefabricated optoelectronic devices (e.g. a DFB laser array) are bonded upside down on a suitable substrate (e.g. a recess in the PIC) [7]. In some cases the substrate is largely removed before bonding ([8, 9]). No or little comprises are required in the design of the optoelectronic devices and they can be pretested. Therefore, for small to medium volumes this is certainly an attractive route, although reaching the required placement accuracy (typically +/- 1um) is far from trivial and the interface can exhibit considerable loss. For large scale integration however, there is a need for an integration approach compatible with waferscale technologies as described above.

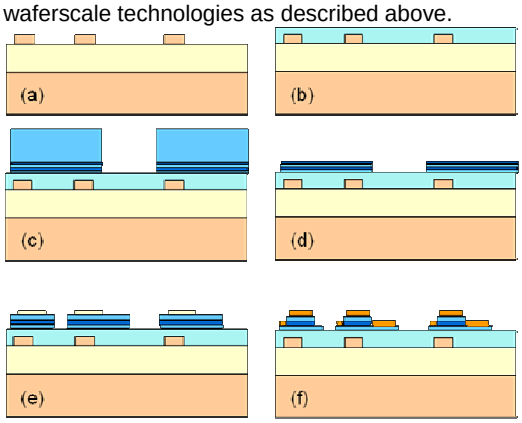

Fig. 1: Typical integration scheme

The basic scheme as developed by several groups now is shown in Fig. 1. The starting point is a wafer containing the silicon waveguide circuits. Next, the compound semiconductor material is bonded on these circuits using some variation of classic wafer bonding technologies, with the epitaxial layers facing the silicon waveguide circuits (Fig. 1c). Then the substrate of the compound semiconductor material is removed using a combination of grinding and chemical etching, leaving a wafer which is again

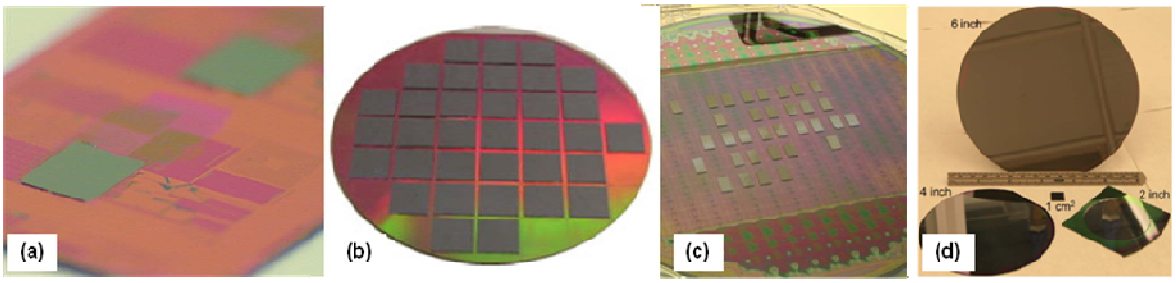

Fig. 2: (a) BCB-bonded InP dies on SOI (from [1]) (b) BCB-bonded InP dies on IBM CMOS (from [2]) (c) InP dies on SOI through molecular bonding (see [3, 4]) (d) Direct bonded InP-wafers on SOI (from [5, 6])

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compatible with classic waferscale processing technologies such as pattern definition (Fig. 1e), etching and metallisation (Fig. 1f). Several variations of the bonding process (Fig. 1c) have been developed. Roelkens e.a. [10] developed an adhesive die-to-wafer bonding process using BCB as a planarization layer (Fig. 1b) and as the bonding agent. Fig. 2a shows a SOI-substrate containing passive waveguide circuits with 2 300nm thick InP-based epitaxial layer structures bonded on top. The adhesive BCB layer was approximately 100nm thick in this case [1]. A similar approach was demonstrated in [2] albeit for a totally different application: the integration of InP HBTs with CMOS. In this case (Fig. 2b) the substrate consisted of a fully processed IBM 130nm RF-CMOS wafer, cut to 3 inch wafers. The BCB-layer has the advantage of being self-planarising, is very tolerant to roughness and small particles, is chemically resistant and is compatible with postprocessing temperatures of at least up to 350C. In [3] a so-called molecular bonding process is developed. In this case the substrate wafer is planarized using silica deposition and CMP (chemical mechanical polishing) and also the InP is covered with a 5-20nm thick SiO_2 layer. Following careful cleaning of both surfaces they are brought into contact and bonding is initiated through van der Waals forces. Fig. 2c shows a 200mm SOI wafer containing silicon waveguide circuits with several III-V dies bonded on top. [5, 6]. The SiO_2 interlayer can vary from a few tens of nanometer up to several micrometer. The use of the SiO_2 interlayer makes the process generic and compatible with many substrate types. The molecular bonding process is very sensitive to microroughness and particles on the surface and typically some variation of a micro-cleanroom is needed to perform the bonding step. This is also the case for the direct bonding process illustrated in Fig. 2d. In this case there is no interlayer. To enhance the bonding strength, a plasma activation step was employed [5, 6]. Contrary to the work described in Fig. 2a-c, this work focuses on wafer-to-wafer bonding. Bonding of up to 150mm InP-wafers was demonstrated. These are currently the largest InP substrates commercially available. Full wafer bonding is less sensitive to edge effects and is a better known process compared to die-to-wafer bonding. However, while the most common InP substrates are 2-4inch, all advanced silicon processing is typically carried out on 200mm or 300mm wafers. Therefore, a lot of useful area may get lost when performing only full wafer bonding. Nevertheless it is clear that the most appropriate strategy will depend strongly on the business model chosen. If post-bonding processing is carried out in a CMOS line as in [4] then the substrate must be a 200mm. However, if postprocessing is carried out in a traditional InP-fab, than the original substrate can be cut in smaller wafers ([2]) and full wafer bonding may be more advantageous. In the first case (processing in CMOS fab), adaption of traditional processes such as InP-etching and metallization processes to the CMOS line are obviously required. These efforts are currently under way (e.g. see [11]).

In [12] a variation of the process shown in Fig. 1 is used: in this case the bonding takes place on an unpatterned SOI substrate and silicon waveguides are formed together with the fabrication of the III-V devices. A direct bonding process was employed.

Heterogeneously Integrated Devices

The first electrically injected III-V on silicon lasers were demonstrated in 2006. In [13], Fabry-Pérot lasers were demonstrated using an approach whereby most of the light is concentrated in the III-V area of the laser section and coupled to the silicon waveguide through a polymer taper once exciting the laser facet. In [14] a hybrid integration platform was demonstrated whereby most of the light is concentrated in the silicon waveguide and the mode is evanescently coupled to the waveguide region on top. This platform was rapidly extended to more complex laser designs. DFB-lasers as well as DBR-lasers were demonstrated, with output powers of respectively over 4mW and over 9mW. In combination with quantum well intermixing (prebonding) for defining regions with different band gap also integrated sampled grating DBR-EAMs were shown. See [6] for a recent review.

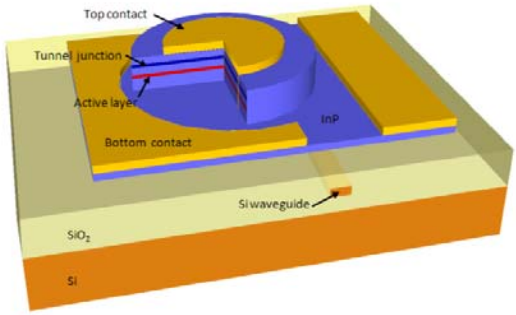

Fig. 3: Microdisk source schematic

For short reach interconnect applications and all-optical signal processing however low power laser sources are required. Therefore we developed electrically injected microdisk sources, employing a whispering gallery mode in a III-V semiconductor disk structure. Initial devices had a threshold current of 0.5mA and where limited in output power [4]. In recent devices, having an improved heat sink, the threshold current was reduced to 0.260mA and the output power (CW operation) increased to 0.120mW [15]. These devices can also be used as electro-optic modulators [16], all-optical wavelength convertors [17] or as part of a compact multi-wavelength laser [18].

Conclusions

Heterogeneous integration of compound semiconductors has proven to be a very powerful platform for realising efficient sources integrated with silicon waveguides. Further improvement will require new device structure, e.g. using photonic crystal structures for improved light confinement [19] or new material types. Promising candidates are self-assembled materials such as colloidal quantum dots [20] or compound semiconductor nanowires [21].

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