Silicon-on-Insulator Spectral Filters Fabricated With CMOS Technology

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Abstract—We give an overview of recent progress in passive spectral filters and demultiplexers based on silicon-on-insulator photonic wire waveguides: ring resonators, interferometers, arrayed waveguide gratings, and echelle diffraction gratings, all benefit from the high-index contrast possible with silicon photonics. We show how the current generation of devices has improved crosstalk levels, insertion loss, and uniformity due to an improved fabrication process based on 193 nm lithography.

Index Terms—Arrayed waveguide grating (AWG), echelle grating, nanophotonics, photonic wire, planar concave grating (PCG), ring resonator, silicon-on-insulator (SOI), silicon photonics.

I. INTRODUCTION

SILICON photonics has become one of the focus technology platforms for photonic integration in the last ten years. This can be mainly attributed to the combination of a very high-index contrast (and thus strong miniaturization) and the compatibility with CMOS fabrication technology [1], which allows the leverage of existing investments in electronics fabrication facilities. As we will discuss extensively in this paper, silicon passive waveguide technology has been steadily improving in terms of performance, uniformity, and reproducibility [2]–[4]. In addition, over the past years, there have been many demonstrations of integrated active devices, including modulators [5], Germanium-based photodetectors, and even III–V integrated sources and detectors [6], [7].

The essential components we will discuss here are, different types of wavelength filters- or spectral filters. With such filters, one can separate a broad spectrum into wavelength channels.

This is essential for wavelength division multiplexing (WDM) communications, but it can find also important applications in sensing [8]–[10] or spectroscopy. In Section II, we discuss the operational principles of waveguide-based spectral filters and the implications on the technology.

Silicon photonic wires confine light in a submicrometer waveguide core, enabling sharp bends, and thus, compact components. Compared to silica waveguide technologies or even many III–V semiconductor waveguides, the reduction in chip real estate for a given function is reduced with several orders of magnitude. Put differently, silicon photonics can integrate more components on the same chip area [1]. The high index and sharp bends also reduce the footprint of many wavelength filtering components, such as ring resonators or wavelength demultiplexers based on arrayed waveguide gratings (AWGs) [11] or planar echelle diffraction gratings [12]. The operating principles of these different spectral filters are described in Section II.

Silicon photonic circuits feature submicrometer components, which are well within the capabilities of today's industrial fabrication tools based on 193 nm optical projection lithography for electronic circuitry [13], compared to the previous technology generation based on 248 nm lithography [1], [14]. In Section III, we show more details on how we use such industrial tools to make high-quality silicon photonic wire circuits. This has been an essential part of our paper in the past ten years, possible because of the research facilities in Interuniversity Microelectronics Center (IMEC), which combine many high-end industrial CMOS fabrication, including 248 and 193 nm optical lithography steppers in a research environment. Recently, we have switched for the pattern definition to the shorter illumination wavelength, dramatically improving pattern fidelity and device performance. In addition, we have standardized on the use of two different etch layers to incorporate waveguide structures with both a high- and a low-lateral-refractive index contrast. The shallow etch is also used to define diffractive gratings, which are used for coupling light in to and out of the chip.

In Section IV, we discuss basic photonic wire waveguides for on-chip interconnections, and the implication for spectral filters. The obvious performance metric here is the waveguide loss, but also some essential components, such as low-loss crossing and splitters are being discussed. [15]. Section V continues to present recent experimental results for a variety of wavelength selective devices: ring resonators, Mach–Zehnder interferometers (MZI), AWGs, planar concave gratings (PCG), and splitters.

Finally, in Section VI, we take a quick look beyond the performance of a single device and into the reproducibility of device functionality from wafer to wafer, as well as uniformity within a wafer. This is essential for the filter components discussed here, as the optical length of delay lines must be controlled to a very high accuracy. We will show that IMEC's advanced CMOS technology is capable of supporting very stable processes for nanophotonic devices with linewidth uniformities down to a few nanometers. While this might seem much for wavelength selective components, this is a remarkable technological feat on an industrial platform used to tolerances of 10% (5% for the more recent deep submicrometer nodes). Also, the spread in CDs is sufficiently low to enable low-power tuning of the optical length of delay lines using thermal or carrier-based effects.

II. SPECTRAL FILTERING

A. Principles

Spectral filters (wavelength filters) are used for functions such as multiplexing many frequency channels into one waveguide, selecting one or multiple channels from an incoming bundle, equalizing channel powers, and dispersion compensation. Linear wavelength filters work by interference of multiple light paths, which experience a phase delay with respect to each other that is usually a multiple of a certain unit delay. The interfering paths can be spatially separated waveguides, giving a *feedforward* mechanism, or self-interfering paths in a resonant optical structure, giving a *feedback* mechanism. Multimode interference in a single (waveguide) structure is also a possible approach. Feedforward and feedback filter stages can be combined to yield more complex devices with a larger degree of freedom in design. Note that the properties of feedback and feedforward filter stages are very different, for instance with respect to group delay. Only with suitable feedforward filters, it is possible to achieve linear phase behavior (and then only if they are designed for that purpose).

The choice for a filter architecture depends very much on the application, which can traditionally be found in optical communications, but is now being used increasingly for spectral sensors or spectroscopy. In some cases, a single large demultiplexing device, such as an AWG may be ideal, while in other cases, for instance, when much more fine-grained control is needed, multistage filters are necessary.

Most filters are based on the concept of a unit delay length ΔL by which light paths in the filter are delayed with respect to each other, and the filter order m that defines how many times the wavelength fits in the unit delay. The frequency at which constructive or destructive interference is obtained, resulting in a maximum or minimum transmission from a certain input to a certain output, is then defined by $f_0 = mc/n_{\text{eff}}\Delta L$, with n_{eff} be the effective index of the waveguide at that frequency. For filters implemented with silicon-on-insulator (SOI) photonic wires, it is important to realize that this effective index is very dependent on the wavelength. Therefore, in a first-order approximation, it is the group index of the waveguides, which determines other aspects of the filter transmission, such as free spectral range (FSR), channel separation, and transmission-line

shape. The FSR is given by $\Delta f_{\text{FSR}} = c/n_g\Delta L$. In the silicon photonic wires discussed here, the group index is quite large, between 3.4 and 4.0, depending on the waveguide width. Also in order to study the dependence of the filter characteristics on influences such as temperature or fabrication tolerances, the group index should be taken into account. For instance, in a first-order approximation, the temperature dependence of a filter spectrum around a frequency f_0 is given by

$$\frac{df_0}{dT} \approx -\frac{n_{\text{eff}}}{n_g}f_0\left(\frac{\partial n_{\text{eff}}}{\partial T}\frac{1}{n_{\text{eff}}^0} + \alpha\right) \quad (1)$$

with α the thermal expansion coefficient.

This thermal dependence can be a problem for some applications, it can also be actively harnessed as a tuning mechanism to alter the optical delay length, and therefore, the filter behavior [17]. In photonic wires, the thermal shift is of the order of 80–90 pm/°C, or about 10 GHz/°C. If thermal tuning is not an option, it is also possible to reduce thermal dependence by introducing a cladding material with opposite thermal shift [18], [19] but this requires careful tuning of both the waveguide geometry and the material properties.

B. Single Channel Filters

In order to select a single channel out of a broader spectrum, multiple approaches are possible. With a resonant filter such as a ring resonator, a very sharp channel selection is achieved. Ring resonators in SOI can be as small as $10 \times 10 \ \mu m^2$, yielding a FSR, which easily exceeds 10 nm. The feedback in the resonator gives rise to a strong field enhancement, which can be used for applications such as sensing [8]–[10]. However, this field enhancement can have detrimental effects, as silicon ring resonators will exhibit distorted spectra due to nonlinear effects (mainly secondary temperature effects) even for very modest input powers [20], [21]. An experimental example is shown in Section V.

In MZI only two contributions interfere, which results in a simple sinusoidal filter characteristic. As they do not induce feedback, there is no field enhancement in the waveguides and they do not suffer from unwanted nonlinear effects, even at milliwatt power levels. Filters based on MZ stages can be designed to drop a single (or multiple) channels from a set of incoming channels. However, multiple filter stages are needed to achieve a sufficient extinction and channel separation [11]. However, in such filters, the coupling ratio between the stages is very critical to the correct filter behavior. Also, the delay lengths in the stages should be correctly matched. For many real-life applications, mainly in communications, a tuning mechanism to fine-tune both the coupling strength and the delay length will be necessary, but good process control can help to keep the required tuning power low.

C. Channel Demultiplexers

To demultiplex a broad spectrum into many wavelength channels simultaneously, usually a different approach is taken and a larger device is used, tailored to that function. The two major types are echelle gratings (PCG) [12] and AWGs [11], [22].
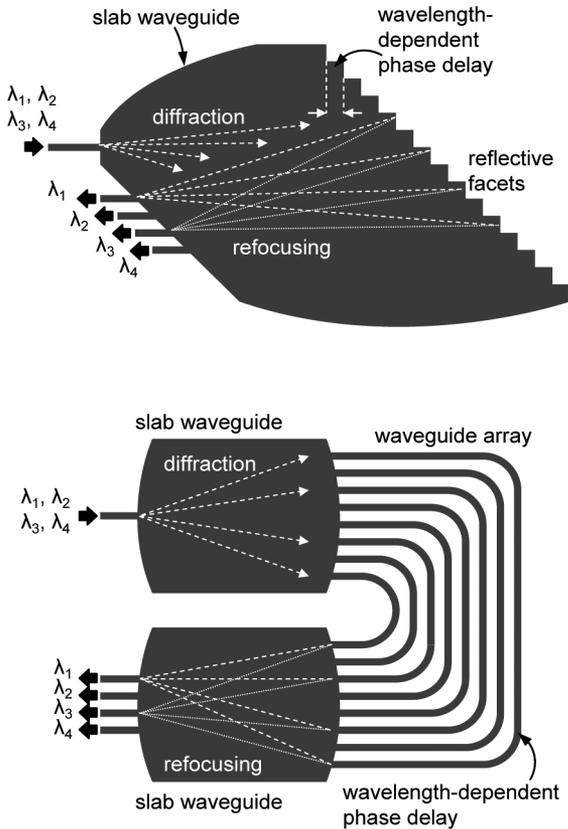
Fig. 1. Operating principles of distributed wavelength demultiplexers. (Top) Echelle grating. (Bottom) Arrayed Waveguide Grating.

Again, these are based on interferometry, but here a multipath delay is combined with a "free-space" focusing medium. This is illustrated in Fig. 1. In both types of devices of which we will demonstrate experimental examples, the focusing function is implemented in an SOI slab waveguide. This is combined with a diffractive grating, where the facets/teeth exhibit a phase delay with respect to each other. In the AWG, this phase delay is obtained by splitting the incoming signal over many different waveguides (with an increasing delay length) mounted in an array. In a PCG, the phase delay is obtained by a difference in path length between the grating teeth for a freely propagating beam in a slab waveguide.

While the governing principles of both devices are similar, there are some distinct differences. In a PCG, the delay medium is the slab waveguide, i.e., the same as the focusing medium. While this can lead to more efficient use of space, it also results in a larger physical delay length (for a given set of specifications, such as FSR) because the ratio of n_g/n_{eff} of the slab medium is lower than that of a photonic wire. Also, the shared diffraction/refocusing medium gives restrictions on the positioning of input and output waveguides. The physical scaling of a PCG layout is inversely proportional to the channel spacing, for narrower wavelength channels, the spatial focusing resolution of the device needs to be increased, which requires a larger slab region. For a fixed tooth size, this requires a higher grating tooth count.

On the other hand, in AWGs two focusing regions are needed, but in return there is a much larger design freedom. Input and output waveguide design can be largely decoupled. It is also easier to tune the individual delay lines (lowering phase noise introduced by geometric fluctuations), there is more freedom to arrange the physical layout, and the delay lines will typically be shorter because of the higher group index. Their footprint scales in more complex way than a PCG, dictated by a combination of FSR (a large FSR translates into a short delay line), number of channels (many channels need more delay lines), and physical layout parameters, such as bend radius and waveguide spacing.

Both PCGs and AWGs can be used in parallel by multiple inputs, and in AWGs, it is possible to use the delay lines in both directions simultaneously [23]. This can be an elegant approach to ensure that the delays are exactly identical without having to resort to active tuning mechanisms.

III. FABRICATION AND CHARACTERIZATION

A. Fabrication With CMOS Technology

We fabricate our devices using industrial CMOS tools suitable for 130 and 90 nm transistors. This includes the same optical lithography as used for the fabrication of CMOS electronics. In contrast, with most research groups in silicon photonics, we make use of optical projection lithography instead of e-beam writing. Originally, we used 248 nm deep UV lithography for the photonic circuit definition, but recently we have switched to the the higher resolution of 193 nm lithography. The waveguides are made in SOI, where a 220-nm-thin silicon layer with refractive index $n = 3.45$ acts as a waveguide layer, separated from the silicon substrate by a 2 μm buried oxide cladding layer ($n = 1.45$).

The use of SOI for photonic circuits makes it compatible with CMOS processes in terms of materials and processing chemistry. This implies that photonics can be made in the same tools, but the requirements in terms of feature size and layer thickness are quite different from those for electronics. The devices discussed here are made on industrial 200 mm tools used for a 130 and 90 nm CMOS technology node. A mask pattern is defined using 193 nm optical projection lithography. After baking and developing, the pattern is transferred into the silicon using an inductive coupled plasma reactive ion etch (ICP-RIE) etch. Finally, the resist is stripped [3]. The recent switch from 248 nm lithography [1], [14], [24] to 193 nm lithography has resulted in a considerable improvement in terms of fidelity of the fabricated structure to the original design. This is illustrated in Fig. 2, due to the spatial low-pass filter effect of the optical system, this simple splitter design exhibits severe corner rounding with 248 nm lithography. With 193 nm lithography, this effect is dramatically reduced.

B. Deep and Shallow Etch

Photonic wires, with their large index contrast, enable sharp bends and compact interconnects. However, in some cases, a lower index contrast is desirable. This can be achieved by using a shallow etch, which results in an effective lateral index
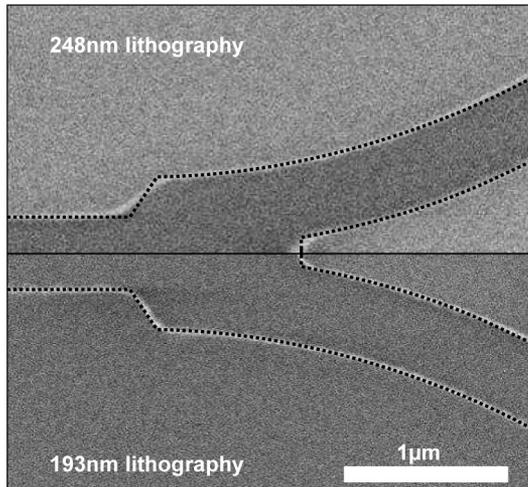
Fig. 2. Improvement in fabrication fidelity from 248 nm lithography to 193 nm lithography.

Fig. 4. Transition between a photonic wire and a lower contrast rib waveguide.
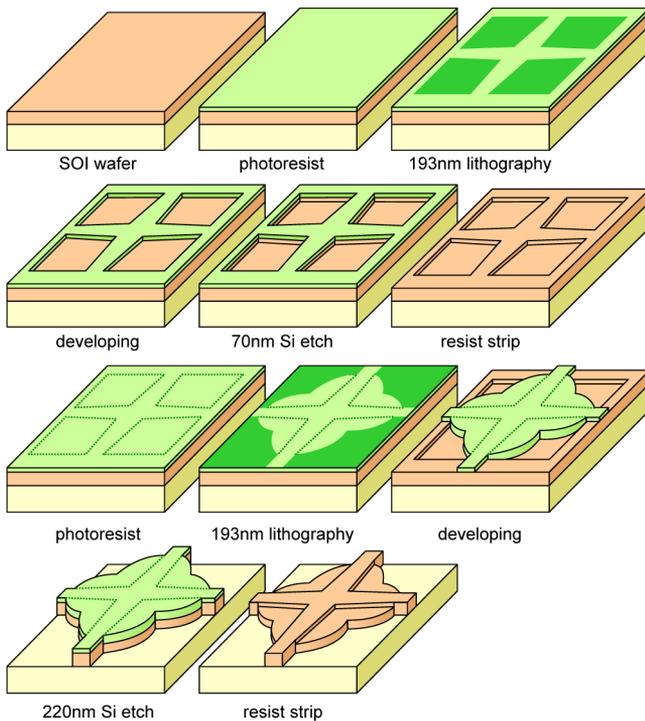

Fig. 3. Fabrication process for passive silicon nanophotonic waveguide components, illustrated with the waveguide crossing in Fig. 7. Two etch layers are used. First, as shallow-etch layer is patterned, which contains diffraction grating couplers and low-contrast rib waveguides. After that, the deep-etched regions, such as the waveguide trenches, are defined.

contrast of 2.8 to 2.5. To combine these low-contrast waveguides with photonic wires, we use two etch layers. First, shallow-etch regions (70 nm etch depth) are defined, followed by the deeply etched waveguide trenches. This is shown in Fig. 3. With this dual index contrast, we can make very compact devices without some of the penalties that come with the high-contrast photonic wires. Overlay alignment accuracy between the two etch layers is better than 20 nm, due to the wafer-scale alignment functions in the lithography steppers.
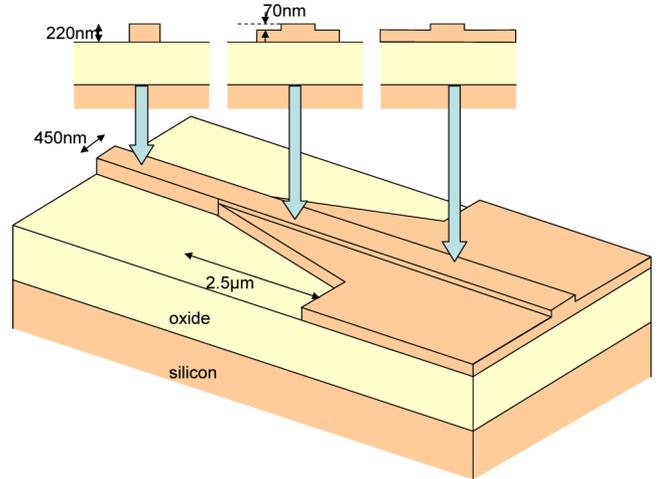
To couple from a photonic wire with a 450 nm width to a low-contrast rib, we use the transition in Fig. 4. The deep-etch waveguide is flared out over a length of a few micrometers. Inside this deep-etch taper, we etch the shallow waveguide. As the deep taper expands, the shallow waveguide will take over the confinement of the light.

C. Measurements With Grating Couplers

We measure the transmission of the devices using diffractive grating couplers [25]. These consist of 70 nm deep lines etched in a 10 μm broad waveguide to get the best overlap with a standard single-mode fiber. The fabrication is done in the same shallow-etch step as the low-contrast waveguides. The fiber is oriented at a 10° angle with the vertical [24]. Coupling efficiency is 33% (-5dB) per grating. In contrast to more efficient edge-coupling schemes [26], [27], this technique does not require any cleaving or polishing, and is therefore, very attractive for packaging and wafer-scale testing. Higher coupling efficiencies can be obtained by further optimizing the design and introducing new degrees of freedom in the processing [28], [29]. The fiber couplers used here couple the light into the waveguide TE-mode (the electric field largely in the plane of the chip).

Note that it is also possible to implement TM-mode waveguides as well as TM-mode grating couplers. However, the current choice of layer thickness favors the use of TE polarization, as this is the fundamental mode of a waveguide of 450 nm width. This width is chosen because it is single mode, gives the smallest mode size (that is, for TE), and therefore, allows for quite sharp bend radii. TM modes are typically less confined, and in the case of a shallow-etched waveguide structure, the TM mode is very prone to leak to TE modes in the shallow-etched slab waveguide [30].

IV. WAVEGUIDES

A. Propagation LOSSES

The quintessential component of a photonic integrated circuit is the waveguide. Not only does it transport light over the chip
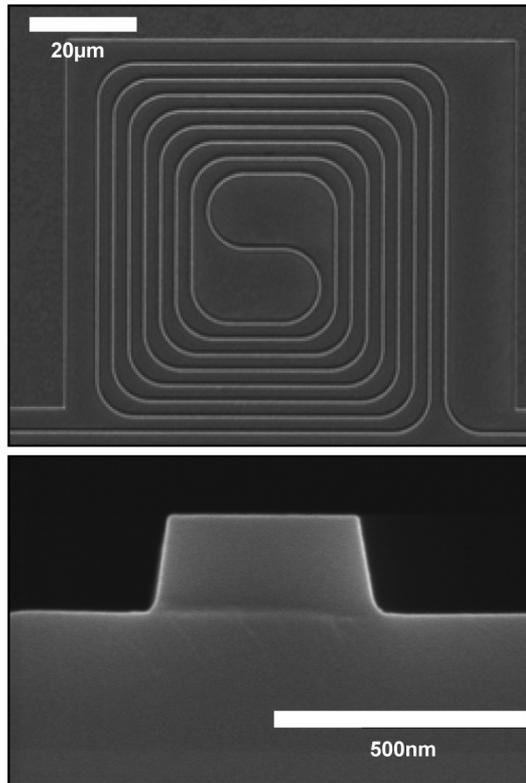
Fig. 5.   SOI photonic wire. (Top) Spiral waveguide for waveguide loss characterization. (Bottom) Cross section.
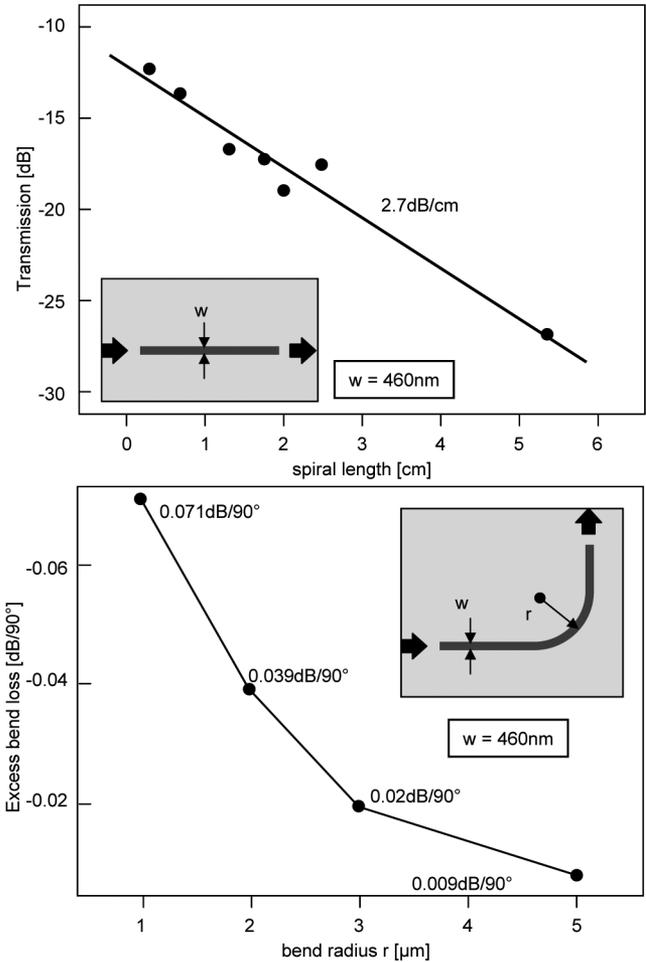

Fig. 6.   Losses in photonic wires, extracted from spiral waveguides as shown in Fig. 5. (Top) Propagation of straight waveguides. (Bottom) Excess loss in bends.

surface, it also acts as a functional element in spectral filters. Therefore, waveguide quality must be sufficiently high in order to implement useful functions. The waveguide also dictate the scale of integration. For this, they should have a compact core with high confinement, which allows dense packing and sharp bends, and the propagation loss should be sufficiently low such that a typical light path on a chip does not introduce unacceptable losses. In a silicon nanophotonic circuit, this typical length is of the order of a few millimeters to 1 cm. A spiral waveguide, as well as a cross section, is plotted in Fig. 5. The waveguide losses, as well as the excess bend losses are plotted in Fig. 6. For wire widths between 400 and 500 nm, the straight losses are a uniform 2.7 dB/cm. These numbers are similar, or even slightly lower than results published by other groups with comparable facilities [31]. Excess bend losses depend on the bend radius, increasing sharply for short bends. For bends larger than 3 μm, the bend losses are becoming negligible. Similar waveguides fabricated with the less accurate lithography at 248 nm have losses of the order of 7 dB/cm [1]. Somewhat lower propagation losses have been reported using e-beam lithography [32], [33], but these techniques do not lend themselves to mass fabrication. Alternatively, waveguides with lower loss can be made by reducing the lateral confinement [34], but this in turn, increases the bend radius, and therefore, the integration density.

To reduce losses over longer distances, the waveguides are flared out to wider widths in long straight sections. While this results in multimode waveguides, adiabatic tapering suppresses the excitation of higher order modes. Also, in the bends the

waveguide width is reduced to 450 nm, where higher order modes are suppressed. The expanded width is 3 μm for access waveguides, and 800 nm for shorter delay lines. In these delay lines, the wider width also reduces the phase errors introduced by sidewall roughness and nonuniformity [11].

B. Crossings

In larger, more complex photonic circuits, routing the waveguides can give rise to topology problems, which can only be solved by either routing waveguides on different levels or using direct waveguide crossings. Unlike in electronics, transferring light from one circuit layer to another is not straightforward, while conversely, it is possible to directly intersect two waveguides. However, the high-refractive index contrast of a silicon photonic wire has, as a consequence, a simple direct crossing of two nanophotonic wires that will introduce substantial loss (about 30%) and crosstalk (-10 dB). Therefore, the crossing geometry need thorough optimization, which we can make easier by combining the deep and shallow etch, as shown in Fig. 7. One possibility is using a multimode interferometer (MMI) to tailor the phase front at the intersection, but this approach
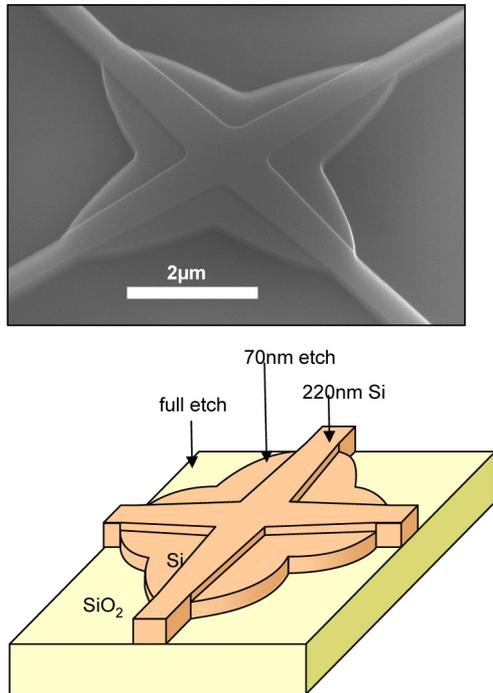
Fig. 7. Low-loss waveguide crossing. Reflections and crosstalk are minimized by locally reducing the refractive index contrast with a shallow-etch step.
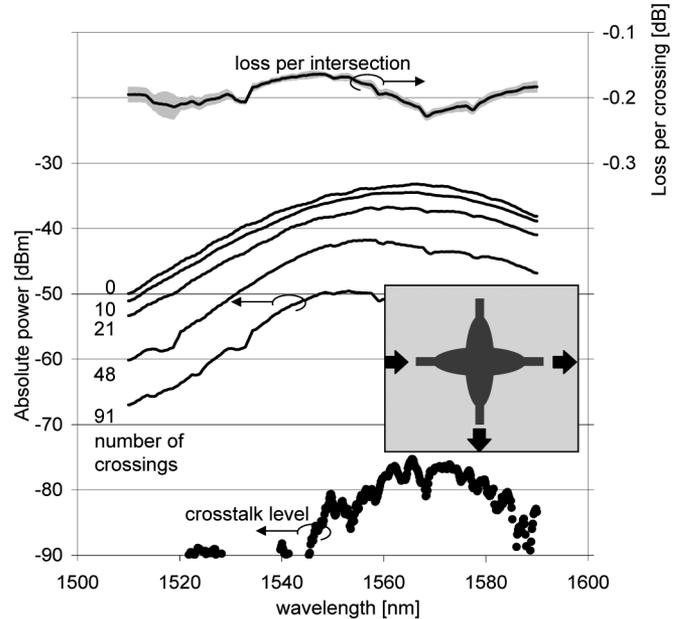

Fig. 8. Low-loss waveguide crossing. Reflections and crosstalk are minimized by locally reducing the refractive index contrast with a shallow-etch step. (Left) SEM picture showing the two etch regions. (Right) Transmission as a function of wavelength.

results in a rather large crossing area and also some unwanted reflections [35]. Alternatively, we can locally reduce the index contrast of the shallow-etched waveguide, and the additional degree of freedom gives us to possibility to optimize the phase fronts of the light in the crossing in such a way that it is almost flat at the center, suppressing diffraction and crosstalk [15]. As discussed later, this shallow etch is a step that is already used to fabricate the grating-based input–output structure. If such a shallow etch is not possible, a more rigourous optimization of the geometry at the intersection can already reduce the loss to 0.2 dB [16].

Fig. 8 shows the transmission of a series of up to 90 crossings. From this, the loss per crossing can be extracted. By careful optimizing the design, we reduced crossing losses to -0.15 dB and crosstalk to -40 dB, in an area of less than $6 \times 6 \ \mu m^2$.

C. Splitters

A similar approach can be used for other components, which have strong discontinuities. MMIs are such an example. These can be used to redistribute light in different waveguides. The simplest example is a 1×2 symmetric splitter, which can be used for signal distribution or to split light in a symmetric MZI. Fig. 9 shows an MMI-based splitter, where the transition between the waveguide and the MMI are implemented in a shallow-etched waveguide. The excess loss of the entire splitter (including deep-shallow waveguide transitions) is of the order of -0.2 dB or less, with an imbalance lower than 0.02 dB (measured on a serial chain of splitters). It is tolerant to fabrication errors up of 100 nm for a maximum allowed splitter loss of only 0.20 dB. This also ensures a broadband operation.
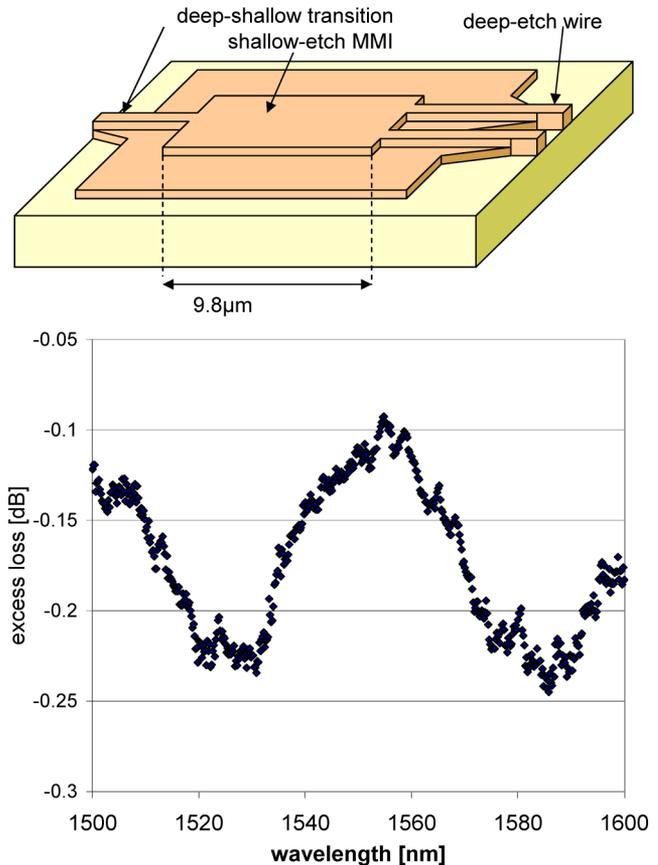

Fig. 9. Photonic wire splitter based on a shallow-etched MMI. (Top) Concept of a shallow MMI. (Bottom) Measured excess loss as a function of wavelength.
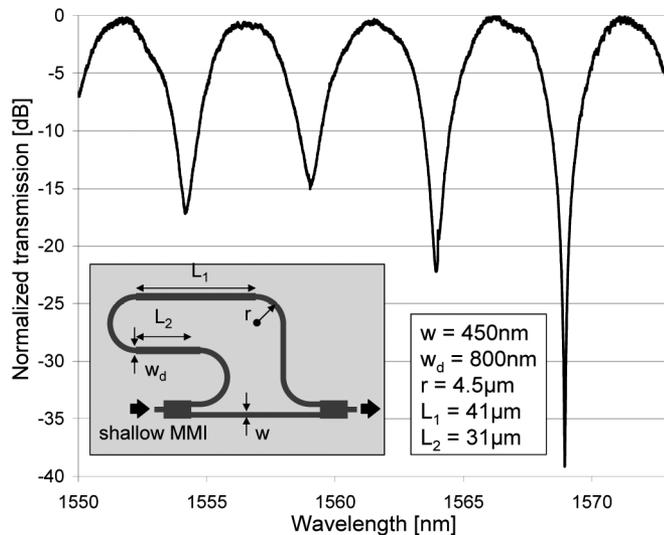
Fig. 10. Transmission of an asymmetric MZI with splitter and combiner implemented in a shallow-etch MMI.

Fig. 11. Normalized transmission of a ring resonator with a Q of 9500 at different power settings. Due to the field enhancement in the ring, the nonlinear effects in the ring strongly distort the resonance, leading to bistable behavior.

This is a significant improvement to the more simple (yet more compact) splitter design in Fig. 2, where the excess splitter loss was of the order of 1.5 dB.

V. FILTERS: EXPERIMENTAL RESULTS

A. Mach–Zehnder Interferometers

A waveguide-based MZI consists of a splitter, two waveguides with a given group delay, and a combiner. When the splitting and combing ratio is 50%, the MZI is balanced. In this case, we can obtain complete destructive interference when the phases in both arms are opposite. In other words, an MZI can be used as a filter, but also to evaluate the balance of a splitter, or the excess loss of one arm with respect to the other. Fig. 10 shows the transmission of an asymmetric MZI using shallow-etched MMI couplers. The insertion loss of the device is much less than 1 dB. From the ratio between adjacent minima and maxima, we can extract the imbalance in the arms, either due to coupling or excess loss in the delay line. From the plot, we can see that the extinction ratio is wavelength dependent, which translates in an imbalance ranging from a 45/55 around 1560 nm to an almost perfect 50/50 ratio near 1570 nm.

While a single MZI is limited to such a sine-like spectral filter characteristic, cascading with different coupling ratios can be used to construct complex filters [11], [36]. However, there it becomes very critical to control both the coupling constants in each coupler, as well as the spectral alignment of the various filter stages. This can be accomplished using external tuning mechanisms (e.g., local heaters).

B. Rings

Ring resonators can be used as wavelength filters when the wavelength fits a whole multiple times in the circumference of the ring [11], [37]. In most cases, the light in the bus waveguide is 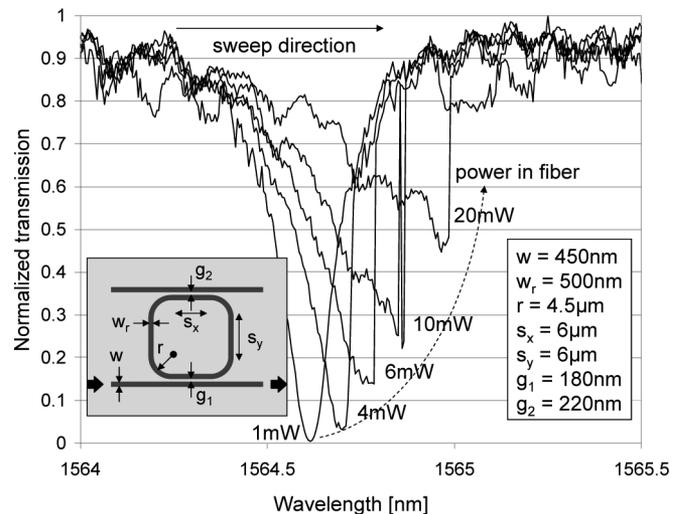coupled to the ring using a directional coupler, but MMI-based couplers are also possible. On resonance, light is transferred to the drop waveguide. The quality factor Q of the ring determines the bandwidth of dropped wavelength range, with higher Q values resulting in a narrower spectral peak. These compact ring resonators are possible in photonic wires because of the short bend radius. A compact ring allows for a large FSR, which allows us to use the ring over a wide spectral bandwidth. However, the combination of high Q values and strong confinement of light gives rise to strong nonlinear effects. These lead to distortion or degradation of the resonance, and even bistable behavior [20], [21]. This is shown in Fig. 11, where inserted power in the access waveguide is increased strongly and the filter shape of the ring is dramatically altered. The effect here is illustrated using a linear wavelength sweep (from short to longer wavelengths) with a tunable laser.

To measure the filter shape of a ring, we therefore use a very low-power level (0.5 mW), to keep the nonlinear effects much smaller than the linear behavior. The transmission of a ring filter in both pass and drop ports is shown in Fig. 12. After fitting, the quality factor Q in both ports matches closely to a value around 15 500. Coupling efficiency on resonance is around 90%. By changing the coupling section and the bend radius, quality factors and drop efficiencies can be tuned in a relatively wide range [8], [11], [37]. Smaller bends give rise to higher bend losses, and this can lower the Q of the ring. Still, rings with bend radii of 2 μm and smaller have been shown to have Qs of around 5000 [38]. Such small rings can also have a quite large FSR up to 50 nm [39]. To obtain the desired functionality, the coupling and round-trip length need to be controlled well, especially when constructing higher order filters based on multiple rings in series or in parallel [40], [41].

However, while such rings appear to be a very efficient way to implement wavelength filtering with a very small footprint, this is only useful at very low powers, as the nonlinear effects will
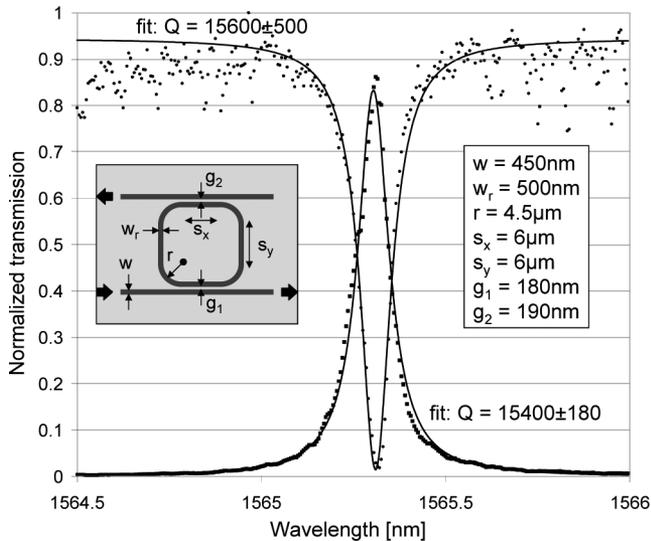
Fig. 12. Transmission of a ring resonator drop filter in SOI. Both the pass and the drop ports are shown. Q of both curves is of the order of 15 500.

quickly come to dominate due to the strong power enhancement in the ring.

C. Echelle Diffraction Grating

Implementing echelle gratings in an SOI waveguide configuration is relatively straightforward by etching reflective facets in the slab. An example is shown in Fig. 13. When using a single reflective interface ("Fresnel reflection"), the reflection is only about 30%, with results in a high insertion loss of the device [12]. However, this can be improved by using strong Bragg mirrors in the facets (see inset in Fig. 13) [42]. This increases the reflectivity to over 80%. Also, we can reduce the insertion loss by using a shallow etch at the waveguide–slab interface.

The nature of such echelle gratings is that the size scales inversely with the channel spacing. Therefore, a demultiplexer with 30 channels spaced at only 400 GHz (3.2 nm) as presented here, will be much larger than a coarse demultiplexer with only a few channels [12], [42]. Still, the device in Fig. 13 has a footprint of only 0.5 mm^2. This device was measured using a 1 mW broadband light source and an optical spectrum analyzer (OSA). Unlike rings, this device is not resonant and nonlinear effects are much weaker. The transmission of the 30 output ports is plotted in Fig. 14. The insertion loss is 3 dB for the center wavelength channels, and rolls-off to 6–7 dB for the outer channels at longer wavelengths. This is still relatively high, and can be partially attributed to imperfect reflections at the DBR facets, which have a wavelength-dependent reflectivity, which is lower beyond 1580 nm. Near-channel crosstalk is relatively high at −15 dB, but this rolls-off to a −25 dB crosstalk level. Again, scattering at corners can be a source, as well as inhomogeneities in the slab thickness. This latter effect becomes more important when the device area is larger. With a large FSR and a large channel count, this PCG device has possible applications in near-infrared spectroscopy.
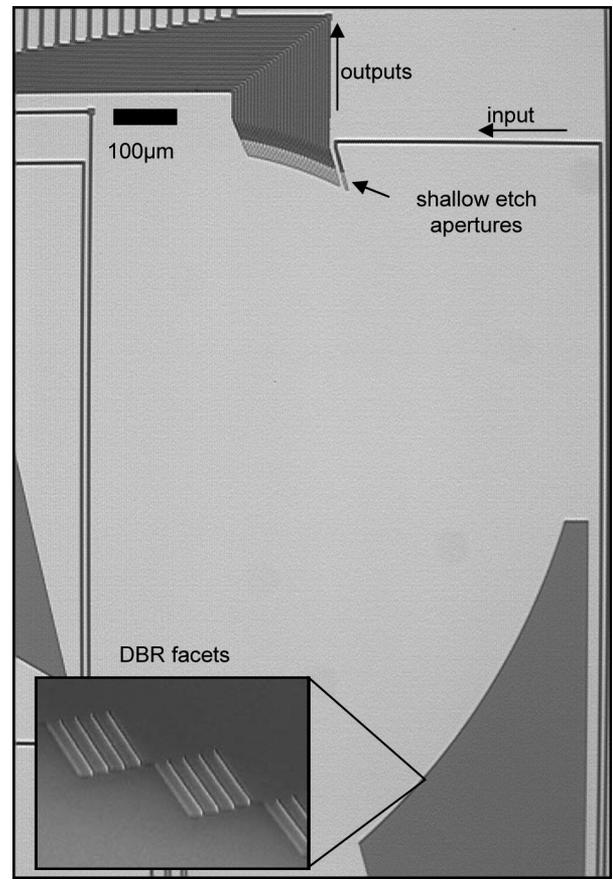

Fig. 13. Planar concave echelle grating with 30 wavelength channels and facets consisting of distributed Bragg reflectors (DBR).

Fig. 14. Transmission of all 30 outputs of the demultiplexer in Fig. 13 overlaid on top of each other. Insertion loss of the center channels is 3 dB with a roll-off to the outer channels to 6–7 dB.

D. Arrayed Waveguide Gratings

For narrow wavelength channels, AWGs scale better. An AWG with 8×400 GHz channels is shown in Fig. 15, taking a footprint of only 200×350 μm^2. An echelle grating with the same configuration would be similar in size to the one discussed above, but scaling up this AWG to 30 channels would result in
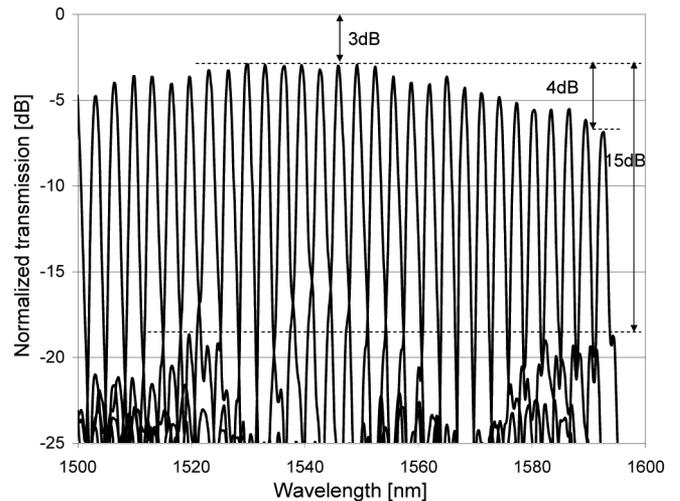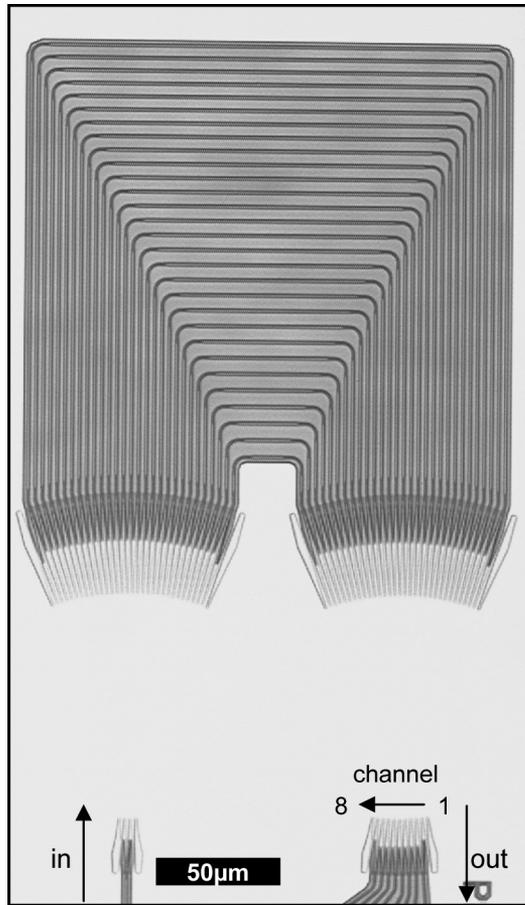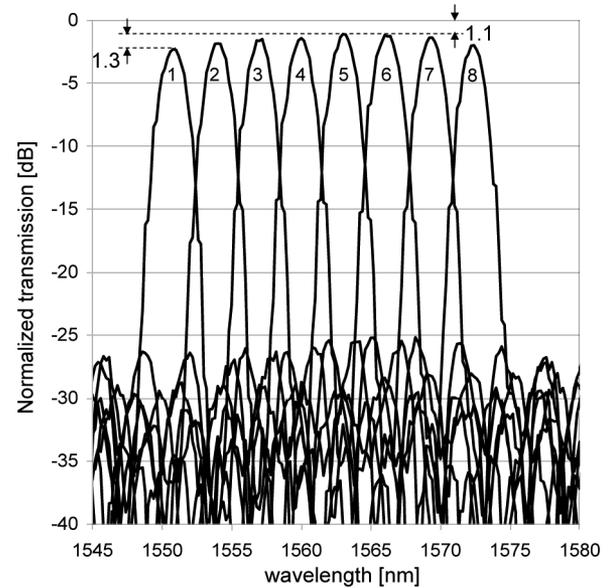
Fig. 15.   AWG with 8 × 400 GHz channels.

Fig. 16.   Transmission of all eight outputs of the AWG in Fig. 15 overlaid on top of each other. Insertion loss of the center channel is 1.1 dB with a roll-off to the outer channels to 2.4 dB.

a device that has at least the same footprint. On the other hand, the AWG can scale down to smaller channel spacings with less penalty than the echelle grating.

The transmission of the eight channels, measured in the same way as the echelle grating, is plotted in Fig. 16. Insertion loss is exceptionally low at 1.1 dB for the center channels, which can be attributed to several factors. Here, too, the waveguide–slab interface is implemented in a shallow etch, and the arrayed waveguides are widened in the straight sections to reduce losses as well as phase noise [11]. The low-phase noise translates into a low crosstalk level, at −25 dB.

VI. Effect of Fabrication Process

An undesirable consequence of the high-index contrast and tight confinement in SOI waveguides is the increased sensitivity to imperfections, such as the scattering at roughness on the core–cladding interface [43]. Also, wavelength filters are susceptible to phase fluctuations due to small changes in waveguide geometry (width, SOI slab thickness, etc.). While these can often be compensated by active tuning mechanisms, this will consume power, and it is not always possible to tune over a large wavelength range. Therefore, to minimize these effects, it is important to have a very good pattern fidelity, as well as a good uniformity (e.g., constant waveguide width over the entire

wafer) and reproducibility (constant width from wafer to wafer and batch to batch). More than resolution, this dictates the need for high-quality fabrication tools, such as the CMOS fabrication equipment used for this paper. These same requirements are ever more important for electronics as the features shrink, and this development is also beneficial for nanophotonic fabrication.

To give an idea of the performance in terms of uniformity and reproducibility of these fabrication processes, we will present here some isolated results.

A. Uniformity

To characterize uniformity, we measure multiple identical reference designs over a die, as well as over an entire wafer. Fig. 17 shows the transmission of nominally identical four MZIs on a single chip, arranged in pairs spaced several millimeters apart. The MZIs here are less advanced than the device in Fig. 10, using the abrupt splitter from Fig. 2 instead of the shallow-MMI-based splitter from Fig. 9. From this, and from die-to-die measurements, it is possible to extract a map of both short-range and long-range uniformity over the wafer. Within a single die, we see that the uniformity of the wavelength of the dip is within 1 nm. Note that this is far more accurate than can be extracted from direct physical measurements, such as SEM inspections. This uniformity is much better than what can be achieved with previous generations of optical lithography, such as 248 nm deep UV lithography [1]. There, we find a uniformity of the wavelength dip of several nanometers, using the same photomask [2], [13].

B. Reproducibility

To get a view on the reproducibility between wafers, we did a SEM inspection of the most critical dimension (CD): the linewidth of a standard waveguide, which is designed for
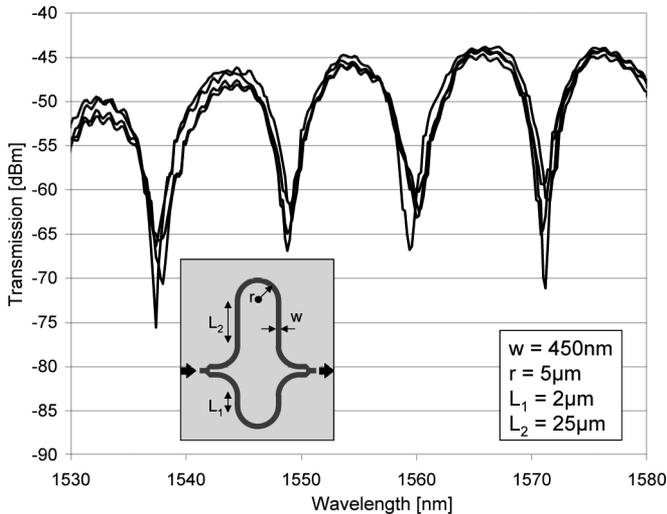
Fig. 17. Transmission of four identically designed MZIs on the same chip, spaced 25 μm apart in pairs, with the pairs spaced several millimeters. Uniformity of the dip wavelength is within 1 nm.
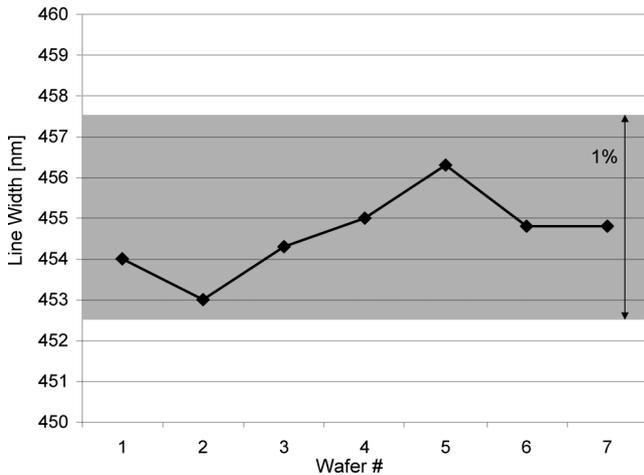

Fig. 18. Linewidth as measured through SEM inspection of a 455 nm waveguide, for different wafers in the same batch. The 1% window is shaded.

450 nm. These measurements (which included several points per wafer) are shown in Fig. 18 and indicate a very good reproducibility, well within a window of 1% of the CD, or a few nanometers. Note however that this value is of the same order as the measurement error. Still, it gives a good indication of the reproducibility of the process.

VII. CONCLUSION

We have discussed recent progress on spectral filters in SOI nanophotonic waveguides, fabricated with advanced CMOS tools. Due to improved processing, using 193 nm lithography compared to 248 nm lithography [1], [24], the performance of the devices has significantly improved compared to previous device generations. The new process results in better pattern fidelity, higher efficiencies, lower insertion losses, and very good uniformity and reproducibility. Waveguide losses are below 3 dB/cm (from 7 dB/cm) with low bend losses. Using the

combination of a deep and shallow etch, we managed to make standard building blocks like crossings and splitters with an excess loss of about 0.15 dB. We have shown ring resonators with good drop efficiency and quality factor of about 15 000, well-balanced MZ filters, and demultiplexers with insertion losses as low as 1.1 and −25 dB crosstalk. Especially, these wavelength filters will benefit most from the improved processing, as they are exceptionally prone to imperfections.

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