Focused-ion-beam lithography for prototyping of silicon photonic components

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Silicon-on-insulator is rapidly emerging as the material system of interest for future photonic devices for the consumer market. Optical lithography with 248 nm and 193 nm UV lithography on wafer scale is the ideal tool for volume production of devices [1,2]. However, due to the cost of masks and processing it is expensive and often slow to fabricate prototypes of new device concepts with optical lithography. Furthermore feature sizes are limited to more than 100 nm, which is not sufficient for various new concepts.

These problems can be circumvented by a hybrid approach: UV lithography followed by a serial lithography technique with higher resolution. For mass fabrication one could use electron beam lithography. On dedicated tools a minimum feature size and overlay accuracy below 20 nm are feasible.

We propose an alternative technique, Focused-ion-beam (FIB) lithography, where a ceramic/metallic layer is directly patterned by sputtering. This process can be performed in a machine without high energy column (> 50 keV) and without interferometric translation stage. The pre-patterned sample is first covered with a 50 nm layer of sapphire (Al_2O_3) and a 50 nm layer of titanium by evaporation. These layers follow the topography of the sample; and the titanium layer is conductive, which guarantees easy visual overlay alignment to existing structures. In the second process step the Ti layer is etched by Focused-ion-beam lithography, where the sapphire layers acts as a protective mask for the underlying silicon structures. In a subsequent step the sapphire layer is opened by chemical etching. Then the silicon is etched in an Inductively Coupled Plasma (ICP) where the sapphire layer acts as hard mask. This is depicted in Figure 1. Finally the sacrificial layers are removed chemically.

We have optimized the process for etching both broad (~400 nm) and narrow (~100 nm) trenches in the 220 nm top silicon layer of a silicon-on-insulator substrate. The silicon was etched in an SF_6/O_2 inductively coupled plasma. The resulting slits have nearly vertical sidewalls, as shown in Figures 2 and 3. We believe that this technique can be further optimized to etch 50 – 100 nm wide slits.

1. S. Selvaraja, P. Jaenen, S. Beckx, W. Bogaerts, P. Dumon, D. Van Thourhout, R. Baets, LEOS Annual Meeting 2007, United States (2007)
2. P. Dumon, W. Bogaerts, V. Wiaux, J. Wouters, S. Beckx, J. Van Campenhout, D. Taillaert, B. Luyssaert, P. Bienstman, D. Van Thourhout, R. Baets, IEEE Photonics Technology Letters, 16(5), p.1328-1330 (2004)

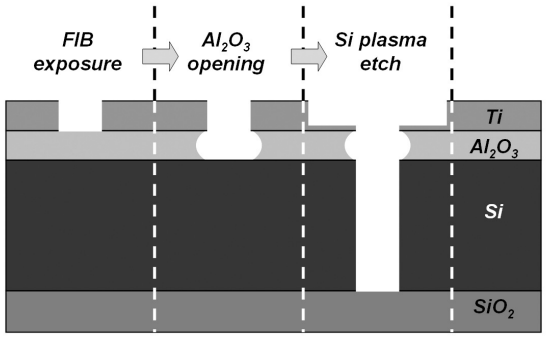

Figure 1. Schematic overview of the three-step process flow. In the first step Al_2O_3 acts as etch stop layer and protects the silicon, in the final step Al_2O_3 is again etched slowly and acts as hard mask.

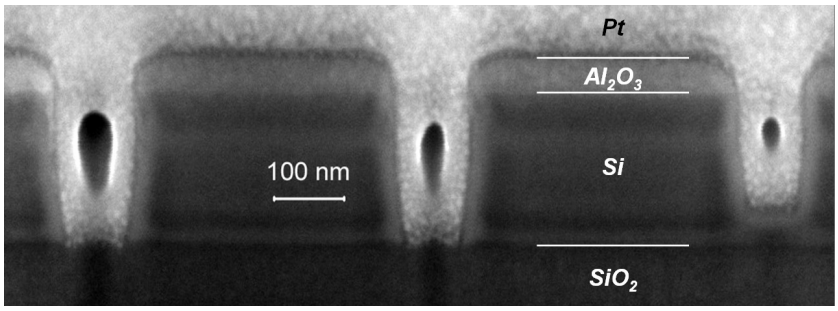

Figure 2. Cross-section micrograph of fabricated 100nm wide slits in the top 220 nm silicon layer of a silicon-on-insulator substrate. Pt was deposited in the slits to keep them intact while making the cross-section with FIB.

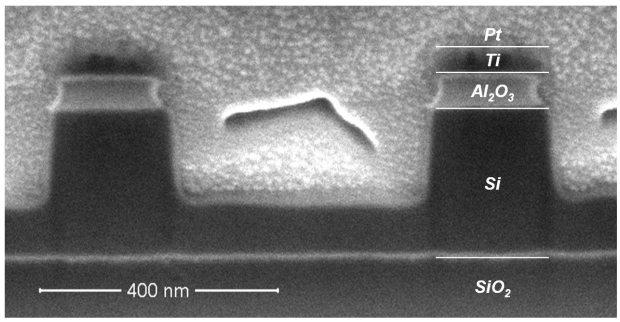

Figure 3. Cross-section micrograph of fabricated 400 nm wide and 150 nm deep trenches in the top 220 nm silicon layer of a silicon-on-insulator. Some Ti is still visible on top of the Al_2O_3.