Planar Concave Grating Demultiplexer With High Reflective Bragg Reflector Facets

J. Brouckaert, *Student Member, IEEE*, W. Bogaerts, *Member, IEEE*, S. Selvaraja, *Student Member, IEEE*, P. Dumon, *Student Member, IEEE*, R. Baets, *Fellow, IEEE*, and D. Van Thourhout, *Member, IEEE*

***Abstract*—We present measurement results of an ultracompact four-channel silicon-on-insulator planar concave grating demultiplexer fabricated in a complimentary metal–oxide–semiconductor line using deep-ultraviolet lithography. The demultiplexer has four output channels separated by 20 nm and a footprint of only 280 μm $\times$ 150 μm. The crosstalk is better than -25 dB and the on-chip loss is drastically reduced down to 1.9 dB by replacing each facet by a second-order Bragg reflector.**

***Index Terms*—Demultiplexing, diffraction, distributed Bragg reflector (DBR), grating, silicon-on-insulator (SOI).**

I. Introduction

PLANAR spectrographs like arrayed waveguide gratings (AWGs) [1] and planar concave gratings (PCGs) [2] are one of the key components in wavelength-division-multiplexed optical communication systems. These devices have been realized in many material systems including silica-on-silicon, III–V's, and large core silicon-on-insulator (SOI) substrates [2]. AWGs fabricated in these material systems have become increasingly popular due to their more simple and tolerant technology as compared to PCGs. Grating-based devices require deeply etched grating facets and the insertion loss of these devices critically depends on the verticality of these deeply etched grating facets.

We recently demonstrated a PCG demultiplexer fabricated on a nanophotonic SOI platform consisting of a 220-nm-thick Si layer on top of a 1-μm-thick SiO_2 burried layer on a Si substrate [3]. This material system has gained much research attention in recent years due to several factors. First of all, photonic components can be fabricated in a complimentary metal–oxide–semiconductor line on high-quality substrates. Second, the large omnidirectional index contrast allows us to dramatically reduce the size of these devices by making use of nanophotonic waveguides. On top of that, the nanophotonic SOI platform offers certain specific advantages for the fabrication of PCGs as compared with other material systems. Besides the reduction in size, performance can be increased due to the fact that the grating facets only need to be etched 220 nm deep. This has some important consequences. First of all, the strict tolerances on facet verticality, which exist in other material systems, are strongly relaxed. Second, a more perfect grating profile can be obtained without the need of dedicated deep etching techniques, and third, since the Si slab only supports one guided TE- and TM-polarized mode, there is no deterioration of insertion loss and crosstalk caused by coupling to higher order modes [3].

The four-channel SOI PCG demultiplexer we previously reported had an on-chip loss of 7.5 dB. The largest contribution, 4.6 dB was caused by Fresnel reflection loss at the grating facets [3]. We showed in a different paper that the insertion loss of PCGs fabricated on a nanophotonic SOI platform can be drastically reduced by replacing each grating facet with a second-order distributed Bragg reflector (DBR) [4]. In this letter, we discuss this method in detail and show that the on-chip loss can be reduced down to 1.9 dB.

II. Design and Fabrication

In order to assess the performance of the DBR-type facets, we fabricated two identical PCG demultiplexers. One device is equipped with standard flat facets and for the second device, the flat facets are replaced with DBR-type facets.

A. Grating Demultiplexer Design

The layout of the PCGs discussed in this letter is shown in Fig. 1. It provides four output channels with a spacing of 20 nm around a central wavelength of 1550 nm. The total footprint, including photonic wire access waveguides is only 280×150 μm^2. The design of this 1×4 demultiplexer is based on the Rowland geometry and is discussed in detail in a previous publication [3]. Structures were defined with 193-nm deep-ultraviolet (DUV) lithography, and transferred into the silicon using inductively coupled plasma–reactive ion etching (ICP-RIE). The etching process is described in detail in [5]. The lithography is a two-step process which combines deep- and shallow etching. For the definition of the grating facets and the photonic wires, the 220-nm-thick Si layer is etched through. A more shallow etch (70 nm) is used for the definition of the fiber couplers and the 2-μm-wide entrance and exit waveguides on the Rowland circle. The fiber couplers are gratings that convert the mode between a broad access waveguide and the fiber to allow characterization of the component [5]. A double adiabatic taper is used for the transition from the 500-nm-wide deeply etched photonic wire waveguides to the 2-μm-wide shallowly

Manuscript received August 28, 2007; revised October 24, 2007. This work was supported in part by the Institute for the Promotion of Innovation through Science and Technology in Flanders (IWT-Vlaanderen) under the SBO epSOC Project, and in part by the European Union in the framework of the IST-ePIXnet Network of Excellence and the Silicon Photonics Platform. The work of W. Bogaerts was supported by the Flemisch Fund for Scientific Research (FWO-Vlaanderen) for a postdoctoral fellowship. The work of P. Dumon was supported by a scholarship from IWT-Vlaanderen.

The authors are with the Photonics Research Group, Department of Information Technology, Ghent University—IMEC, 9000 Gent, Belgium (e-mail: Joost.Brouckaert@intec.UGent.be).

Digital Object Identifier 10.1109/LPT.2007.915585

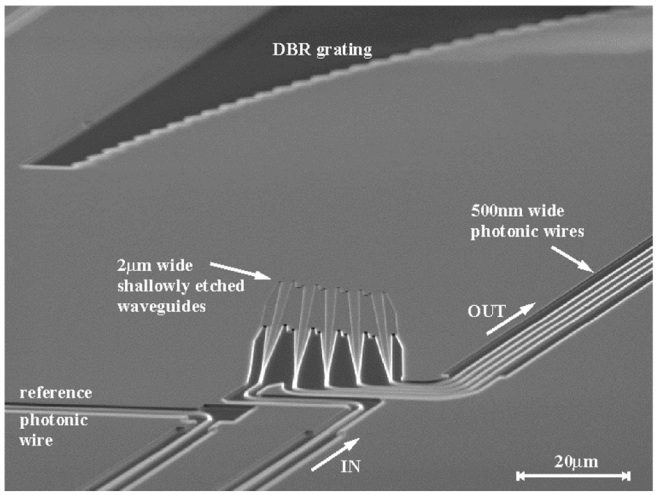

Fig. 1. Scanning electron microscope (SEM) picture of 1×4 PCG demultiplexer with DBR-type facets.

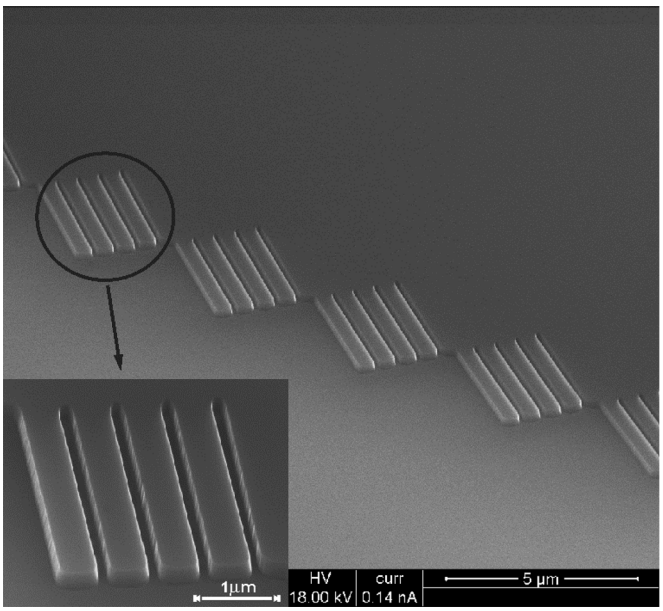

Fig. 2. Top view of DBR-type grating facets.

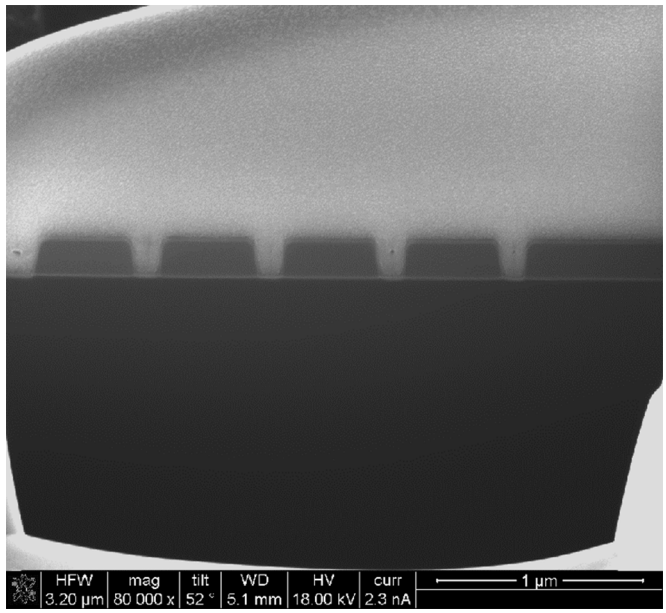

Fig. 3. Cross-section SEM picture of a DBR-type facet.

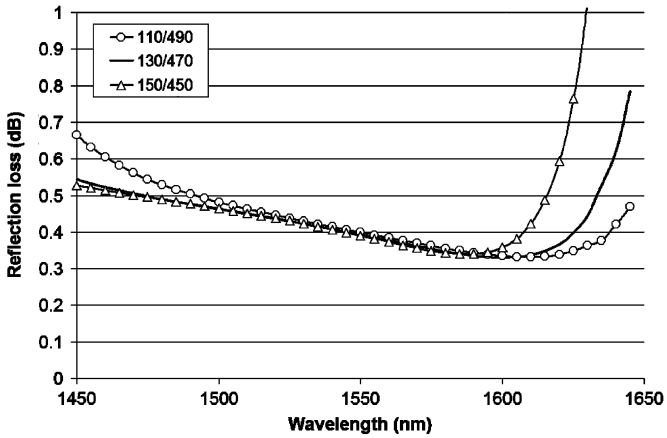

Fig. 4. Simulation results of the reflection loss of a four-period DBR-type facet. The period is 600 nm and the trench width varies from 110 to 150 nm, the unetched part from 490 to 450 nm. Perfect vertical sidewalls are supposed.

etched input and exit waveguides on the Rowland circle as can be seen in Fig. 1.

B. Facet Design

Different possibilities exist to avoid the Fresnel reflection loss at the grating facets. One possibility is to coat the back of the grating facets with a reflecting metal. On-chip losses as low as 1.8 dB have been obtained using this method, however, this results in additional processing steps [6]. Another approach to increase the reflectivity is to change the shape of the facets. This can be done by replacing each single facet with a V-shaped total internal reflection-type facet [7]. Because the number of corners is doubled, the losses due to corner rounding are increased and some design freedom is lost due to the fact that these facets are retro-reflecting. In this letter, we replaced each single facet by a DBR. We propose a deeply etched (220 nm) second-order DBR consisting of four periods as can be seen in Figs. 2 and 3. The simulated reflection loss of a DBR-type facet consisting of four 600-nm periods and vertical sidewalls is shown in Fig. 4. Reflection loss below 0.5 dB can be obtained in the entire 1.5- to 1.6-μm wavelength range using a trench width of 130 nm. These reflection losses were calculated by means of CAMFR, a two-dimensional fully vectorial tool based on eigenmode expansion. As can be seen in Fig. 4, these DBRs are very tolerant on fabrication errors. A 15% trench width deviation does not result in a higher loss for wavelengths from 1.5 μm up to 1.6 μm.

III. Measurement Results

Light from a single-mode fiber is coupled into the nanophotonic waveguides using shallowly etched fiber couplers [5]. The measured transmission spectra are for TE-polarized light (E-field in plane) and are normalized to a reference photonic wire waveguide (Fig. 1) in order to exclude the transmission spectra of the fiber couplers. All waveguide structures, including the fiber couplers, are designed for TE-polarized light

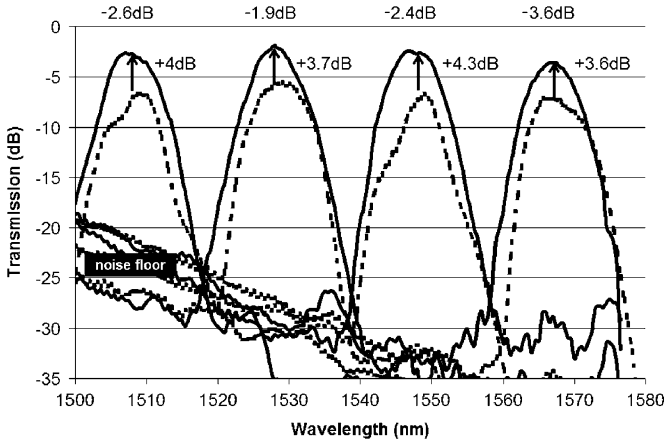

Fig. 5. Transmission spectrum of a 1×4 demultiplexer fabricated with 193-nm DUV lithography. Demultiplexers with flat (dashed line) and DBR-type facets are compared.

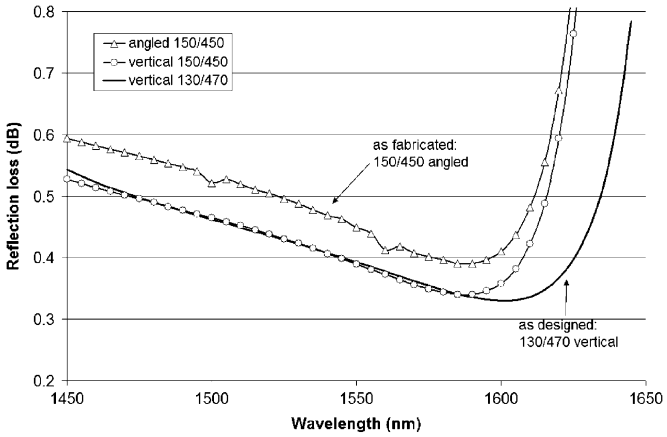

Fig. 6. Simulated reflection loss of a four-period DBR-type facet. The ideal DBR (470 nm/130 nm and vertical sidewalls) is compared with the fabricated DBR (450 nm/150 nm and 10° nonverticality for the isolated sidewall, 5° for the nonisolated sidewalls).

only (due to the high propagation loss of the TM-mode in this material system) [3].

A. PCG With Flat Facets

Fig. 5 shows the superimposed transmission spectra of PCGs with flat (dashed line) and DBR-type facets. As can be seen, these spectra are slightly disturbed by the high noise floor of the measurement setup. The average insertion loss of the central channels of the flat facet device is ∼6.3 dB. The largest contribution, 4.6 dB, is caused by the Fresnel loss at the grating facets. The etching process is not optimized to create perfect vertical sidewalls and results in a large nonverticality of ∼10°. However, this only gives rise to an additional loss of 0.3 dB, resulting in a total grating reflection loss of 4.9 dB [3]. These values were calculated by means of CAMFR and a staircase approximation was used for the angled facets. Other contributions are diffraction loss of 0.5 dB (calculated with scalar diffraction theory [3]) and excess loss (mainly caused by grating profile imperfections), which adds 0.9 dB.

B. PCG With DBR-Type Facets

The insertion loss of the DBR-type facets device is 3.9 dB better on average as compared with the flat facet device (Fig. 5). This means that the average reflection loss at the facets decreases from 4.9 dB down to 1.0 dB by replacing the facets with second-order DBRs. This value is slightly higher as compared with the simulation results showed in Fig. 4 which predict an average facet loss of 0.4 dB in the 1.5- to 1.6-μm range. However, these simulations do not take into account fabrication imperfections like grating nonverticality and trench width deviation of the DBRs. The cross section (Fig. 3) revealed a trench width of 150 nm and a deviation from verticality of ∼5° for the nonisolated sidewalls and ∼10° for the isolated sidewall. These simulation results are shown in Fig. 6 and predict an increase of only 0.1 dB in the 1.5- to 1.6-μm range. This means that the somewhat higher than expected facet reflection loss is due to other DBR imperfections like roughness and trench-width nonuniformity. It is important to notice that large grating nonverticalities have no major influence on the reflection loss. PCGs fabricated in other material systems have a several micrometer thick slab region with deeply etched facets. Sidewall nonverticalities as reported here would have a severe influence on the transmission characteristics of these devices [2], [3].

The crosstalk of the device does not seem to be deteriorated by the use of the DBR-type facets and is better than −25 dB. However, it is difficult to draw conclusions concerning crosstalk values due to the high noise floor of the setup.

IV. Conclusion

We presented measurement results of ultracompact PCG demultiplexers fabricated on a nanophotonic SOI platform. The on-chip loss was reduced by 3.9 dB on average for wavelengths ranging from 1500 nm up to 1600 nm by utilizing DBR-type grating facets instead of flat facets. This method does not require extra processing steps and is very tolerant concerning fabrication imperfections.

References

[1] P. Dumon, W. Bogaerts, D. Van Thourhout, D. Taillaert, R. Baets, J. Wouters, S. Beckx, and P. Jaenen, "Compact wavelength router based on a silicon-on-insulator arrayed waveguide grating pigtailed to a fiber array," *Opt. Express*, vol. 14, pp. 664–669, 2006.

[2] W. H. Wang, Y. Z. Tang, Y. X. Wang, H. C. Qu, Y. M. Wu, T. Li, J. Y. Yang, Y. L. Wang, and M. Liu, "Etched-diffraction-grating-based planar waveguide demultiplexer on silicon-on-insulator," *Opt. Quantum Electron.*, vol. 36, pp. 559–566, 2004.

[3] J. Brouckaert, W. Bogaerts, P. Dumon, D. Van Thourhout, and R. Baets, "Planar concave grating demultiplexer fabricated on a nanophotonic silicon-on-insulator platform," *J. Lightw. Technol.*, vol. 25, no. 5, pp. 1053–1060, May 2007.

[4] J. Brouckaert, W. Bogaerts, P. Dumon, S. Selvaraja, G. Roelkens, D. Van Thourhout, and R. Baets, "Planar concave grating demultiplexer with distributed Bragg reflection facets," in *4th Int. Conf. Group IV Photonics*, 2007, pp. 13–15.

[5] W. Bogaerts, D. Taillaert, B. Luyssaert, P. Dumon, J. Van Campenhout, P. Bienstman, D. Van Thourhout, R. Baets, V. Wiaux, and S. Beckx, "Basic structures for photonic integrated circuits in silicon-on-insulator," *Opt. Express*, vol. 12, pp. 1583–1591, 2004.

[6] S. Bidnyk, D. Feng, A. Balakrishnan, M. Pearson, M. Gao, H. Liang, W. Qian, C.-C. Kung, J. Fong, J. Yin, and M. Asghari, "Silicon-on-insulator based planar circuit for passive optical network applications," *IEEE Photon. Technol. Lett.*, vol. 18, no. 22, pp. 2392–2394, Nov. 15, 2006.

[7] M. S. D. Smith and K. A. McGreer, "Diffraction gratings utilizing total internal reflection facets in littrow configuration," *IEEE Photon. Technol. Lett.*, vol. 11, no. 1, pp. 84–86, Jan. 1999.