Compact arrayed waveguide grating devices in Silicon-on-insulator

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Very compact arrayed waveguide gratings were fabricated in Silicon-on-Insulator using CMOS compatible processes. The high index contrast makes a 5 micron bend radius possible. Now, the device size is not limited by the bend radius anymore. The insertion loss of the devices is kept low by applying a double etch technique, and the cross-talk level is reduced by broadening the waveguides were there is no absolute need for single mode waveguides. Measured insertion losses are around 3.5 dB, while the crosstalk level is better than -12dB. A 4×4 AWG was pigtailed and used in a 10 gigabit/s optical backplane interconnect application.

Introduction

Submicron Silicon-on-insulator (SOI) *photonic wire* waveguides can deliver very compact passive photonic integrated circuits. By exploiting a high index contrast, bend radii of just 3 to 5µm are possible with very low loss. With a higher integration grade, much more functionality can be integrated on the same or smaller die size than with planar lightwave circuit technology. Combined with CMOS technology, nanophotonic SOI technology even has the prospect of volume fabrication.
Here we present arrayed waveguide grating (AWG) devices fabricated with CMOS based processes, including 248nm deep UV lithography. The device size is not limited by the bend radius anymore, but merely by the number of arrayed waveguides and the star coupler size. With high index contrast technology, devices are more difficult to optimize for low insertion losses and low crosstalk however. Here we reduce insertion losses by applying a two etch step scheme. We fibre pigtailed a 4×4 device with reduced insertion losses. Phase errors in the arrayed waveguides contribute considerably to the sidelobes in the transmission spectra (giving rise to crosstalk). We studied reducing these sidelobes by broadening the waveguides.
Structures are defined on waferscale on 200mm SOI wafers with a 220nm thick Si top layer and a 1μm burried oxide. The Si layer is completely etched in order to obtain a high index contrast. A top oxide cladding can be applied. Details about the fabrication processes can be found in [1]. Earlier, we showed propagation losses as low as 2.4dB/cm for 500nm wide wires. Bends have excess losses lower than 0.004dB for a 90°bend.

Arrayed waveguide grating in SOI

Our interest was primarily in circular AWG devices with WDM compatible channel spacings up to 400GHz and a limited number of wavelength channels. In this case,

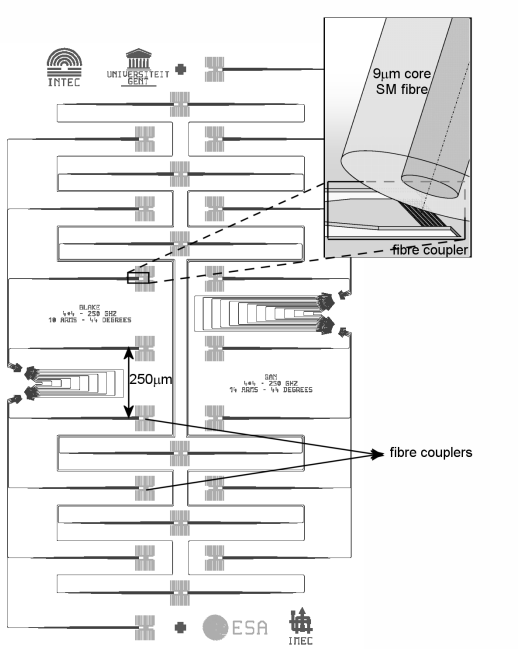

Figure 1: Chip layout, with two AWG devices, access and alignment waveguides, fibre couplers and alignment features. The inset illustrates the use of vertical fibre coupler gratings.

the frequency free spectral range (FSR) is relatively small (e.g. 1THz) and the device size is limited by the needed delay length and the number of arrayed waveguides.
Insertion losses are mostly due to the finite gap size between the arrayed waveguides at the star coupler edge. In our case, these gaps are limited to about 200nm, which is a lot for this high index contrast system. In order to circumvent this problem, using a lower index contrast for the star coupler is a well-known solution. We used this approach by applying a two etch step scheme. In a first shallow etch step (70nm), the star couplers and their short access waveguides are defined. The second etch step is deep (220nm) and defines the high index contrast waveguides. A double taper approach is used to convert between the high and low index contrast. The alignment accuracy between the two lithography steps is done on waferscale and is good enough to not introduce noticeable excess losses.
While first AWG designs had best channel insertion losses of about 8dB, the AWG devices with dual etch steps now have insertion losses of about 3.5dB for the best channels.

Fibre pigtailing

We pigtailed a 4×4 AWG device with 250GHz channel spacing to standard single mode fibres. This was done using broadband grating couplers [2] and a commercially available eight fibre array connector. The actual AWG is only 400x350 µm^2 in size. This is illustrated by the chip layout in Figure 1. Even with access waveguides and fibre couplers, de die size is smaller than the array connector surface. The great alignment tolerances of the fibre couplers, combined with features on the chip, facilitated alignment during characterization and pigtailing. After first characterization,

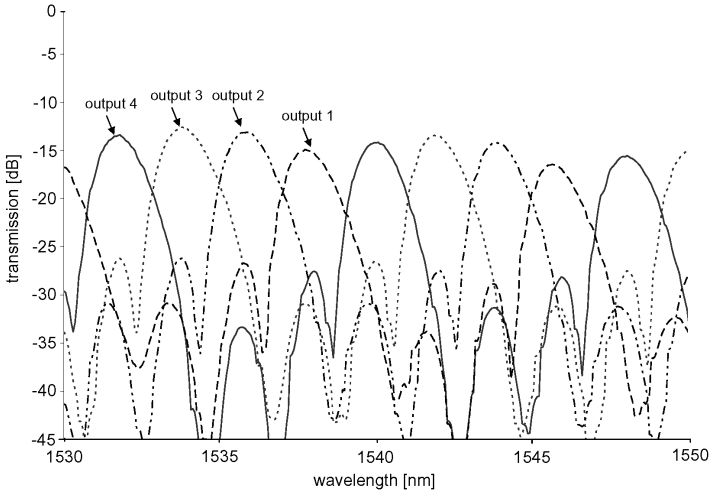

Figure 2: Fibre to fibre transmission spectrum of a 4-channel, 250GHz channel spacing AWG. Overlayed spectra from the third input to all outputs are shown.

the connector was glued to the chip using a UV cureable glue. The SOI device has a 750nm thick oxide top cladding, serving as a passivating and protective layer, and enhancing the fibre coupler transmission. The glue also acts as an index matching material between the fibre and this oxide top cladding. The total fibre-to-fibre insertion loss is 12.5dB for the best channels. Figure 2 shows the transmission spectrum of the pigtailed device, from one input to all four outputs.
The pigtailed device was packaged with a peltier element and thermistor for temperature control, and applied as the wavelength router in a wavelength routed 10Gb/s reconfigurable optical backplane using tuneable lasers. Allthought the -12dB sidelobe level is still high, it was within spec for this application and indeed delivered low enough single channel crosstalk.

Reduction of the sidelobe level

The high sidelobes are partly due to phase errors in the arrayed waveguides. Roughness of just a few nm and longer scale variations of about the same amplitude, can give rise to considerable phase errors. As the longer arrayed waveguide lengths have a length of a few 100µm considering the FSR, these phase errors become important. In broader waveguides, the effective index of the ground mode changes less with the waveguide width. Simulation of the waveguide mode combined with a statistical roughness model, showed that even a broadening of the waveguides from 500nm to 800nm would considerably reduce the phase errors and therefore the sidelobes in the AWG transmission spectra. Then, whereas the second generation device that was fibre pigtailed had a sidelobe level of -12dB only in a small fabrication parameter range, we expected AWG devices employing broader arrayed waveguides to systematically show lower sidelobes. Because 800nm wide wires are not single mode anymore, part of the waveguide is kept narrower and linear tapers of 3µm length convert between narrow and broad parts. In all characterized devices, this broadening leads to better transmission characteristics. This is illustrated by the example in Figure 3, where the transmission spectrum for one input to output path of an

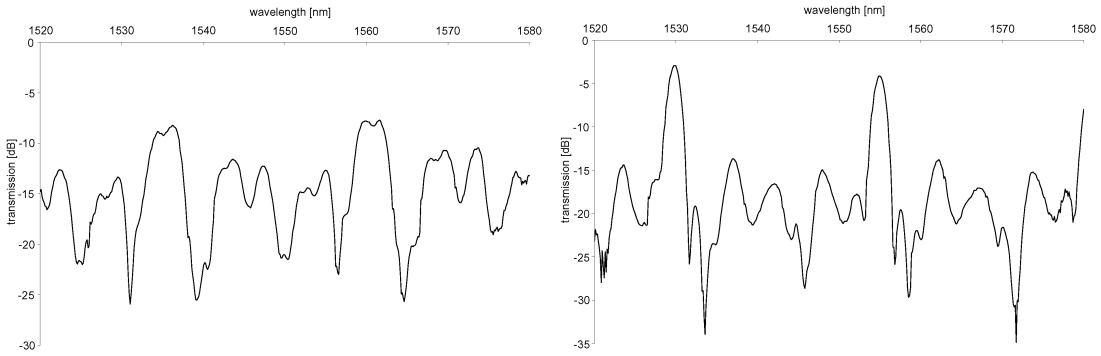

Figure 3: Normalized AWG transmission spectrum of one channel of an 8x8 AWG with 400GHz channel spacing (3.2THz or 25nm FSR) and 19 arrayed waveguides. left: without broadening of the arrayed waveguides right: with broadened waveguides

8×8 AWG is plotted. Both AWG devices are the same expect one has broadened waveguides while the other one does not. The AWG without broadened waveguides does not even seem to have a proper filter characteristic, whereas the AWG with broadened waveguides has clearly identifiable channels with about -12dB sidelobes.

Conclusion

We fabricated arrayed waveguide grating devices in Silicon-on-insulator using CMOS based processes. Devices using lower index contrast star couplers by applying two etch steps show reduced insertion losses. A 4×4 AWG with 250GHz channel spacing was fibre pigtailed using vertical fibre couplers and an eight fibre array connector. We also show a reduction of the sidelobe level by broadening the arrayed waveguides.

References

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