# Silicon-on-Insulator based Nano-photonics: Why, How, What for?

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**Abstract** *Silicon-on-Insulator is rapidly emerging as a versatile platform for a variety of integrated nano-photonic components. This paper discusses the variety of merits offered by this system. The key technological challenges are discussed as well as the potential in multiple application fields.*

## Introduction

The integration of micro-photonic functions in Silicon or above Silicon has for many years been considered to be a holy grail, since it was expected to enable complex low-cost photonic integrated circuits in a way similar to what has happened in the field of microelectronics. There are already several established examples - both in high volume markets as well as in specialized niche markets - where this dream has come true. These include for example Silicon camera chips, MEMS- or liquid crystal based microdisplays above Silicon, Silica-on-Silicon planar lightwave circuits for functions in WDM telecom networks etc.

In recent years a new technology has been emerging from research labs worldwide: the use of standard Silicon-on-Insulator (SOI) wafers and standard Silicon processing technologies to create ultra-compact so-called "nano-photonic" components and circuits in Silicon [1-3]. In these circuits one uses high refractive-index-contrast single-mode waveguides with a cross-section of the order of the wavelength squared to make passive or active devices. The core of the waveguide is Silicon while the cladding is either a dielectric such as silica or air. The waveguide can be a conventional waveguide based on guiding by total internal reflection or a photonic crystal waveguide based on guiding by Bragg diffraction. The active functions – light emission, modulation, switching, amplification, detection - can be based on the properties of Silicon itself or on the properties of a special cladding material.

The term "nano-photonic" calls for some interpretation. The typical smallest feature sizes – widths, thicknesses, lengths – in wavelength-scale photonic structures are in the range of one tenth of a wavelength to one wavelength. For operation at a wavelength of 1550 nm for example – corresponding to a wavelength in Silicon of about 500 nm – the required smallest feature sizes are typically between 50 and 500 nm. This matches nicely the capabilities of present day's CMOS technology. However, the accuracy and reproducibility of the spectral behaviour of the optical functions are directly correlated to the geometric accuracy of these features in the device. As a rule of thumb one can say that a spectral accuracy of 1 nm (relative to a wavelength of 1550 nm) translates into a geometric accuracy of 1 nm (relative to a feature size of 50-500 nm). Furthermore the high-index contrast interfaces in these devices need to be smooth down to the 1 nm level to avoid scattering losses.

In this paper we will try to answer three questions relating to the SOI nano-photonic platform: why, how and what for. While answering these questions we will also discuss the major challenges faced by this platform.

## Why?

One can distinguish between at least three classes of arguments in favour of Silicon-on-Insulator nano-photonics: functionality and performance arguments, technological arguments and economical arguments.

In terms of functionality and performance the SOI platform distinguishes itself from most planar waveguide platforms in terms of the high vertical index contrast. Combined with etching through the (thin) Silicon core the resulting waveguides have a high index contrast both vertically and horizontally. With this contrast the waveguide cross-section becomes very small and the inter-waveguide spacing can be very small before coupling effects occur. Furthermore one can make virtually lossless curved waveguides with very small radii of curvature – down to a few micrometer – and this has a large impact on circuit layout. In terms of functional components the high index contrast has enormous merits for microcavities, which undoubtedly can be considered to be one of the most important generic components for passive and active functions. High index contrast is the key to achieve microcavities with small cavity volume and high cavity quality factor [4-5]. The high confinement and field enhancement brought by high index contrast and by cavity effects can also be exploited in non-linear optical components so as to turn weak non-linear effects into practical performance at low power levels.

Since Silicon is not a suitable material for all types of active functionality one has to make use of heterogeneous integration in which overlay materials are combined with SOI waveguides. By modifying the Silicon waveguide dimensions one can tailor the overlap of the optical field

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with the overlay material. In principle one could use several functional overlay materials on the same chip.

A last functionality argument in favour of SOI is of course the fact that one can integrate nano-photonic functions with microelectronic circuitry.

The technological arguments in support of SOI technology are heavyweight arguments. Silicon technology has reached a level of maturity which outperforms any other planar chip manufacturing technology by orders of magnitude in terms of performance, throughput and reproducibility. The processes, once developed, are amazingly reproducible across a wafer and from wafer to wafer. The processes needed to define the basic waveguide structure in SOI nano-photonic circuits are fully compatible with front-end processes for fabricating CMOS.

Finally there are strong economic arguments supporting SOI nano-photonics. First of all, large diameter SOI wafers of very good quality are commercially available at moderate cost, at least if one uses a standard type of wafer. When one processes nano-photonic ICs by means of wafer scale processes on these large wafers, the resulting cost per chip will be small. Furthermore several groups have demonstrated techniques for wafer-level testing of photonic-components by using surface coupling techniques from vertical optical fibers into horizontal on-wafer waveguides. This wafer-level testing can in principle be highly automated. Since the cost of a photonic module is very often dominated by packaging it is important to make this packaging as simple as possible. In recent years several techniques have been successfully demonstrated in which a spot-size converter is integrated on the chip by means of wafer-scale techniques, thereby making the packaging simpler and cheaper.

The main economic driver for SOI-based nano-photonics may well be the fact however that one can operate a photonic IC company in a fabless way, whereby the key front-end technological processes are subcontracted to a foundry-like Silicon CMOS fab. This is of key importance as long as the product volumes do not allow for the ownership of a dedicated fab. This is the case for the majority of photonic IC applications today.

**How?**

Figure 1 shows a possible future process flow for the manufacturing of an SOI nano-photonic component. Each block in the diagram could in principle represent a different industrial actor.

The product developer is assumed to be a fabless company that takes care of the entire product specification, design, the testing of packaged components and their integration in subassemblies or even in complete systems.

The SOI wafer manufacturer delivers 200 or 300 mm SOI wafers to the CMOS fab. He will offer a small number of standard SOI-wafers for photonic applications with different thicknesses for the Silicon and the silica layer and possibly even variants with multiple Silicon layers.

The CMOS fab will use its standard CMOS processes for the fabrication of the nano-photonic IC's. Depending on the smallest feature size it will choose the most appropriate lithography process. For many types of components a 248 nm deep UV process will suffice, but for demanding applications the choice will be to use the 193 nm stepper. In special cases one may need to use immersion lithography or extreme UV lithography. Whatever standard processes available for CMOS can be used for nano-photonic circuits.

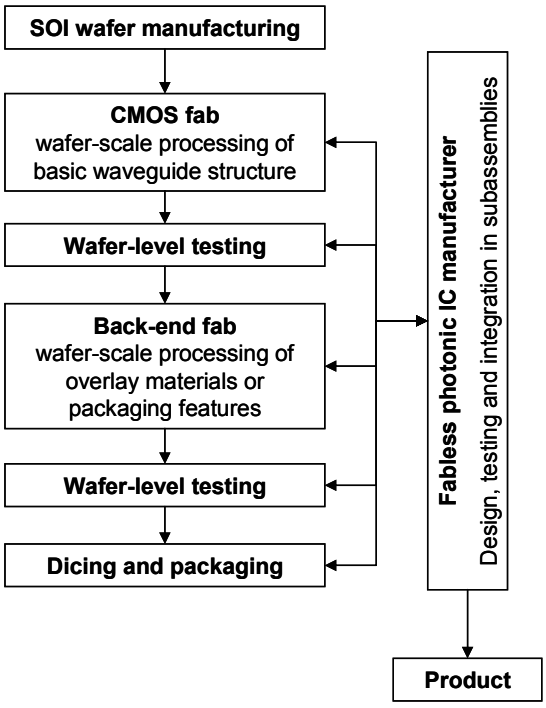


*Figure 1. Possible process flow for the manufacturing of SOI nano-photonic components.*

An important cost factor, especially in low volume applications and in prototyping, is the mask cost. If this turns out to be an issue it may make sense to collect many designs on a single mask, thereby sharing the cost between different products or different companies.

The etching processes needed to define the waveguides are in principle within reach of CMOS etching processes but the required geometrical accuracy and interface smoothness may require that these processes are optimized to a "photonic grade" level. In recent years it has been demonstrated that SOI photonic wires defined by optical lithography and CMOS etching processes can produce low loss waveguides [1].

After processing of the basic waveguide structures the wafers will be automatically tested. This is particularly important for functions with a strong wavelength selectivity. The geometrical accuracy requirements are very extreme in this case and may be at the limit of the CMOS fab capability. Automated wafer-level testing will

allow to select good dies or to identify the parameters for a later automated trimming process. The wafer-level testing is only possible of course when the circuits are provided with surface coupling structures allowing to couple light from a fiber or from a microscope objective into the chip. Such coupling structures can easily be realized and good coupling efficiencies – certainly good enough for testing -have been demonstrated [6].

The wafers then move to back-end processing. This step will be much less generic than the previous steps and will be very much product specific. It may involve overlay materials (and their structuring) for active functionality or for simple packaging or for trimming. Some overlay functions are relatively straightforward and have already been demonstrated today at research level. Examples include adiabatic transitions to fiber matched spin-on polymer waveguides for easy fiber coupling [7] and liquid crystal overlays for tuning. Other overlay functions are beyond today's state of the art: an example is the integration of an electrically fed bonded membrane InP microlaser or optical amplifier coupling efficiently into an SOI waveguide [8]. In any case it is important that the back-end processes are as much as possible wafer-scale processes.

The back-end processing may be followed by another wafer-level testing step, after which the wafers move to a packaging company where they are diced and mounted in a package with optical and possibly also electrical and thermal interfaces. The packaged components are then tested and possibly integrated into a (sub)system.

In the case where SOI nano-photonic functions need to be integrated with CMOS logic, the overall process flow of fig. 1 does not change much conceptually, except that the wafers will undergo a very complex set of processes in the CMOS fab. Any process in the backend stages will then need to be compatible (in terms of chemicals and thermal budget) with the presence of the electronic circuitry.

**What for?**

The process flow described in the previous section only makes sense if there are applications of sufficient volume. It is impossible to imagine and predict all the applications of SOI nanophotonic ICs but in the remainder of this paper a number of examples of such applications are given. The examples hereafter go from short-term applications to long-term applications.

*Transceivers:* integration of a high speed optical transmitter (light source, modulator, drive electronics) with a high speed receiver (detector, receiver electronics), a duplexer and possibly coarse WDM functionality.

*Dense WDM components:* arrayed waveguide gratings [9], possibly integrated with detectors and receiver electronics; add-drop multiplexers, possibly reconfigurable; tunable lasers etc.

*Sensors*: any function a fiber Bragg grating can do, and more; spectroscopic sensors; disposable bio-sensors etc.

*Optical interconnect:* provide a solution for the interconnect bottleneck in high-end CMOS circuits by building a photonic interconnect layer above CMOS, involving microlasers, dense waveguides and microdetectors.

*Digital photonics:* integrate optical logic gates and optical memory elements for digital all-optical processing at ultra-high data rate.

**Conclusion**

We have reviewed the rationale behind the emergence of Silicon-on-Insulator nano-photonics. A model has been presented for an industrial process flow in which fabless photonic IC manufacturers develop novel products based on CMOS foundry access, wafer-scale back-end processing and automated wafer-scale testing.

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