Packaging solution with a 3-dimensional coupling scheme for direct optical interconnects to the chip

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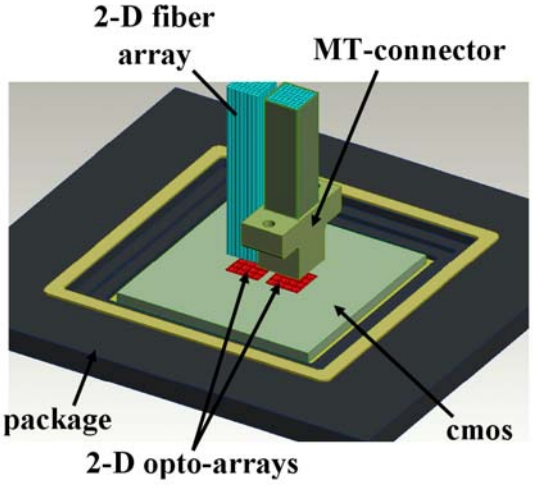
Inter-Chip Optical Interconnects are viable alternatives for conventional copper wires. However, the costly assembly and packaging process is the major obstacle to their commercial breakthrough, where especially the coupling of optical components seems to be the most critical aspect.
This paper describes the packaging and 3-D coupling scheme we have developed for a 2-D parallel optical interconnect module with on-chip access. It is a passive index alignment method that measures the coordinates of alignment features to achieve correct alignment. We belief it is a possible low cost solution as full automation is possible.

Introduction: 2-D parallel optical interconnects for inter-chip links

As data rates inside electronic systems increase, the bandwidth of electrical interconnects is limited by power consumption, signal distortion, cross-talk and pin-out capacity. No matter how inventive the solutions or workarounds to extend the electrical interconnect bandwidth, in the end the fundamental aspect ratio limit [1] remains.

Optical interconnects are a viable alternative as they offer the true physical means to overcome this so-called interconnect bottleneck [2],[3],[4]. In that respect, Vertical Cavity Surface Emitting Lasers (VCSELs) have been a key-enabling technology in the development of short-reach optical interconnects. Their on-wafer processing and on-wafer testing results in high-yields and low-costs and their low-divergence circular beams lead to more efficient fiber coupling.



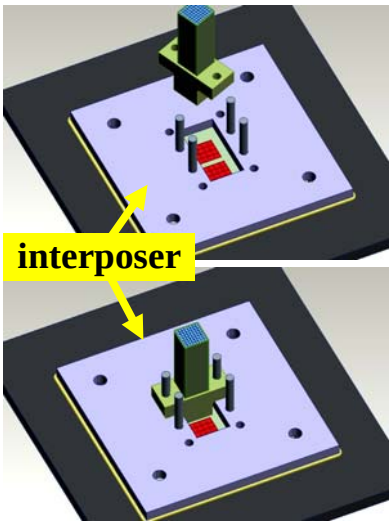
However, most optical interconnect modules are based on 1-Dimensional (1-D) arrays ([4]-[8]) and do not fully exploit the spatial advantage that VCSELs offer. We believe that, at the inter-chip level, optical interconnects based on 2-D arrays of VCSELs, detectors and multimode optical waveguides combined with integrated wiring-technologies such as flip-chip bonding offer high-speed and low-cost data access. Such a module is illustrated in figure 1.

Figure 1: packaged cmos with flip-chipped 2-D arrays and 2-D fiber ferrule arriving vertically

Packaging and assembly: coupling of light is critical

As low-cost and high-yield the different components may be, the costly assembly and packaging processes are road-blocks on the commercial success of inter-chip optical interconnects. More specifically, the alignment of the optical components to each other is a critical issue, where typically we have to deal with positional tolerances ranging form 10 down to 1 μm. This assembly step greatly impacts the overall system cost, performance, manufacturability, yield, and reliability.

We are dealing with 2-D arrays of components with the fibers arriving vertically to the chip. Proper alignment of these 2-D arrays requires full control of all 6 degrees of freedom (DOF). Especially the tight control of the longitudinal distance between 2 arrays is quite a challenging task.



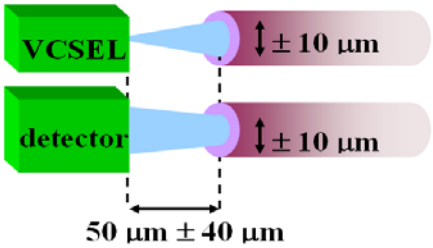
Our approach is to extend an existing electrical package with a guiding structure to accept an MT-like fiber ferrule. This guiding structure basically is a kind of spacer-plate with MT pins (see figure 2), which we call the interposer. If we achieve correct alignment of this interposer to the 2-D opto-arrays (VCSELs and detectors), sliding the fiber connector over the MT pins will guide the ferrule into correct position Note that the self-alignment property of the applied flip-chip technology results in an accurate alignment of the opto-chip to the CMOS-chip. This way we can shift our task to aligning the alignment plate to the CMOS-chip.

Figure 2: sliding the MT ferrule over the MT pins guides the ferrule into desired position

Analysis of the needed accuracy

To guarantee 90 % of maximum power throughput at each stage and to keep the crosstalk between neighbouring channels below -30 dB, the distance between the fiber-ends and the opto-arrays must be 50 μm ± 40 μm, while the lateral misalignment has to be less than 10 μm.

Figure 3: alignment tolerances



Bear in mind however that we need to take into account all the dimensional variations of the parts in between: fiber diameter and concentricity, true fiber position in the array, pin-hole diameter, pin diameter, true pin position in the alignment plate, true pin-hole position in the connector, etc. In the end all these tolerance add up to a total dimensional variation of 5 μm in the lateral dimension and 20 μm in the longitudinal dimension.

This 5 μm respectively 20 μm variation has to be distracted from the 10 μm respectively 40 μm tolerances on the fiber coupling. This leaves us with a needed alignment accuracy of 5 μm lateral and 20 μm longitudinal. In the next section we describe our approach to achieve the needed alignment accuracy.

Virtual index alignment using a 3-D CMM

Active alignment is a time-consuming, labor intensive procedure and difficult to automate. Especially for 2-D arrays the searching algorithm is quite complex. Passive alignment on the other hand can easily be automated but suffers from high component cost due to the high dimensional accuracy needed.

Index-alignment can be easily automated while keeping component cost down. This procedure tries to align two parts that both display alignment features (for example crosses) on their top surfaces by aligning those features with help of a vision system, as in a mask-aligner. As you project the features onto a screen, you lose the height information, making it impossible to control the longitudinal offset.
You can prevent this loss of height-information by using a 3-D Coordinate Measuring Microscope (CMM) as the vision system. A 3-D CMM allows to measure the (x,y,z) coordinates of a certain feature if it has a lens system with a small enough depth of focus. Therefore we need to provide high precision alignment features on both the CMOS and the alignment plate. The CMOS can easily be patterned by high accuracy lithographic means, while the interposer can be fabricated using spark erosion or laser-ablation techniques.

Set-up and Procedure

The interposer and the packaged CMOS-chip are held with vacuum chucks and are placed on rotation and translation stages, enabling to control all 6 Degrees Of Freedom (DOF). The alignment procedure is described below:

1. Measurement of the position of the CMOS
2. Calculation of the position of the interposer
3. Measurement of the position of the interposer
4. Rotation and translation of the interposer to bring it into the desired position
5. Iteration of step 3 and step 4 until the achieved alignment accuracy is within specification
6. Fixation of parts by UV-curing of low-shrinkage glue

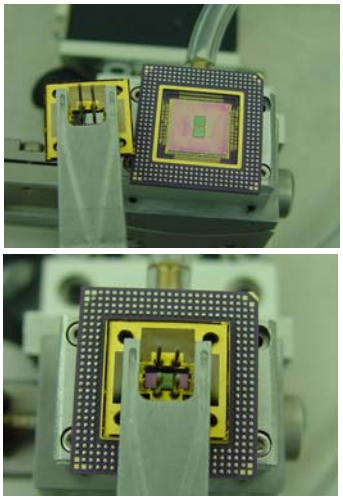


Figure 4: alignment of the interposer to the packaged CMOS

Results

We have built a demonstrator as described in the text. Firstly, the interposer was fabricated in PolyCarbonate (PC), using excimer laser ablation to drill the holes in the PC plate. PC is selected due to its excellent ablation characteristics [9]. A thin metal layer was deposited on the PC, and patterned to provide the alignment features on this interposer. In a second step, the plate is positioned on the ceramic, as shown in figure 4, and finally the module was fixed by UV-curing the low-shrinkage glue.

We measured the translational and rotational misalignments and found that everywhere in the array, alignment tolerances are within specifications. Rotational misalignment causes the lateral and longitudinal misalignments to be maximal at the rim of the opto-arrays. The maximum lateral misalignment is 2,8 μm, while the maximum longitudinal misalignment is 14,9 μm. (see figure 5)

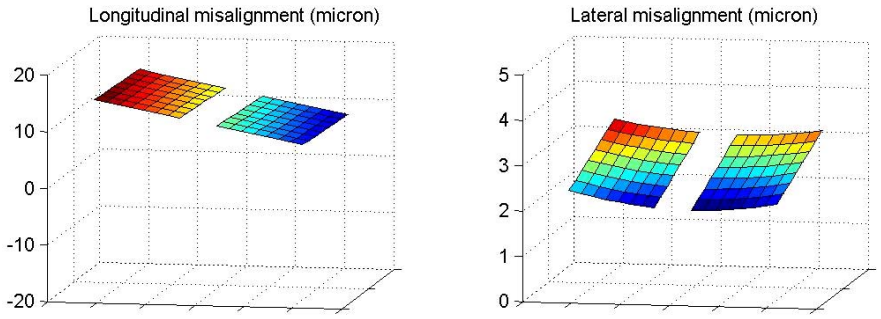


Figure 5: calculated longitudinal and lateral misalignment between interposer and the 2 opto-arrays

Conclusions

This paper presents a novel alignment technique to assemble modules for short-reach inter-chip parallel optical interconnects. The great advantage of our approach is its flexibility. First of all the interposer does not need to be transparent. Secondly, the alignment features can be anywhere on both the CMOS and the interposer. They do not need to be directly above each other as in the normal index alignment approach, giving CMOS designers the choice where to place the alignment features best. Note that this process flexibility allows adapting it to other applications such as assembly of MEMS, optical storage devices, and medical devices. Furthermore the process can be automated using machine-vision software tools communicating with translation and rotation drivers.

Acknowledgements

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