Large-scale production techniques for photonic nanostructures

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ABSTRACT

Nanophotonic ICs promise to play a major role in the future of opto-electronic signal processing and telecommunications. But for these devices, which consist of large numbers of wavelength-scale photonic components, to be successful, reliable and cost-effective mass-fabrication technology is needed. Photonic components, and among them photonic crystals, require a high degree of accuracy, which translates to low fabrication tolerances. Today, similar demands are made for high-end CMOS components, made of Silicon, for which a large manufacturing base is installed.

We demonstrate the fabrication of nanophotonic components, like photonic crystal waveguides and photonic wires, using state-of-the-art CMOS processing tools. The foremost of these is deep UV lithography at 248nm and 193nm, combined with dry-etch processes. To maintain compatibility with standard CMOS processes, we use Silicon-on-Insulator (SOI) as our material system. SOI is transparent at telecom wavelengths and provides a good substrate for high-index contrast optical waveguides. Moreover, recent studies have shown that nanophotonic components in SOI are less sensitive to surface roughness than similar components made in III-V semiconductor.

Although deep UV lithography cannot attain the resolution of e-beam lithography, this can be compensated with thorough process characterization, and the technique offers more speed because of its parallel nature. We will illustrate this with experimental results, and will also discuss some of the issues that have arisen in the course of this project.

Keywords: Nanophotonics, photonic crystals, deep UV lithography

1. INTRODUCTION

Like the shrinking of electronic building blocks led to ULSI electronics with billions of elements on a single chip, nanophotonics opens similar integration perspectives for photonics. Today's commercial photonic components more resemble the lumped transistor elements of the sixties and early seventies than an advanced microprocessor. One of the main reasons for this lack of integration is de difficulty to pull off a similar reduction in scale. Photonic waveguides, the core element on a photonic integrated circuit (PIC) that guide light from one functional block to the next need to make large bends to keep the light confined. This is because in most cases the waveguides guide light through total internal reflection, and the confinement is largely determined by the contrast in refractive index between the waveguide core and the surrounding cladding. In semiconductor material systems, the index contrast between core and cladding can be increased by etching the waveguides deeper into the semiconductor substrate. However, as the index contrast increases, the waveguide will support mode guided modes. Because single-mode behavior is desired for most waveguiding applications, this must be corrected by decreasing the waveguide width. For very high contrasts, like semiconductor (n=3.45) to air (n=1.0) or semiconductor to silica (n=1.45), waveguides become so small that they cannot be accurately defined with optical lithography, and the uneven etched surfaces can scatter the guided light, causes unwanted propagation losses.

There are two alternatives for these ultra-compact waveguides. One is to use a scaled down version of the index-guided waveguides discussed above. These so-called photonic wires typically have a width of 300-500nm. As we will show further, the performance is limited by the scattering at sidewall roughness, so these waveguides require very good processing technology.

Alternatively, light can be guided in a photonic crystal slab. Photonic crystals are periodic structures with a high refractive index contrast and a period of the order of the wavelength of the light in the material [1]. Because of this strong

contrast and the periodicity, photonic crystals have peculiar optical properties, including a photonic band gap (PBG). This is a wavelength (or energy, frequency) range where light is not permitted to propagate through the photonic crystal. When a defect is introduced into a photonic crystal, a defect state can be created in the PBG, and light can be confined to the defect [2]. By creating a line defect in a photonic crystal, one effectively creates a waveguide, and light has no other option than to follow the defect. Because of this, bends in photonic crystals can, in principle, be very abruptly. However, to obtain full control over the light with a photonic crystal, one needs a 3-D periodic structure. A 2-D alternative is the so-called photonic crystal slab. In this structure, only a 2-D periodic structure is used, and in the third, vertical, direction, the light is confined by a refractive index contrast. A 2-D photonic crystal slab can be fabricated using high-resolution lithography and dry etching in a semiconductor layer stack.

For telecom wavelengths, at 1.3μm and 1.55μm, both photonic wires and photonic crystals have dimensions of a few hundred nanometers. However, the accuracy required of the fabrication, is of the order of 10nm. Therefore, we can rightfully speak of nanophotonics. For research purposes, nanophotonic components are traditionally fabricated using e-beam lithography. While this is a very accurate technique, it is a serial writing process, making it slow and unsuitable for mass-fabrication. Alternatively, conventional lithography, with illumination wavelengths down to 365nm, is used for the fabrication of current photonic ICs, but lacks the resolution to define the dense nanophotonic structures like photonic crystals and photonic wires. Deep UV lithography, the technology used for advanced CMOS fabrication, offers both the required resolution and the throughput needed for commercial applications. However, technology development for 248nm, 193nm and recently 157nm is driven by the CMOS industry, and processes are therefore not always suited for nanophotonic structures.

In this paper we will describe our results in adapting CMOS fabrication tools to improve its capability for fabricating photonic nanostructures, like photonic crystals and photonic wires. We have made a variety of photonic components, including various waveguide structures and interface structures to optical fibers. We will first give an overview of the fabrication process, including some of the obstacle we had to overcome in order to migrate the process from CMOS to nanophotonics. Then we will describe a number of our fabricated components.

2. FABRICATION AND FABRICATION ISSUES

For our high-contrast photonic structures, we use Silicon-on-Insulator. This material has become popular in high-end CMOS because the top layer, in which the transistors are defined, is separated from the Silicon substrate by a layer of Oxide, eliminating leakage current and capacitive coupling. In photonics, SOI is equally attractive. The top Silicon layer provides a good waveguide core, because its high refractive index (n=3.45) contrasts very well with the underlying oxide (n=1.45). The function of the oxide is here to optically separate the guiding top layer from the substrate, which has a similar large refractive index. Therefore, the oxide should be thicker than needed for CMOS applications [1].

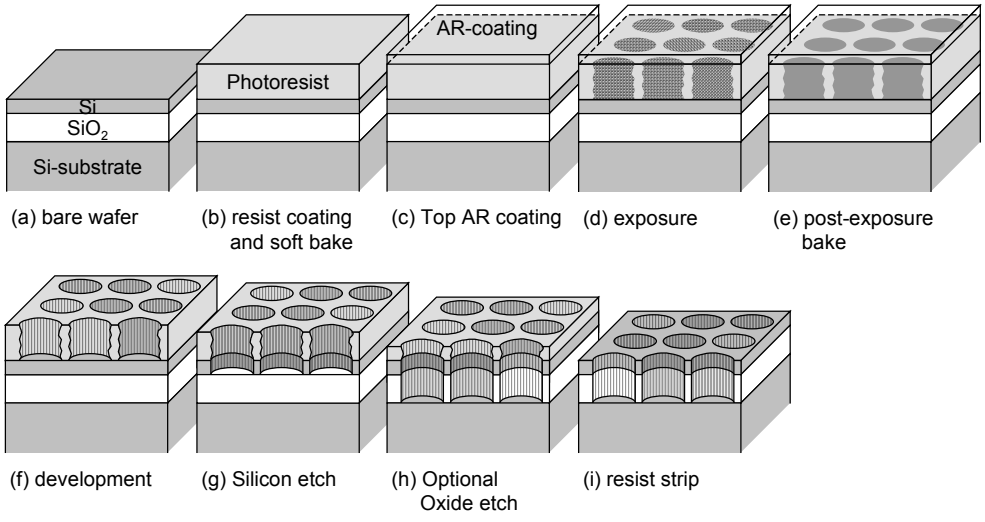

Figure 1: Fabrication process for photonic nanostructures in SOI using deep UV lithography and dry etching.

The fabrication process with deep UV lithography is similar to that of conventional optical lithography or e-beam lithography. The process is illustrated in Figure 1. First, A photoresist is coated on top of a 200mm SOI wafer, and then

pre-baked. On top of the resist, an anti-reflective coating is spun to eliminate standing waves in the photoresist. Then the wafer is sent to the stepper, which illuminates the photoresist with the pattern on the mask. As a 200mm wafer can contain many structures, the die with the pattern is repeated across the wafer. This can be done with varying exposure conditions. After lithography, the resist goes through a post-exposure bake, and is then developed. For our experiments we used Shipley UV3 resist, opening up the exposed areas. The developed photoresist is then used directly as a mask for etching. We can either etch just the top Silicon layer, or etch through both the Silicon and the oxide layer. Also, a number of post-processing steps are possible, including thermal oxidation or oxide deposition.

2.1. Wafer fabrication

High-quality Silicon-on-Insulator wafers are typically fabricated using wafer bonding. For our experiments, we ordered commercial wafers from SOITEC fabricated with the UNIBOND® process. First a wafer is oxidised to create the buried Oxide layer. Then Hydrogen ions are implanted at a well-controlled depth, creating a Smart Cut®. This wafer is then bonded to a clean Silicon wafer. Then the substrate of the first wafer is separated along the implanted Smart Cut®, and then annealed and polished [5].

For the first experiments, we used standard UNIBOND wafers with a buried oxide of 400nm and a top silicon layer of 205nm. Because this oxide thickness is too thin [1], causing optical leakage too the substrate, we switched to custom-made wafers with a Silicon thickness of 220nm and an oxide layer of 1μm. As we can deduce from our measurements, this thickness provides adequate spacing for the TE polarisation.

2.2. Lithography

For research purposes, e-beam lithography is the workhorse for the fabrication of photonic nanostructures. As already mentioned, this technique is not suitable for commercial application. Therefore we explore the possibilities to use deep UV lithography for this purpose. For our experiments we had access to the CMOS fabrication equipment of IMEC in Leuven, Belgium. Because lithography at a wavelength of 248nm is now the mainstream fabrication tool for high-end CMOS, we used this for the majority of our fabrication runs. For this, we used an ASML PAS5500/750 stepper connected to an automated track for preprocessing (coating and baking) and postprocessing (baking and developing).

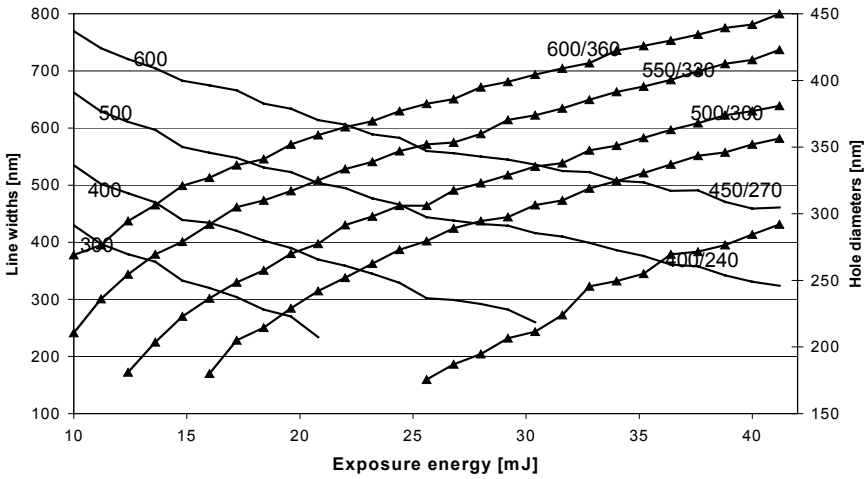

Figure 2: Hole sizes and line widths after lithography for various design dimensions as a function of lithography energy dose. For increasing dose, the lines narrow down and the holes grow.

Photonic nanostructures typically consist of a variety of structures. While for CMOS processes different types of structures are fabricated separately, alignment requirements for photonics make this impossible: All nanostructures should be printed in the same lithography step. However, this is not trivial, as not all types of structures print on target for the same lithography conditions. Especially the exposure dose, i.e. the amount of laser light projected on the photoresist has a significant influence on the feature size. Figure 2 shows the feature size for both isolated line (like photonic wires) and holes in a triangular lattice (like photonic crystals) for different design values. We can see that the hole size increases with higher doses, while the line width decreases. As both structures are very different, lines being an

isolated dark feature in a light field, and a photonic crystal being dense light features against a dark background, the dose-to-target will differ significantly. To fabricate both simultaneously, a bias needs to be applied to one or the other. This is the easiest for lines, being isolated features. Depending on the line width and the photonic crystal parameters, lines should be made between 10 and 100nm broader that originally designed to print together with photonic crystals.

However, varying the exposure dose can also be used to lithographically change the structure parameters. As we can print many dies onto a 200mm wafer with different exposure conditions, this gives us the ability to fabricate a number of different line widths and hole sizes in a single processing run, with a single mask. As can be seen from Figure 3, lithography gives us a large range of feature sizes for a given design, while the variation is gradual enough to guarantee reproducible processing.

In parallel with our 248nm device fabrication, we investigated the improvements that could be gained by switching to a wavelength of 193nm. As the resolution of optical lithography is proportional to the illumination wavelength [6], finer structures should be possible. Also, resolution can be increased by using a larger numerical aperture of the lens system, or using better photoresists. We experimentally compared different processes to determine the influence of these factors. As a comparison we measured the largest elliptical process window in the Focus-Exposure space for a triangular lattice of holes. We did this for a pitch of 500 and a target diameter of 300nm, and for holes with a pitch of 400nm and a target diameter of 200nm. We defined the process window as the largest ellipse where the hole siameter deviated less than 5% from its target value. Table 1 lists the 4 processes, where A is the standard process used for the majority of our experiments. For B we increased the numerical aperture of the stepper. While this reduces the depth of focus for the lithography process, this is not much of a problem as we always fabricate on a flat substrate. For experiment C we used an advanced bi-layer resist, with less thickness and a better nonlinear response. For experiment D we switched to 193nm, also with a bi-layer resist. The results of a final experiment at 193nm with a numerical aperture of 0.75 were not available at the time of writing.

	λ	NA	Resist
A	248nm	0.63	UV3
B	248nm	0.70	UV3
C	248nm	0.70	TIS248
D	193nm	0.63	TIS193

Table 1: Lithography processes compared for the fabrication of photonic crystal structures.

Figure 3 shows the elliptical process windows for the experiments of Table 1. While our standard process delivers a sufficiently large process window for most structures, we can see that we can significantly improve the performance of the process even without migrating to the more expensive 193nm lithography. Note that while we expect less depth of focus for experiment B than for experiment A, this is only the case for the smallest holes.

We can see that deep UV lithography is able to pattern nanophotonic structures, including photonic crystals. The process has good reproducibility, and by changing the exposure dose we can tune the photonic crystal parameters.

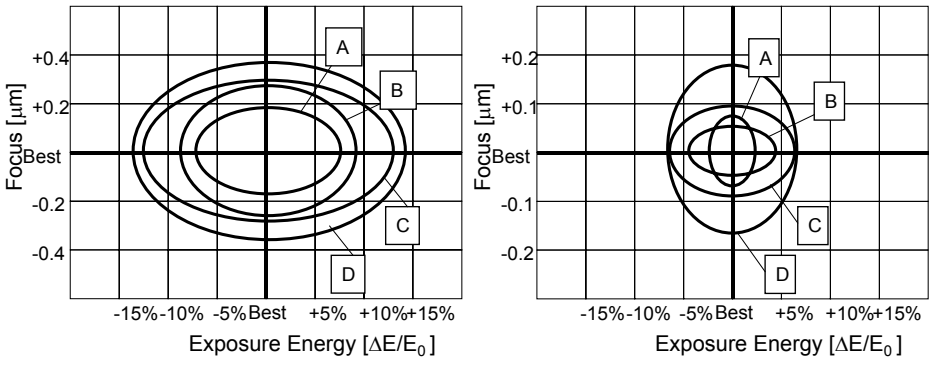

Figure 3: Elliptical process window for 5% deviation of the target size for the various lithography processes of Table 1. Left: Triangular lattice of holes with 500nm pitch and 300nm diameter. Right: Triangular lattice of holes with 400nm pitch and 200nm diameter.

2.3. Optical proximity effects

Photonic crystals are superdense periodic structures with feature sizes close to the illumination wavelength. This causes neighboring holes to interfere with each other during lithography. Because of this, holes in a photonic crystal may interfere constructively and print larger or interfere destructively and print smaller than solitary holes. In uniform lattices, this effect is not noticeable, as the illumination energy will be chosen to print the holes in the lattice on target. However, at the boundaries of the lattice, or near defects like a waveguide or cavity, some holes lack neighbors and will therefore print differently than their counterparts in the bulk of the lattice. This phenomenon is described as optical proximity effects (OPE). An example is given in Figure 4: Although its hard to see visually, the holes near the line defect are 40nm smaller than the holes in the bulk, and in the corner this effect is even worse, with the corner hole being 70nm smaller. As in photonic crystals the behavior of the component is largely determined by the shape of the defect, optical proximity effects are a very serious problem.

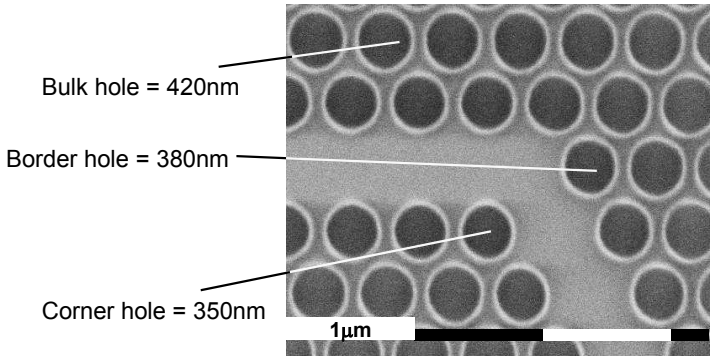

Figure 4: Illustration of optical proximity effects. The holes near the photonic crystal defect are printed smaller than the holes in the bulk of the lattice.

While proximity effects are also known in e-beam lithography, the serial nature of the process makes this an additive process, as the exposure in a certain area can only increase. For deep UV lithography, this is not the case, as the whole structure is defined in one illumination step, and the patterns can therefore interfere. This makes that OPE can be either constructive or destructive and are very hard to model accurately.

To correct for OPE, the features on the mask should be altered. This is illustrated in Figure 5. Holes near a lattice defect are printed smaller, and are therefore enlarged on the mask. It is evident that a good understanding of the OPE is necessary to design the structures with optical proximity correction (OPC).

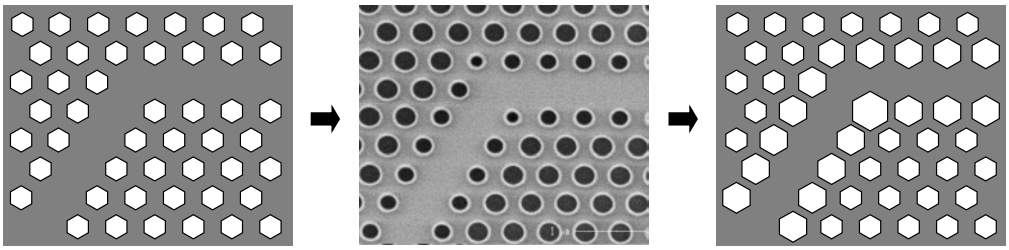

Figure 5: Principle of optical proximity corrections for photonic crystal structures. When uncorrected, the design on the mask (a) will print the defect holes differently than the bulk holes (b) due to optical proximity effects. To correct this, the design on the mask should be altered in advance (c).

To characterize optical proximity effects and the needed corrections in photonic crystal, we have designed a structure consisting of various photonic crystal waveguides along with a large number of bends, cavities and other possible components. We then repeated this structure on a mask with many variations of bulk hole sizes, and corrections on corners and borders. This makes it possible for us to measure the optical proximity effects and the required corrections directly and implement them on future mask designs.

2.4. Deep Etching

For etching the Silicon-on-insulator we could also make use of the IMEC processing facilities. In our case, this consisted of a multi-chamber LAM A6 platform with various process modules for the different etch processes. The wafer can be transferred between etch chambers without disrupting the vacuum. For the Silicon top layer we used a an ICP low pressure/high density etch system with a chemistry based on Cl_2/HBr/He/O_2. For the buried oxide, a dual frequency, medium pressure/medium density etch system with a CF_4/CHF_3 chemistry was used.

For our first experiments, on the wafers with only 400nm oxide, we successfully etched through both Silicon and oxide, with very good quality of the etched sidewalls. However, as already discussed, the thin oxide caused massive leakage to the Silicon substrate. For subsequent experiments, we used wafers with 1μm of oxide, but etching through this layer with only the photoresist as an etch mask proved quite a challenge. As shown in the top row of Figure 6 and in the left part of Figure 7, we succeeded in etching 800nm into the buried oxide, but at the cost of significant sidewall roughness.

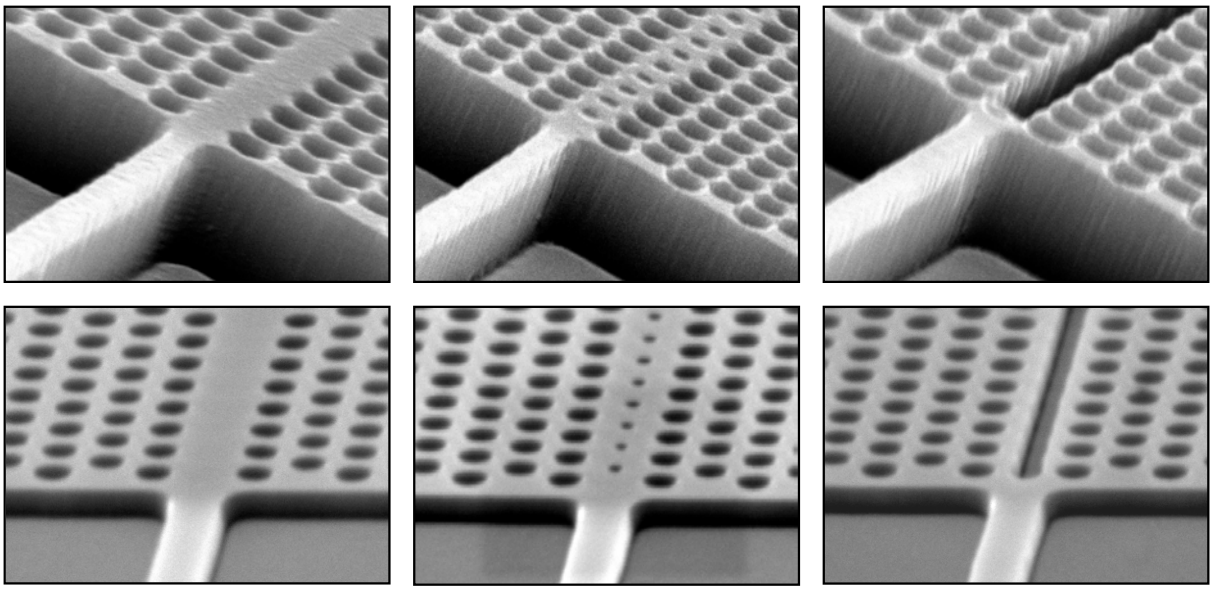

Figure 6: Photonic crystal waveguides fabricated with deep UV lithography and dry etching. Top row: 3 waveguide designs fabricated with deep etching, through both top silicon layer and oxide. Bottom row: The same designs, but fabricated with only oxide etch.

2.5. Sidewall roughness reduction

Rough surfaces cause scattering. Because the amount of scattering is proportional to the square of the difference in dielectric constant on the surface interface, the effect is dramatic for high-contrast material systems, like Silicon-on insulator [4]. To reduce these scattering losses, one can either avoid creating rough surfaces, or smoothen existing surfaces.

In order to avoid creating rough surfaces, we have explored two options. One is to expose the photoresist to a plasma treatment before etching. Lam research has already demonstrated this technique for CMOS applications. However, our experiments showed that this could only be done at the expense of resist thickness, and loss of line width. Because a thick layer of resist is needed for deep etching, this was not an option.

Alternatively, we just refrained from etching the buried oxide. By leaving out the second etch step, the sidewall roughness was drastically reduced. This can be seen in Figure 6 and the detail in Figure 7. The sidewall roughness is almost completely eliminated.

However, not etching the oxide created a layer structure that was even less symmetric in the vertical direction than the structure with etched oxide. Because a vertical symmetry has a positive effect on photonic crystal modal behaviour, this additional asymmetry was undesired.

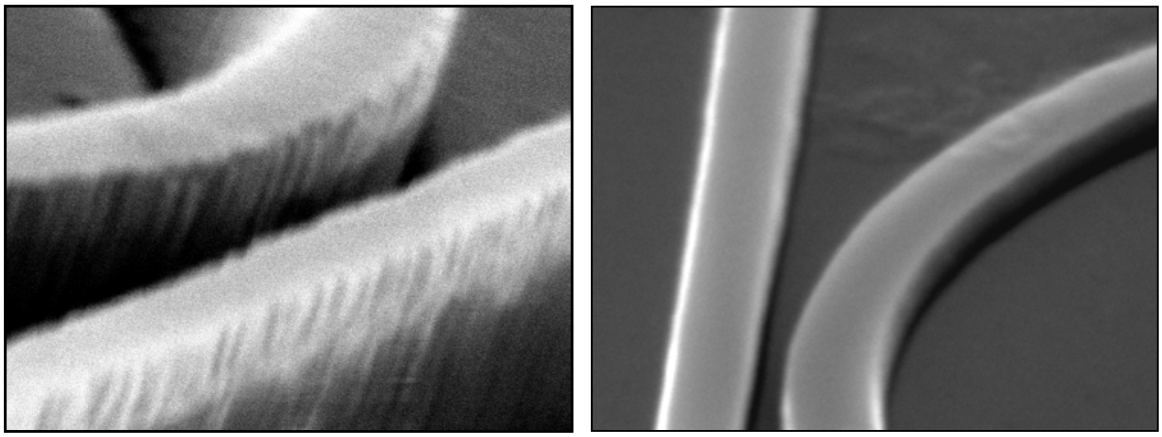

Figure 7: Detail of the coupling section between a straight photonic wire and a ring resonator. Left: Deep etch through both silicon and oxide. Right: Silicon-only etch. It is clear that the deep etching causes significantly more sidewall roughness.

Instead of avoiding sidewall roughness in the first place, we also tried to alleviate the sidewall roughness by treating the deeply etched structures. It has already been shown that thermal oxidation of Silicon-on-insulator waveguides can smoothen the sidewalls of both photonic crystal waveguides[7] and photonic wires[8,9]. The principle is illustrated in Figure 8. As the rate of oxidation is well documented and can be controlled quite accurately with the temperature, this is a reliable way of reducing roughness.

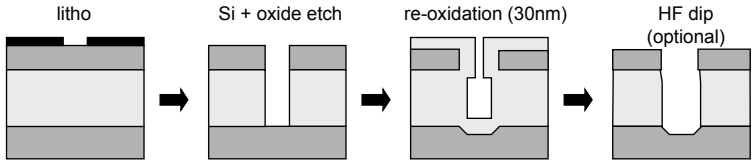

Figure 8: Roughness reduction using thermal oxidation of the Silicon sidewalls

In Figure 9 we see an example of a photonic crystal hole with different amounts of oxidation. The first impression is that the oxidation increases the amount of roughness on the sidewalls, blowing up the existing irregularities. However, because the new roughness is on an oxide-air interface instead of on a Silicon-air interface, the impact is less dramatic. Although this is hard to establish experimentally, we can assume that the underlying Silicon-oxide interface is smoother, due to the diffuse nature of the oxidation process. We can also see that the volume of the top layer increases after oxidation, creating a rounded core layer in cross section.

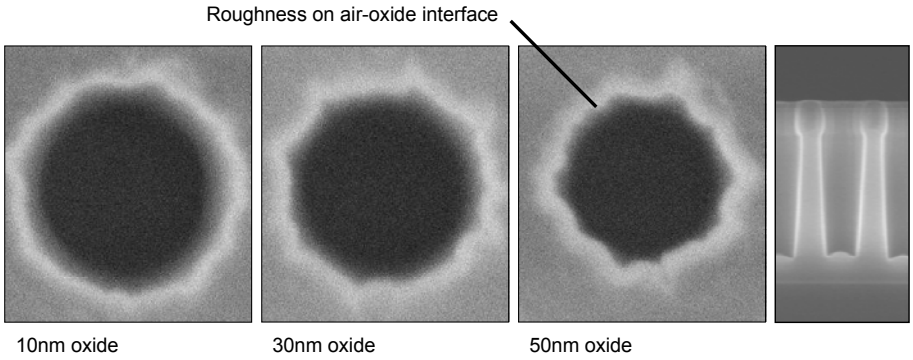

Figure 9: Deeply-etched photonic crystal holes after partial oxidation of the top silicon layer. Although the sidewall roughness seems more severe after oxidation, the irregularities are on the oxide-air interface, causing far less scattering than on the silicon-air interface.

While oxidation can improve the roughness in the top Silicon layer, it has little or no effect on the underlying oxide layer. Therefore, light can still be scattered by the roughness in the cladding. A solution to that problem would be to remove the cladding layer, creating a free-standing membrane. While this is a valid option for small areas of photonic crystal structures, it is harder to achieve for photonic wires, as the line waveguides are unsupported by the substrate.

While etching only the silicon can reduce the roughness, we end up with an asymmetric layer structure. On the other side, when we etch both silicon and oxide, oxidation can only smoothen the sidewalls of the top layer, and still keep some residual roughness at the oxide-air interface. However, we can combine the advantages of both approaches if we can make the layer structure symmetric again. This is illustrated in Figure 10: After a silicon-only etch, which causes little sidewall roughness of its own, we can do a short thermal oxidation. After that, we can do an oxide deposition, which makes the structure symmetric in the vertical direction.

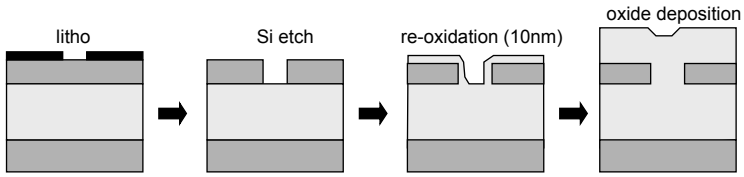

Figure 10: Roughness reduction using a short thermal oxidation and making the structure symmetric using oxide deposition.

An early experimental example of this technique is shown in Figure 11. While the Silicon is not fully etched, we can see that the oxide deposition creates a smooth, planar top cladding and no artifacts (like voids) in the photonic crystal holes. One side effect of this technique is that the SOI structure is sealed from the outside world. While can be advantageous for commercial components, for research purposes it makes close inspection of the structures with an SEM impossible. At the time of writing, no devices have been fabricated with this technique.

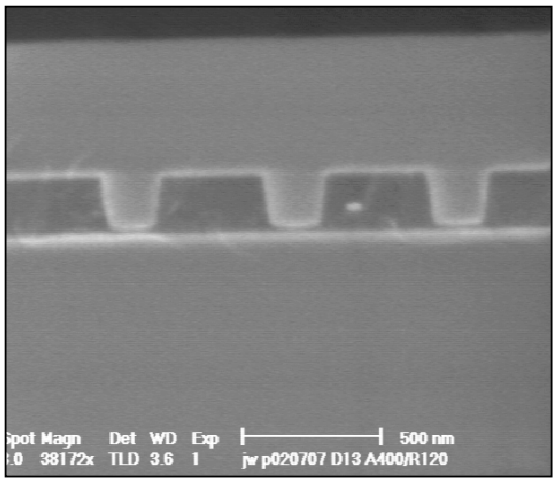

Figure 11: Cross section of photonic crystal holes with 500nm pitch after 5nm oxidation and oxide deposition. Note that there are no voids in the deposited oxide, and that the top surface is planarized.

2.6. Conclusion

We have shown that deep UV lithography with dry etching is a very good candidate for commercial fabrication of nanophotonic structures. However, a detailed process characterization and optimization is needed to reliably produce high-quality components. For lithography, the necessary biases and optical proximity corrections are needed before mask fabrication, and for deep etching one has to care about the sidewall roughness. For optical proximity effects, we have fabricated test structures to measure the necessary corrections. To reduce sidewall roughness due to etching, we can either use thermal oxidation on the silicon top layer, or not etch the oxide and optionally deposit an additional top cladding layer.

3. FABRICATED STRUCTURES

Even though it takes time to go through the design cycle for an expensive photomask, Deep UV lithography is a versatile fabrication tool. We therefore used to fabricate a variety of structures with different purposes in a nanophotonic circuit. We will discuss photonic wires and photonic crystal waveguides, as well as spot-size converters to interface between broad waveguides and nanophotonic waveguides, and grating structures to couple light to and from a single mode fiber.

3.1. Photonic wires and resonators

Because of their small core and high confinement, photonic wires are an ideal structure to test the fabrication quality. Also, they are ideal to make compact resonators, the most common being the ring and racetrack resonator, illustrated in Figure 12. For the deeply etched photonic wires we measured propagation losses of 30dB/mm for 500nm wide wires and 6dB/mm for 600nm wide wires. At that width, however, the wires become multi-mode and unsuitable for nanophotonic ICs.

When we etch only the silicon, matters improve dramatically. As can bee seen in Figure 7, the sidewall roughness is much less, and so are the propagation losses. For 500nm wide wires, we now measure **0.24dB/mm**, an improvement of 25 times with respect to the deeply etched structures. When the wire gets narrower, losses increase exponentially, with 0.74dB/mm for 450nm wires and 3.4dB/mm for 400nm wires. We expect to reduce the losses even more when we apply a thermal oxidation step to smoothen the sidewalls.

We have also measured the transmission of ring resonators. For the racetrack resonator illustrated in the middle of Figure 12 we found well defined, transmission peaks with a quality factor Q≈3000. The resonator has a bend radius of 3μm and a straight coupling section of 3μm.

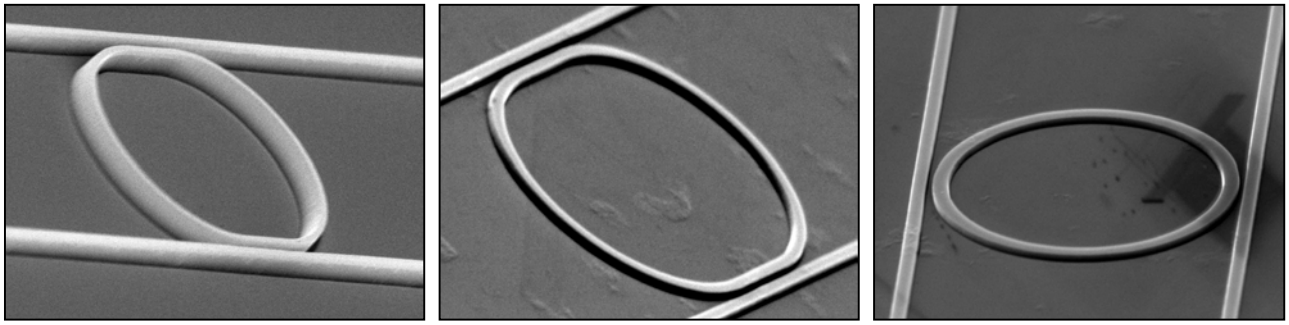

Figure 12: Photonic wire-based ring resonator and racetrack resonator fabricated with deep UV lithography ans Silicon-only etch. No additional roughness reduction techniques have been applied. The left structure is deeply etched, the two right structure have a Silicon-only etch.

3.2. Photonic crystal waveguides

Figure 6 shows a number of photonic crystal waveguides fabricated with deep UV lithography. The top row contains structures where both the top layer and the oxide are etched, while the bottom row contains the same structures, but with a Silicon-only etch. For the deeply etched structures, the losses were excessive because of the scattering of light at the rough sidewalls. For a W1 waveguide with a lattice period of 500nm and a hole size of 320nm we measured waveguide losses of **20dB/mm** in a guided mode in the lattice PBG. At the time of writing, the structures fabricated with a Silicon-only etch have not yet been characterized.

3.3. Compact spot-size converters

Because nanophotonic waveguides have a much smaller spot size than conventional photonic waveguides or optical fibers, it is hard to couple light from one to the other. While a conventional adiabatic taper can do the job, it should be very long to couple from a 10μm wide fiber mode to a 500nm wide photonic wire or photonic crystal waveguide. Therefore, a more compact solution is to design a structure that creates a multi-mode interference pattern to image the light of the large mode onto the smaller mode and vice versa [12]. One of these structures is illustrated in Figure 13. After optimization, this type of spot-size converters can have over 90% transmission.

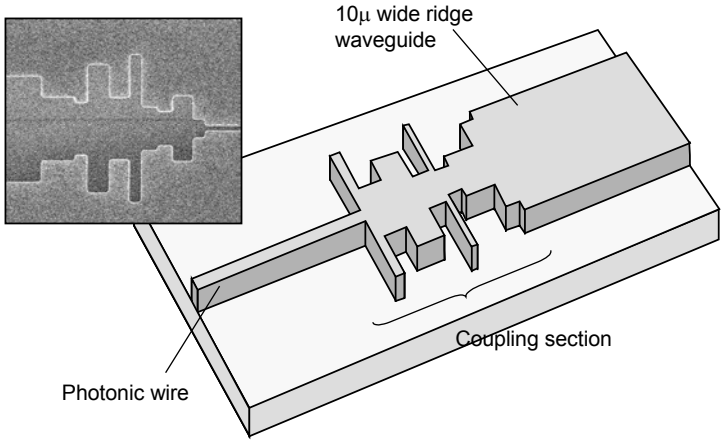

Figure 13: Short spot-size converter between a 10μm wide ridge waveguide and a 500nm wide photonic wire. The irregular shape creates an interference pattern that effectively couples the ground mode of the broad waveguide to the ground mode of the photonic wire.

3.4. Coupling to Single mode fiber

Because silicon-on-insulator has only a thin core layer, butt-coupling to a single-mode fiber introduces unacceptable losses, even from a 10μm wide ridge waveguide. While this can be solved by fabricating a low-index taper structure on top of the waveguide[9], this approach may be undesirable because it consumes a large surface area, and the top layer may be incompatible with other processing steps.

We have demonstrated a fiber coupler consisting of a second-order diffractive grating to couple from a broad ridge waveguide to a vertically oriented, butt-coupled single-mode fiber[11]. This is illustrated in the left part of Figure 14. Although the grating is etched only 50nm into the silicon, it is a strong grating, as the etch depth is a significant fraction of the 220nm core thickness. Theoretical calculations show that this grating can couple about 20% of the light to and from the fiber. When enhanced with an optimized multi-layer SOI stack and an additional first-order grating, the efficiency can be boosted to more than 70%.

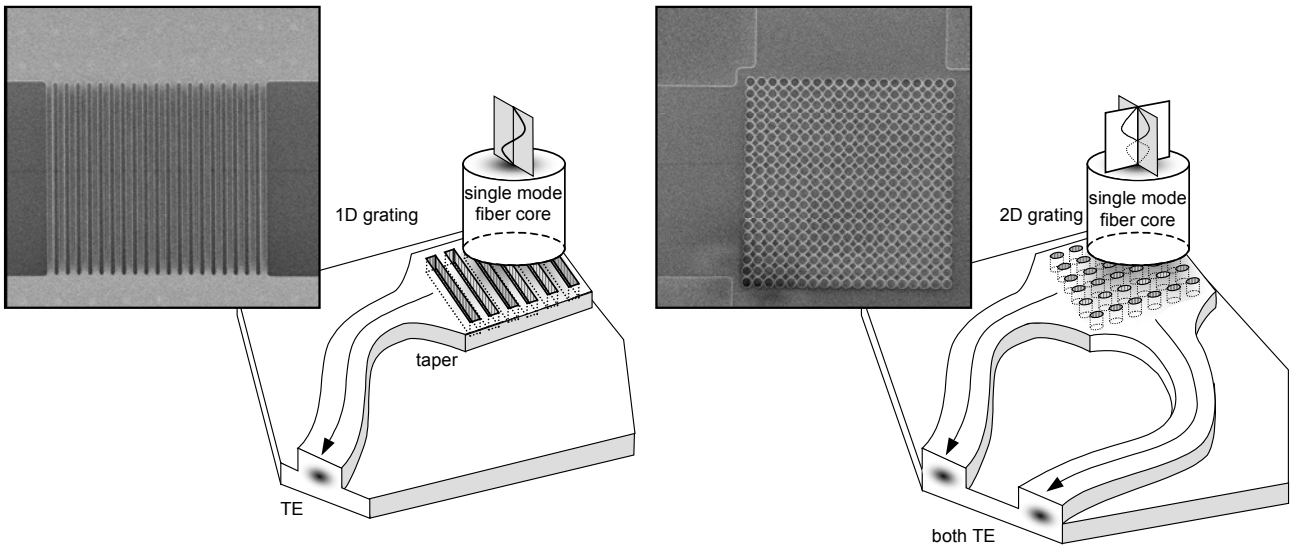

Figure 14: Fiber coupling structures in Silicon-on-insulator. The single mode fiber is oriented perpendicular to the substrate. Left: 1-D grating, coupling one fiber polarization to the TE mode of a ridge waveguide. Right: a 2-D grating, coupling both fiber polarizations to its own waveguide, both in the TE waveguide polarization.

The grating is polarization sensitive. Using the 1-D grating would therefore result in the loss of one fiber polarization. As the polarization of a single-mode fiber is generally an unknown, this is unacceptable. Therefore, we have designed a 2-D grating that couples both fiber polarizations to its own waveguide, as shown in the right part of Figure 14. The polarization in both ridge waveguides is then TE, so both signals can be processed in an identical circuit, leading to a simple polarization diversity approach[12].

We have fabricated these structure with deep UV lithography, and both the 1-D and the 2-D gratings perform close to the theoretical prediction with a coupling efficiency of between 16% and 20% [11,12].

3.5. Multi-step processing

Because these fiber couplers require a different etch depth that the other, high-contrast structures, they are to be fabricated in a separate process step. At the time of writing, a photomask has been created add the fiber couplers to our photonic crystal and photonic wire components. Here, we can also take advantage of the technology base of CMOS processing, using the alignment capabilities of the advanced deep UV steppers.

4. CONCLUSIONS

We have demonstrated the use of deep UV lithography for the fabrication of nanophotonic structures. While deep UV lithography is already the workhorse for CMOS fabrication, nanophotonics pose a completely different set of requirements on the fabrication process. As alignment issues are much more critical the single-step processing can introduce a considerable mismatch between de different types of components. Detailed process characterization is required to determine the correct bias for lines, holes and other types of structures. Also, the dense nature of photonic crystals gives rise to optical proximity effects. Being a coherent effect, these are hard to model. We have fabricated test structures to experimentally measure optical proximity effects, and the necessary corrections to apply on the mask.

For the fabrication we used the photoresist as an etch mask. Because the deep etching, though both silicon and oxide caused a large amount of sidewall roughness, we had to look for roughness reduction technique. The most promising proves to be not to etch the oxide, but only the top Silicon layer. Optionally, an additional oxide layer can be deposited on top of the silicon to make the structure more vertically symmetric.

We have fabricated and characterized a number of components. For deeply etched photonic crystal waveguides we measured waveguide losses of about 20dB/mm. Photonic wires fabricated with the same process have losses of 30dB/mm for 500nm narrow wires down to 6dB/mm for 600nm narrow wire. These rather high losses are attributed to sidewall roughness. When we etch only the Silicon, effectively eliminating a large amount of roughness, the wire losses for 500nm wires drop to 0.24dB/mm.

We have also designed and fabricated mode converters and grating structures to facilitate the interface to single-mode fiber. Our experimental results show a coupling efficiency of up to 20% to and from a single mode fiber to a 10μm wide SOI ridge waveguide.

Summarized, we can state that deep UV lithography has the potential to provide a commercial mass-manufacturing base for nanophotonic components. While detailed process characterization and development is required, we have shows that man fabrication hurdles can be overcome.

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