FACULTY OF ENGINEERING AND ARCHITECTURE

III-V-ON-SI SOAS AND DFB/DBR LASERS REALISED USING MICRO-TRANSFER PRINTING

Bahawal Haq

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Interreg France-Wallonie-Vlaanderen UNION EUROPÉENNE EUROPESE UNIE

SAFESIDE

LIGHT AS WE SEE IT!

Dispersion

Reflection

Scattering

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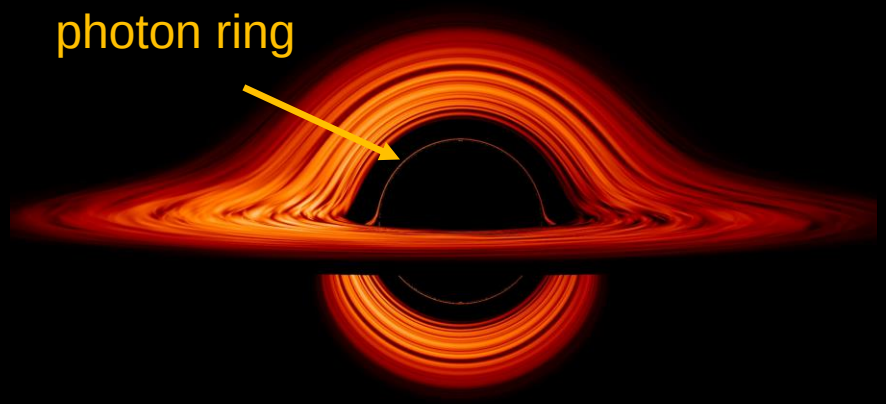
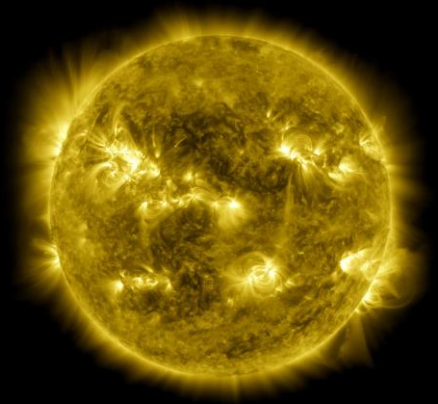
MARVELS OF LIGHT

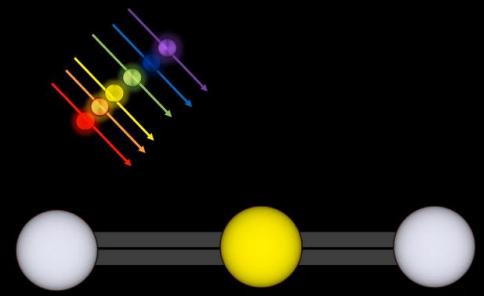
Light interacts with matter at every scale



NASA's Goddard Space Flight Center



NASA's Goddard Space Flight Center

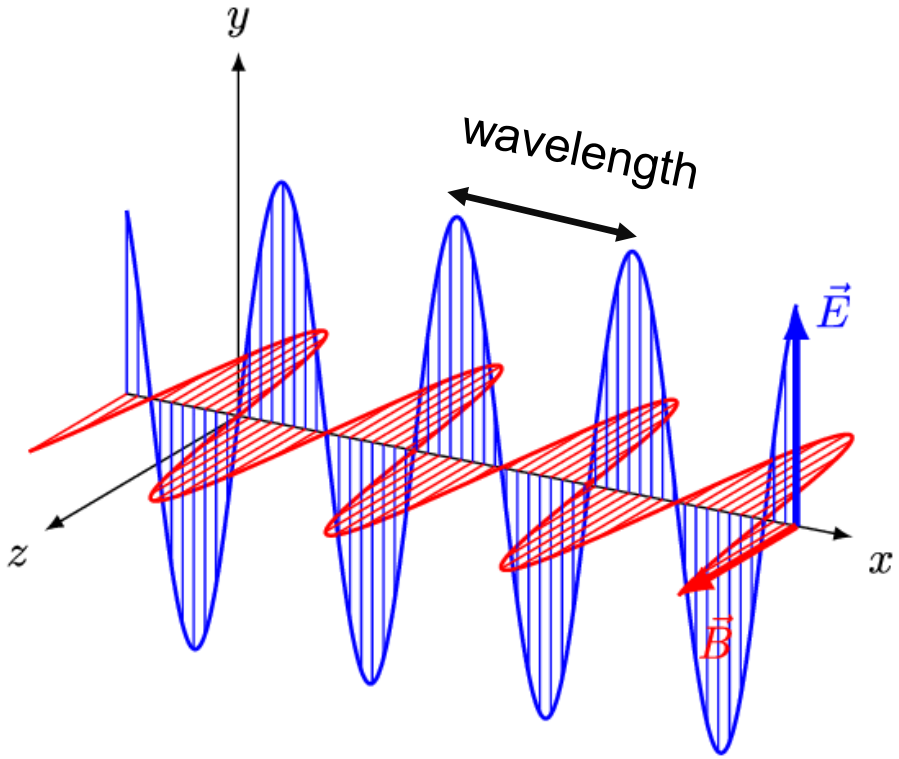


Vibrational mode of gas molecules

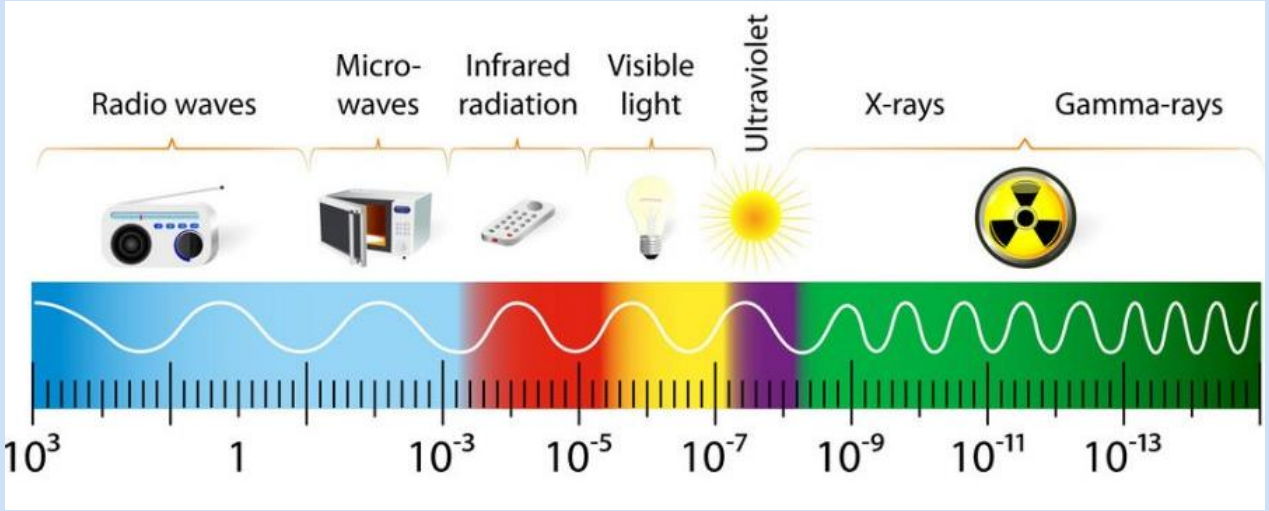
From celestial bodies to molecules

PHYSICS OF LIGHT

Electric and magnetic fields



Electromagnetic Spectrum



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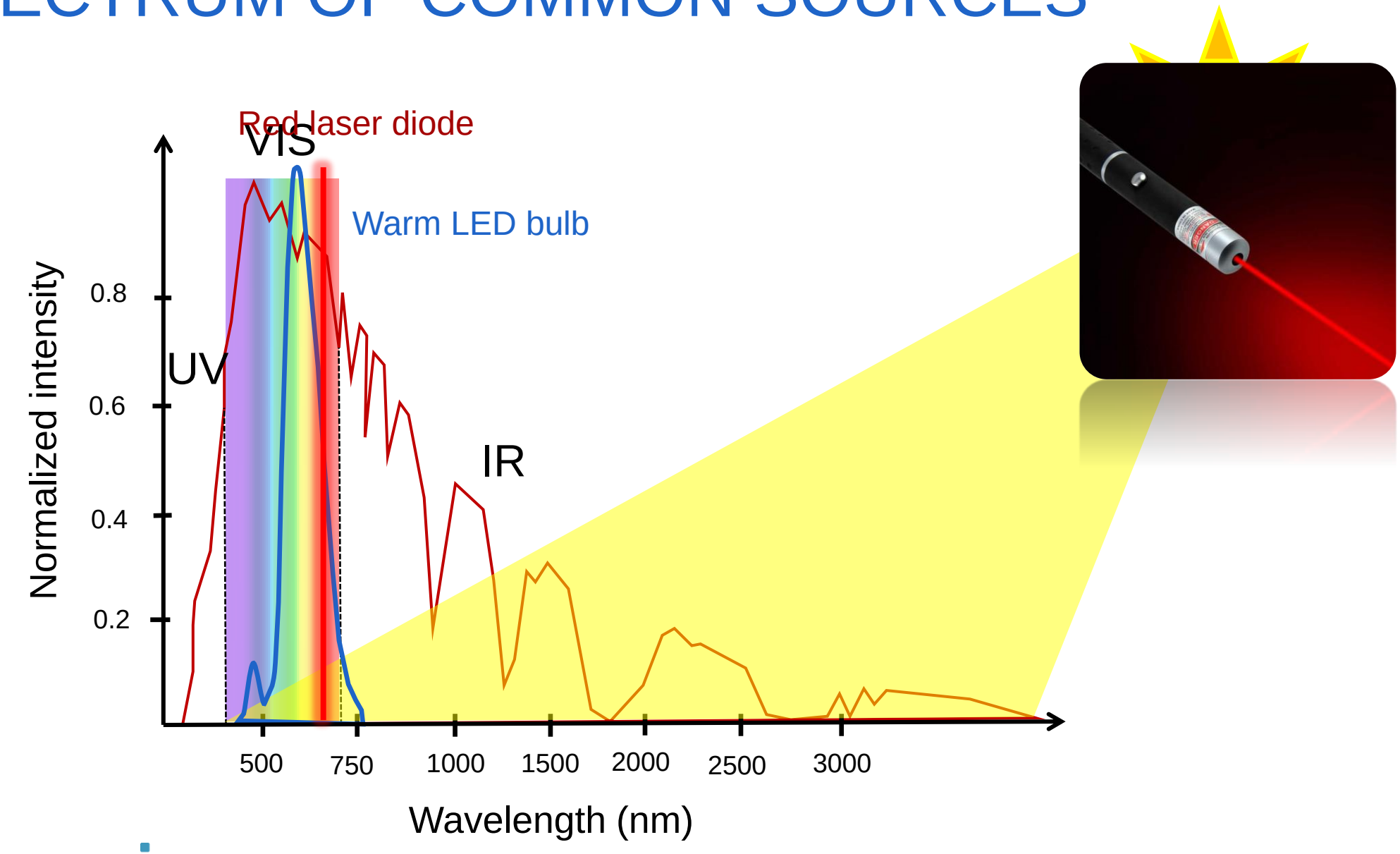
SPECTRUM OF COMMON SOURCES



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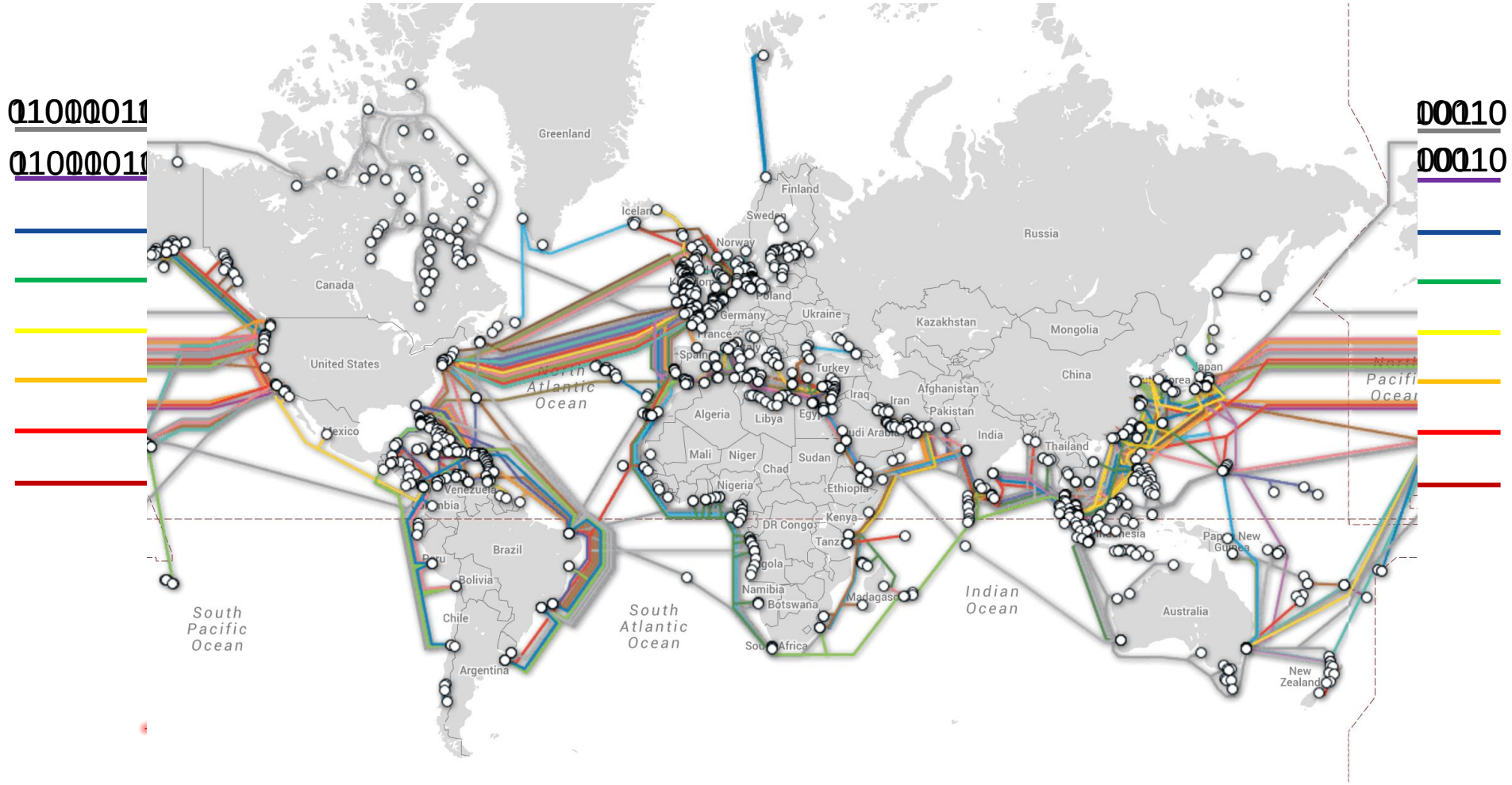
OPTICAL COMMUNICATION



Underwater fiber optics network connects the world

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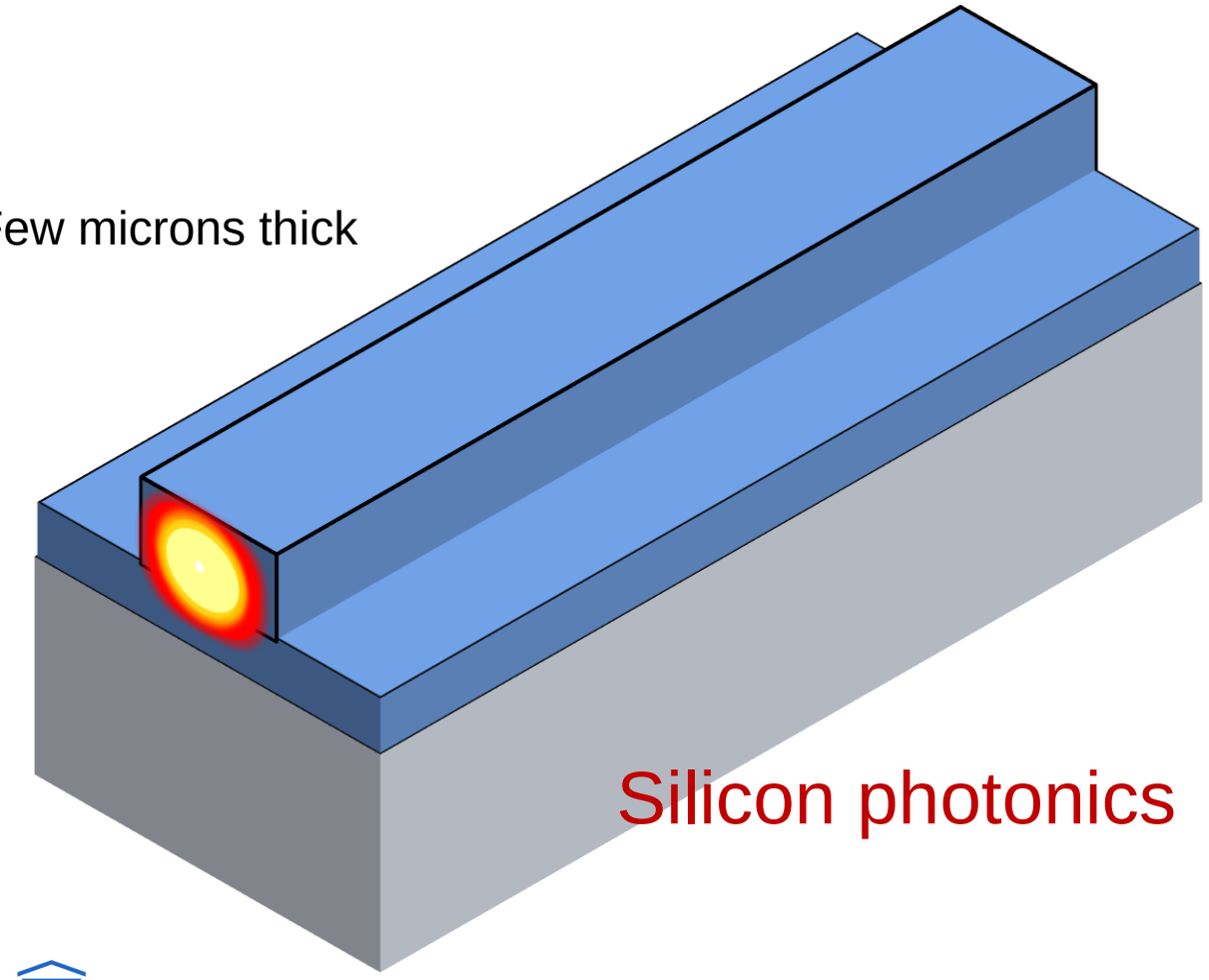
LIGHT CAN BE GUIDED ON-CHIP

Few microns thick

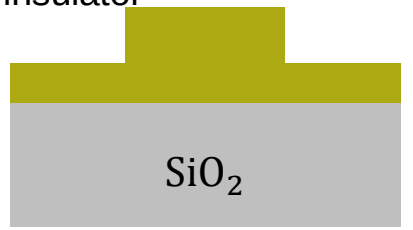


Silicon photonics

AlGaAs-on-insulator

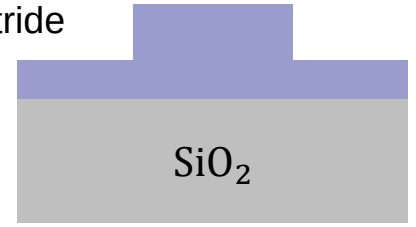
- Excellent non-linear properties
- Both active and passive devices are possible
- Mosly used in R&D
- High cost and low volume

Lithium niobate-on-insulator



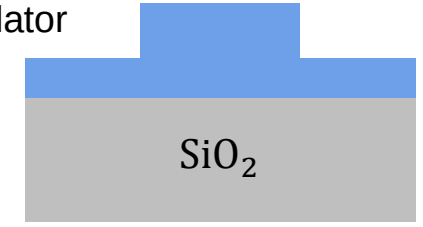
- Good Electro-optic and acoustic-optic properties
- Not mature platform, still under develpoment

Silicon nitride



- CMOS compatible
- Relatively mature
- Ultra-low loss platform
- Larger bend radii and lower density of integration

Silicon-on-insulator



- CMOS compatible and mature ecosystem
- Monolithic electronics-photonics integration
- Inefficient light sources

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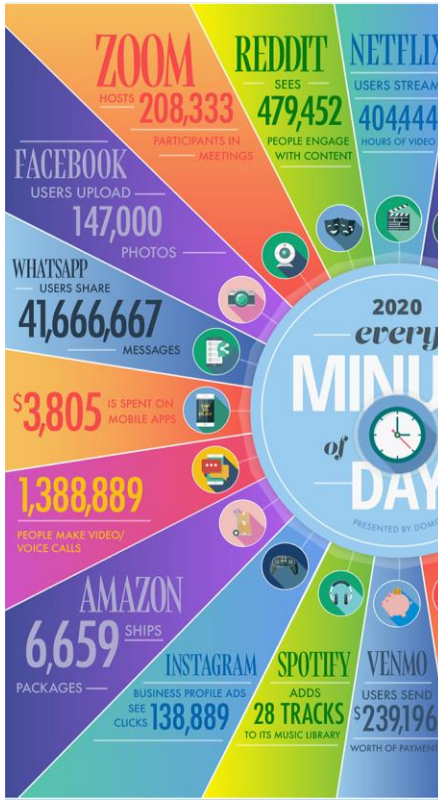
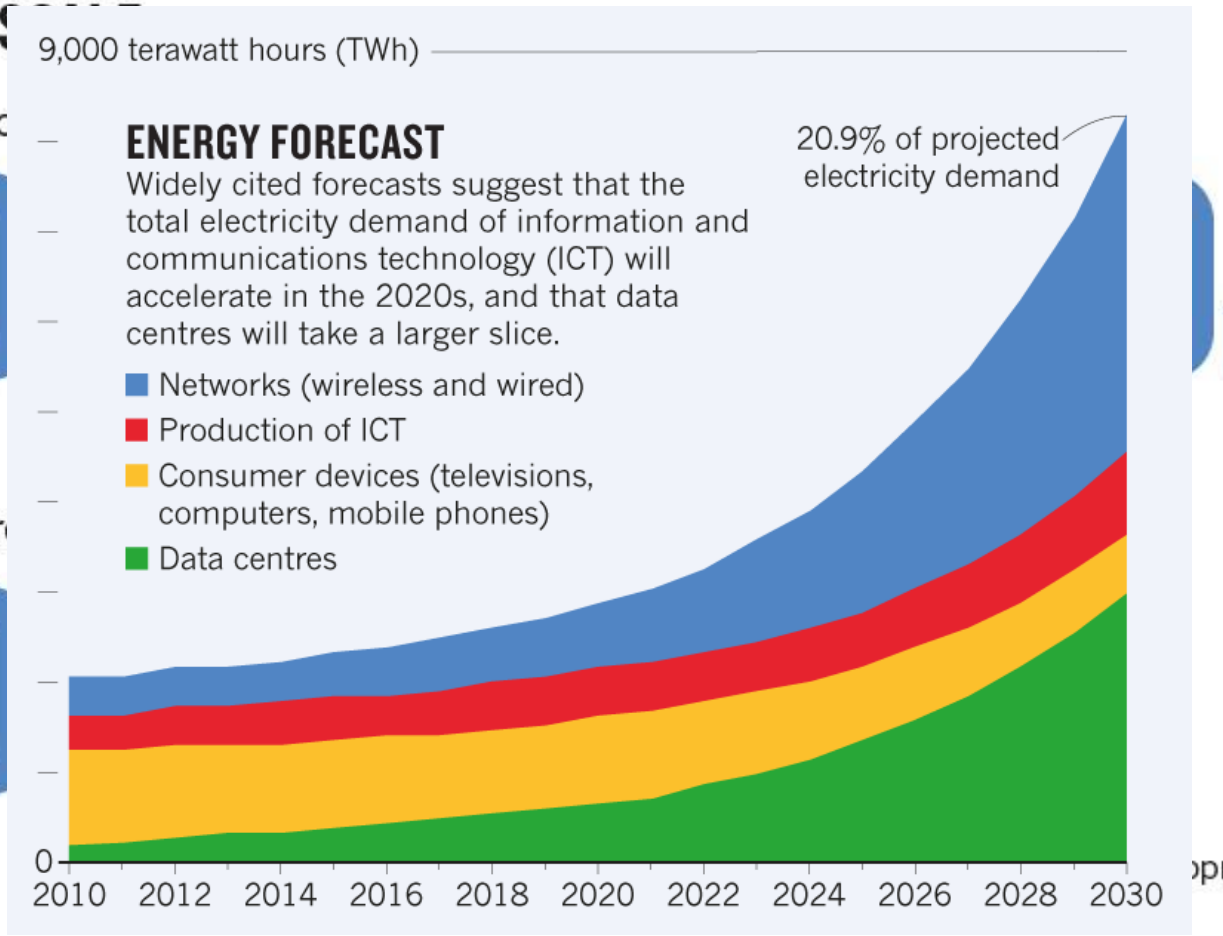
WHY GO ON-CHIP? (1)

Astronomical amount of data





TWh

ata

en servers which

erates heat.

pproximate.

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TO PUT INTO CONTEXT

60 mins of video streaming

https://www.carbonbrief.org/factcheck-what-is-the-carbon-footprint-of-streaming-video-on-netflix

1.1 Km

Running distance for a 75 Kg person

https://www.runningtools.com/energyusage.htm

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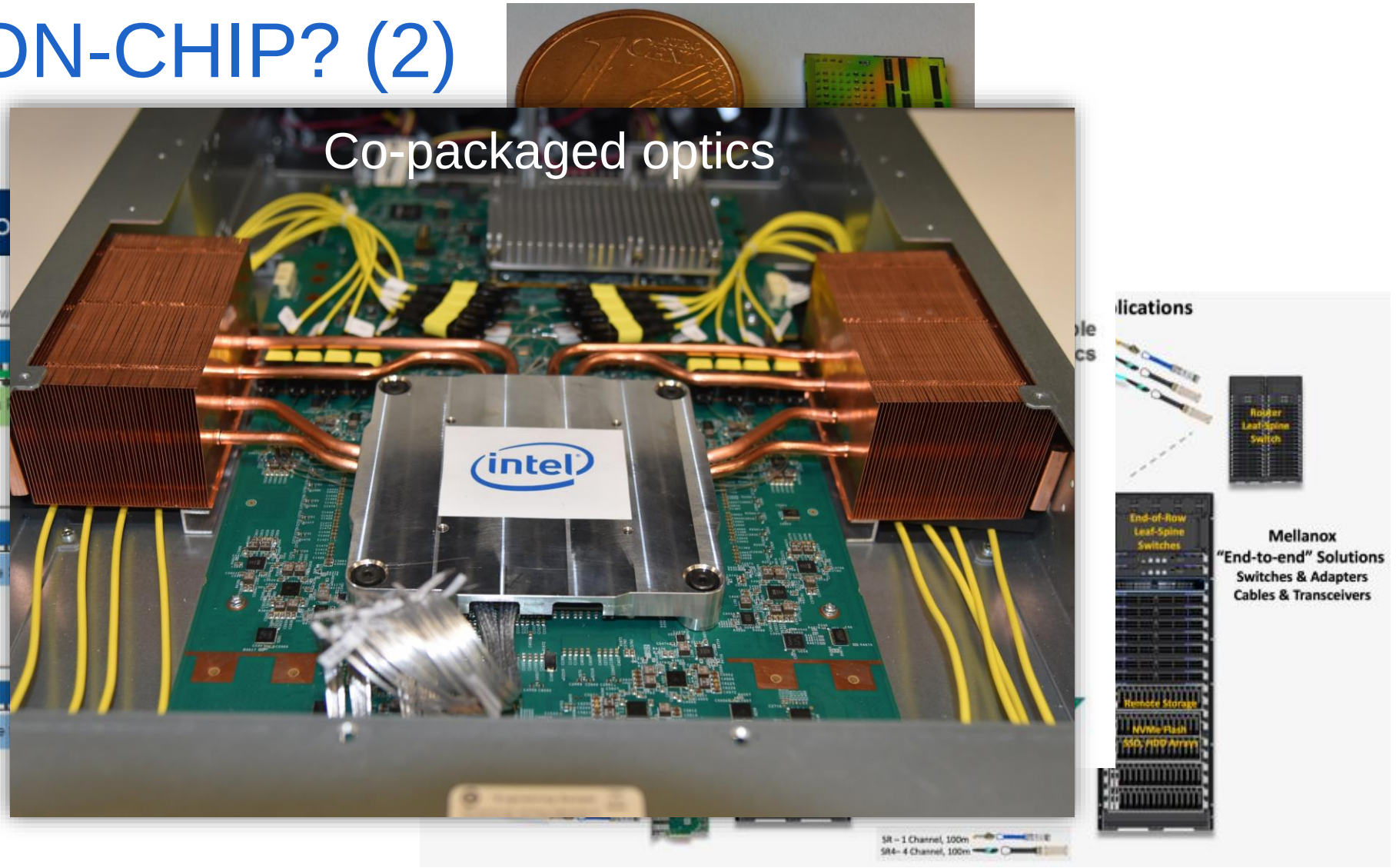
WHY GO ON-CHIP? (2)



- It allow us to n
  and inexpensi
  modules

Integration of 1.6 Tbps silicon photonics engine with its 12.8 Tbps programmable Ethernet switch.

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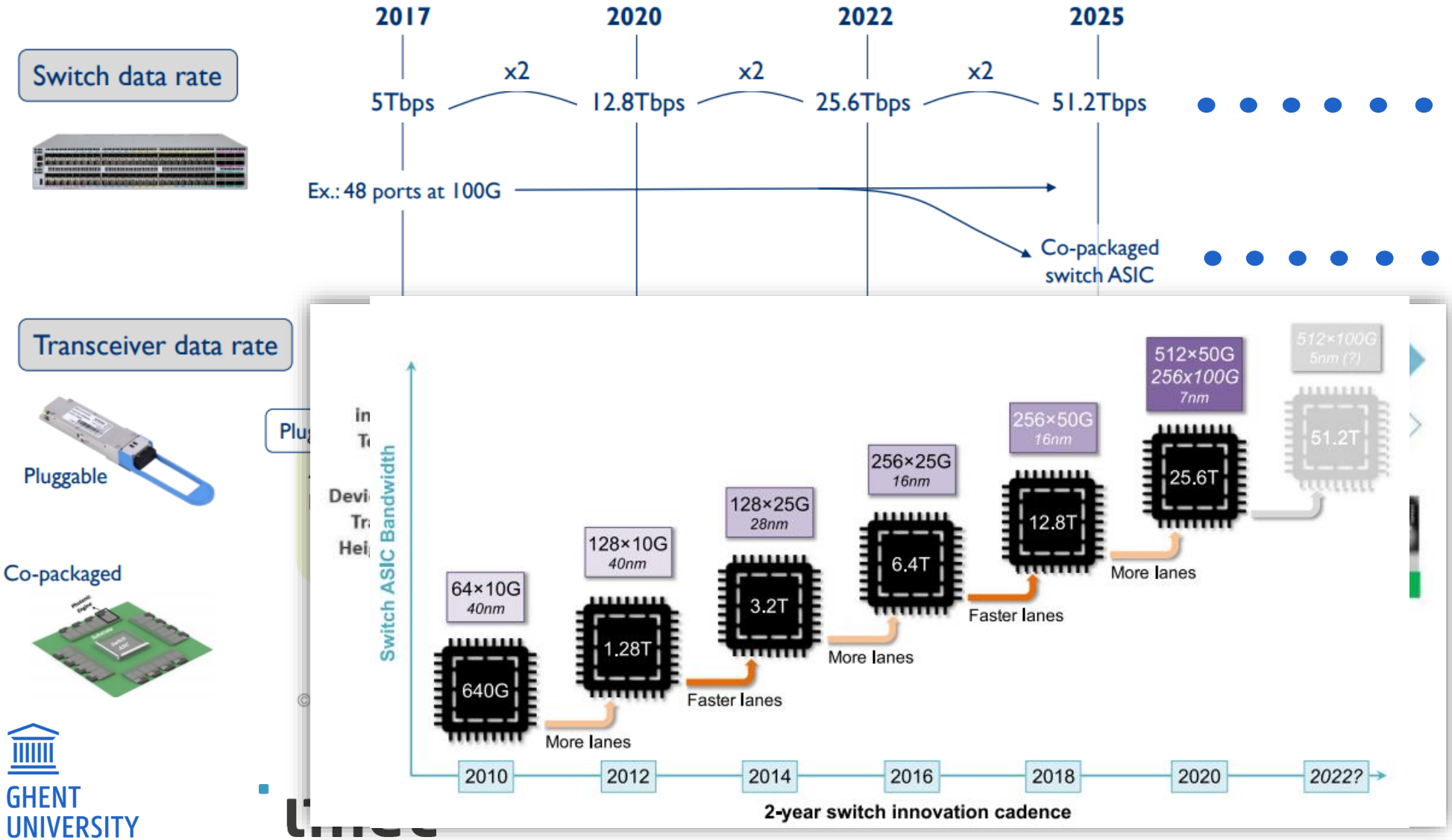
WHAT'S NEXT



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Moore's Law will continue

More intimate integration (modular)

Faster, smaller and cheaper

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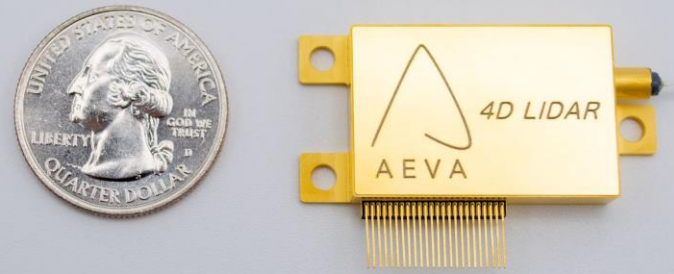
THERE IS MORE TO IT! (LIDAR)

LiDAR on chip

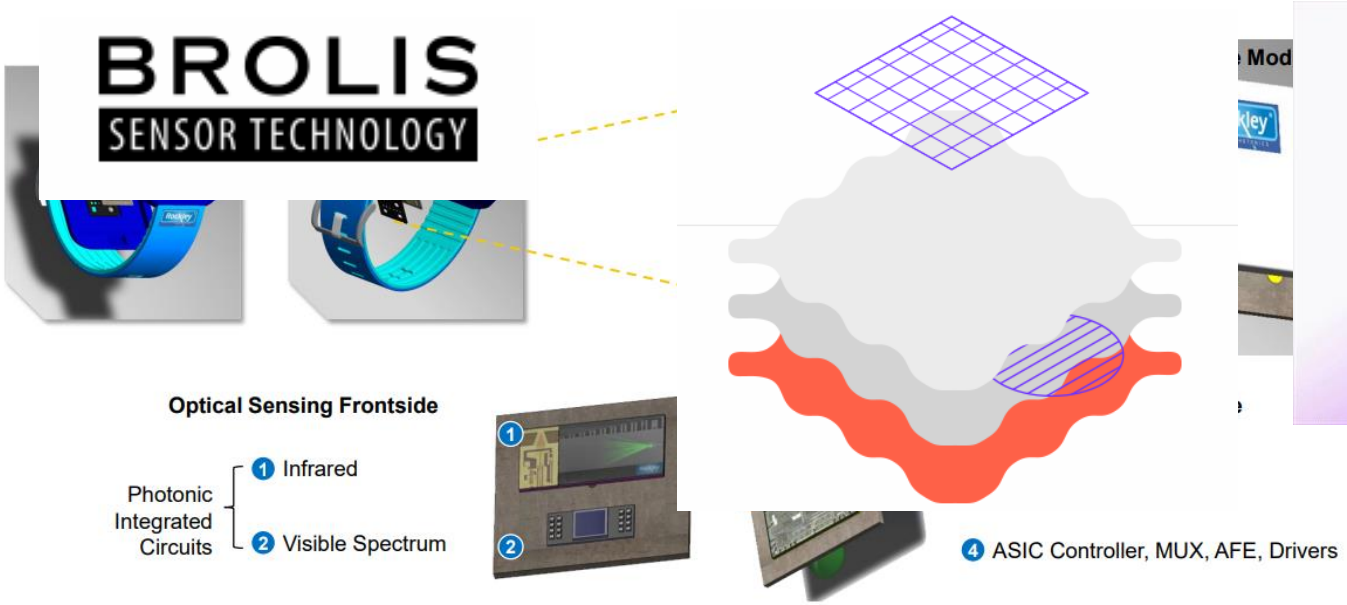


Lighter, smaller and cheaper

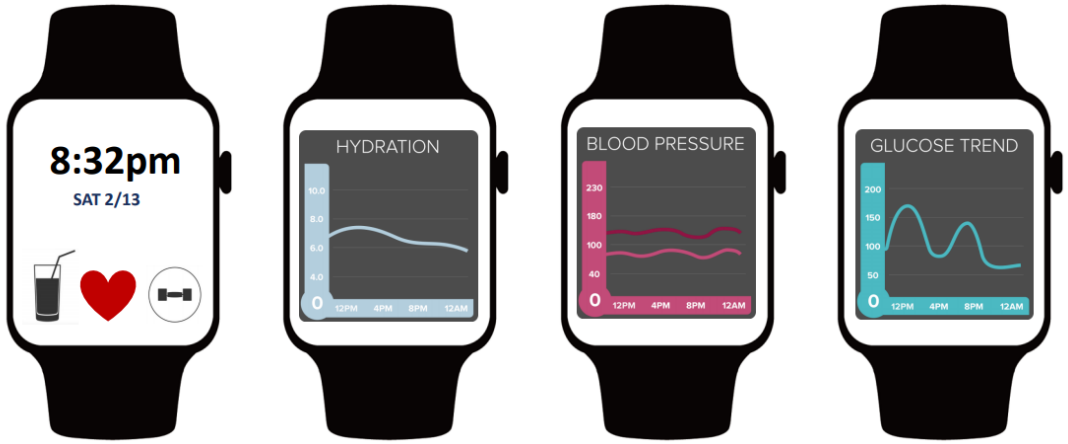
- Bulky with expensive optics

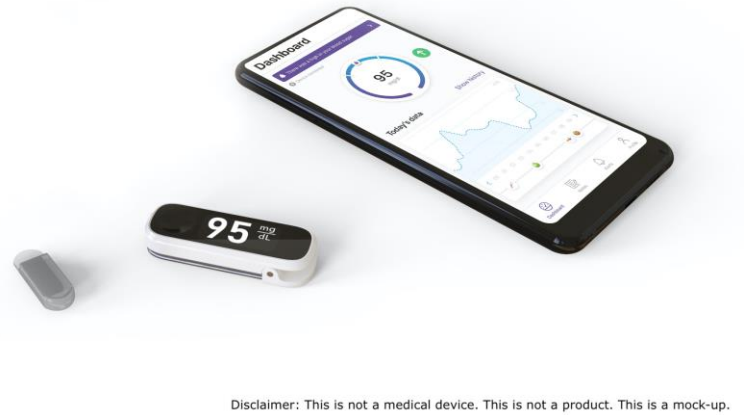
AND MORE! (HEALTHCARE)

Si Photonics in action



Transdermal sensing of blood for glucose, lactate and ethanol





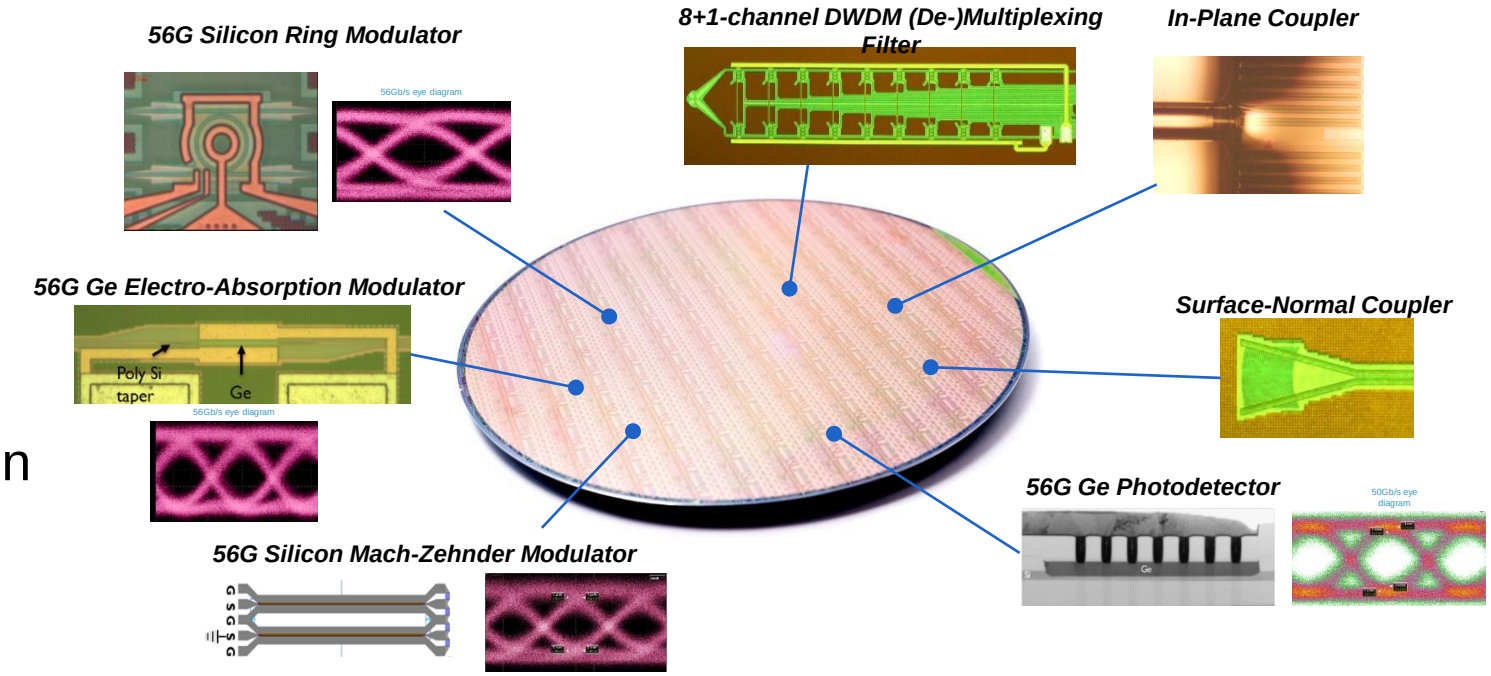
Continuous Glucose Monitoring (CGM) systems

WHAT IS MISSING IN SI PHOTONICS?

IMEC's 56G platform

Missing

- III-V-on-Si integration
- SOAs on-chip
- Lasers on-chip



- Designed for 1.3 - 1.55 μm communication window
- Co-integration of the various building blocks in a single platform
- Today available on 200mm wafer size, coming soon on 300mm
- 95% compatible with CMOS130 in commercial foundries

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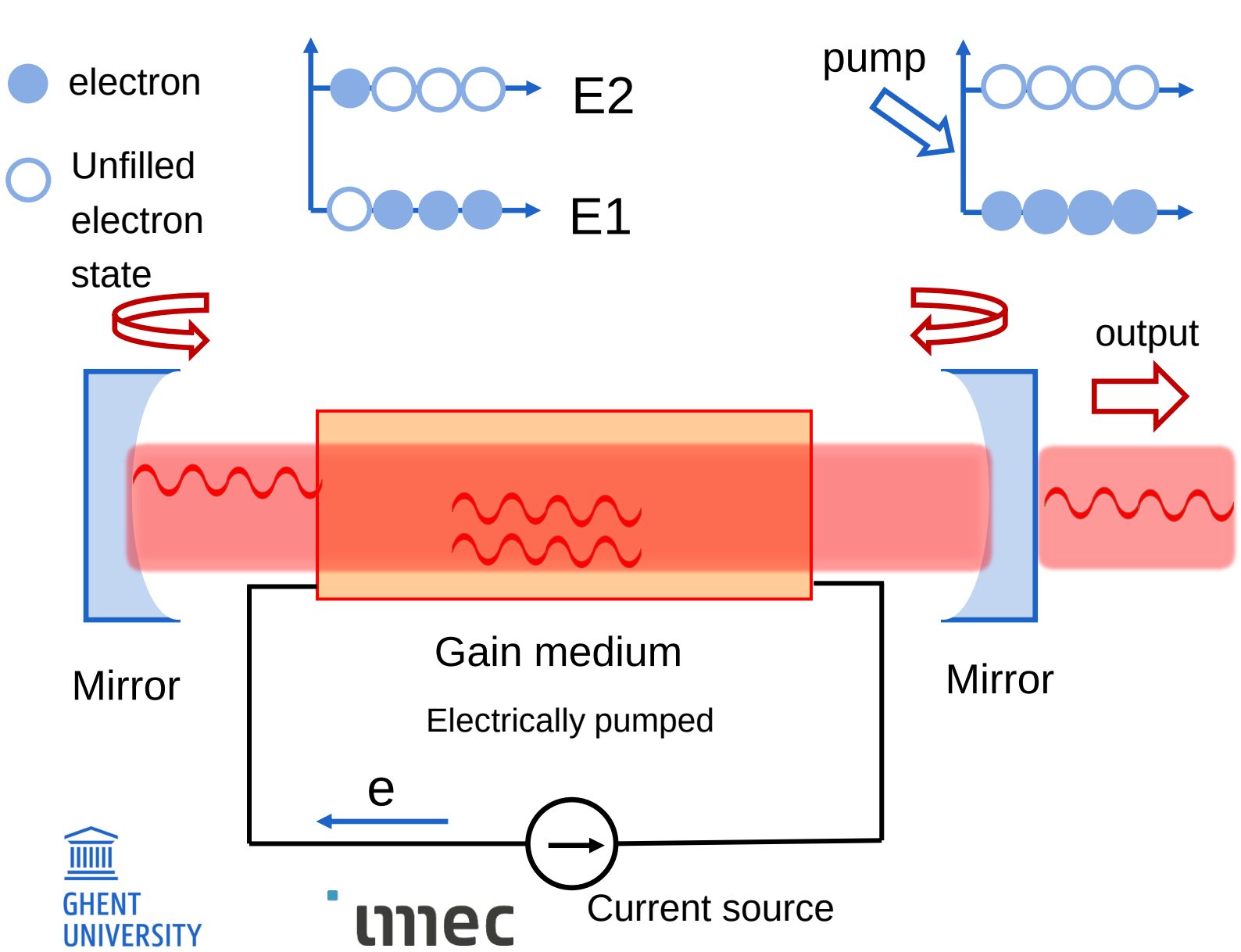
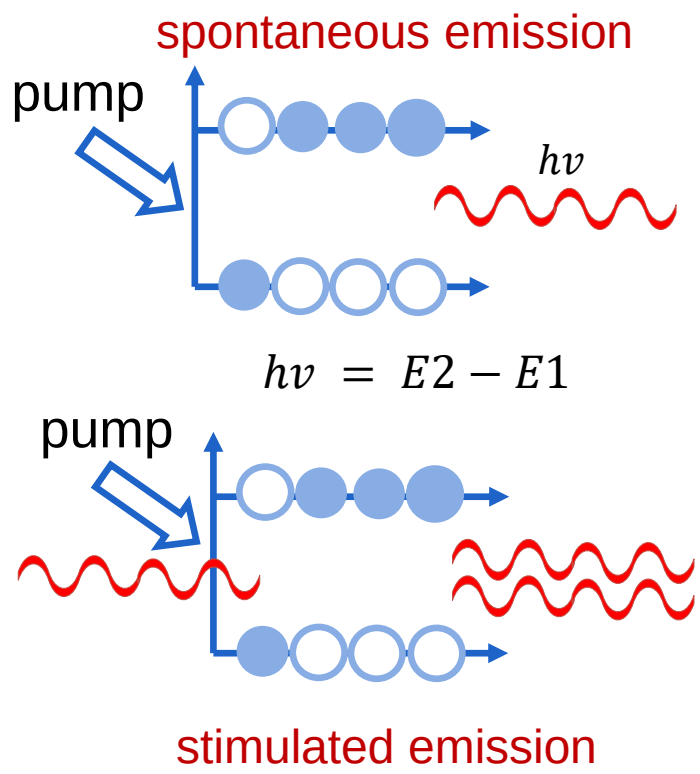
WHAT IS A LASER?

Light amplification by stimulated emission of radiation





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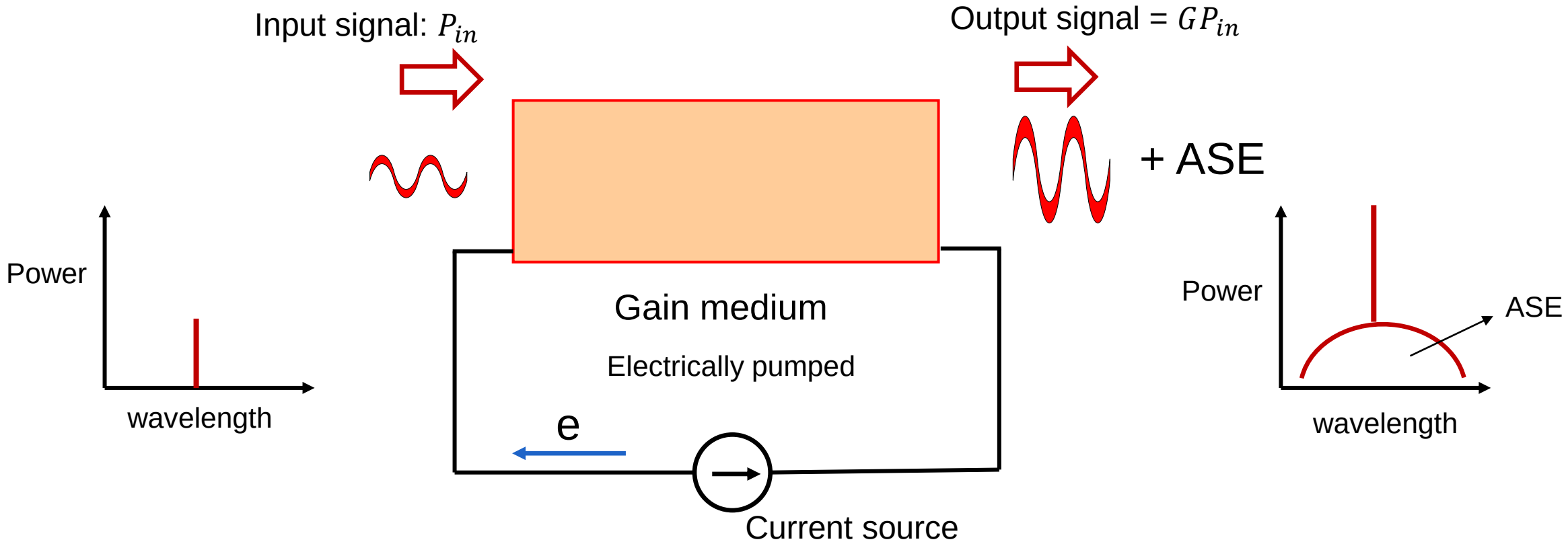
WHAT IS A SOA?

Semiconductor optical amplifier



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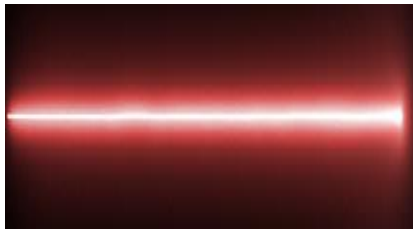
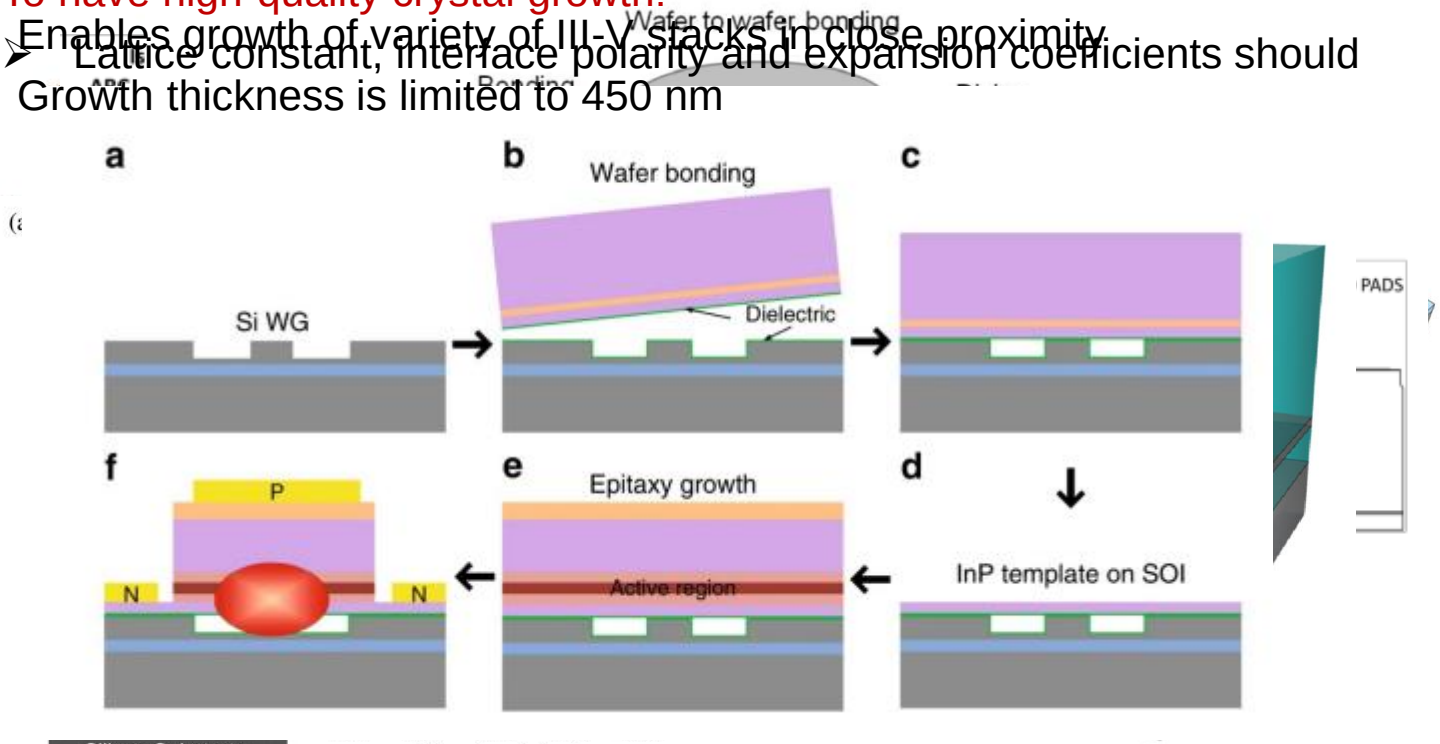
INTEGRATION OF III-V-ON-SILICON

Light sources/SOA

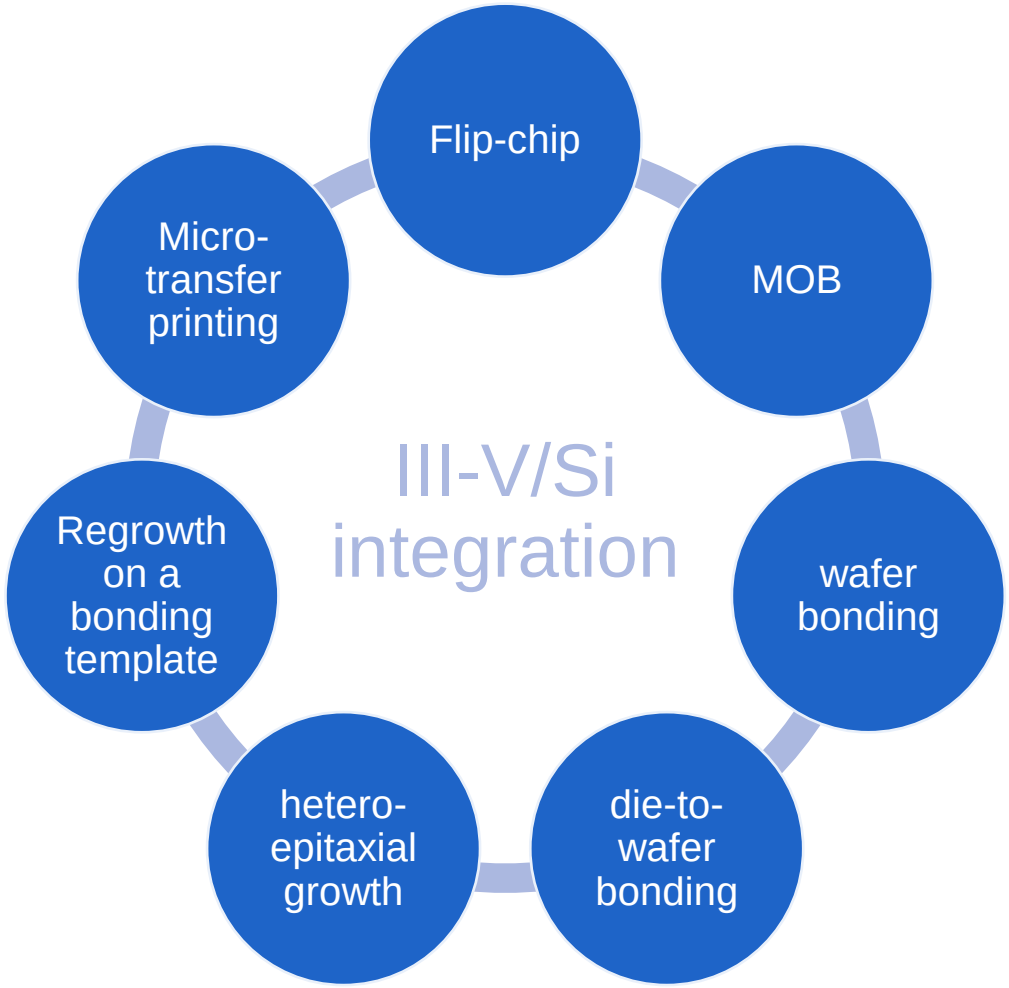


III-V direct bandgap materials

- Combines wafer bonding and epitaxial growth
- To have high-quality crystal growth:
- Enables growth of variety of III-V stacks in close proximity
  - Lattice constant, interface polarity and expansion coefficients should
- Growth thickness is limited to 450 nm

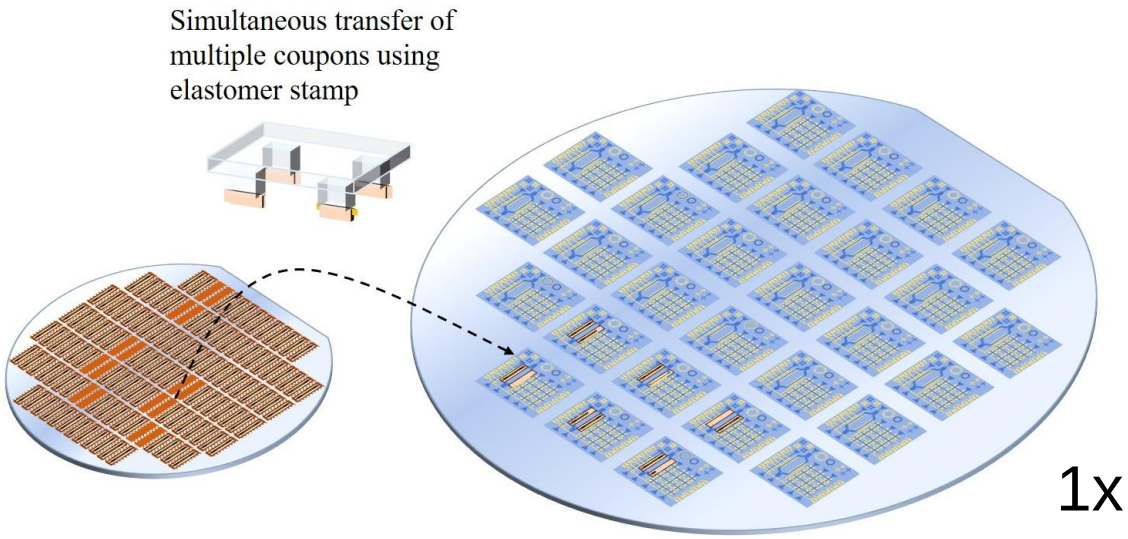


Existing technologies

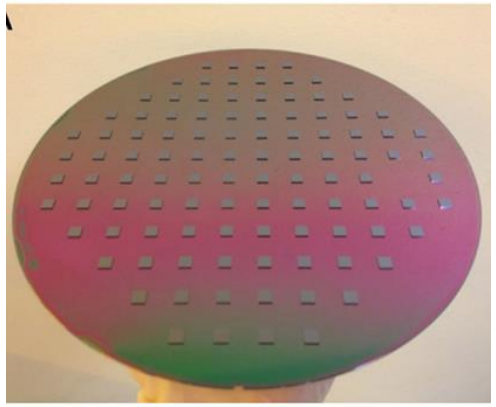


- Not mature and integration with a full SiPh process flow is challenging

MICRO-TRANSFER PRINTING-CONCEPT



1x1 mm^2



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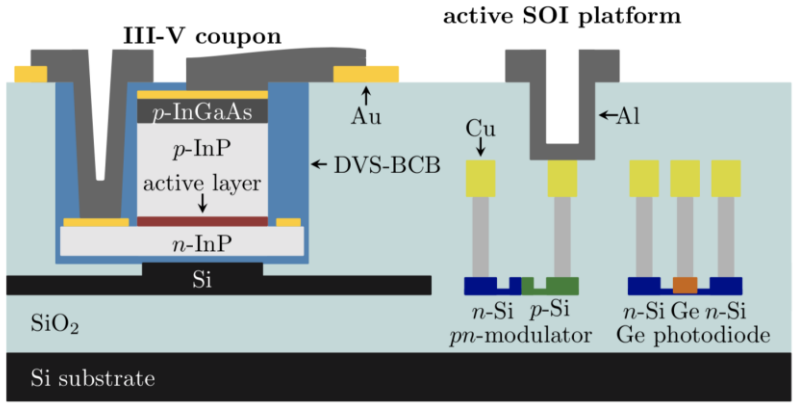

Advantages:

- Efficient use of expensive III-V material/devices
- Devices with different layer epitaxial structure can be populated closely on the SOI wafer.
- Integration of the devices doesn't require modification of FEOL and BEOL Si photonics process in a commercial foundry (modular).

Combines wafer bonding integration approach with flip-chip

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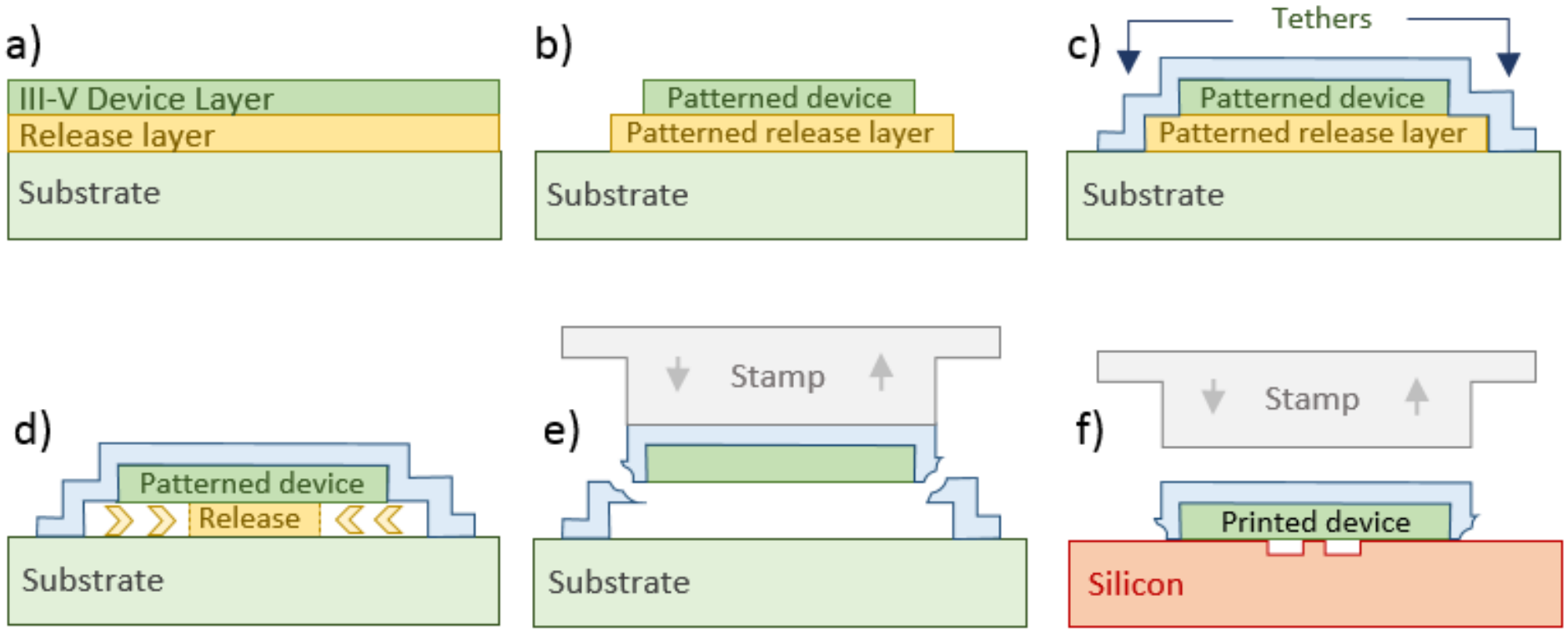
PROCESS FLOW OF μTP



Release layer is incorporated underneath the device functional layers

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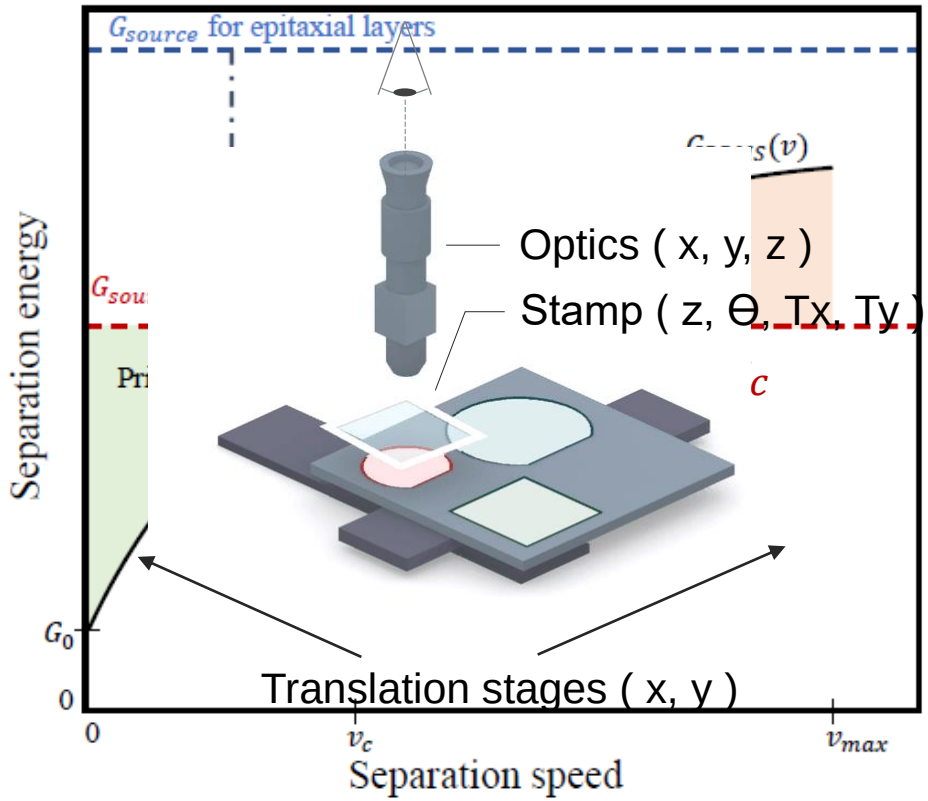
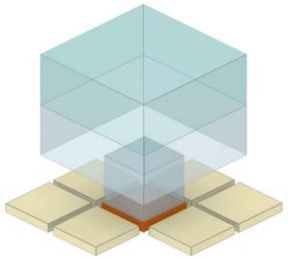
PROPERTIES OF PDMS STAMPS

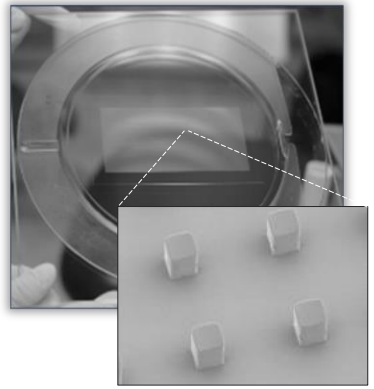
Stamp + Motion + Optics

Visco-elastic property

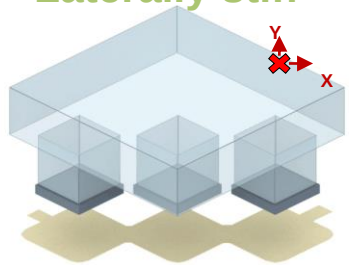


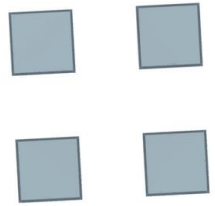
Compliant





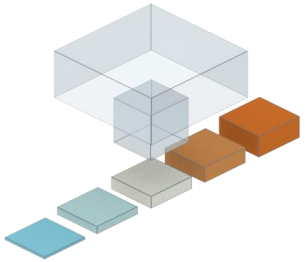
Laterally stiff





Top View

Transparent



Soft

μTP is enabled by PDMS stamps

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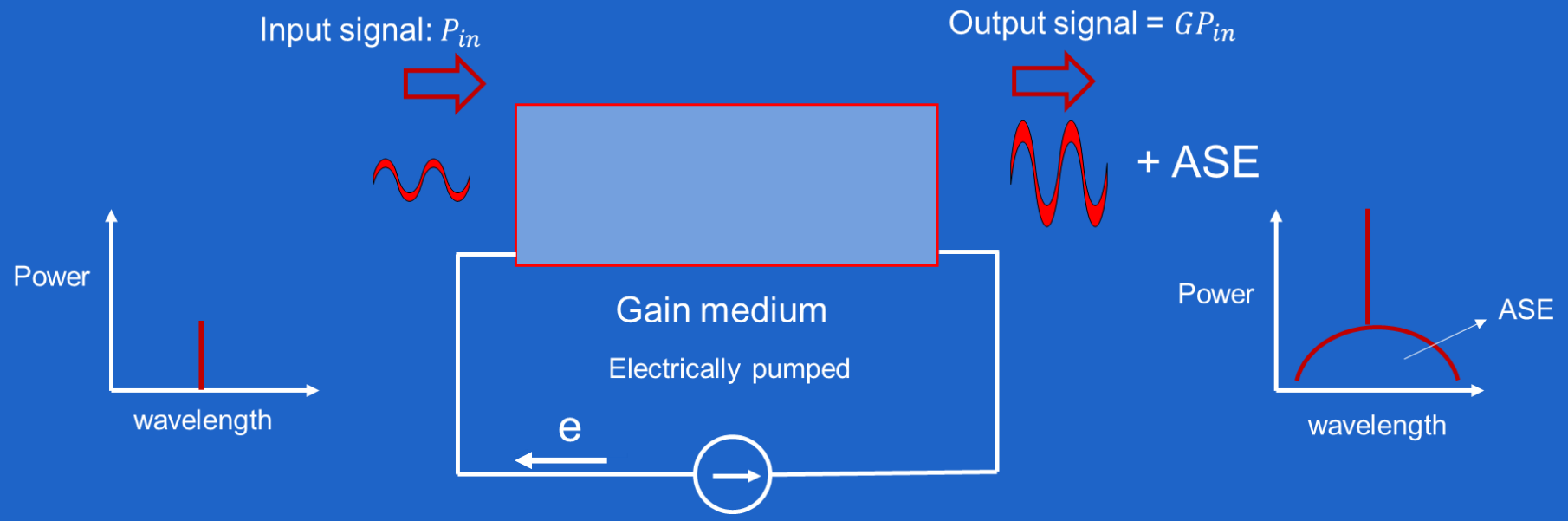

μTRANSFER-PRINTED III-V-ON-SI SOA

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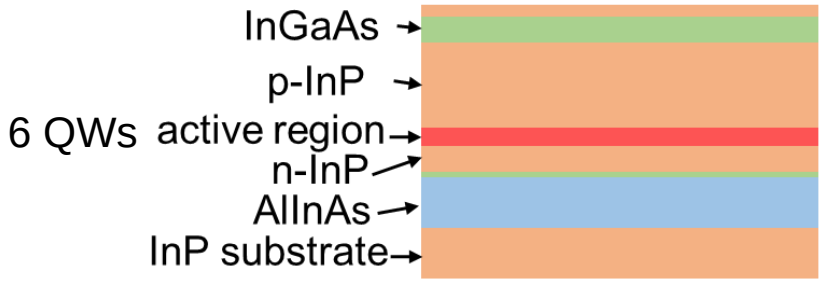
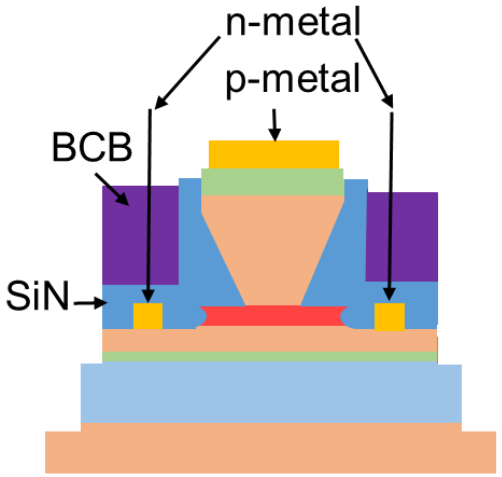
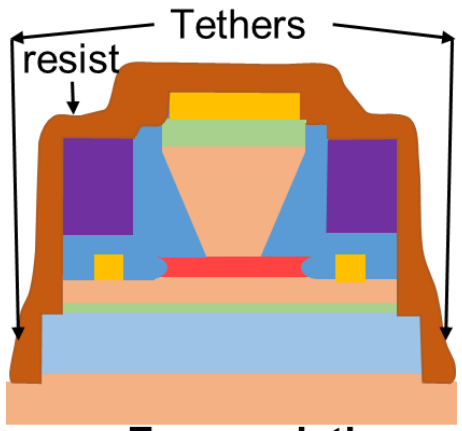
MICRO-TRANSFER-PRINTING SOA PROCESS FLOW



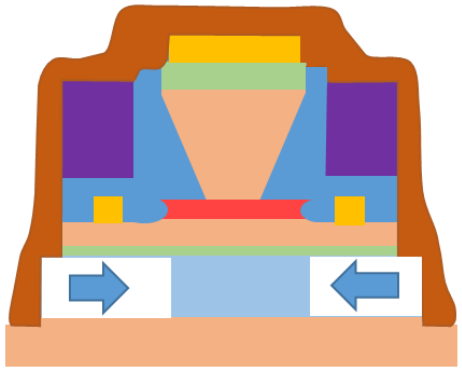
Epitaxial layers



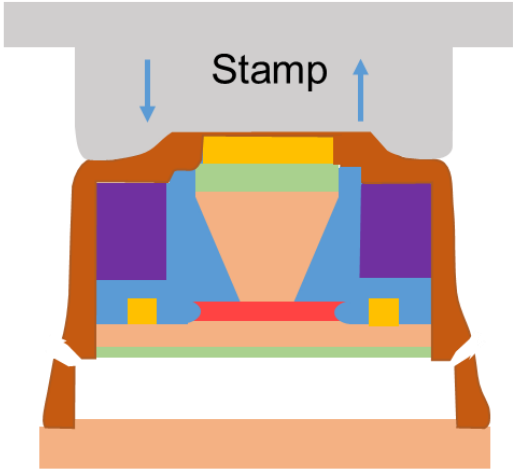
Patterned SOA and release layer



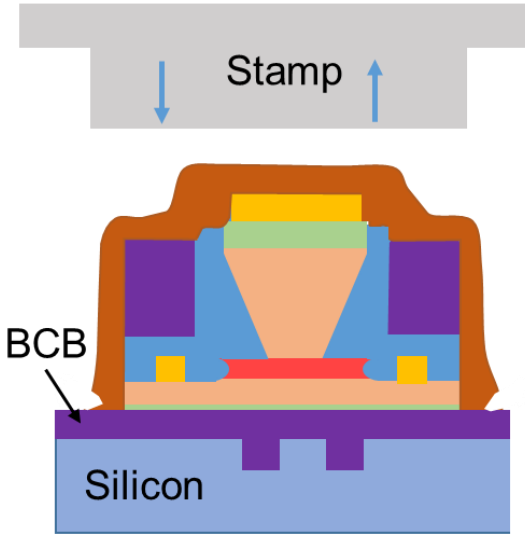
Encapsulation



Release etch



Pick-up



Printing

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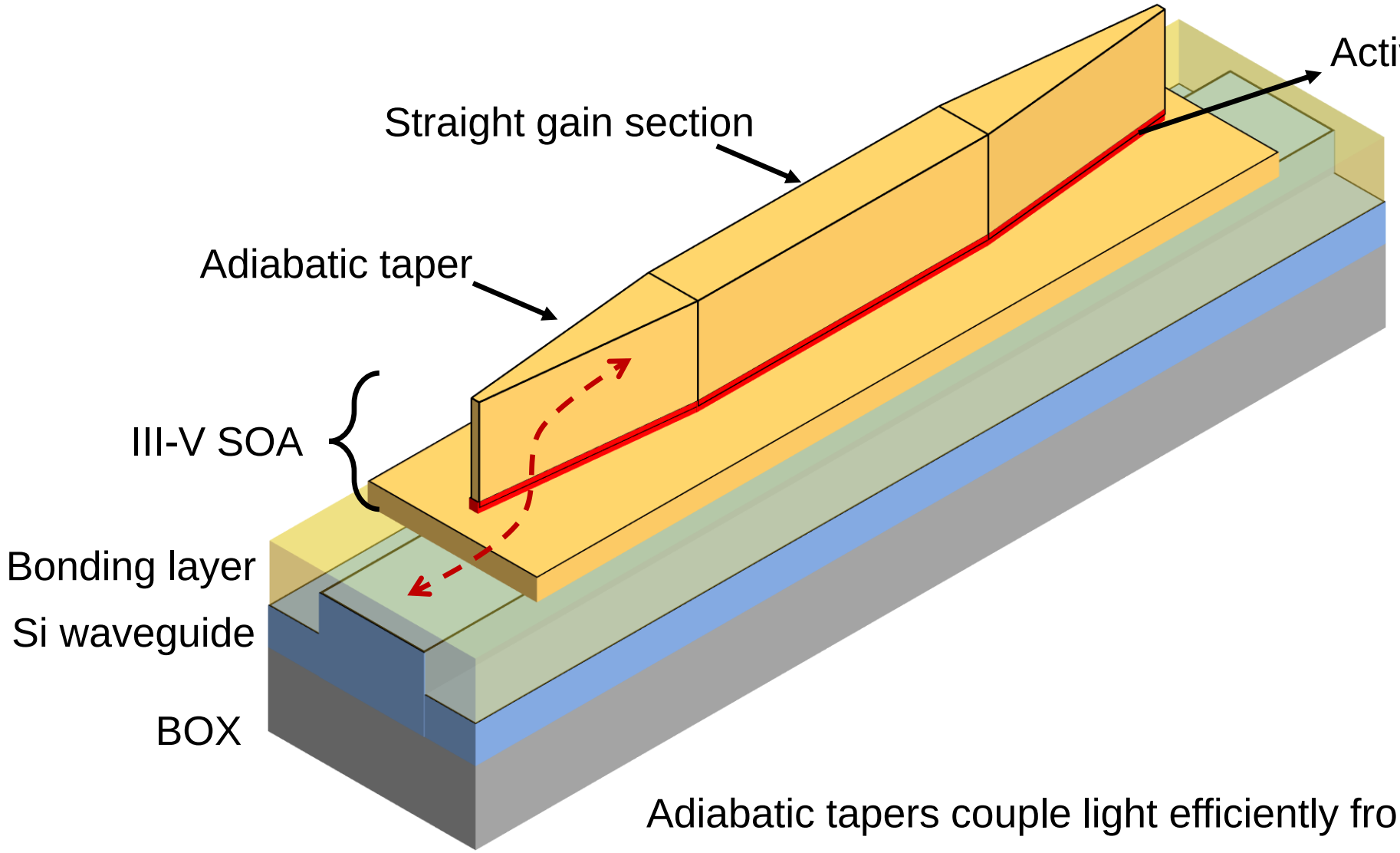
STRUCTURE OF A III-V-ON-SI SOA



Adiabatic tapers couple light efficiently from III-V waveguide to Si waveguide

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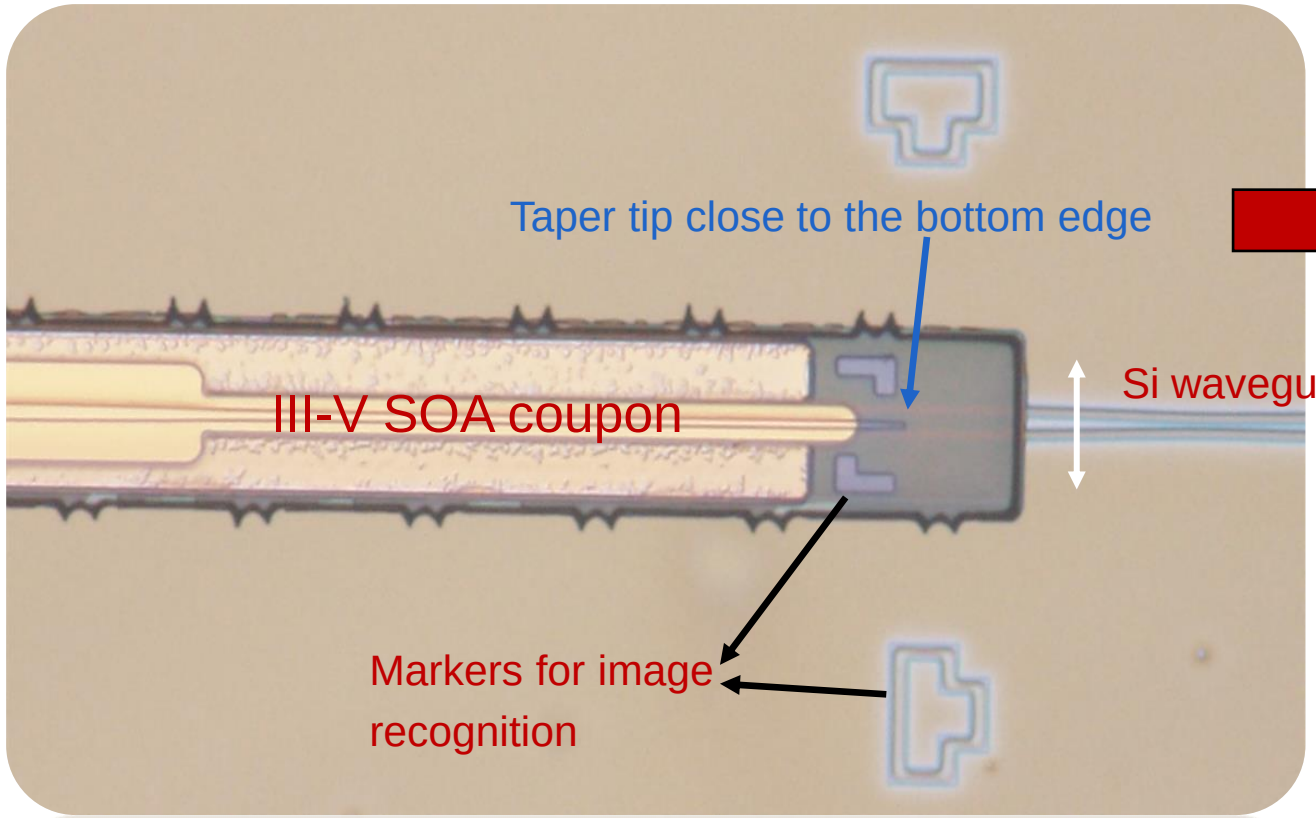
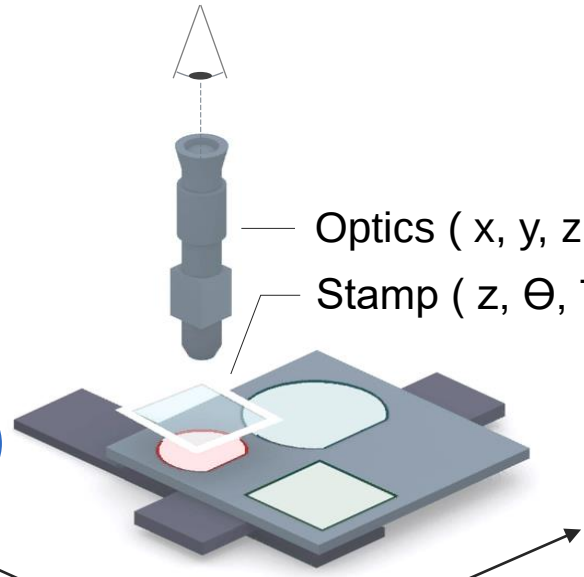
BANE OF TP PRE-PROCESSED SOAS



Challenge

Alignment-tolerant coupling taper



State of the art transfer printing tools provides an alignment accuracy of +/-1.5µm 3σ

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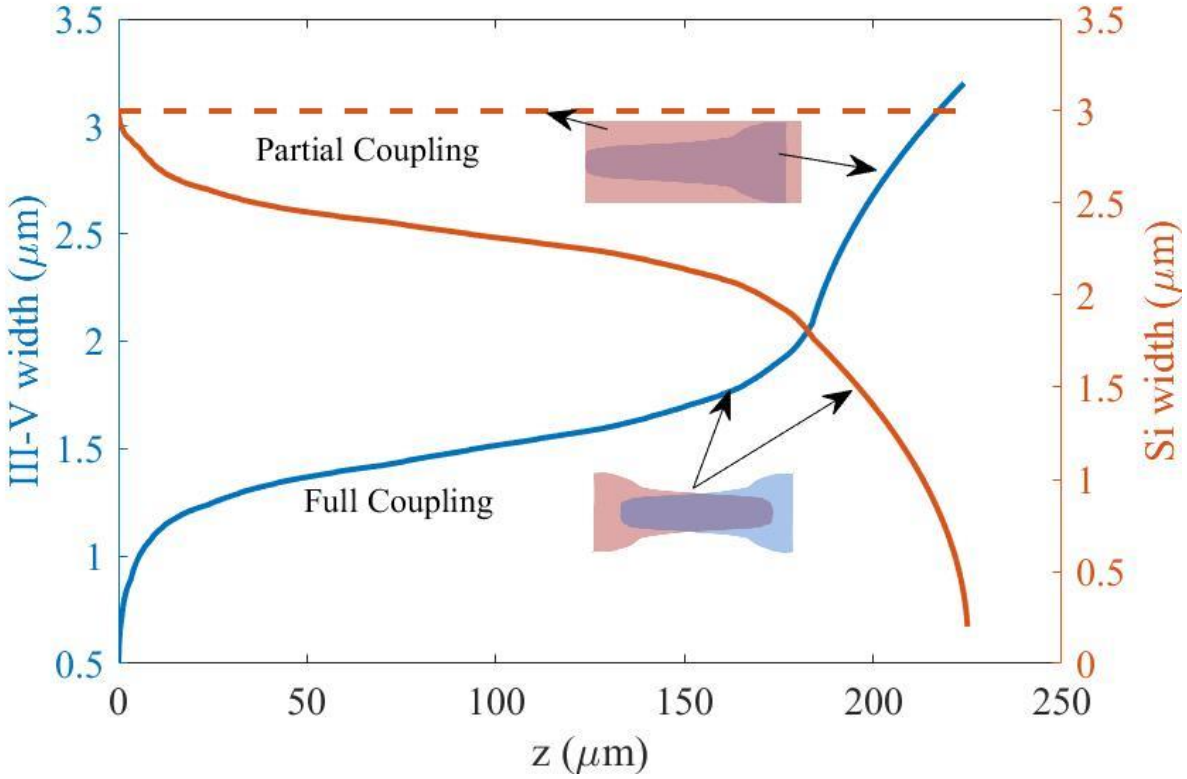
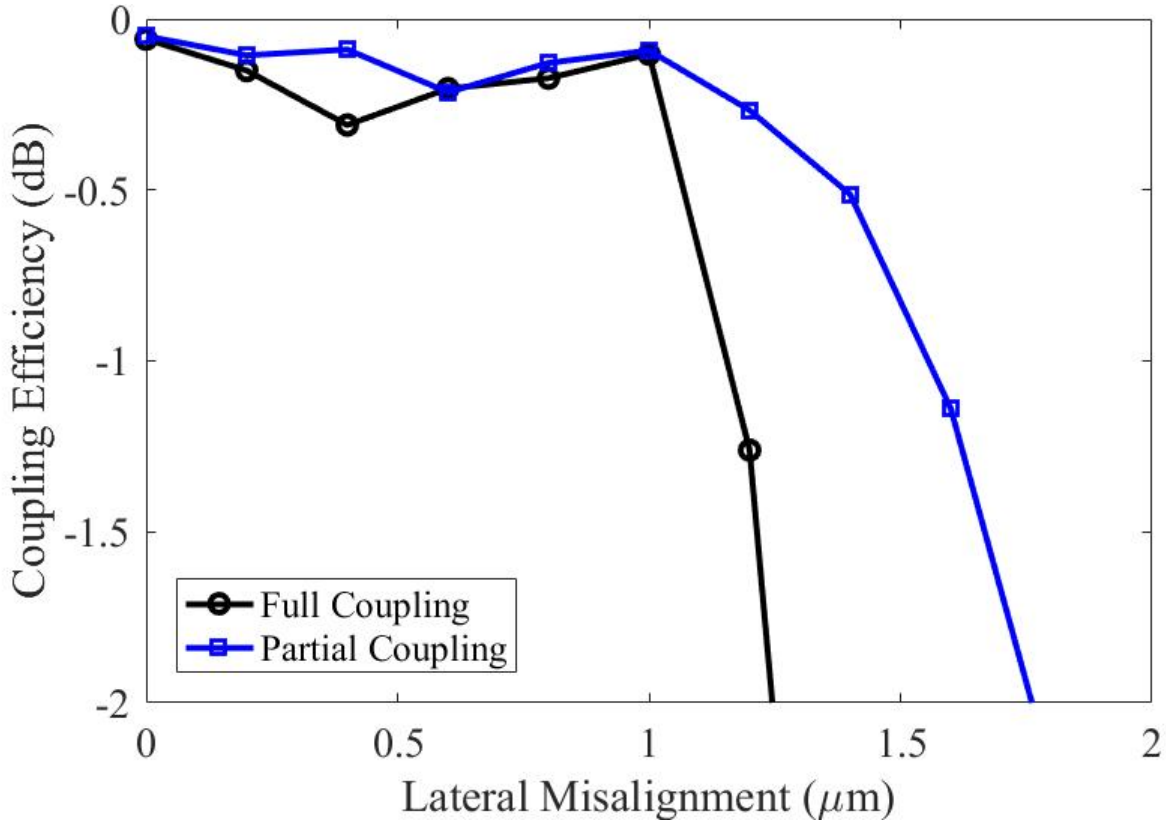
MICRO-TP COMPATIBLE ADIABATIC TAPER

Shape of the adiabatic taper



Calculated coupling efficiency with misalignment



Haq, Bahawal, and Günther Roelkens. "Alignment-tolerant taper design for transfer printed III-V-on-Si devices." *21st European Conference on Integratred Optics (ECIO 2019)*. 2019.

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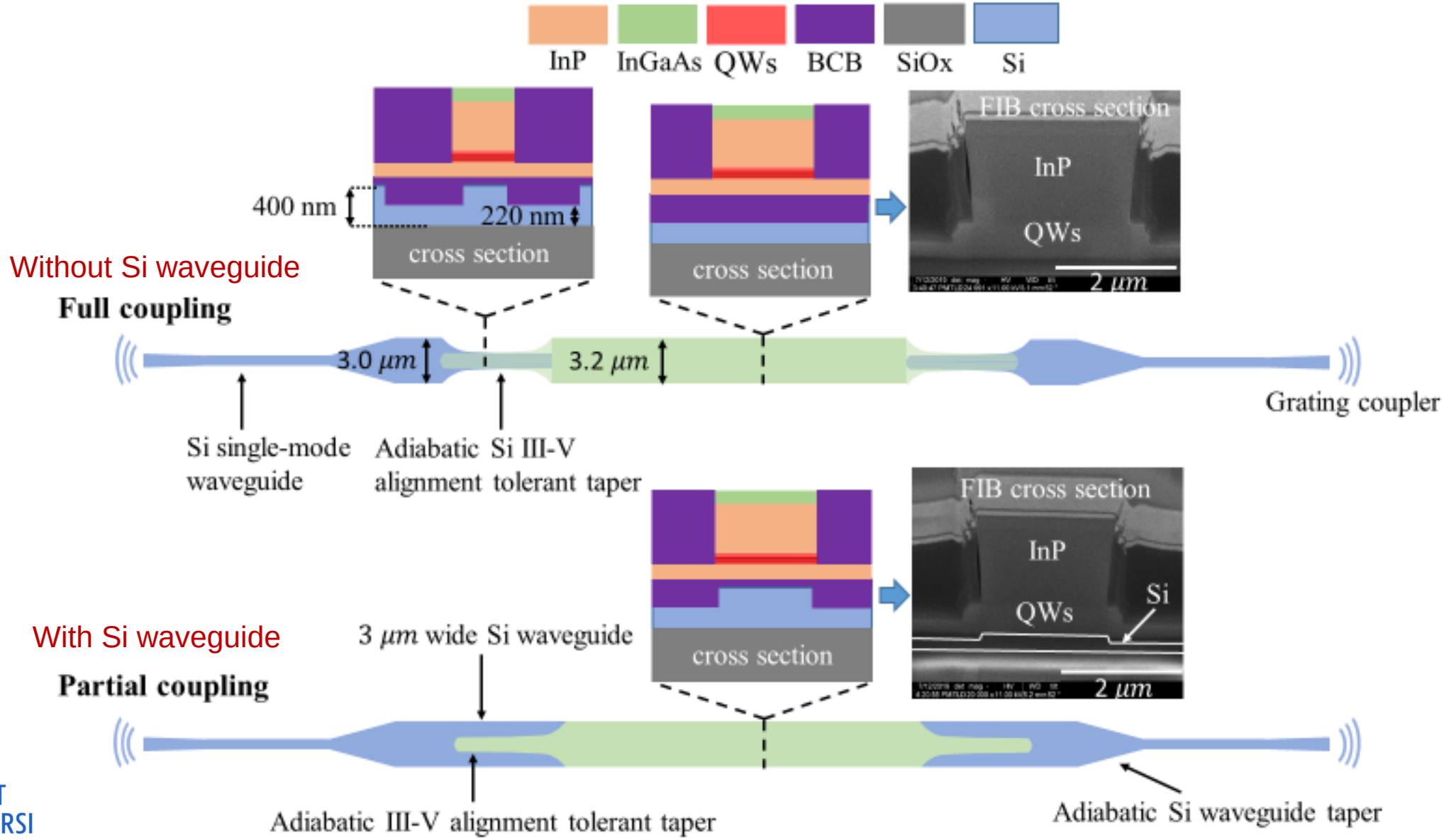
DESIGN OF III-V-ON-SILICON SOA



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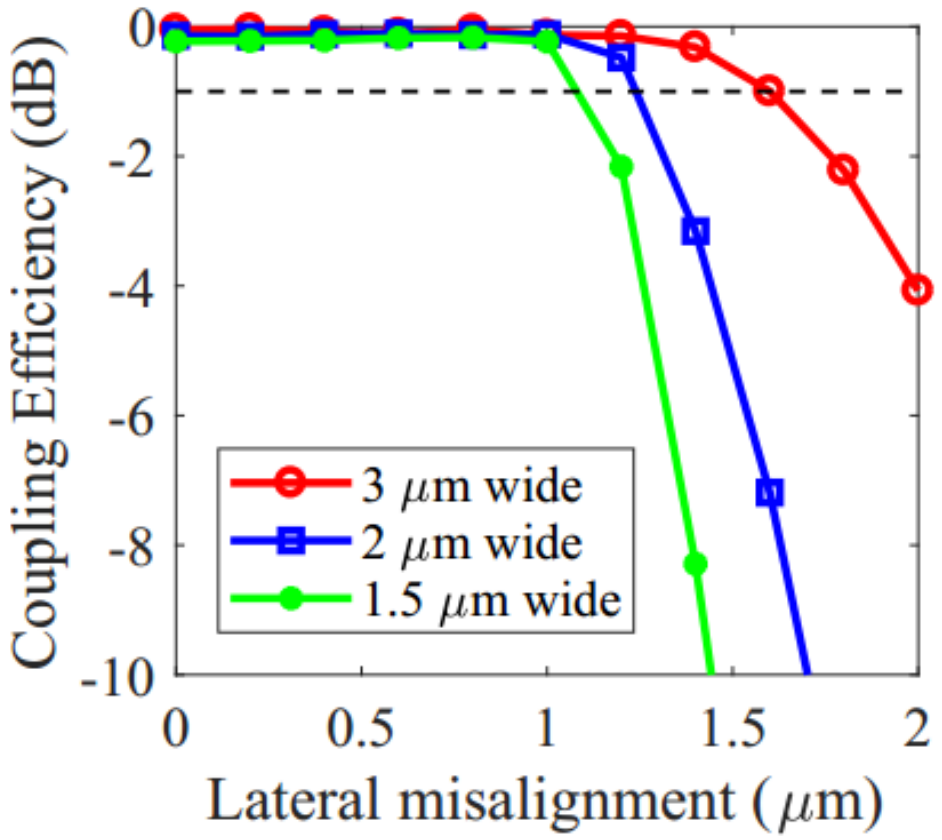
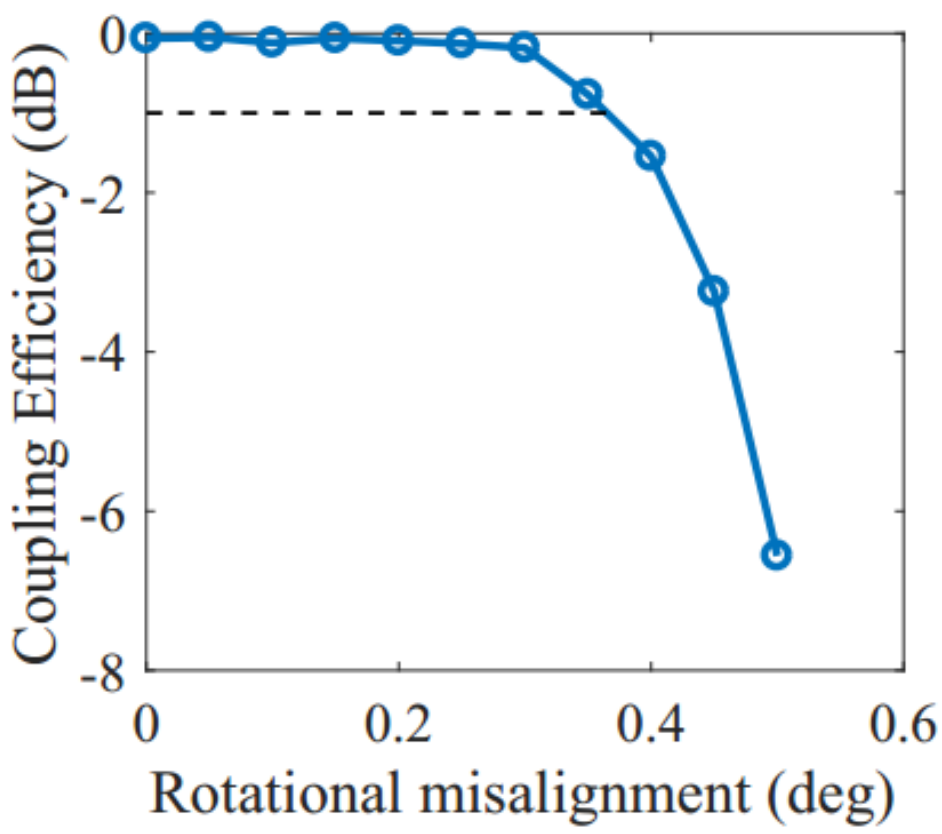
FULL COUPLING DESIGN WORKS IN BOTH CASES





Full coupling adiabatic taper design also shows high power coupling to Si waveguides of various widths.

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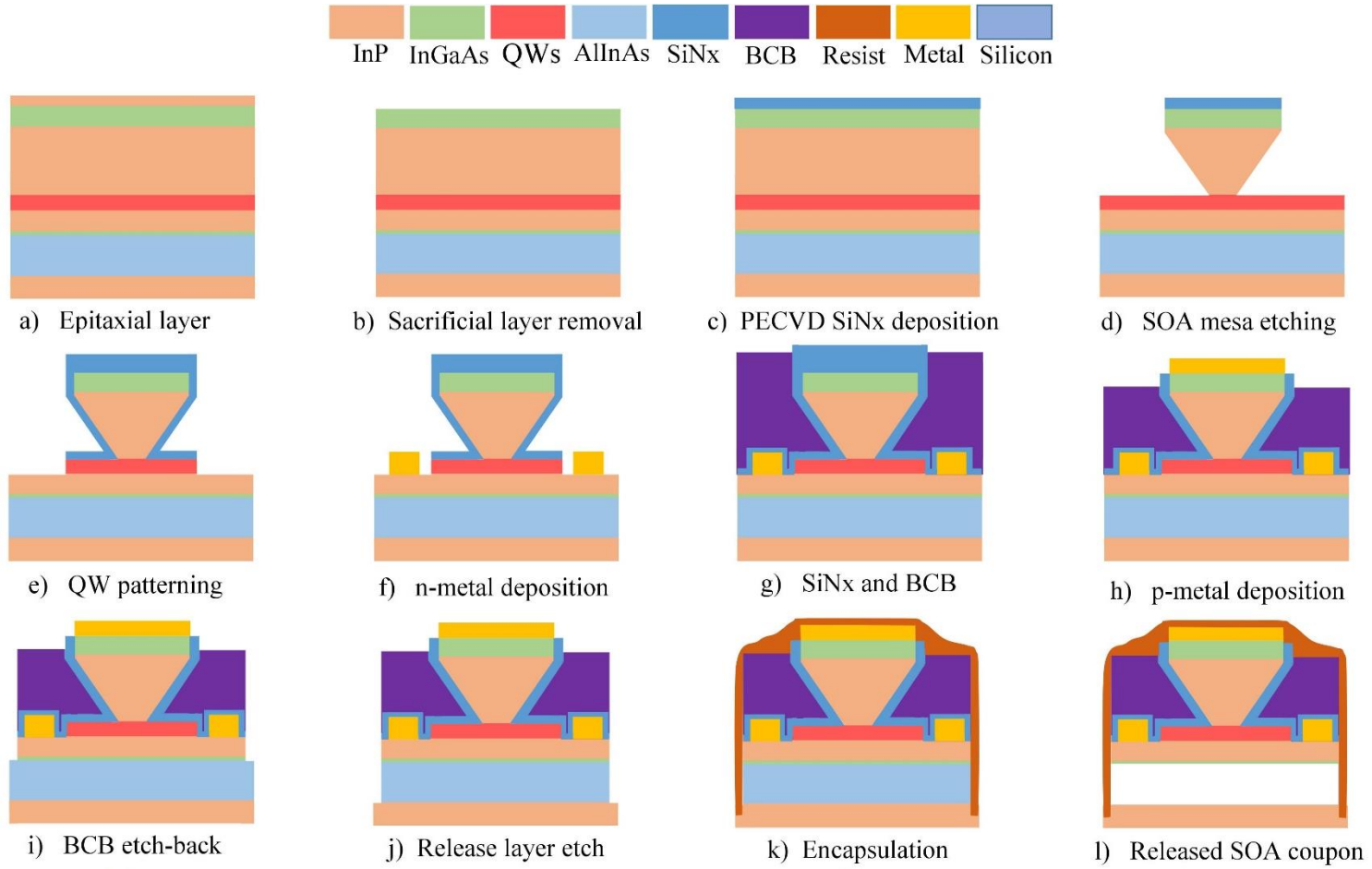
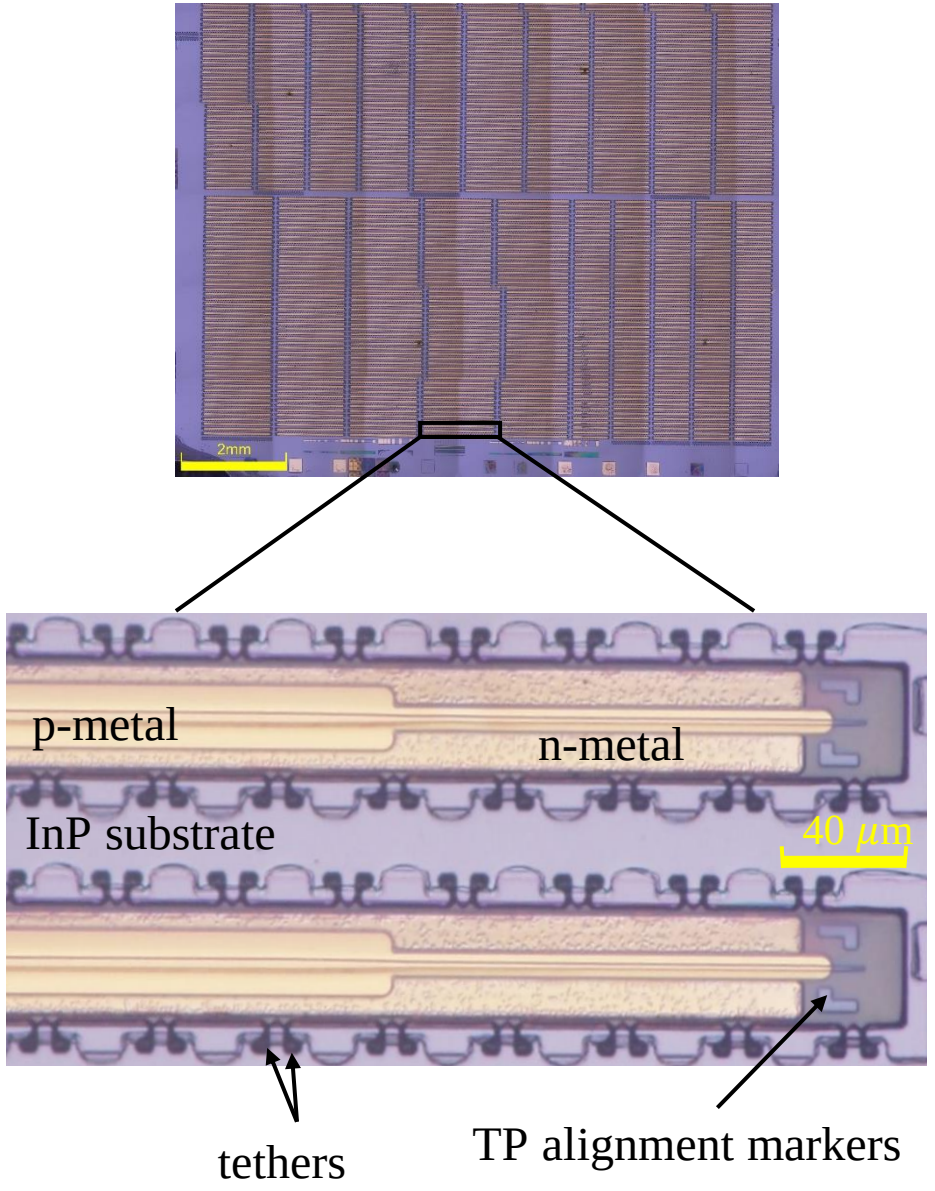
PROCESSING ON THE INP SOURCE



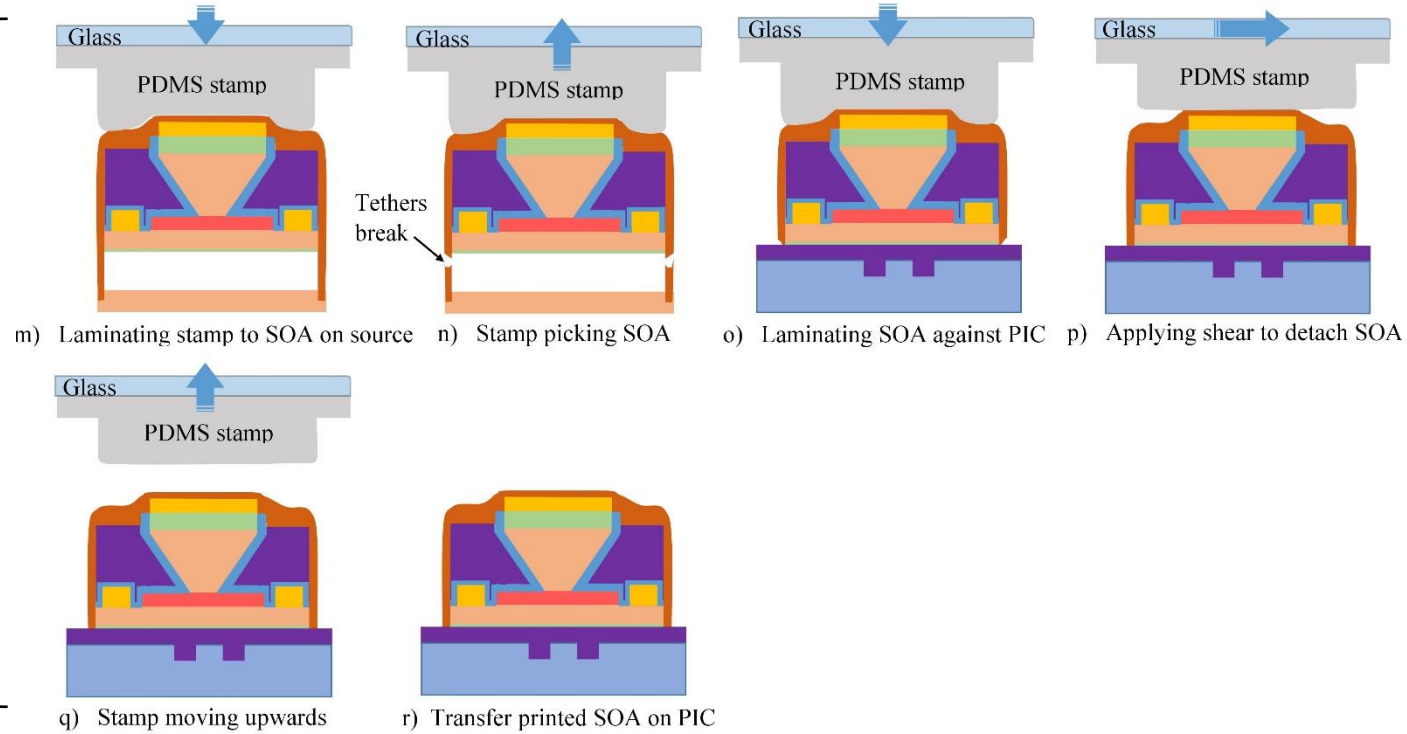
Standard i-line contact lithography

Processed in dense arrays

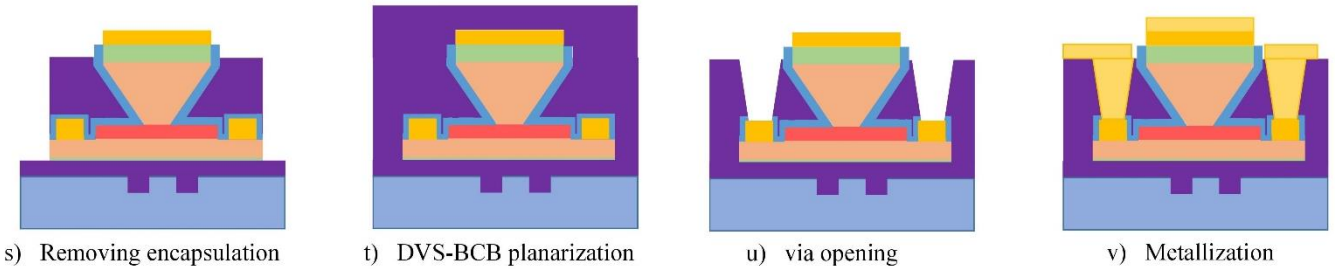


TRANSFER PRINTING AND POST PROCESSING

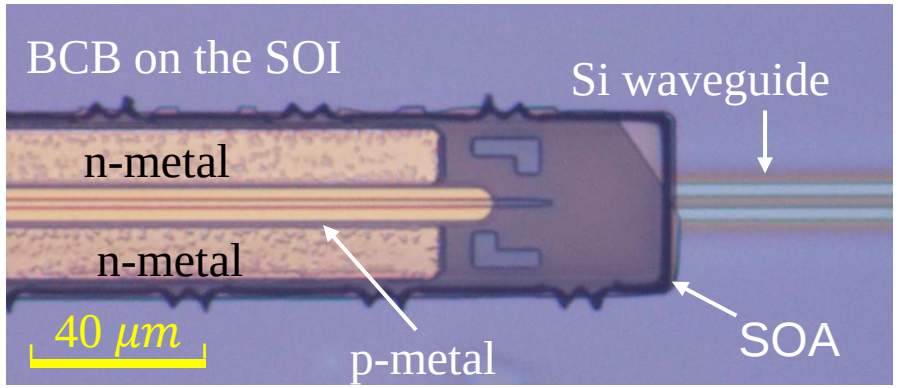
Transfer printing

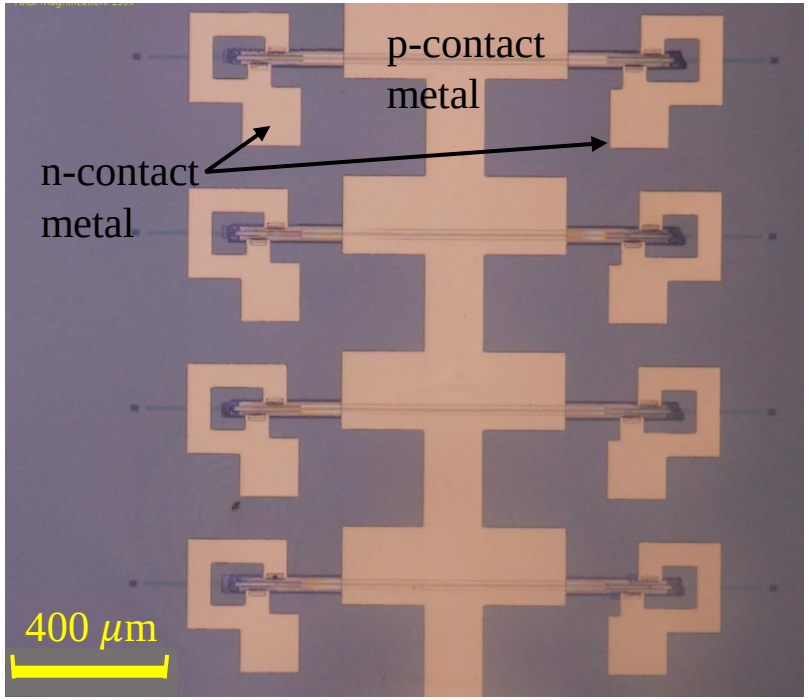


Post processing on the SOI



After printing on the SOI





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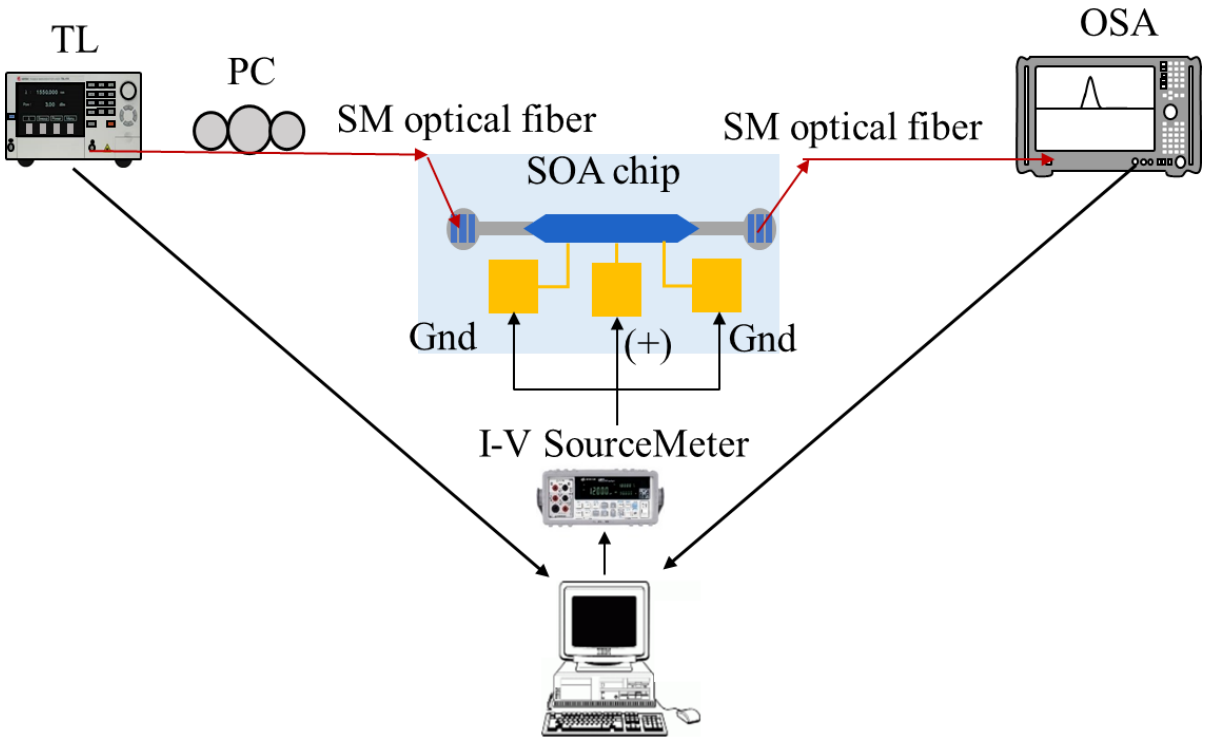
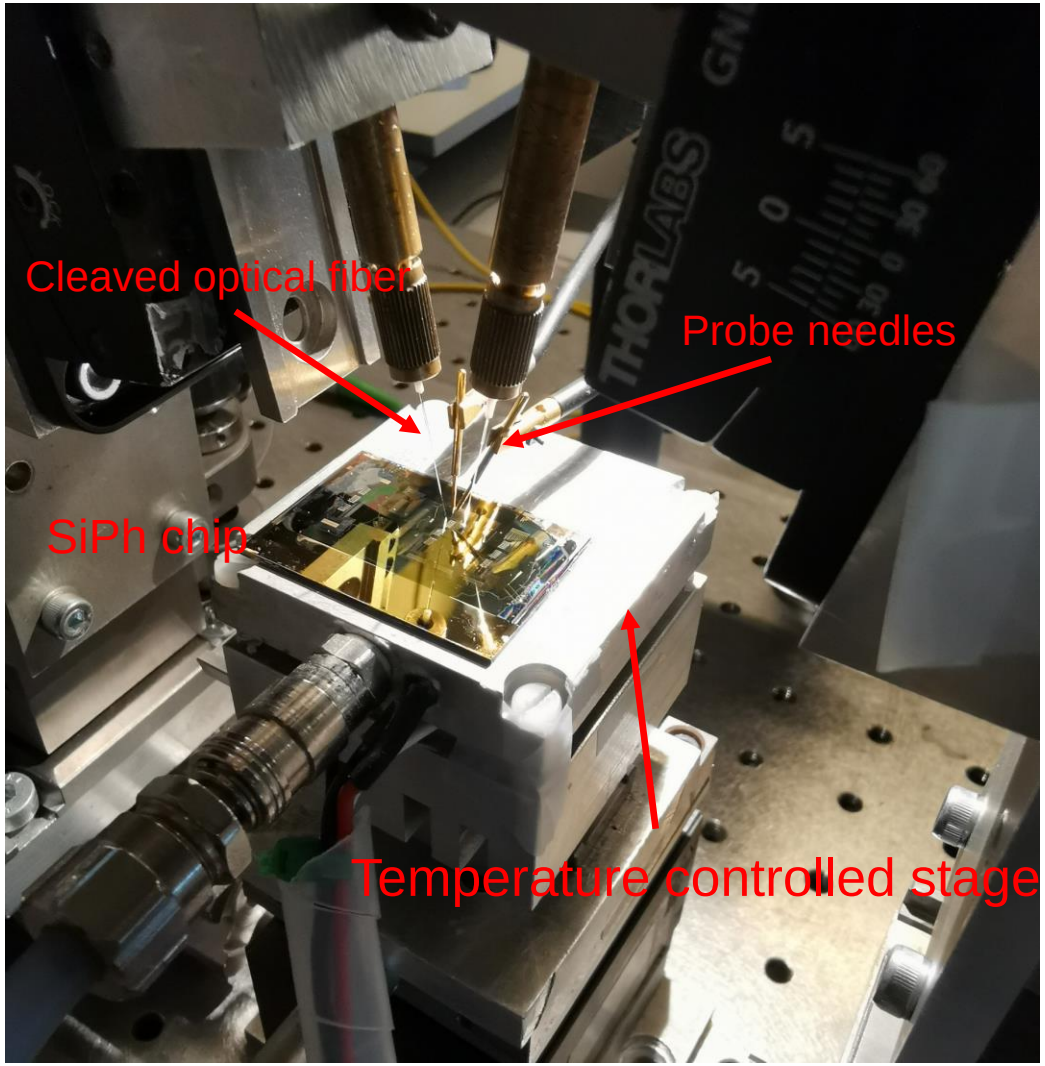
MEASUREMENT SETUP





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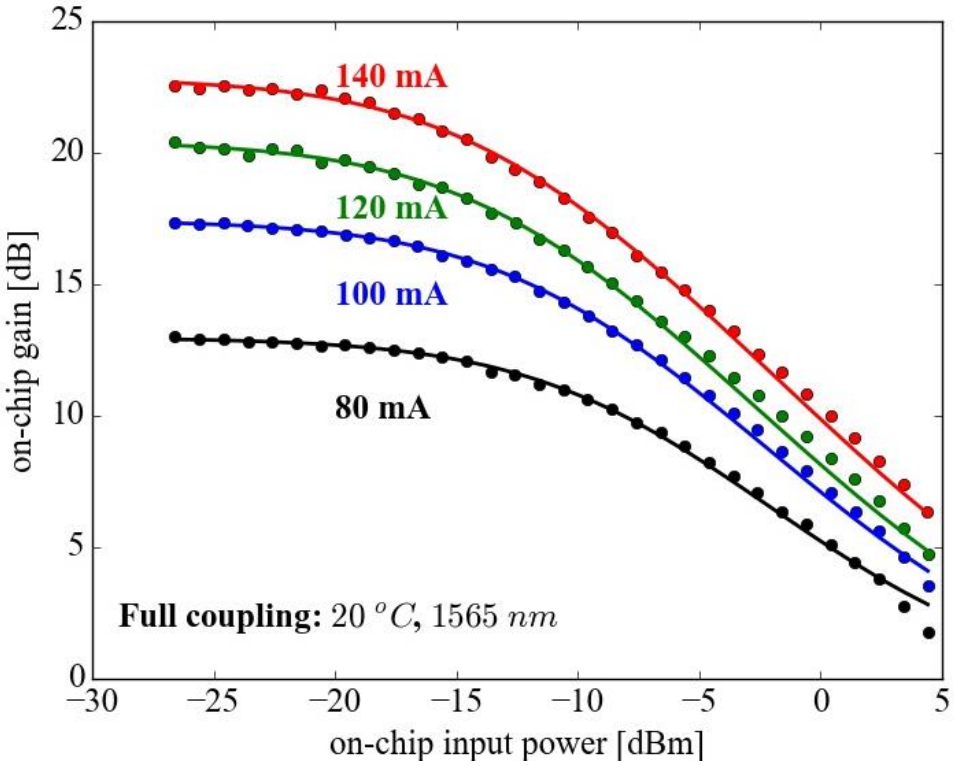
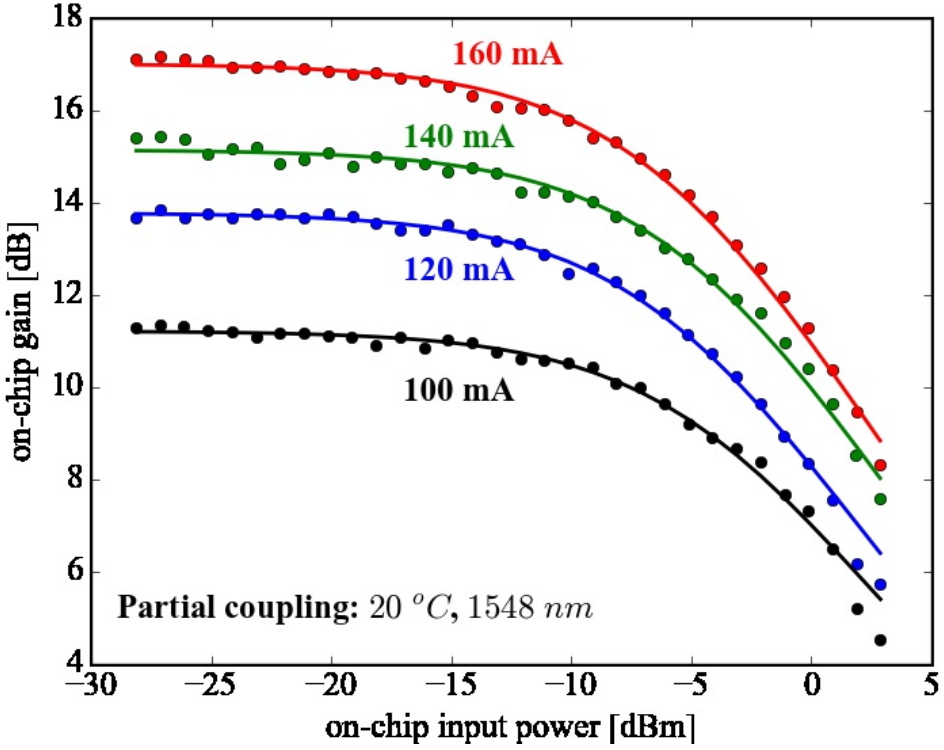
ON-CHIP GAIN AND POWER SATURATION

High confinement factor in the QWs



At 140 mA, the measured on-chip small signal gain is 23 dB and ouput power saturation is 9 mW.

Low confinement factor in the QWs



At 160 mA, the measured on-chip small signal gain is 17 dB and ouput power saturation is 17mW.

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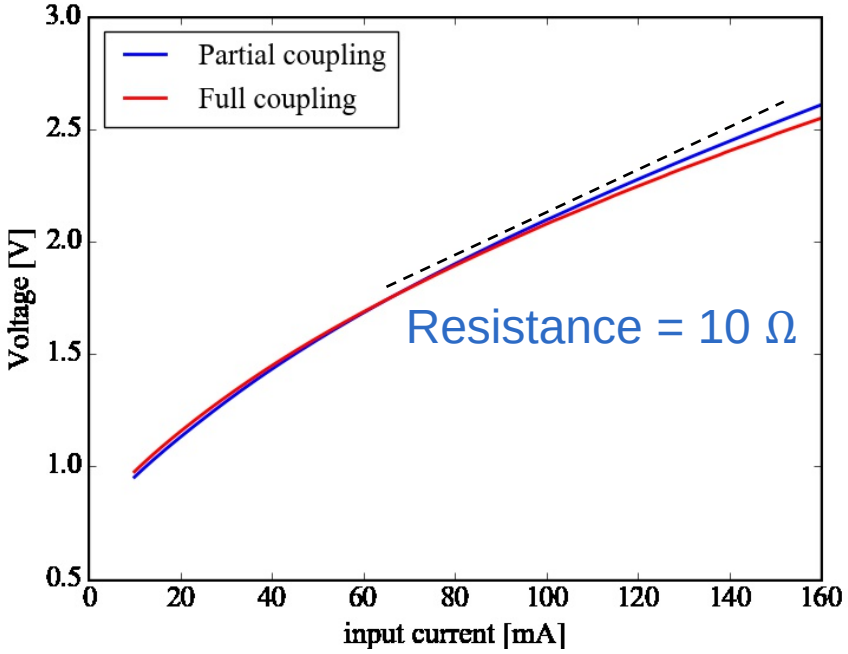
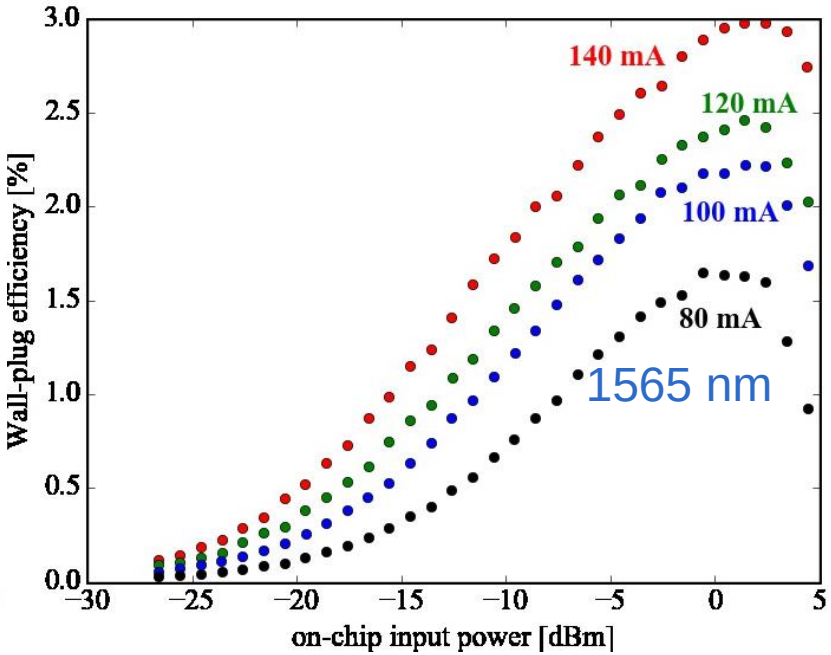
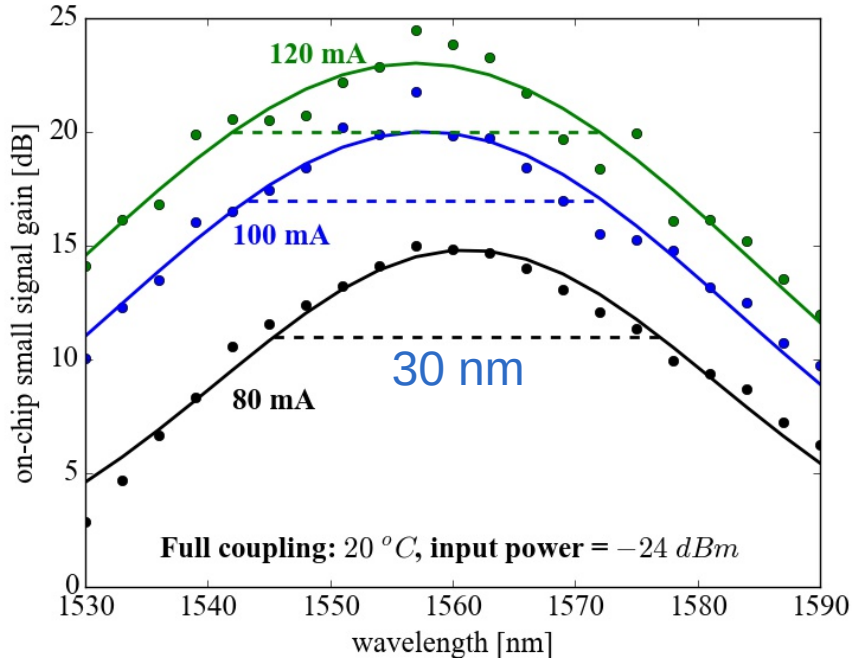
BANDWIDTH AND WALL-PLUG EFFICIENCY







Both the amplifiers have similar 3-dB bandwidth, maximum Wall-plug efficiency and resistance.

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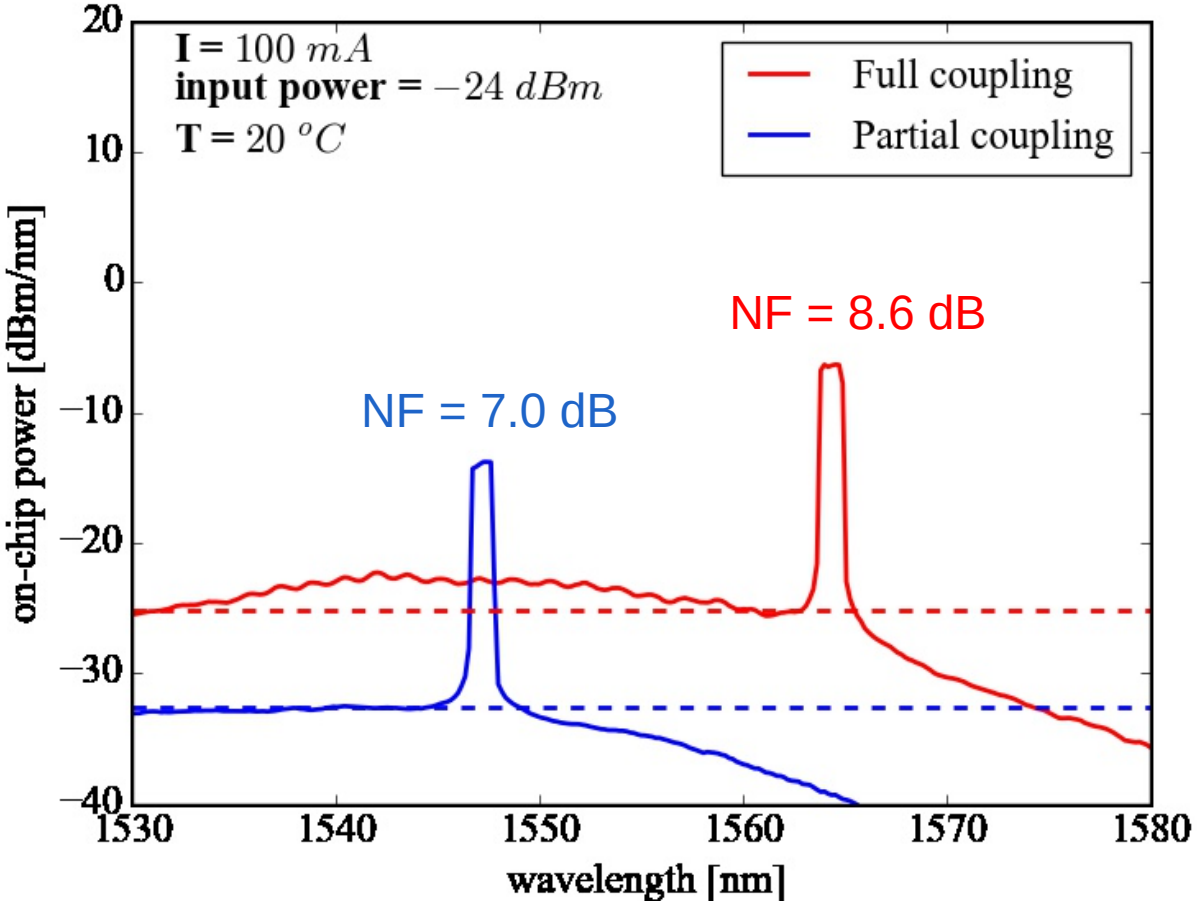
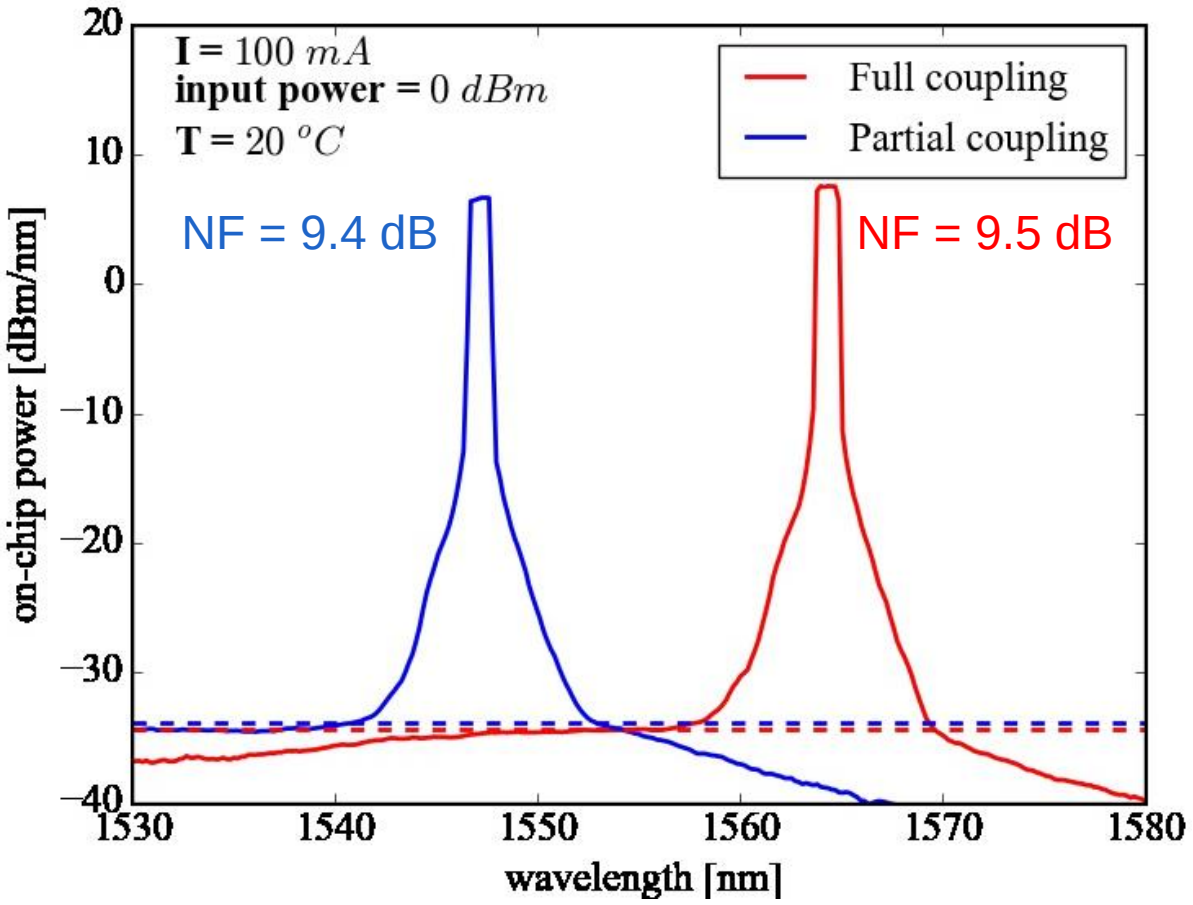
NOISE FIGURE





At high on-chip input powers (0 dBm) both the amplifiers have similar NF values.
At low on-chip input powers (-24 dBm) the partial coupling amplifier has lower NF values.

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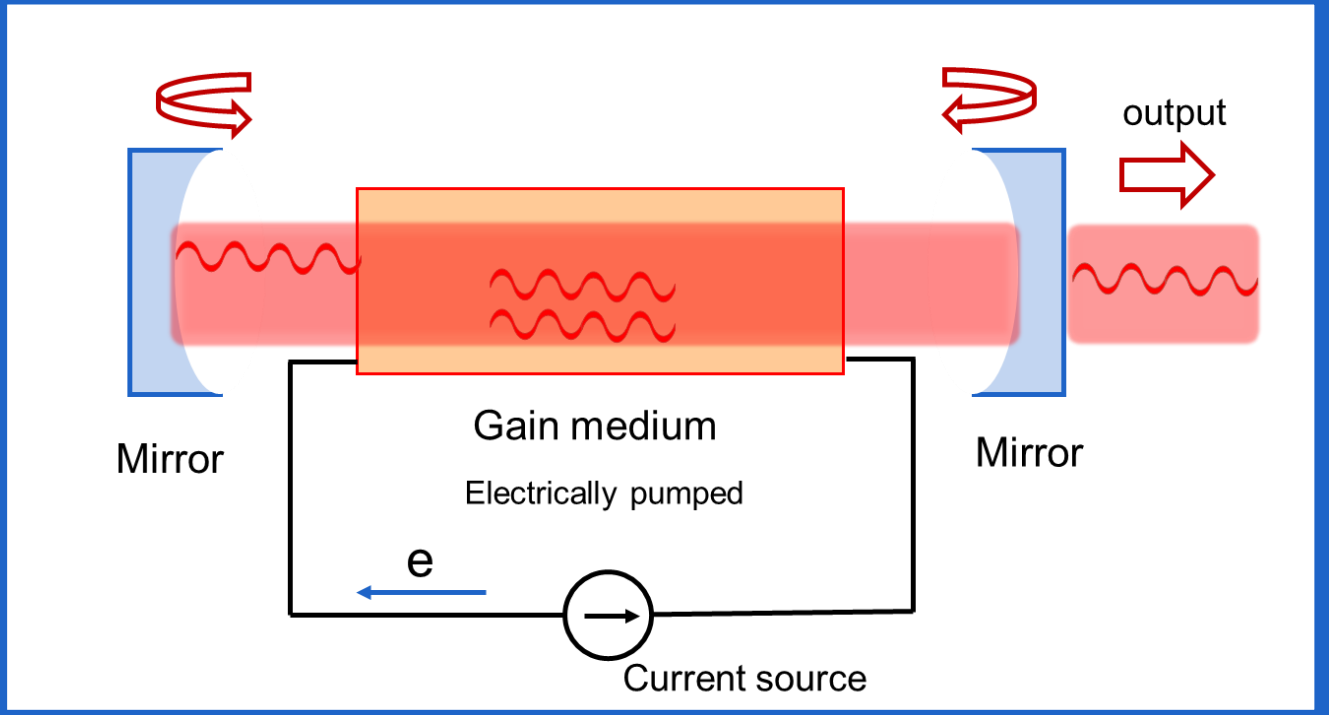

μTRANSFER-PRINTED DFB LASER

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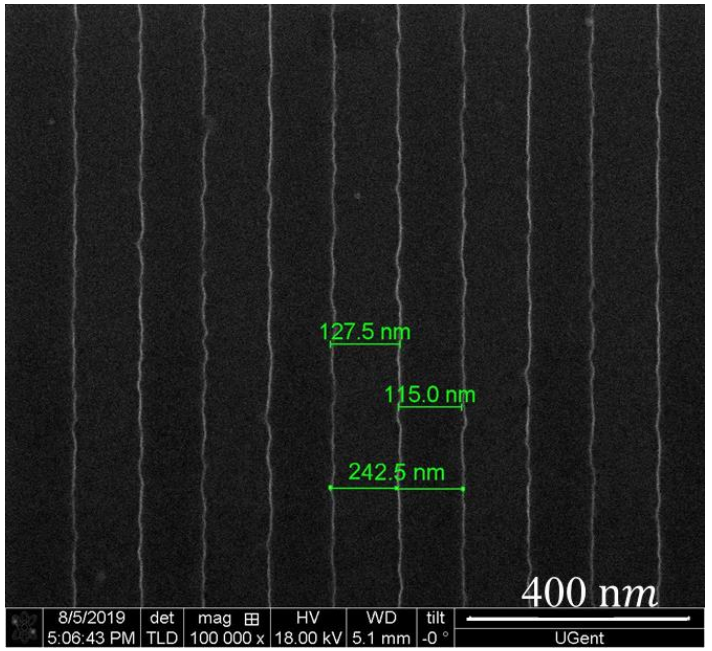
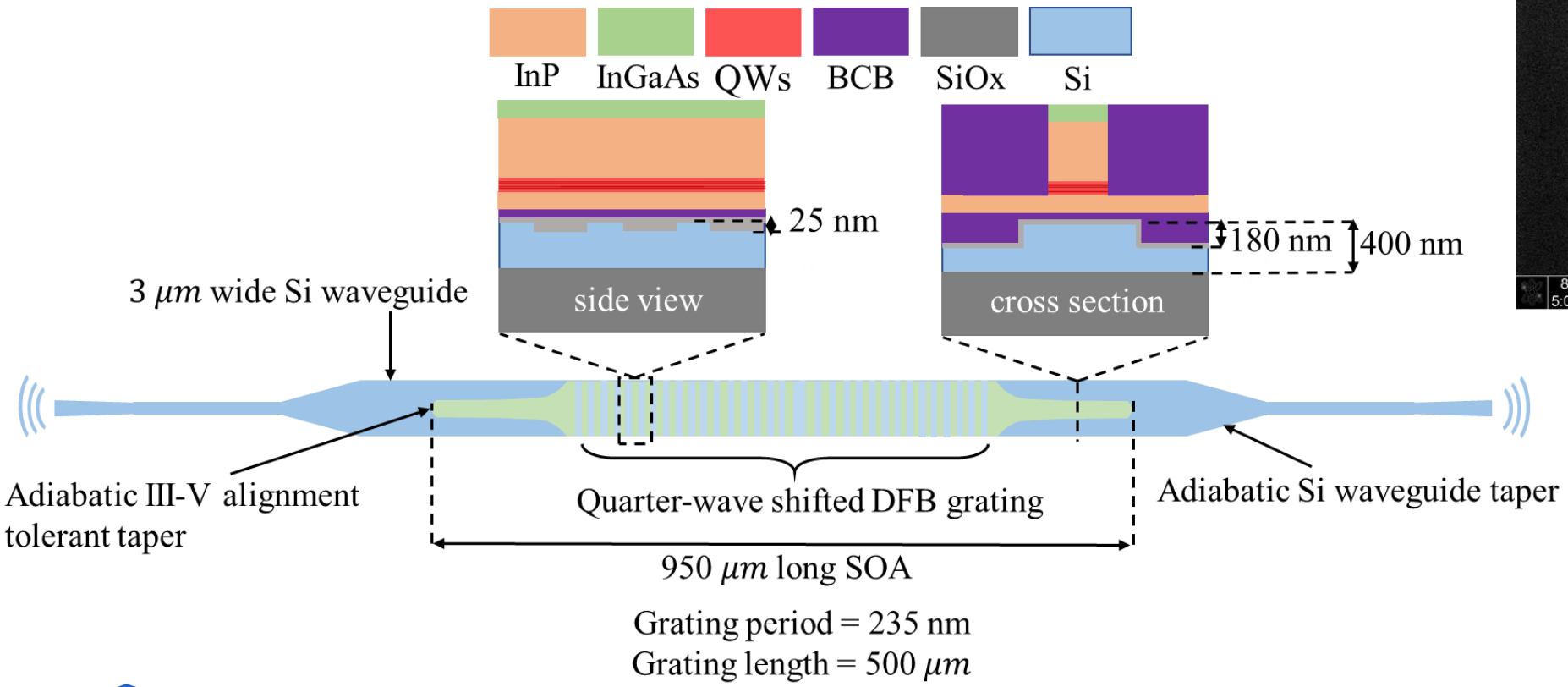
DESIGN OF III-V-ON-SILICON DFB



SEM image of DFB grating



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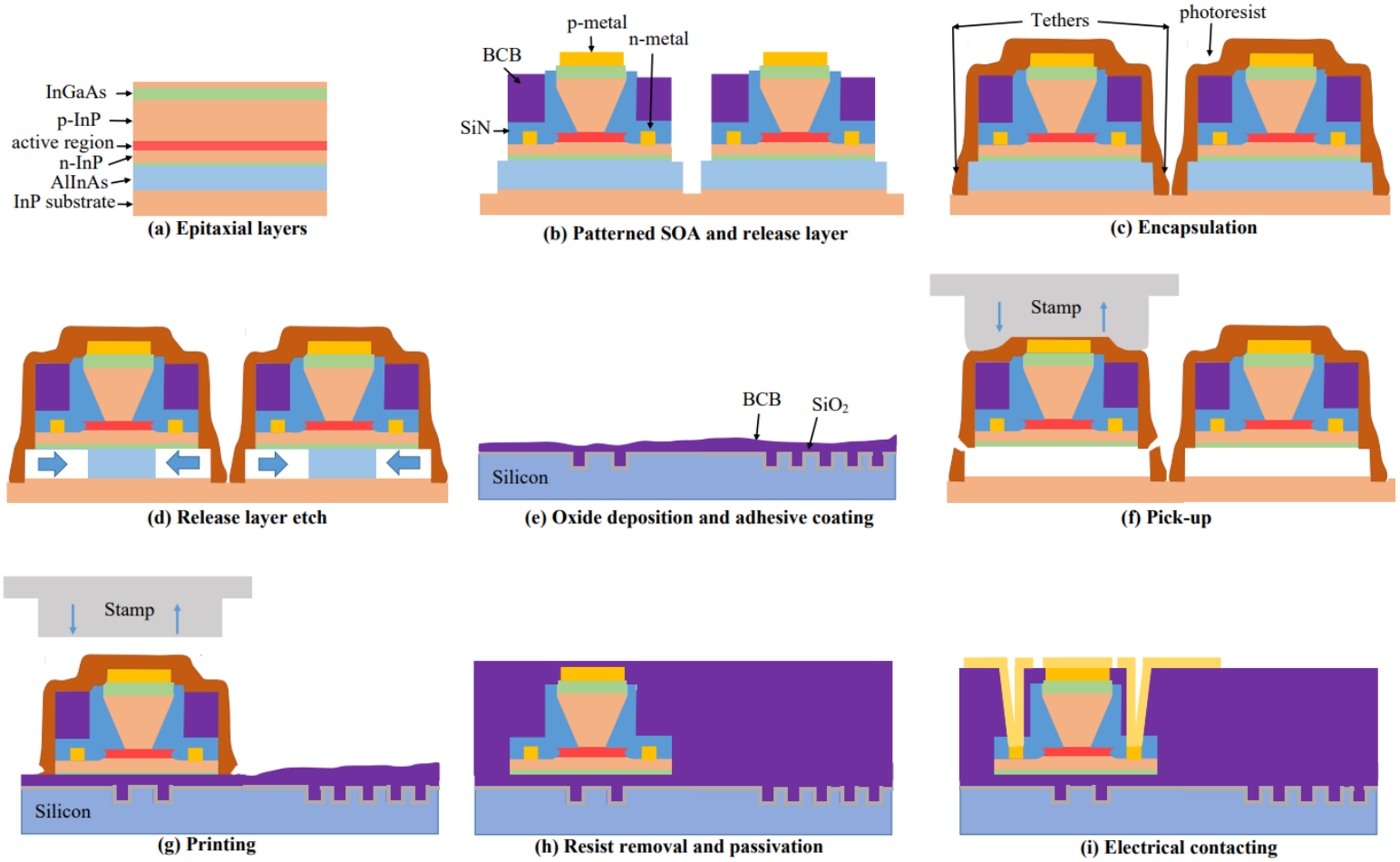
FABRICATION PROCESS FLOW



Similar as in the case of SOA demonstration

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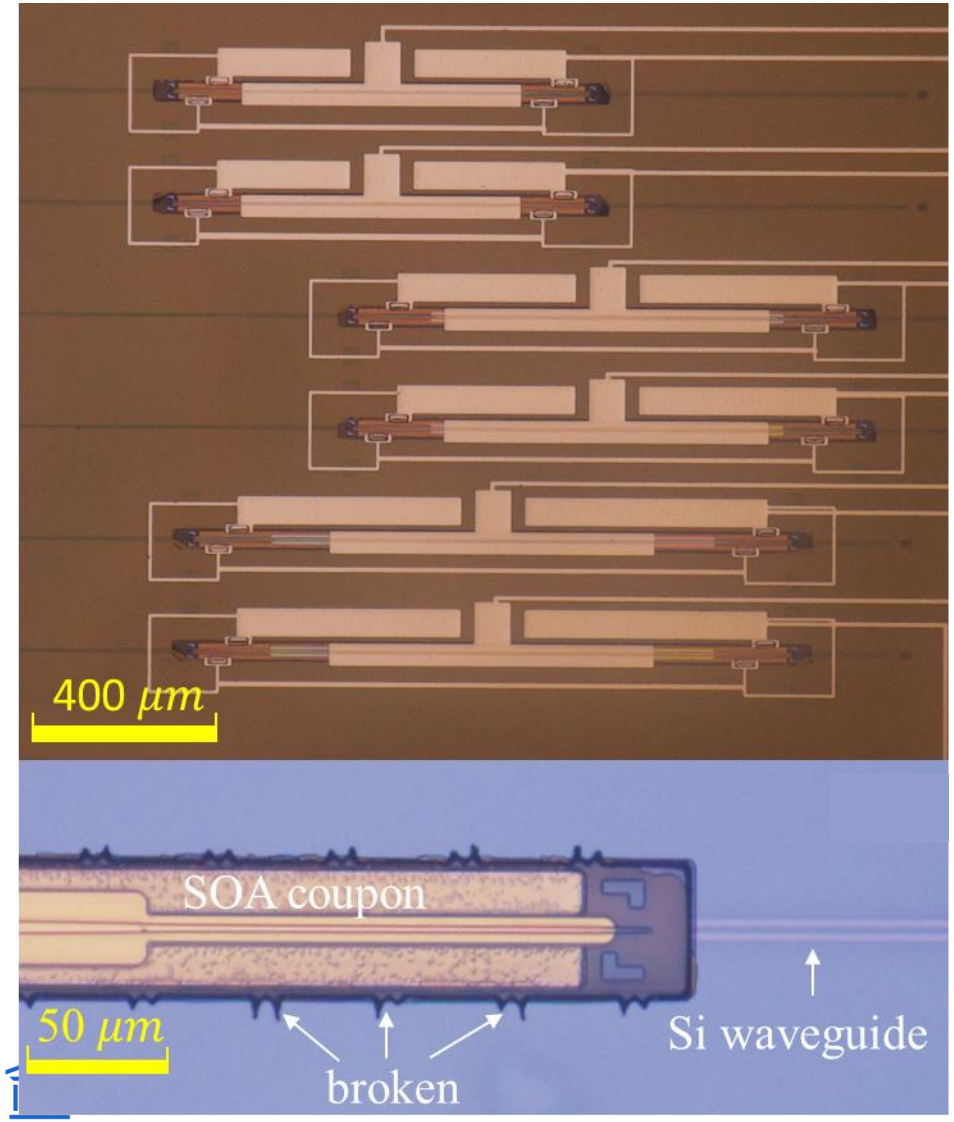
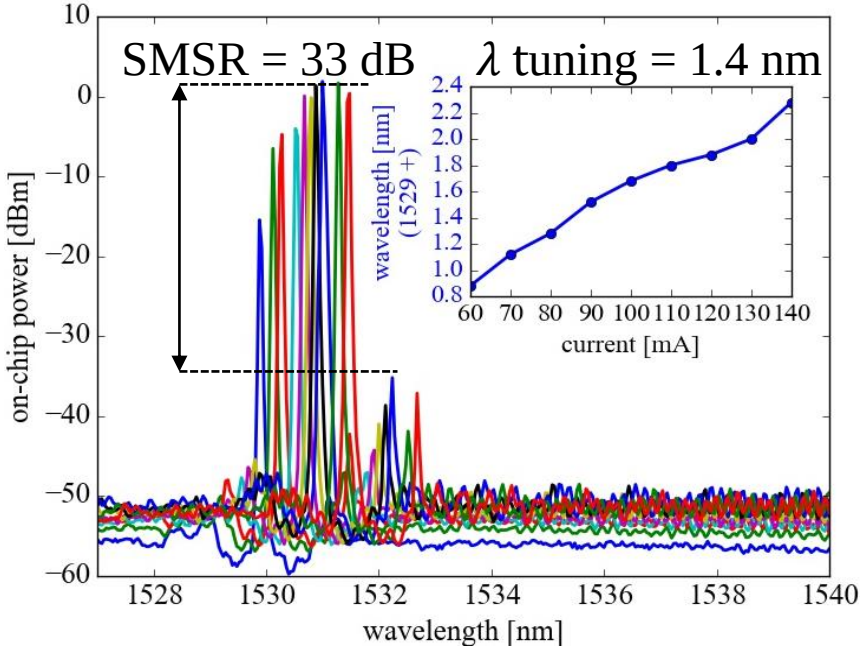
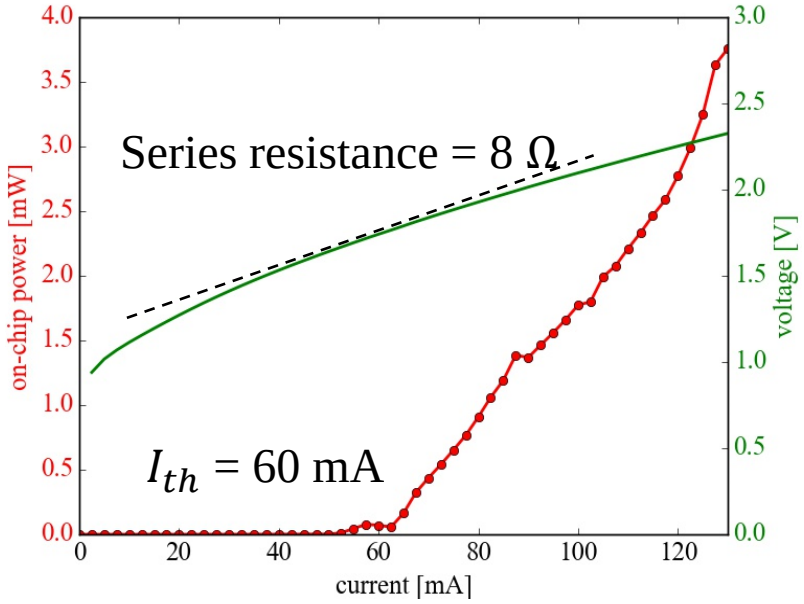
SINGLE MODE DFB LASER (GEN 1)





Single-sided output power = 3.75 mW



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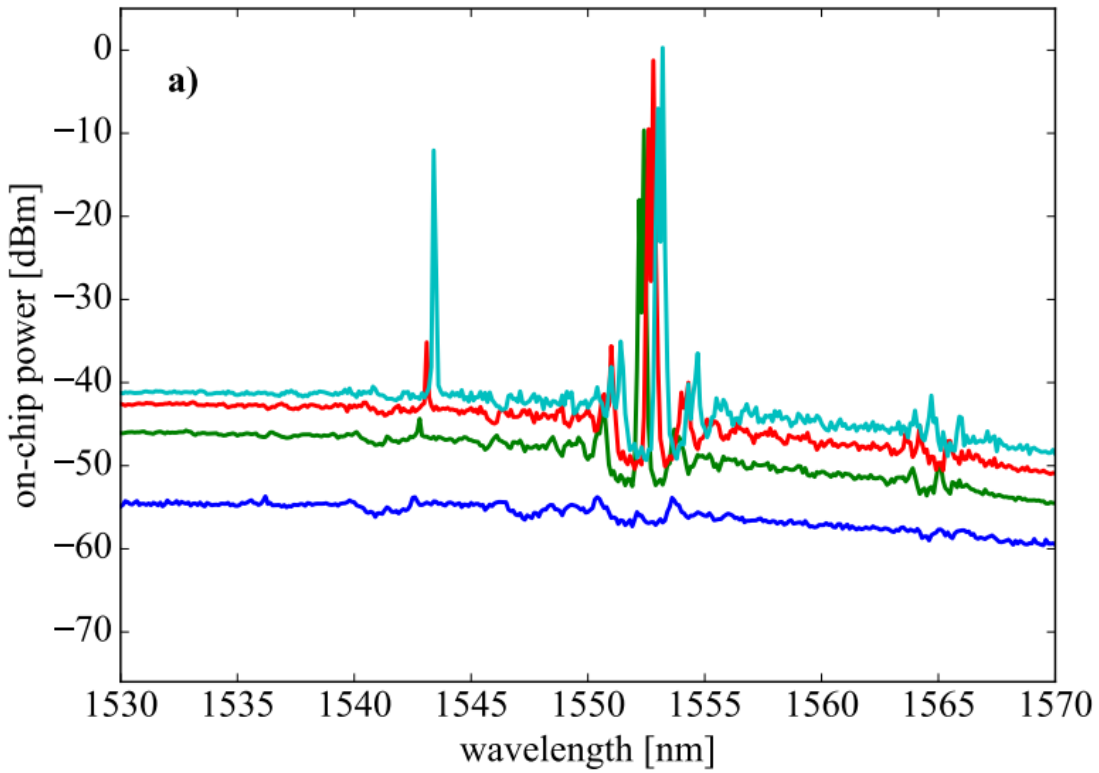
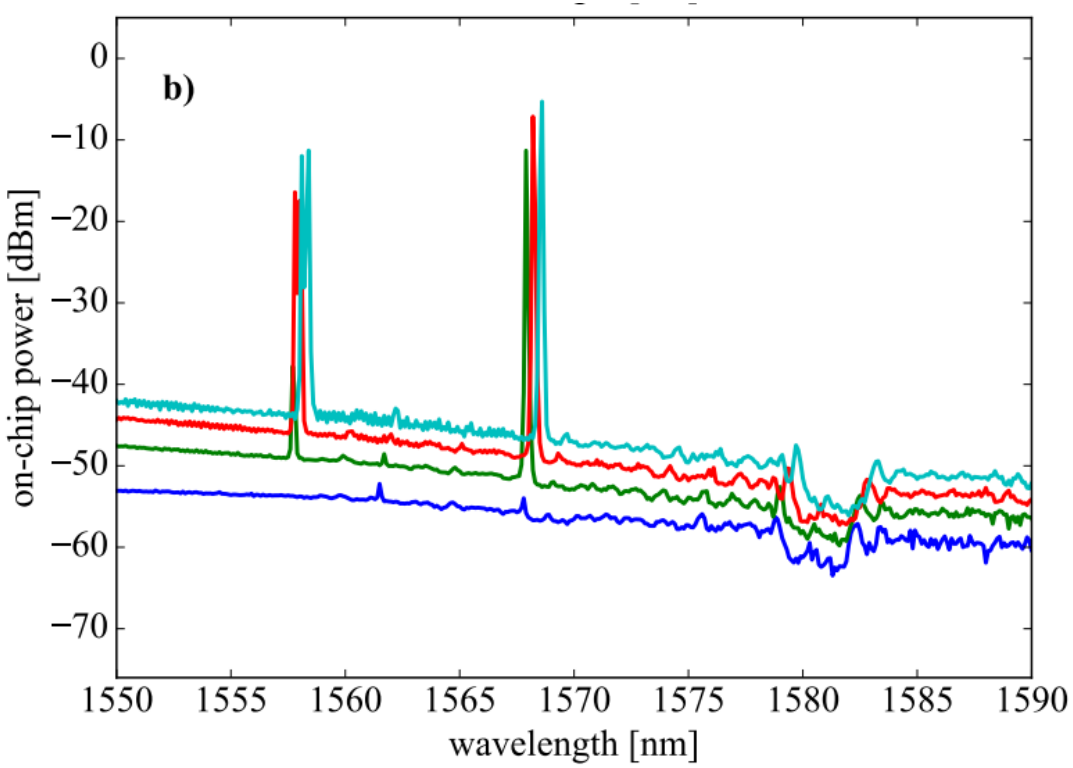
ISSUES WITH GEN 1 DFBS

We want a single laser line in the spectrum at a particular bias current.





Multiple peaks in the spectrum corresponds to higher order transversal modes of the III-V and Si waveguide

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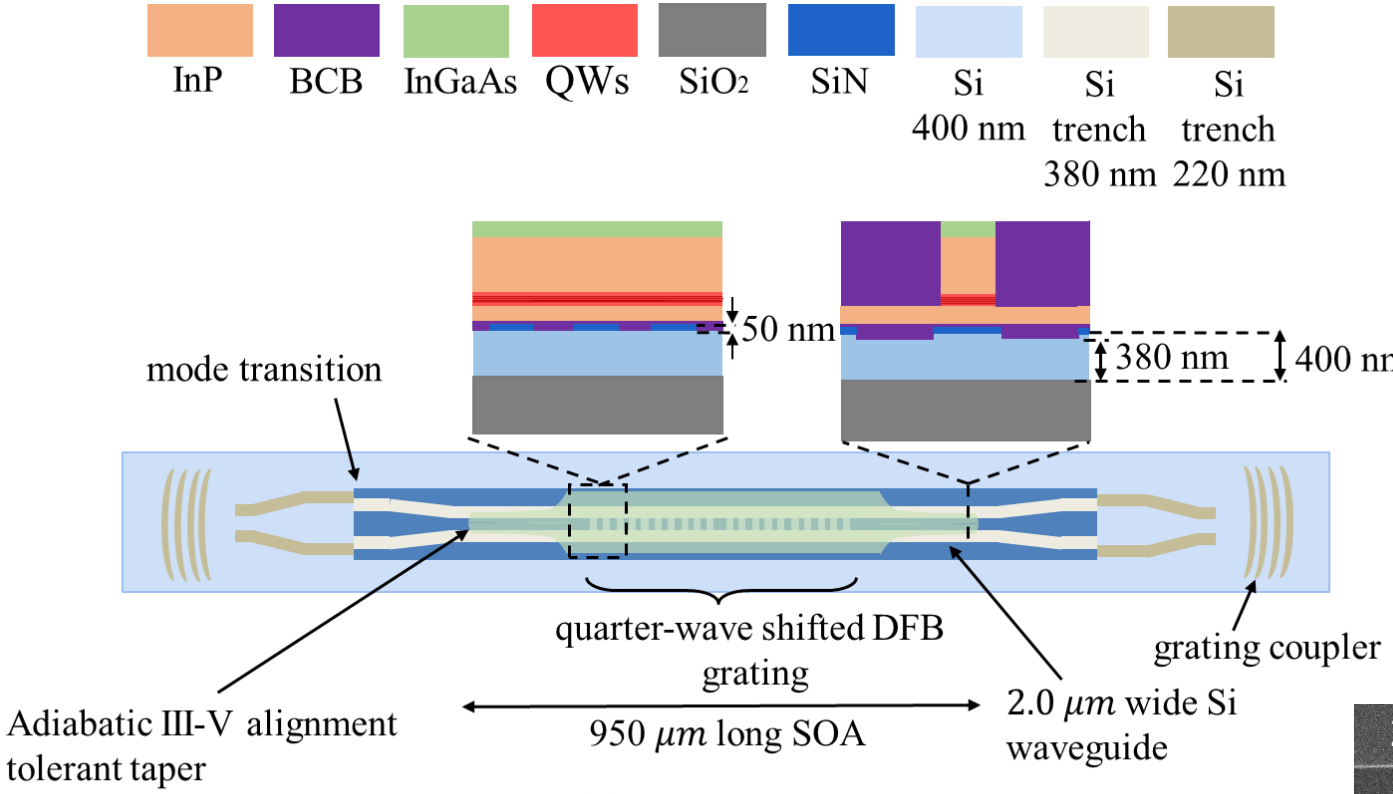
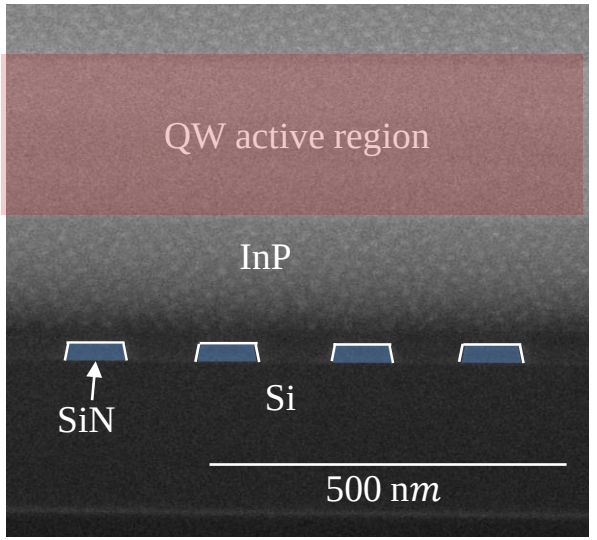
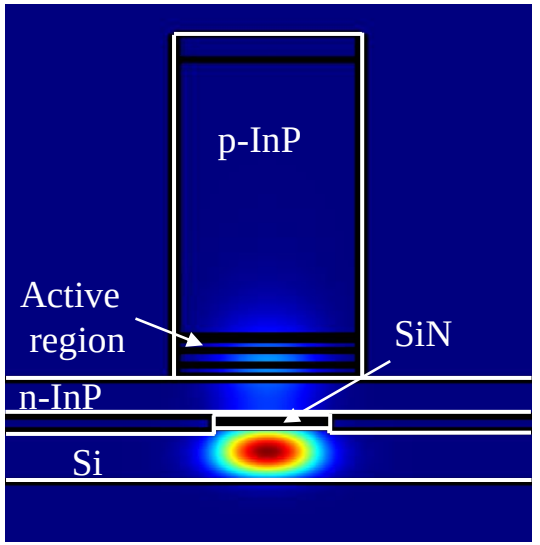
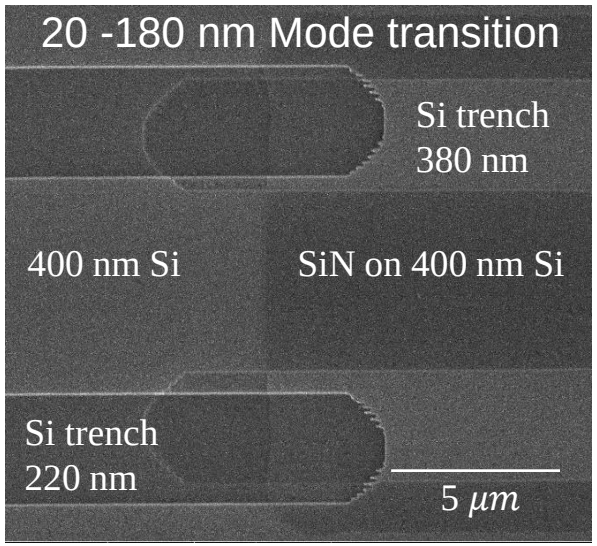
GEN 2 DFB DESIGN









Modifications in Gen 2 design

- The etch-depth of the Si waveguide reduced to 20 nm.
- To reduce the κ grating are defined on 50 nm thick SiN layer deposited on Si.

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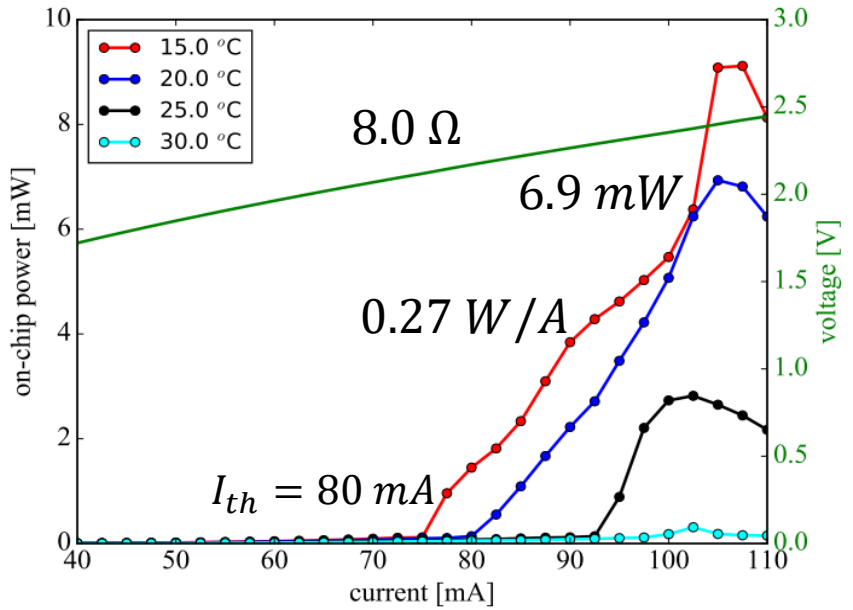
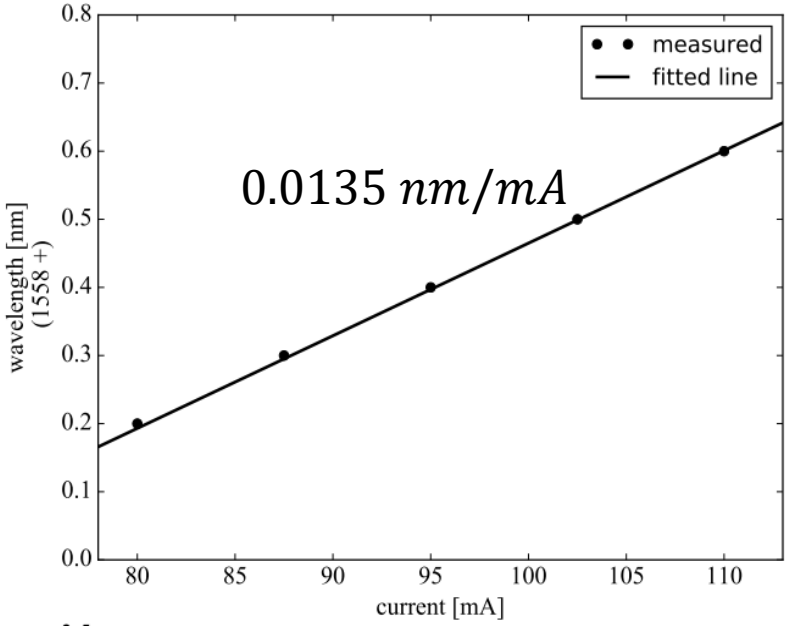
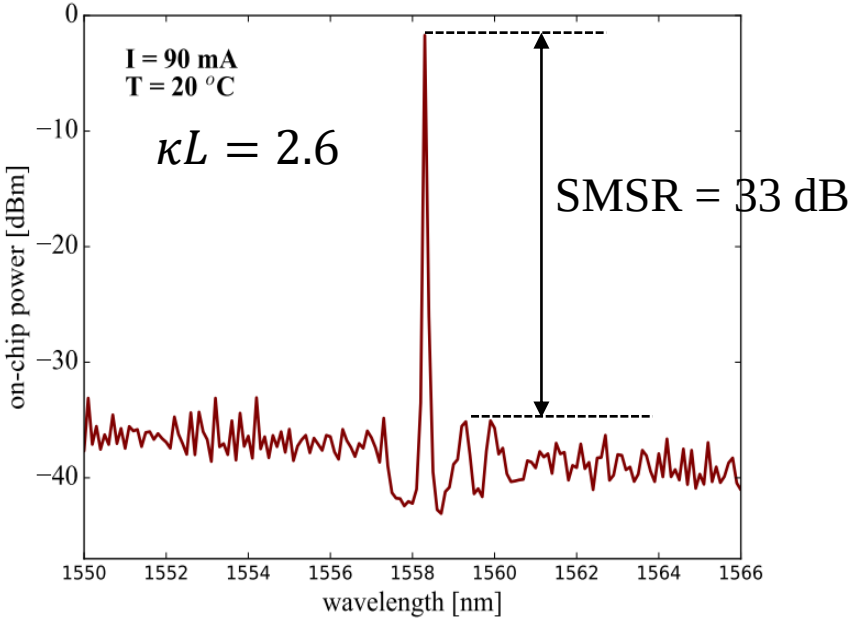
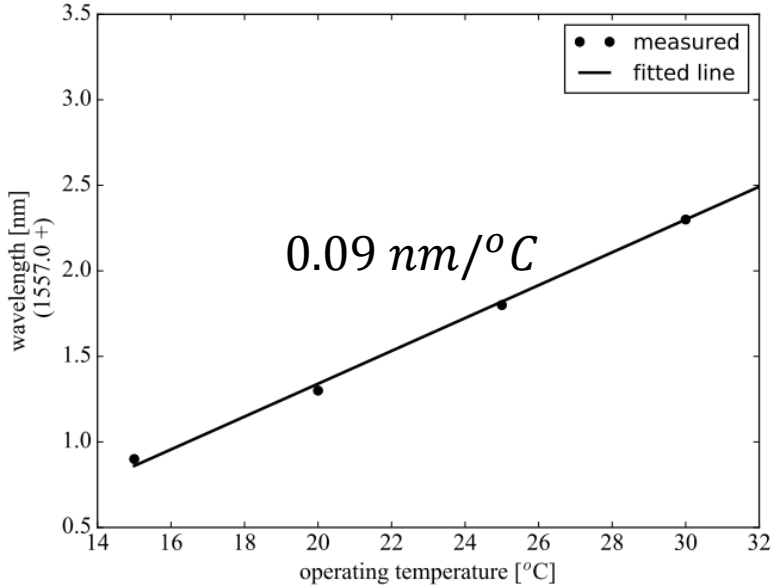
MEASUREMENTS









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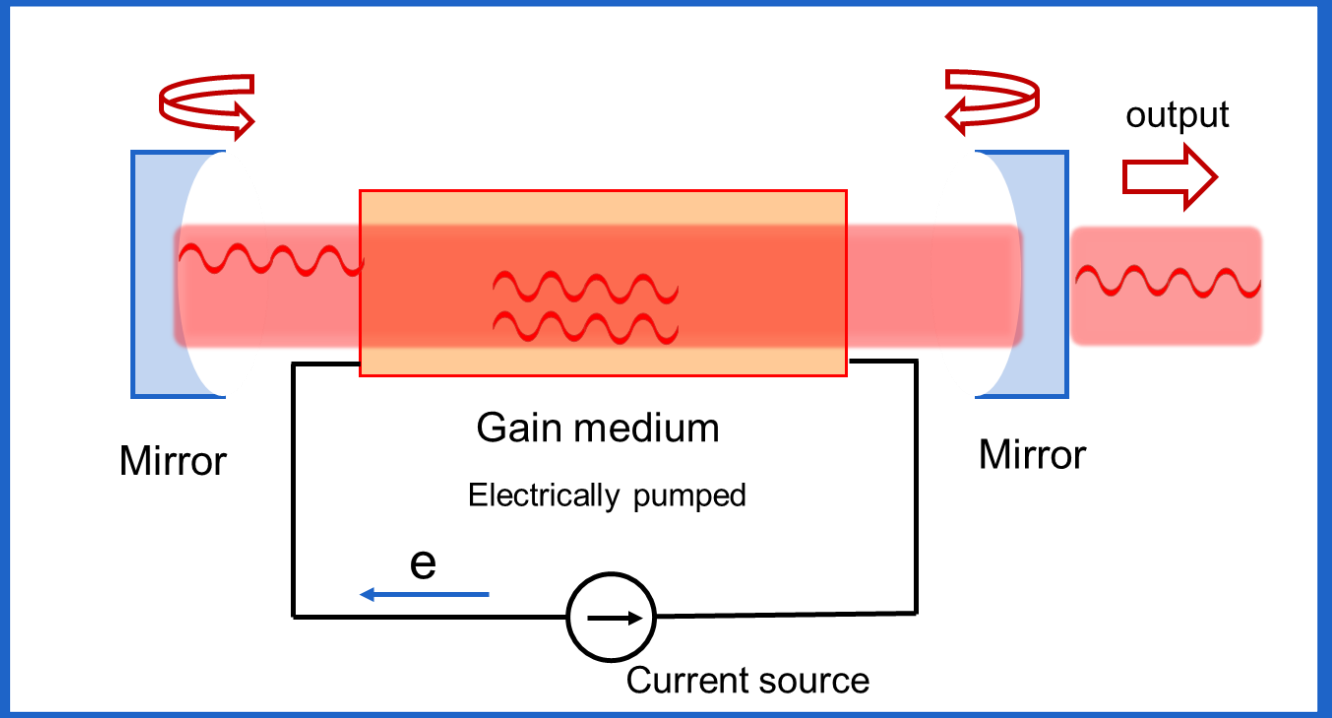

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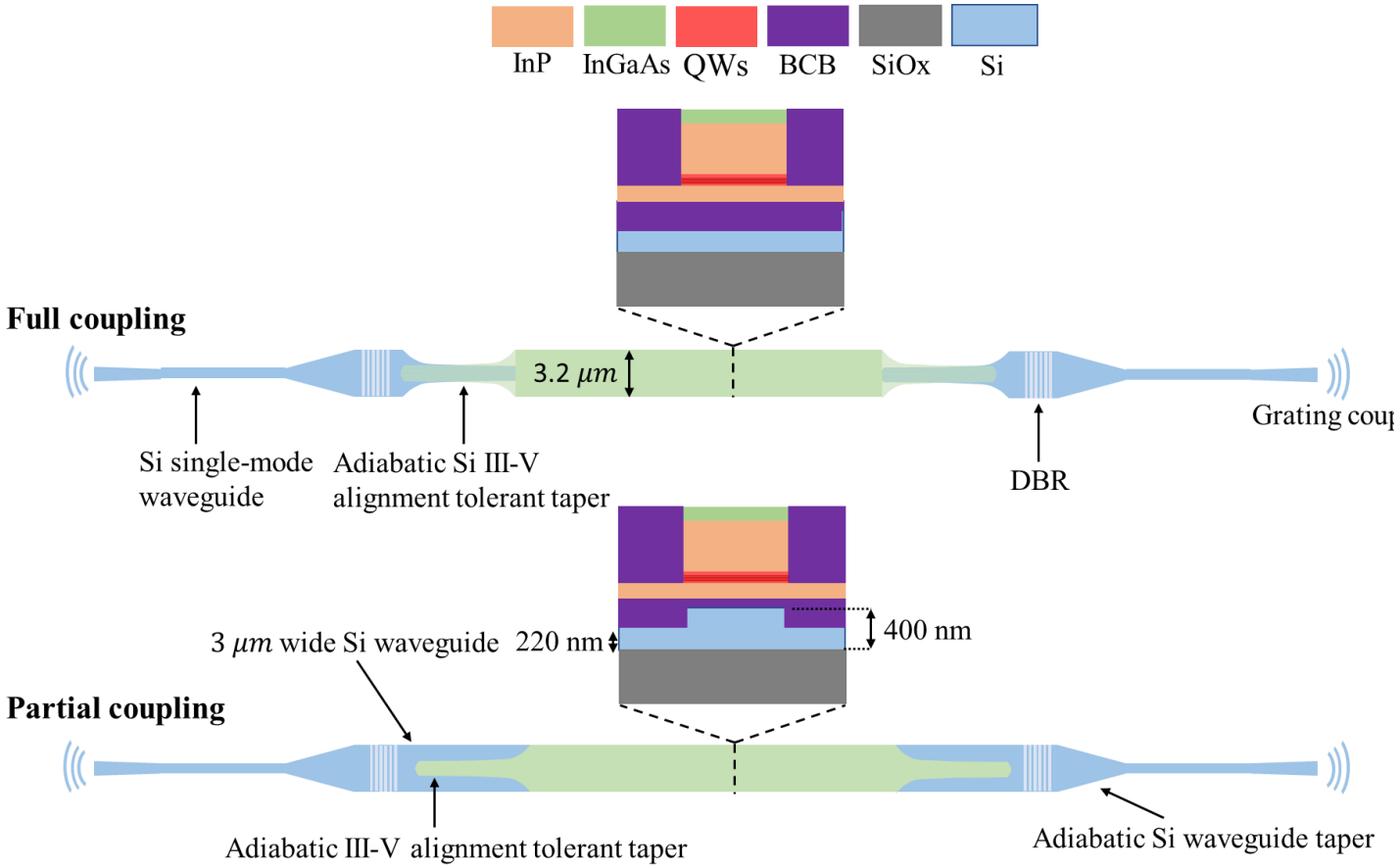
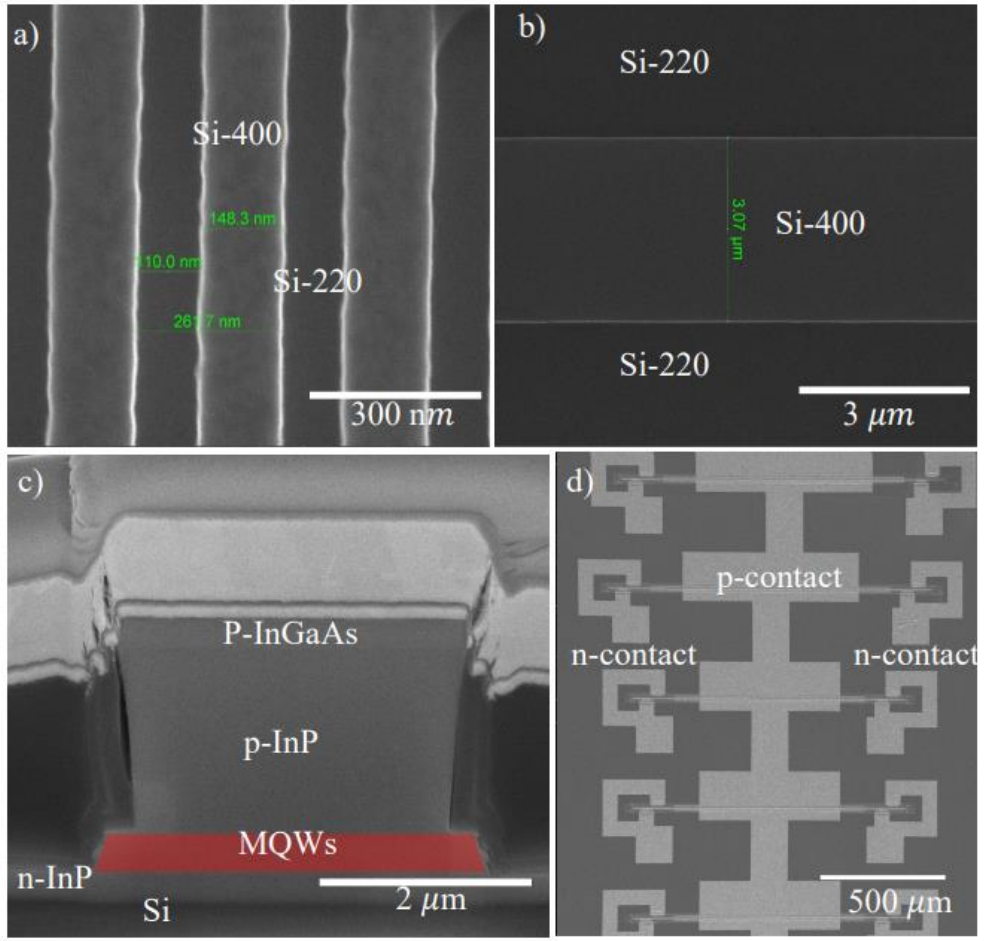
DBR LASERS





Symmetric DBR lasers to study the effect on the threshold current due to lateral misalignment

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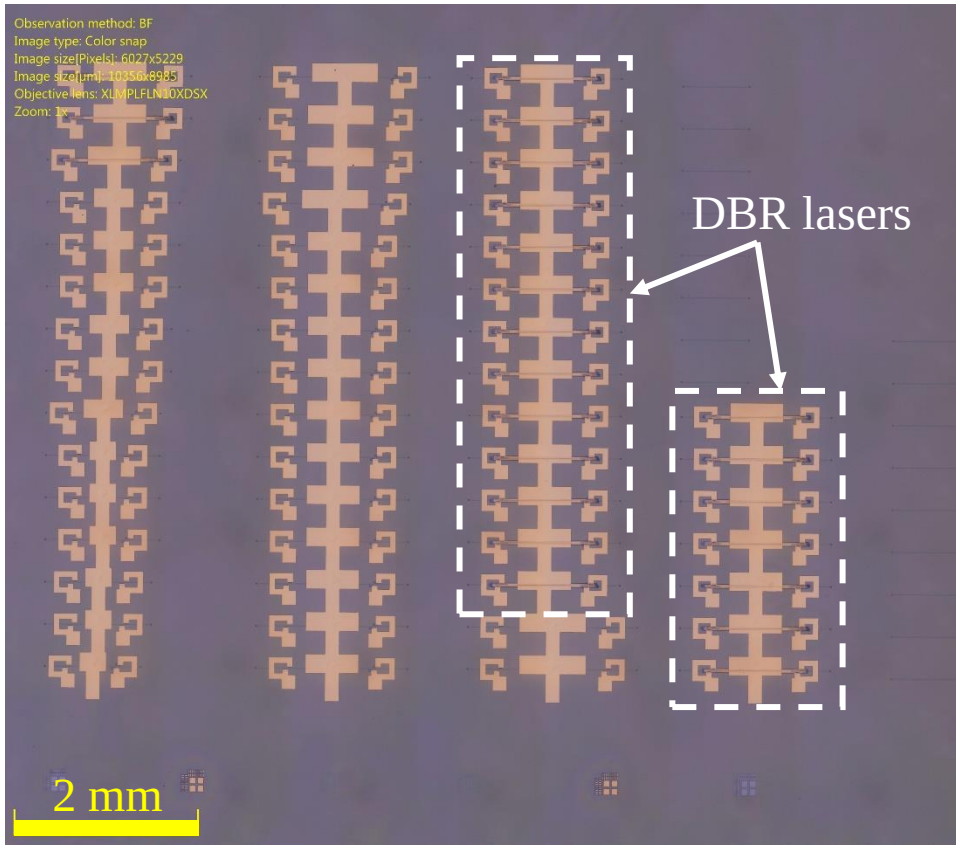
PIC LAYOUT



Array of similar DBR lasers are micro-transfer-printed individually

- To study the effect of micro-transfer-printing process on the performance of the lasers (threshold current)
- Misalignment between SOA and Si waveguide can introduce additional losses in the cavity and increase the threshold current

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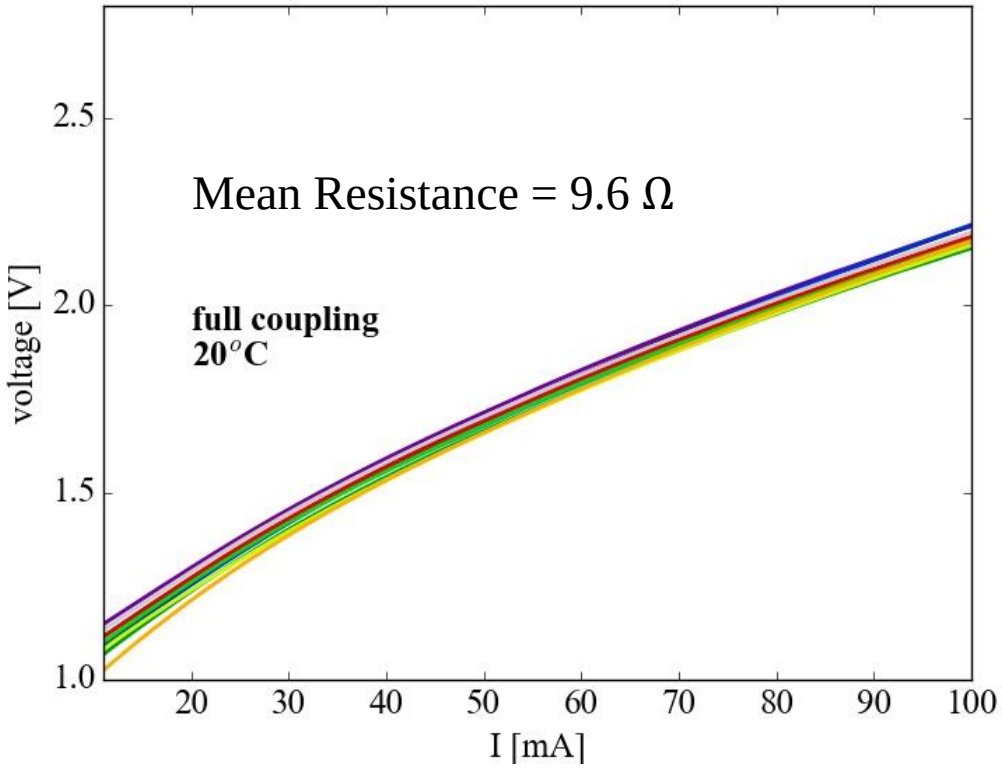
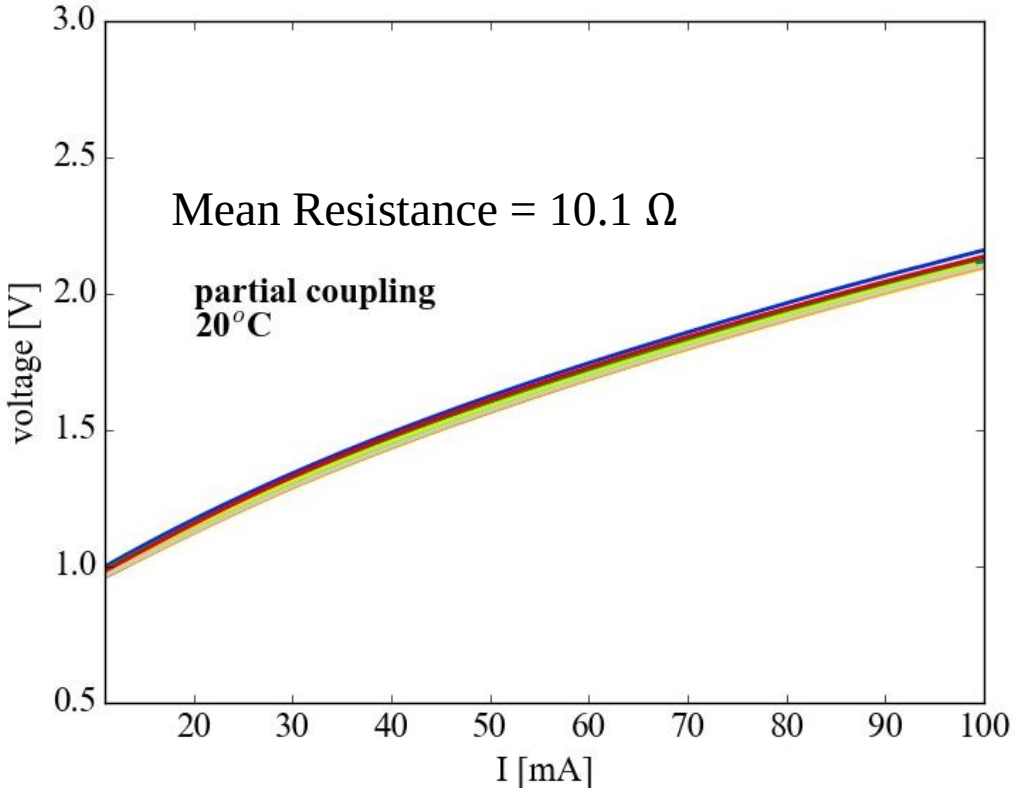
I-V CHARACTERISTICS





Since the SOAs are identical and processed together on an InP die

- They have nominally identical differential resistance

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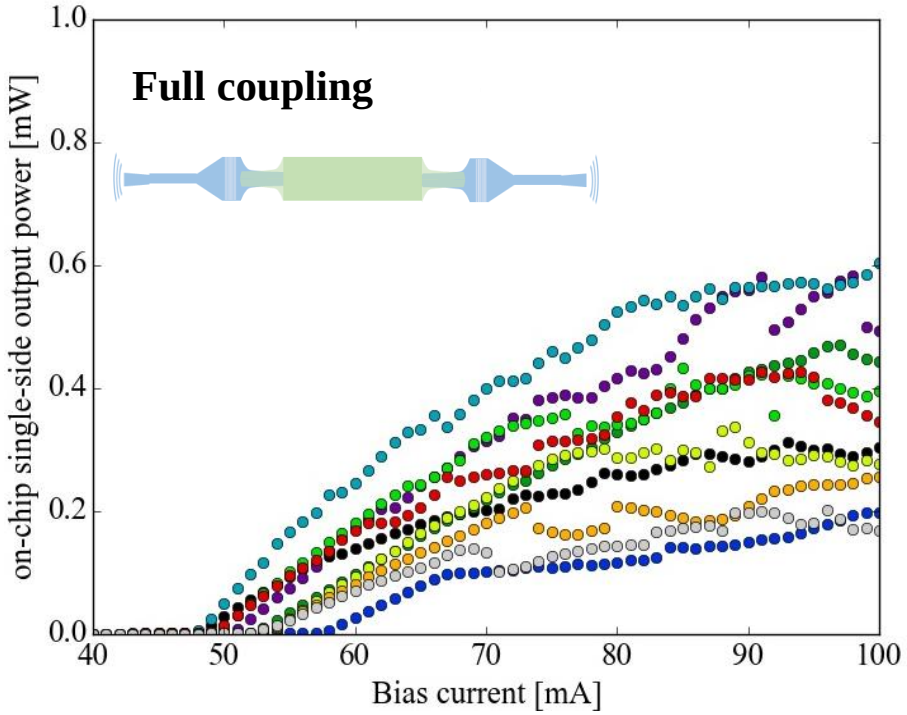
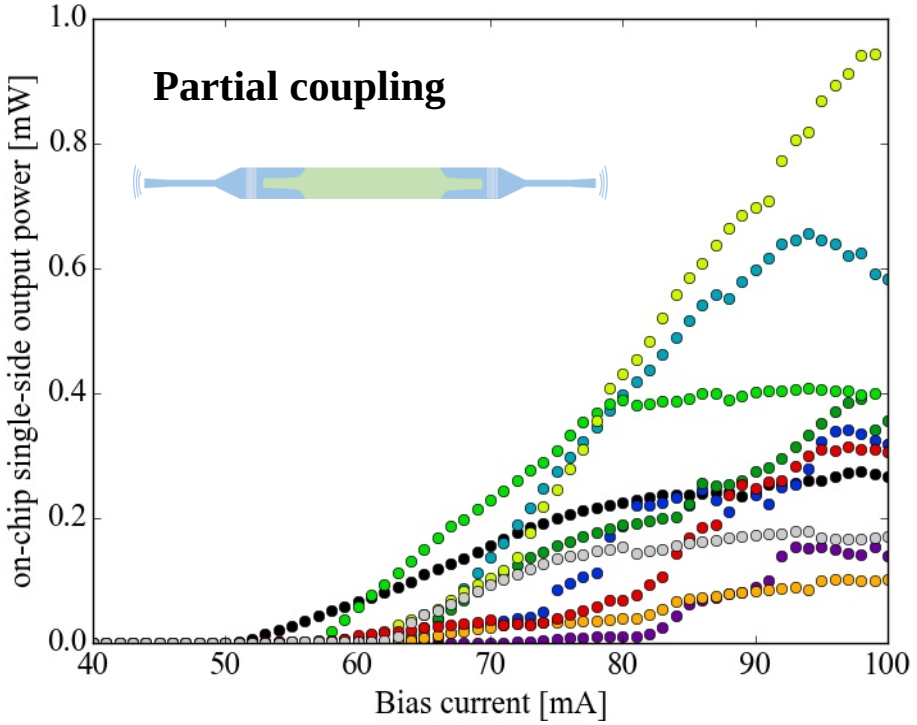
L-I CHARACTERISTICS



Mean threshold current = 51 mA
Standard deviation = 3.24 mA



Mean threshold current = 60 mA
Standard deviation = 5.31 mA

- Large spread in the I_{th} and slope efficiency of partial coupling DBR can be attributed to the variation of the confinement factor in the QW with misalignment
- Moreover, as various transversal modes are supported in the gain section, this can cause the spread to increase further.

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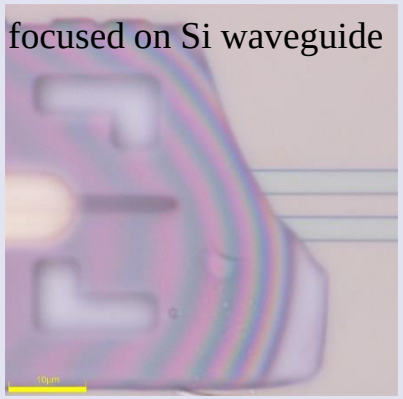
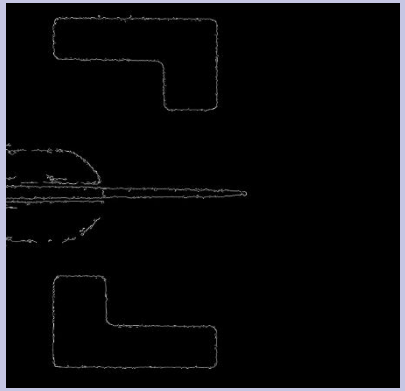
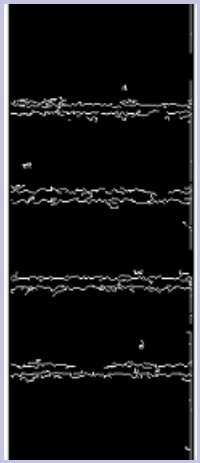
MISALIGNMENT CALCULATION

High-resolution microscope images
43 nm per pixel

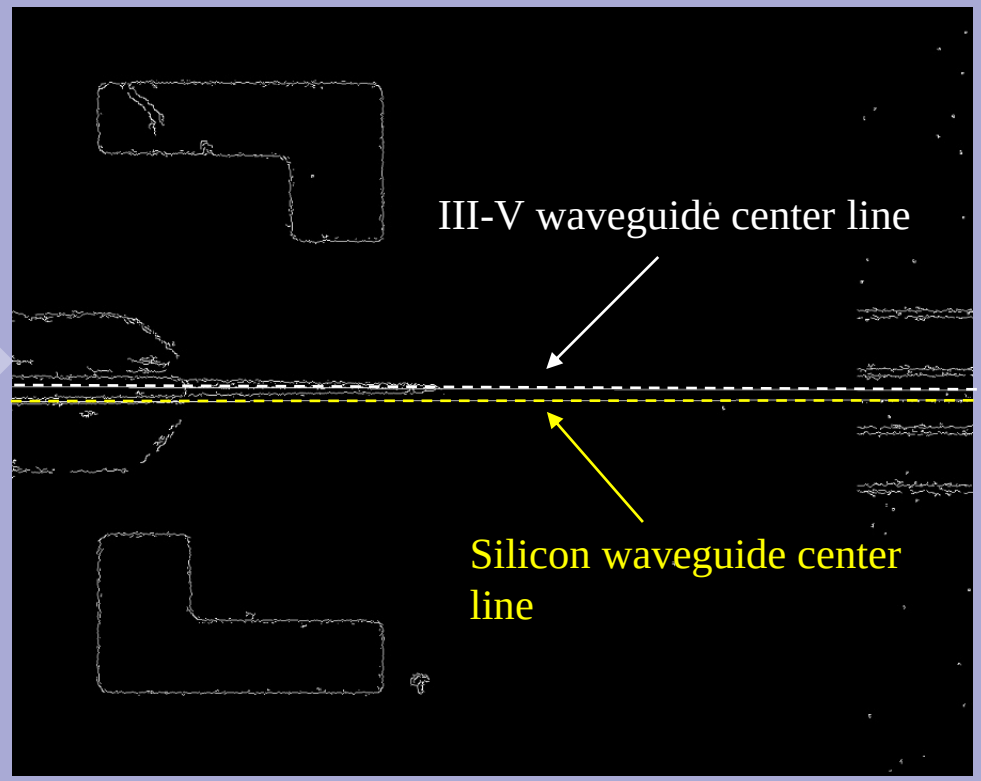


edge detection of III-V and Si waveguide

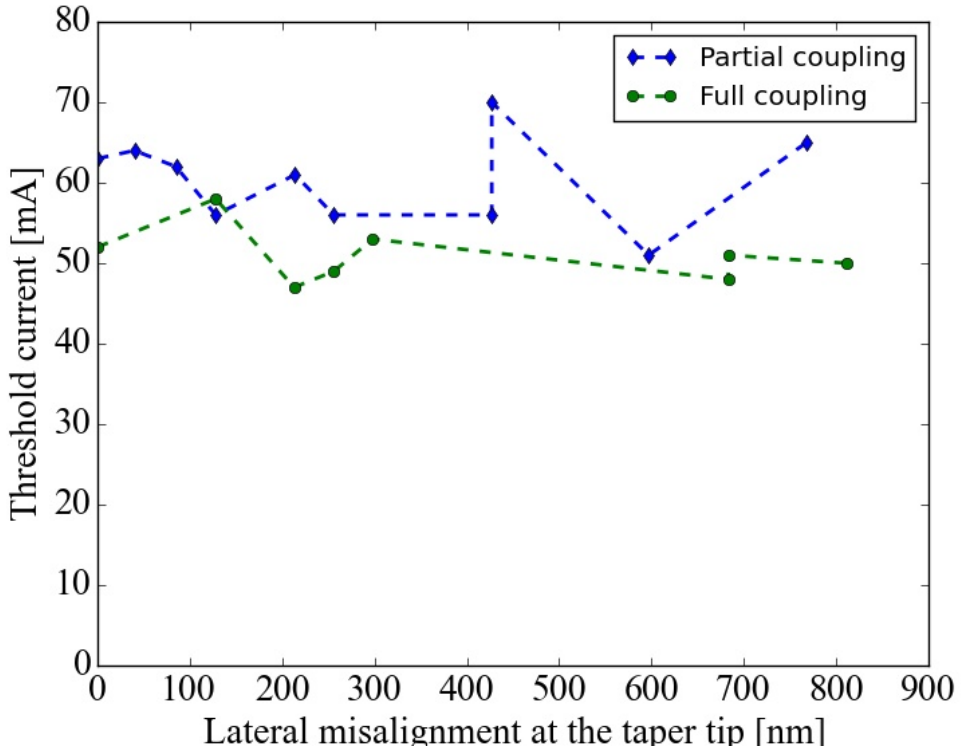




Center-line calculation and fitting



THRESHOLD CURRENT AND MISALIGNMENT



- Misalignment and the threshold current shows no correlation which corroborates the alignment tolerant design of the adiabatic couplers.
- Furthermore, the effect of misalignment is insignificant on the loss as compared to the waveguide loss (~ 40 dB/cm) in the III-V-on-Si waveguide.

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FUTURE OUTLOOK

- Adding contact pads to the coupons for electrical testing and to eliminate processing steps after printing.

- Integration in complex foundry platforms such as ISSIP50G and Ligentec low loss SiN platform

- Integration of best of class devices from multiple material systems such InP lasers, $\mathrm{LiNb}O_3$ modulators, and low loss SiN waveguides.

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Thank you for your attention

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