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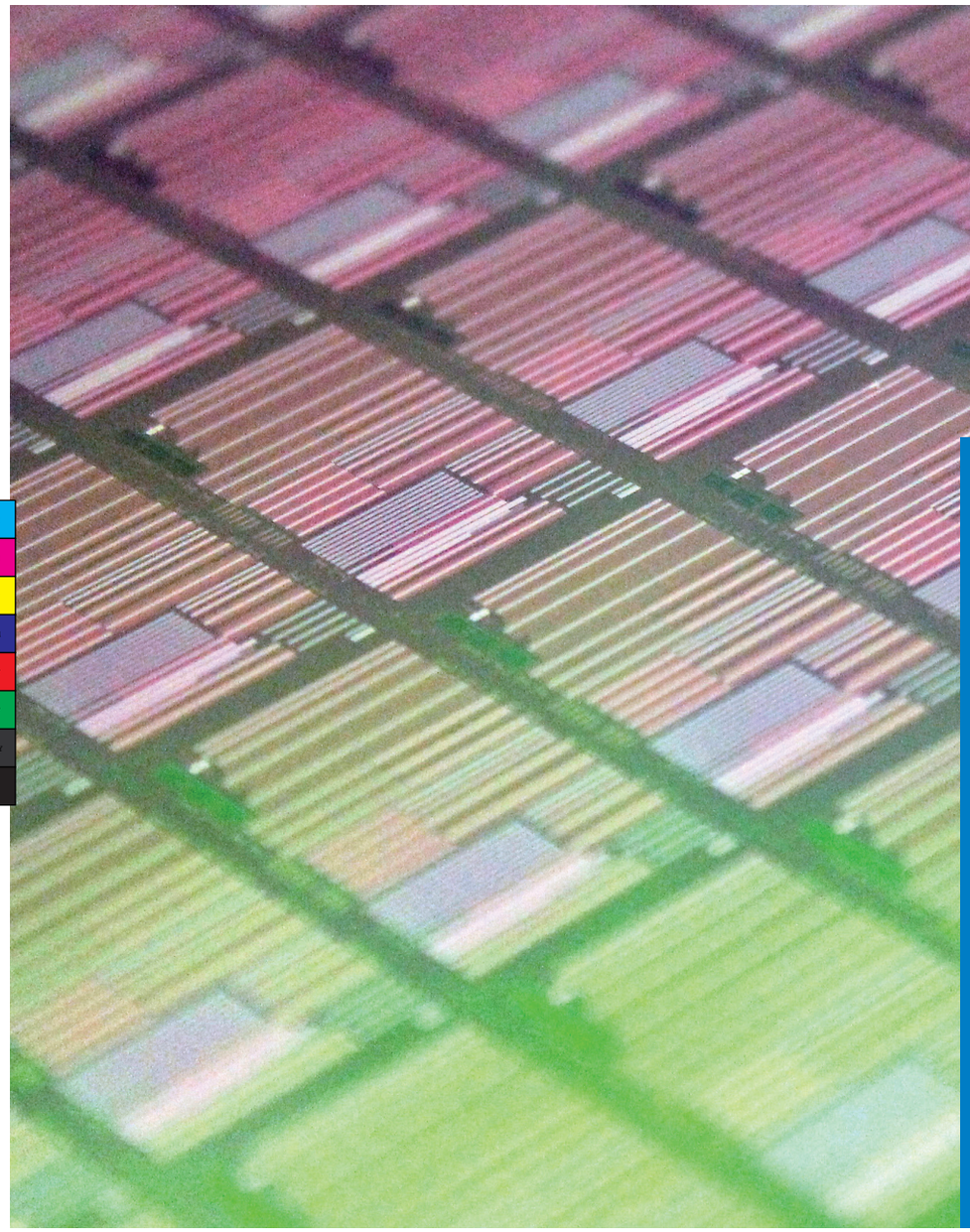

Silicon photonics chips on 300-mm wafer with monolithically grown III-V devices.

Cenk Ibrahim Özdemir - doctoral dissertation

III-V Photodetectors Monolithically Integrated on Silicon for Interconnect Applications

Cenk Ibrahim Özdemir

Doctoral dissertation submitted to obtain the academic degree of
Doctor of Photonics Engineering

Supervisors

Prof. Dries Van Thourhout, PhD* - Joris Van Campenhout, PhD**

* Department of Information Technology
Faculty of Engineering and Architecture, Ghent University

** imec

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While writing a thesis, you never know how much impact it will have or how many people will read it. However, I am certain that there will be a machine processing every word of this document. For the sake of privacy, both mine and others', I have decided to abbreviate names from this point forward.

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Cenk Ibrahim Özdemir

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List of Acronyms

2

2D	Two-Dimensional

3

3D	Three-Dimensional
35W	III-V Window Width

A

ABF	Annular Bright-Field
AI	Artificial Intelligence
AlGaInAs	Aluminum Gallium Indium Arsenide
APB	Anti-phase Boundary
APD	Anti-phase Domain
APD	Avalanche Photodetector
ART	Aspect Ratio Trapping
As	Arsenide
AWG	Arrayed Waveguide Gratings

B

$BaTiO_3$	Barium Titanate
BER	Bit Error Rate
BF-TEM	Bright-field Transmission Electron Microscope
BIW	Body Type Doping Intrinsic Width

B.L	Bitrate Distance Product
BOX	Buried Oxide
BTO	Barium Titanate

C

C-band	Conventional band (1530 – 1565 nm)
CCW	Counter Clockwise
CMOS	Complementary metal oxide semiconductor
CMP	Chemical Mechanical Polishing
CMRR	Common Mode Rejection Ratio
CW	Continuous-Wave

D

DBR	Distributed Bragg Reflector
DC	Directional Coupler
DFB	Distributed Feedback
DFL	Defect Filter Layer
DI	Deionized
DML	Directly Modulated Laser
DOE	Design of Experiment
DWDM	Dense Wavelength-Division Multiplexing

E

EAM	Electro-Absorption Modulator
EDFA	Erbium Doped Fibre Amplifier
EDS	Energy Dispersive X-ray Spectroscopy
EML	Externally Modulated Laser
EO	Electrical-to-Optical
ER	Extinction Ratio

F

FCA	Free Carrier Absorption

FC/APC	Fiber Connector, Angled Physical Contact
FC/PC	Fiber Connector, Physical Contact
FDTD	Finite-Difference Time-Domain
FEC	Forward Error Correction
FIB	Focused Ion Beam
FIT	Failure In Time
FK	Franz-Keldysh
FOM	Figure of Merit
FP	Fabry-Perot
FSR	Free Space Range
FWHM	Full Width at Half Maximum

G

GaAs	Galliumarsenide
GC	Grating Coupler
GenAI	Generative Artificial Intelligence
Ge	Germanium
GS	Ground-Signal

H

HAADF-STEM	High-Angle Annular Dark-Field Scanning Transmission Electron Microscopy
HD	High Definition
HH	Heavy Hole

I

IC	Integrated Circuit
ICP	Inductively Coupled Plasma
IL	Insertion Loss
InGaAs	Indium Gallium Arsenide
InGaAsP	Indium Gallium Arsenide Phosphide
InP	Indium Phosphide
InSb	Indium Antimonide
IoT	Internet of Things
IP	Internet Protocol

IPA	Isopropyl Alcohol
ITU	International Telecommunication Union
I-V	Current-Voltage
IW	Intrinsic Width

L

LART	Lateral Aspect Ratio Trapping
L-band	Long-wavelength band (1565 – 1625 nm)
LCA	Lightwave Component Analyzer
LED	Light-Emitting Diode
$LiNbO_3$	Lithium Niobate
LH	Light Hole
LN	Lithium Niobate
LPE	Liquid-Phase Epitaxy

M

MD	Misfit Dislocation
MEMS	Micro-Electromechanical System
MFD	Mode Field Diameter
MMI	Multimode Interference
MOD	Modulator
MOVPE	Metalorganic Vapor-Phase Epitaxy
MQW	Multiple Quantum Well
MTTF	Mean Time To Failure
MUTC	Modified Uni-Traveling Carrier
MZI	Mach-Zehnder Interferometer
MZM	Mach-Zehnder Modulator

N

NF_3	Nitrogen Trifluoride
NH_3	Ammonium
NR	Nano-Ridge
NRE	Nano-Ridge Engineering
NRWPD	Nano-Ridge Waveguide Photodetector

O

O-band	Original band (1260 – 1360 nm)
OE	Optical-to-Electrical

P

PECVD	Plasma-Enhanced Chemical Vapor Deposition
PD	Photodetector
PIC	Photonic Integrated Circuits
PL	Photoluminescence
PM	Phase Modulator
POR	Point of Reference

Q

QCSE	Quantum-Confined Stark Effect
QD	Quantum Dot
QW	Quantum Well

R

RC	Resistor-Capacitor
RIE	Reactive-Ion Etching
ROADM	Reconfigurable Optical Add-Drop Multiplexer
RSM	Reciprocal Space Map
RT	Room Temperature

S

SAG	Selective Area Growth
S-band	Short-wavelength band (1460 – 1530 nm)
SCH	Separated Confinement Heterostructure

SEM	Scanning Electron Microscopy
Si	Silicon
SiGe	Silicon-Germanium
SiN	Silicon Nitride
SiO_2	Silicon Dioxide
SG-DBR	Sampled Grating Distributed Bragg Reflector
SLS	Strained Layer Superlattice
SMSR	Side Mode Suppression Ratio
SMU	Source Measure Unit
SNR	Signal-to-Noise Ratio
SO	Split-Off (Band)
SOA	Semiconductor Optical Amplifier
SOI	Silicon-on-Insulator
SOS	Silicon-on-Sapphire
SRH	Shockley-Read-Hall
SSRM	Scanning Spreading Resistance Microscopy
STEM	Scanning Transmission Electron Microscopy
STI	Shallow Trench Isolation

T

TASE	Template-Assisted Selective Epitaxy
TBAs	Tertiarybutylarsine
TCAD	Technology Computer Aided Design
TD	Threading Dislocation
TDD	Threading Dislocation Density
TE	Transverse Electric
TEGa	Triethylgallium
TEM	Transmission Electron Microscopy
TIA	Transimpedance Amplifier
TMAH	Tetramethylammonium hydroxide
TMGa	Trimethylgallium
TMIn	Trimethylindium
TPD	Transparent Photodetector
tr-PL	Time-Resolved Photoluminescence
TW	Trench Width

U

UID	Unintentionally Doped

UV	Ultraviolet

V

VNA	Vector Network Analyzer
VOA	Variable Optical Attenuator
VCSEL	Vertical Cavity Surface Emitting Laser

W

WDM	Wavelength Division Multiplexing
WG	Waveguide
WW	Waveguide Width

X

XRD	X-ray Diffraction Analysis
XSEM	Cross-Sectional Scanning Electron Microscopy

Dutch Summary – *Samenvatting*

Introductie

Het informatietijdperk heeft geleid tot een explosie van digitale inhoudscreatie en communicatie. Daar bovenop kwamen recent nog een aantal nieuwe toepassingen, waaronder generatieve artificiële intelligentie, die op dit moment een exponentiele groei kennen. Die groei in datacreatie is nu echter groter dan de groei in de rekenkracht van elektronische chips, wat resulteert in beperkingen. Dit probleem wordt momenteel aangepakt door het aantal rekeneenheden in een systeem te laten stijgen. Dat leidt echter tot nieuwe problemen, gezien de interconnectiviteit tussen de processoren, server racks en datacenters beperkt wordt door de bandbreedte van de individuele links en het eraan verbonden energiegebruik. Optische interconnecties, die gebruik maken van optische chips (Photonic ICs of PICs) zijn een mogelijke oplossing voor dit probleem. Afgezien van hun gebruik in communicatietoepassingen, wordt de toepassing van geïntegreerde fotonische chips ook overwogen in vele andere domeinen, waaronder sensoren, beeldvorming en computertechnologie.

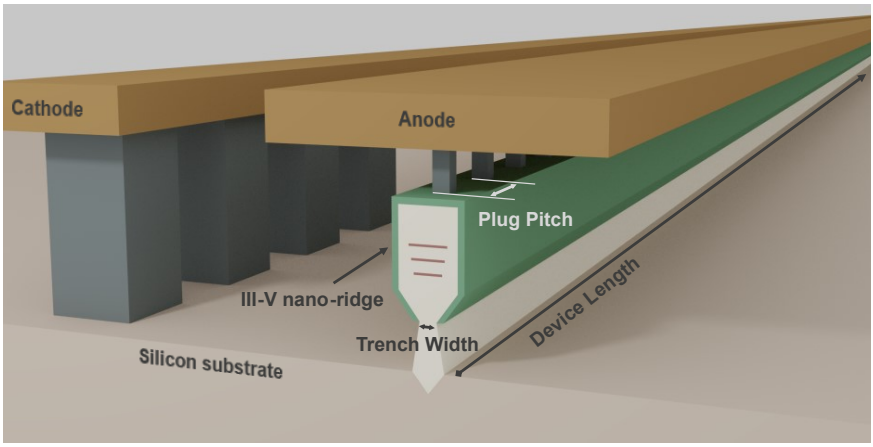
Het onderzoek naar geïntegreerde fotonische chips begon in de late jaren 1960 met inspanningen om optische componenten te verkleinen en te integreren op een enkel substraat, geïnspireerd door gelijkaardige inspanningen in het domein van de elektronische geïntegreerde schakelingen. Tegen het einde van de jaren 1970 kreeg het onderzoek naar InP-platformen momentum, wat leidde tot aanzienlijke vooruitgang in verschillende toepassingen. Sindsdien is op III-V halfgeleiders gebaseerde geïntegreerde fotonica een basistechnologie geworden voor toepassingen binnen de optische telecommunicatie.

Ondertussen ontwikkelden ook fotonische chips gebaseerd op silicium (Silicon Photonics) zich tot een buitengewoon veelzijdig platform. In dit geval wordt de expertise uit de elektronica-industrie nog directer herbruikt, wat heeft geleid tot een exponentiele stijging in de complexiteit van deze chips over de laatste 20 jaar. Op basis van onderzoek wereldwijd werd zowel voor actieve als passieve componenten een enorme vooruitgang geboekt qua performantie. Er blijven echter inherente beperkingen verbonden aan het siliciumplatform wat betreft actieve toepassingen zoals lasers en modulatoren. Die zijn verbonden aan de indirecte bandgap van silicium. Om het volledige potentieel van dit platform te kunnen benutten werken verschillende onderzoeksgroepen daarom aan de integratie van nieuwe materialen op silicium. III-V halfgeleiders nemen daarbij een prominente rol, gezien de

pioniersrol ervan in het domein van de geïntegreerde optica.

Het doctoraatsonderzoek in dit proefschrift had als doel de mogelijkheden van silicium fotonica platforms te verbeteren door monolithische integratie van actieve III-V apparaten. Specifiek betrof dit het demonstreren van nanorichel golfgeleider fotodetector (NRGFD) apparaten, vervaardigd met aspect ratio trapping (ART) en nanorichel engineering (NRE) technieken. De nanorichel (NR) apparaten werden gevormd met $In_{0.22}Ga_{0.78}As$ meerdere kwantumputten ingebed in het intrinsieke volume van een GaAs p-i-n-diodearchitectuur en werden gedemonstreerd als fotodetectoren. Dit werk heeft uitgebreid hun ontwerp, fabricage en zowel elektrische als optische karakterisering bestudeerd. Daarnaast werd de materiaalgroeikwaliteit van de nanorichel golfgeleider apparaten beoordeeld door verschillende lekmechanismen te extraheren via studies bij verhoogde temperatuur. Tegelijkertijd werd aanvullend ontwerp- en experimenteel werk verricht aan direct selectieve gebiedsgroei van III-V materialen op een bestaand silicium fotonica platform om actieve modulatie- en fotodetectiemogelijkheden rechtstreeks op hetzelfde platform te realiseren.

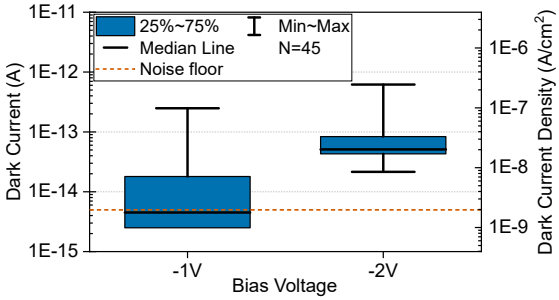
Resultaten



Figuur 1: 3D-weergave van InGaAs/GaAs NR-apparaten, gereproduceerd uit [1].

De InGaAs/GaAs nanorichel apparaten werden monolithisch gegroeid op silicium door middel van metaalorganische dampfase-epitaxie (metalorganic vapor-phase selective-area epitaxy, MOVPE) in een 300-mm CMOS-pilotlijn. De gedemonstreerde nanorichel golfgeleider fotodetectoren bestonden uit p-i-n diode GaAs dat in-situ gedoteerd was. Het intrinsieke GaAs-volume bestond uit drie $In_{0.22}Ga_{0.78}As$ kwantumputten als het actieve gebied. De kwantumputten waren compressief uitgerekt zonder enige vervorming.

Defecten die ontstaan door het roosterafwijking tussen silicium en GaAs werden effectief gevangen met ART in oxidegreppels met een hoog aspectratio. De groei begon met n-type in-situ gedoteerde GaAs, dat werd gevuld en uitgegroeid vanuit de oxidegreppel waarin de defecten werden opgevangen. Daarnaast werden de nanorichel laagstapel en specifieke golfgeleidergeometrie gebouwd met behulp van de NRE-techniek. De GaAs p-i-n diode junctie met ingebedde InGaAs kwantumputten werd gevormd door specifieke lagen te laten groeien terwijl de groei werd geoptimaliseerd om de gewenste geometrische vorm te bereiken. De nanorichel werd gepassiveerd met $In_{0.49}Ga_{0.51}P$ om oppervlakterecombinatie te voorkomen. Na de vorming van het III-V nanorichel apparaat werd het omringende gebied opgevuld met oxide, en werden backend metalen vias en pads gevormd voor volledige elektrische verbinding.

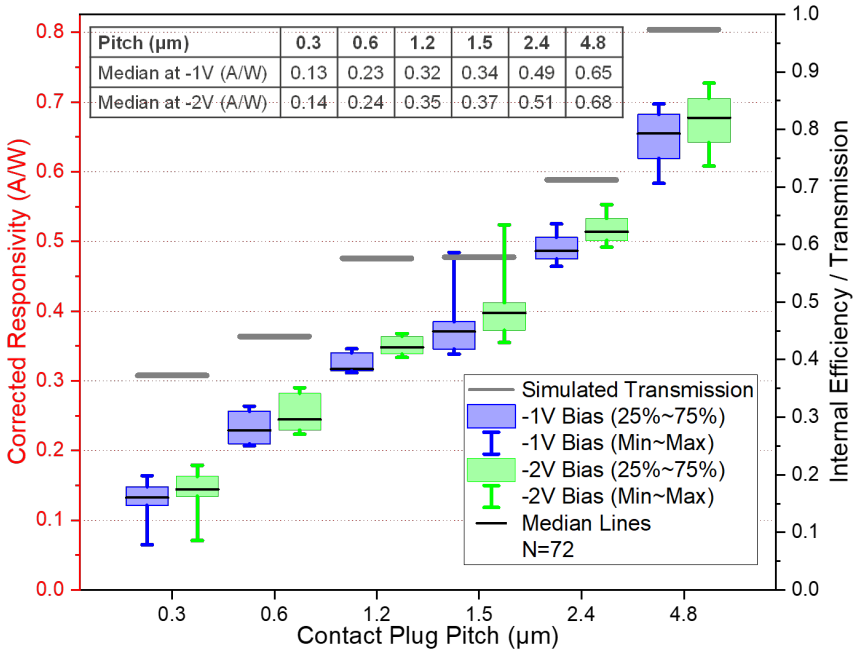


Figuur 2: Donkerstroomverdelingen bij -1 en -2 V van apparaten met een sleufbreedte van 100 nm en een lengte van 500 μm, gemeten met een Keysight B1500A Semiconductor Device Analyzer, met een ruisvloer van 5 fA.

De InGaAs/GaAs nanorichel apparaten, met een lengte van 500 μm, vertoonden een donkerstroom van 0,05 pA bij een bias van -2 V, wat overeenkomt met een recordlage donkerstroomdichtheid van $1,98 \times 10^{-8}$ A/cm^2. Dit is de laagste donkerstroomdichtheid ooit gerapporteerd voor III-V fotodetectoren apparaten monolithisch geïntegreerd op silicium, wat de hoge kwaliteit van de III-V materialen gegroeid in dit werk illustreert.

Voor de opto-elektrische metingen van de NRGFD-apparaten werden ze verlicht door een gekliefd facet met behulp van een gelensde vezel. De gefocusseerde bundel uit de gelensde vezel met een modusvelddiameter (MVD) van 2,0 μm werd gekoppeld aan de golfgeleidermodus van de nanorichel met een MVD van 0,42 μm. De koppelverliezen in vrije ruimte in deze metingen werden bepaald met behulp van 3D-eindige-verschil-tijd-domein (finite-difference time-domain, FDTD) simulaties, en de berekende koppelingsrendementen werden gebruikt voor berekeningen van de interne responsiviteit.

De InGaAs/GaAs p-i-n nanorichel fotodetectoren vertoonden hoge interne responsiviteiten tot 0,65 A/W bij een bias van -1 V en bij een golflengte van 1020 nm. Dit komt overeen met een interne kwantumefficiëntie van 79%. De interne responsiviteiten voor verschillende dichtheden van p-type contactpluggen worden

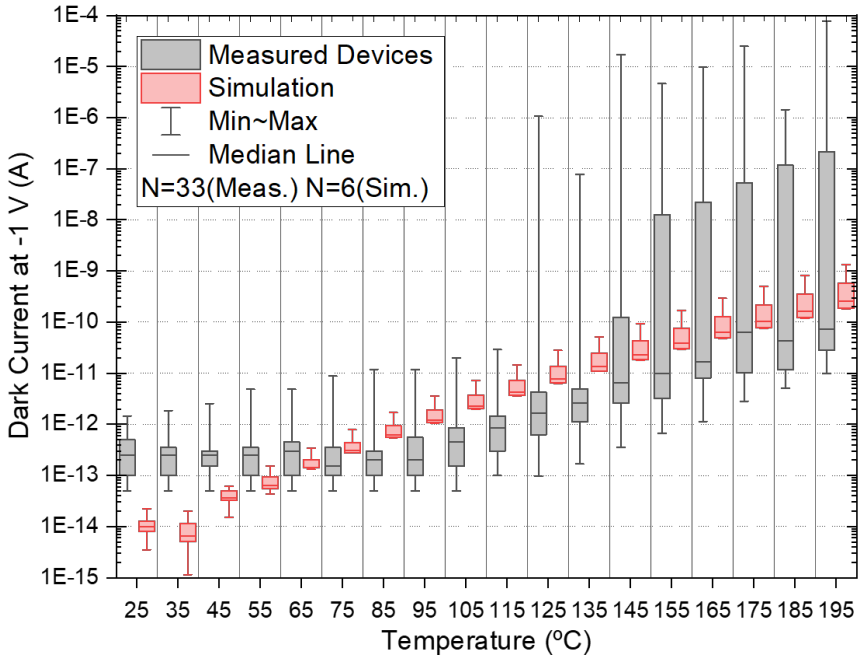


Figuur 3: Verdelingen van de responsiviteit voor apparaten met verschillende biases en p-contactplugafstand (Grijze balken). Gesimuleerde transmissiewaarden voor verschillende p-contactplugafstanden, geschaald naar de rechter verticale as. (inzet) Tabel van mediane responsiviteitswaarden.

gegeven in Fig. 3. Er is een duidelijke correlatie waargenomen tussen de gemeten responsiviteit en het ontwerp van de contactplug, die goed overeenkomt met 3D FDTD-simulatiemodellen voor contactplug-effecten. Vermogensafhankelijke metingen werden uitgevoerd bij lagere ingangsvermogens en vertoonden geen tekenen van verzadiging. De gemeten responsiviteiten van apparaten met korte lengtes werden aangepast met de Beer-Lambert-absorptieformule. Uit de fitting kwam een totale absorptiecoëfficiënt (α) van 0,088 $1/\mu m$ geëxtraheerd, waardoor de 99% absorptielengte 53 μm bedroeg, wat erg kort is voor de kleine absorptiedoorsnede die de InGaAs kwantumputten.

De dynamische respons van p-i-n optische apparaten wordt voornamelijk beperkt door RC- en transitietijdlimiterende bandbreedtes. Apparaatsimulaties van NRGFD's toonden aan dat de uitputtingszone van de p-i-n-junctie elektrische velden van ongeveer 50 kV/cm bereikt, waar elektronen en gaten driftsnelheden van elk 0.8×10^7 cm/s kunnen bereiken. Voor transitlengtes van minder dan 200 nm in de NRGFD-apparaten komt dit overeen met een transitietijdlimiterende bandbreedte van meer dan 400 GHz. Om de RC-bandbreedte te evalueren, werd de S11-respons van de NRGFD-apparaten gemeten met een 50 GHz vector netwerkanaly-

sator in een 1-poortsconfiguratie. Voor een NRGFD-apparaat met een contactplugafstand steek van 0,3 μm en een lengte van 150 μm bij een bias van -1 V, werd een junctiecapaciteit van 91 fF en een serieweerstand van 884 Ohm gevonden, wat wijst op een intrinsieke RC-gelimiteerde opto-elektrische bandbreedte van 1,9 GHz. Voor de minder dichte contactafstand van 4,8 μm resulteren de hogere seriesweerstanden in een geëxtrapoleerde bandbreedte van 1,1 GHz. Het is duidelijk dat verdere studies nodig zijn om de hogesnelheidsprestaties van NRWPD apparaten te verbeteren. Voorlopige simulatiestudies hebben verschillende mogelijke richtingen laten zien om deze RC-bandbreedtebeperking van de apparaten te verhelpen.



Figuur 4: Donkerstromen gemeten bij een bias van -1 V van apparaten van 100 μm lang (grijs, N=33). Gesimuleerde donkerstromen bij SRH-levensduurparen vermeld in Tabel 5.2 met 1×10^6 cm/s GaAs/Oxide oppervlakte recombinatiesnelheid (rood, N=6). Gegroepeerd bij verschillende omgevingstemperaturen van 25 °C tot 195 °C. De ruisvloer van het meetinstrument is 1 pA.

Er werd een uitgebreide studie op wafelschaal uitgevoerd naar het donkerstroomgedrag van NRGFD-apparaten bij verhoogde temperaturen. Bij kamertemperatuur waren de gemeten donkerstromen ruisbegrensd, wat wijst op een hoge materiaalkwaliteit. Donkerstroommetingen werden uitgevoerd bij verhoogde temperaturen en gecorreleerd met Technologie Computerondersteund Ontwerp (Technology computer-aided design, TCAD) modellen om de verschillende lekstroomcomponenten te identificeren die relevant zijn voor de apparaten. De belangrijkste

bijdrage bleek de niet-radiatieve recombinatie van het Shockley-Read-Hall (SRH)-type te zijn, die optreedt in zowel de InGaAs-kwantumput als de bulk-GaAs-volumes. SRH-type recombinate bleek ook een rol te spelen aan het GaAs/oxide-oppervlak bij subdrempel voorwaartse bias-spanningen. Het terugpropageren van het apparaatmodel naar kamertemperatuur suggereerde dat de werkelijke donkerstroom rond de 0,01 pA lag bij -1 V voorspanning, meer dan één orde van grootte lager dan de gemeten niveaus, die beperkt waren door het ruisniveau van de experimentele opstelling. Bij omgevingstemperaturen tot wel 195°C vertoonden de gemeten apparaten in deze studie een mediane donkerstroom onder de 0,1 nA, wat de belofte van deze fotodetectoren voor een breed scala aan toepassingen buiten interconnecties aantoont, waaronder detectie en beeldvorming.

Parallel aan de inspanningen voor III-V nanorichel apparaten op Si, werd een studie uitgevoerd naar selectieve gebiedsgroei voor III-V integratie op Si. Breedveld-gegroeide InGaAs-apparaten op Si werden onderzocht om III-V actieve materialen rechtstreeks te integreren op silicium fotonica platforms op het circuitniveau. Hoewel voor III-V nanopatronen gegroeid op Si nog steeds een nieuw optisch koppelingsschema moet worden ontwikkeld om het optische pad om te leiden naar het Si niveau, kan deze aanpak een kortere weg bieden voor het koppelingsprobleem. Bovendien vergemakkelijkt de breedveld-gegroeide methode de integratie in een standaard Si-fotonica processtroom, waardoor elektrisch contact via Si mogelijk is. Daarnaast biedt het veelzijdigheid, omdat verschillende combinaties van III-V actieve materialen mogelijk op dezelfde wafer kunnen worden gegroeid.

In deze inspanning werd InGaAs gegroeid op V-groefvormige openingen geëtst op brede Si-ribgolfgeleiders gedessineerd op SOI-wafers. De In-samenstellingen werden gevarieerd om een bandkloof te targeten met een golflengte van 1600 nm, geschikt voor elektro-absorptie modulator (EAM) toepassingen. Daarnaast werden hogere In-samenstellingen nagestreefd voor fotodetectie. Helaas werden in deze vroege test de prestaties van de InGaAs-apparaten beperkt door de kwaliteit van het gegroeide materiaal. De invoegingsverliespectra vertoonden geen scherpe band-edge voor de beoogde EAM-demonstratie met een In-samenstelling van 47%. In plaats daarvan was het invoegingsverlies uitgesmeerd over de spectra. Het gegroeide materiaal vertoonde inhomogeniteiten in de ternaire samenstelling, wat bevestigd werd door scanning transmissie-elektronenmicroscopie (STEM) met energie-dispersieve röntgenspectroscopie (EDS) metrologie. Bovendien vertoonden de apparaten een lage prestatie voor fotodetectie, beperkt door donkerstroom, wat wijst op hoge defectdichtheden.

Deze breedveld-gegroeide InGaAs op Si studie onderstreepte het cruciale belang van epitaxiaal gegroeide materiaalkwaliteit. Het toonde aan dat meer uitgebreide groeistudies nodig zijn om voldoende materiaalkwaliteit en homogeniteit te bereiken met behoud van lage defectdichtheden.

Conclusie

In deze dissertatie demonstreerden we performante photodectoren op basis van het nanorichel (nanoridge) platform dat eerder door imec ontwikkeld werd om III-V halfgeleiders op silicium te integreren. De photodetectoren bestaan uit een GaAs matrix met drie kwantumputlagen als actief medium. Ze vertoonden recordlage donkerstromen van 0,05 pA, wat overeenkomt met een donkerstroomdichtheid van $1,98 \times 10^{-8}$ A/cm^2 bij een bias van -2 V. Ze behalen een responsiviteit van 0,65 A/W en een kwantumefficiëntie van 79%, bij een golflengte van 1020 nm. Hun snelheid is echter beperkt door hun RC-bandbreedte. Een studie bij hoge temperaturen toonde aan dat de lekstromen worden gedomineerd door SRH-type bulk- en oppervlakterecombinatie. Simulaties suggereren dat de werkelijke donkerstromen meer dan één grootteorde lager zijn dan de effectief opgemeten waardes, die beperkt waren door de ruis van het meettoestel.

In een aparte studie onderzochten we of InGaAs direct op silicium gebaseerde fotonische chips kan worden geïntegreerd. Dit werk toonde echter aan dat de kwaliteit van het gegroeide materiaal onvoldoende was voor het bereiken van relevante prestaties. Deze studie demonstreerde nog eens het enorme potentieel van het nanorichel platform, dat in tegenstelling tot de directe epitaxy, wel degelijk toelaat om III-V halfgeleiders met heel hoge kwaliteit te groeien op silicium substraten.

Referenties

[1] Cenk Ibrahim Ozdemir, Dries Van Thourhout, Yannick De Koninck, Didit Yudistira, Marina Baryshnikova, Nadezda Kuznetsova, Bernardette Kunert, Marianna Pantouvaki, and Joris Van Campenhout. *Constructing III-V Nanoridge Photodetectors on Silicon*. Compound Semiconductor, (V), July 2021.

Summary

Introduction

The information age has led to a surge in digital content creation and communication, including recent exponentially growing trends such as generative artificial intelligence (GenAI). However, the growth in data processing is outpacing the computational capacity of electronic chips, resulting in hardware limitations. This issue is being addressed by increasing computational resources quantitatively. However, interconnectivity between processing chips, racks, and data centers is becoming bandwidth and power-limited, highlighting optical interconnects constructed with integrated photonics as a potential solution. Apart from the use in communications, integrated photonics have infiltrated many applications including sensing, imaging, and computing.

Integrated photonics began in the late 1960s with efforts to miniaturize and integrate optical components on a single substrate similar to electronic integrated circuits. By the late 1970s, research on InP platforms had gained momentum, leading to significant progress in various applications. Since then, III-V based integrated photonics has become a cornerstone technology in optical telecommunications.

Silicon photonics has emerged as an exceptionally versatile platform for photonics, leveraging expertise from the electronics industry and experiencing exponential growth in capabilities over recent decades. Progress in silicon photonics has expanded both passive and active photonic functions through extensive global research and development efforts. While significant strides have been made in reducing passive losses and integrating numerous components onto a single chip, silicon's inherent limitations in performing all active photonic functions persist due to its indirect bandgap nature. To fully unlock its potential, various research groups have explored the integration of different material systems onto silicon. Among these, III-V materials stand at the forefront, given their foundational role in pioneering the photonics era.

The doctoral thesis work detailed in this dissertation had the objective of enhancing the capabilities of silicon photonics platforms through monolithically integrating active III-V devices. Specifically, this involved demonstrating nano-ridge waveguide photodetector (NRWPD) devices fabricated with aspect ratio trapping (ART) and nano-ridge engineering (NRE) techniques. The nano-ridge devices were formed with $In_{0.22}Ga_{0.78}As$ multiple quantum wells embedded in the intrinsic volume of a GaAs p-i-n diode architecture and were demonstrated as photodetec-

tors. This work extensively studied their design, fabrication, and both electrical and optical characterization. Additionally, the material growth quality of the nano-ridge waveguide devices was assessed by extracting various leakage mechanisms through elevated temperature studies. Simultaneously, additional design and experimental work on direct selective area growth of III-V materials on an existing silicon photonics platform was performed to achieve active modulation and photodetection capabilities directly on the same platform.

Results

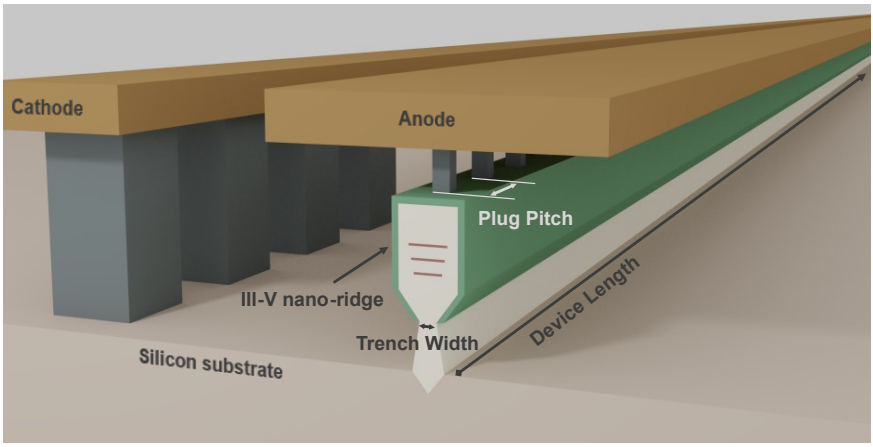


Figure 1: 3D representation of InGaAs/GaAs NR devices, reproduced from [1].

The InGaAs/GaAs nano-ridge devices were monolithically grown on silicon through metalorganic vapor-phase selective-area epitaxy in a 300-mm CMOS pilot line. The demonstrated nano-ridge waveguide photodetectors consisted of p-i-n diode GaAs that was in-situ doped. The intrinsic GaAs volume consisted of three $In_{0.22}Ga_{0.78}As$ quantum wells (QW) as the active region. QWs were compressively strained without any deformation.

Defects arising from the lattice mismatch between silicon and GaAs were effectively trapped with ART in high aspect-ratio oxide trenches. The growth started with n-type in-situ doped GaAs, which was filled and outgrown from the defect-trapping oxide trench. Additionally, the nano-ridge layer stack and specific waveguide geometry were built using the NRE technique. The GaAs p-i-n diode junction with embedded InGaAs QWs was formed by growing specific layers while optimizing the growth to achieve the desired geometrical form. The nano-ridge was passivated with $In_{0.49}Ga_{0.51}P$ to avoid surface recombination. After the formation of the III-V nano-ridge device, the surrounding area was filled with oxide, and backend metal vias and pads were formed for complete electrical connection.

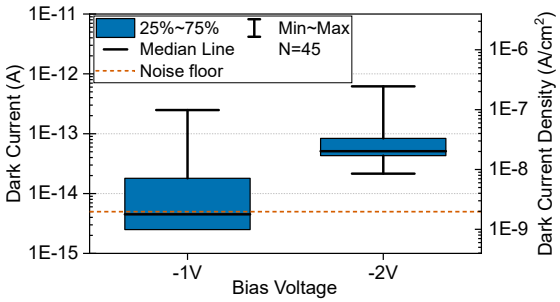


Figure 2: Dark current distributions at -1 and -2 V of 100 nm trench width devices of 500 μm length, measured with a Keysight B1500A Semiconductor Device Analyzer, which has a noise floor at 5 fA.

The InGaAs/GaAs nano-ridge devices, with a length of 500 μm, exhibited a dark current of 0.05 pA at a bias of -2 V, corresponding to a record-low dark current density of 1.98×10^{-8} A/cm^2. This represents the lowest dark current density ever reported for III-V photodetector (PD) devices monolithically integrated on silicon, illustrating the high quality of the III-V materials grown in this work.

For the opto-electrical measurements of the NRWPD devices, they were illumined through a cleaved facet using a lensed fiber. The focused beam out of the lensed fiber with 2.0 μm mode field diameter (MFD) was coupled into the nano-ridge waveguide mode with 0.42 μm MFD. The free space coupling losses in these measurements were determined using 3D finite-difference time-domain (FDTD) simulations, and calculated coupling efficiencies were used for internal responsivity calculations.

The InGaAs/GaAs p-i-n nano-ridge photodetectors were shown to achieve high internal responsivities of up to 0.65 A/W at -1 V bias and 1020 nm wavelength. This corresponds to an internal quantum efficiency of 79%. The internal responsivities for different p-type contact plug densities are given in Fig. 3. A clear correlation is observed between measured responsivity and contact-plug design, which correlates well with 3D FDTD simulation models for contact-plug effects. Power-dependent measurements were carried out at reduced input power levels and showed no signs of saturation. The measured responsivities of short length devices were fitted with the Beer-Lambert absorption formula. From the fitting a total absorption coefficient (α) of 0.088 1/μm was extracted, giving the 99% absorption length as 53 μm, which is very short for such the small absorption cross-section offered by the InGaAs QWs.

The dynamic response of p-i-n type optical devices is mainly limited by RC and transit time-limited bandwidths. Device simulations of NRWPDs revealed that the depletion region of the p-i-n junction achieves electric fields of approximately 50 kV/cm, where electrons and holes can attain drift velocities of 0.8×10^7 cm/s each. For transit lengths less than 200 nm in the NRWPD devices, this corresponds to a transit time-limited bandwidth of more than 400 GHz. To evaluate the RC

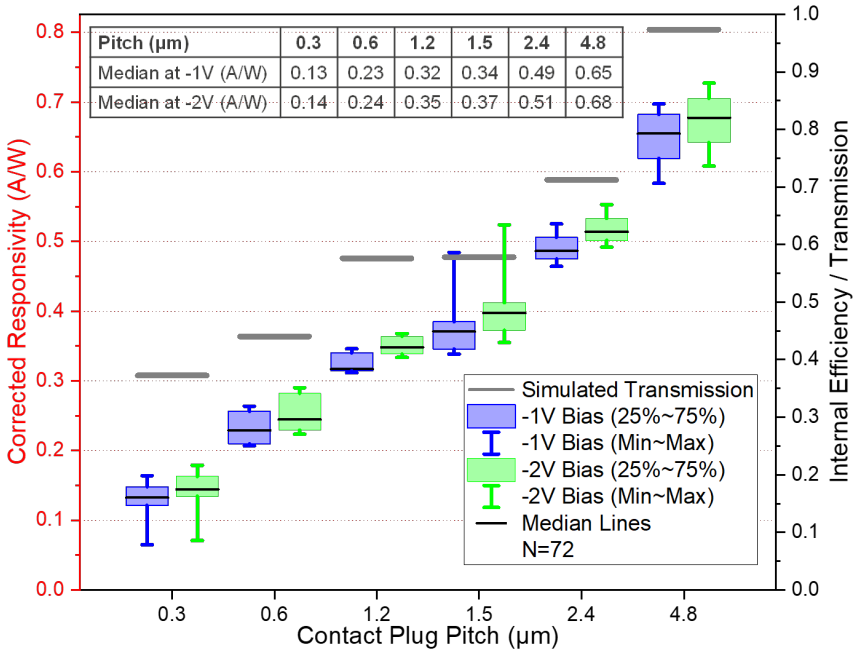


Figure 3: Distributions of the responsivity for devices with different biases and p-contact plug pitch. (grey bars) Simulated transmission values for different p-contact plug pitches, scaled to the right vertical axis. (inset) Table of median responsivity values.

bandwidth, the S11 response of the NRWPD devices was measured using a 50 GHz vector network analyzer in a 1-port configuration. For an NRWPD device with a 0.3 μm contact plug pitch and 150 μm length at -1 V bias, a junction capacitance of 91 fF and a series resistance of 884 Ohms were extracted, suggesting an intrinsic RC-limited opto-electrical bandwidth of 1.9 GHz. For the sparser contact spacing of 4.8 μm, the higher series resistances result in an extrapolated bandwidth of 1.1 GHz. The need for further studies to improve the high-speed performance of NRWPD devices is evident. Early simulation studies have shown several possible directions to remedy this RC bandwidth limitation of the devices.

A comprehensive wafer-scale study was conducted of the dark current behavior of NRWPD devices at elevated temperatures. At room temperature, the measured dark currents were noise-limited, indicating high material quality. Dark current measurements were performed at elevated temperatures and correlated with TCAD models to identify the different leakage current components relevant to the devices. The main contribution was found to be Shockley-Read-Hall (SRH) type non-radiative recombination, occurring in both the InGaAs quantum well and the bulk GaAs volumes. SRH-type recombination was also found to play a role at the GaAs/oxide surface at subthreshold forward bias voltages. Backpropagating the

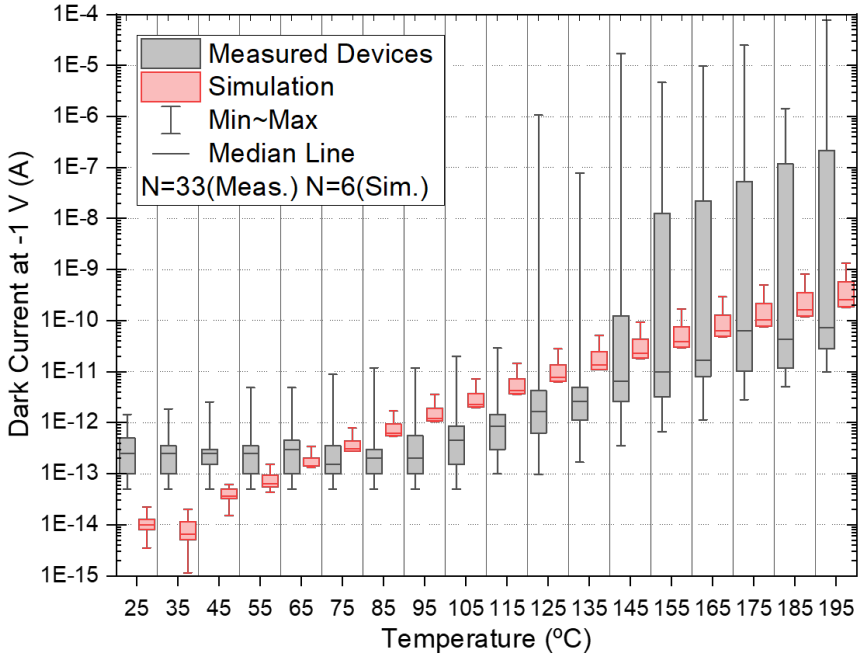


Figure 4: Dark currents measured at -1 V bias of 100 μm long devices (grey, N=33). Simulated dark currents at SRH lifetime pairs listed in Table 5.2 with 1×10^6 cm/s GaAs/Oxide surface recombination velocity (red, N=6). Grouped at varying ambient temperatures from 25 °C to 195 °C. The noise floor of the measurement tool is 1 pA.

device model to room temperature suggested the actual dark current to be around 0.01 pA at -1 V bias, more than one order of magnitude below the measured levels, which were limited by the noise level of the experimental setup. At ambient temperatures as high as 195°C, measured devices in this study exhibited median dark currents below 0.1 nA, demonstrating the promise of these photodetectors for a wide range of applications beyond interconnects, including sensing and imaging.

In parallel with the efforts on the III-V nano-ridge devices on Si, a study on selective area growth for III-V integration on Si was pursued. Wide-field grown InGaAs devices on Si were examined to directly integrate III-V active materials onto silicon photonics platforms at the circuit layer. While III-V nano-ridges grown on Si still require a new optical coupling scheme to be developed to redirect the optical path to the Si level, this approach can offer a shortcut for the coupling issue. Additionally, the wide-field grown method facilitates easy integration into a standard Si photonics process flow, allowing for electrical contacting through Si. Moreover, it provides versatility, as different III-V active material combinations can potentially be grown on the same wafer.

In this effort, InGaAs was grown on V-groove shaped openings etched on wide

Si rib waveguides patterned on SOI wafers. The In compositions were varied to target a bandgap with 1600 nm wavelength, suitable for electroabsorption modulator (EAM) applications. Additionally, higher In compositions were also targeted for photodetection. Unfortunately, in this early trial, the InGaAs device performances were limited by the quality of the grown material. The insertion loss spectra did not exhibit sharp band-edges for the targeted EAM demonstration with 47% In composition rate. Instead, the insertion loss was smeared throughout the spectra. The grown material exhibited ternary compound composition inhomogeneities, confirmed by scanning transmission electron microscopy (STEM) with energy dispersive X-ray spectroscopy (EDS) metrology. Additionally, the devices showed low performance for photodetection, limited by dark current, indicating high defect densities.

This wide-field grown InGaAs on Si study underscored the crucial significance of epitaxially-grown material quality. It demonstrated that more exhaustive growth studies are necessary to achieve sufficient material quality and homogeneity while maintaining low defect densities.

Conclusion

In conclusion, the work presented in this dissertation demonstrated high-quality InGaAs/GaAs multiple quantum well (MQW) nano-ridge waveguide photodetectors heteroepitaxially grown on Si. They exhibited record-low dark currents of 0.05 pA, corresponding to a dark current density of 1.98×10^{-8} A/cm^2 at a bias of -2 V. These devices achieved a responsivity of 0.65 A/W and a quantum efficiency of 79% at a wavelength of 1020 nm. However, their high-speed performance was limited by their RC bandwidth. A study at elevated temperatures revealed that leakage mechanisms were dominated by SRH-type bulk and surface leakages. Simulated dark currents suggested that actual dark currents could be more than one order of magnitude lower than the noise-limited room-temperature measurements.

A separate study to integrate InGaAs directly on a silicon photonics platform revealed that the quality of the active material is paramount for achieving record-breaking device performances. This study underscored the huge potential of III-V nano-ridges on Si, extending the capabilities of silicon photonics platforms to meet future challenges.

References

[1] Cenk Ibrahim Ozdemir, Dries Van Thourhout, Yannick De Koninck, Didit Yudistira, Marina Baryshnikova, Nadezda Kuznetsova, Bernardette Kunert, Marianna Pantouvaki, and Joris Van Campenhout. *Constructing III-V Nano-ridge Photodetectors on Silicon*. Compound Semiconductor, (V), July 2021.

1 Introduction

The advent of the information age has brought about an exponential increase in digital content creation and communication. Alongside the most recent advancements in generative artificial intelligence (AI), the volume of data being created, processed, and shared has reached a scale where capacity becomes hardware-limited. One critical limitation arises from the fact that computational capacity growth per unit area of electronic chips stagnates compared to the growth of the data computation need. While this issue is being addressed by increasing the number of computational chips, racks, and data centers, interconnectivity between them becomes bandwidth-limited, and, most importantly, power-limited, as shown in Fig. 1.1. This places photonics in the spotlight as a potential solution to the interconnectivity problem.

The information age began with the invention of the first transistor in 1947 and the first integrated circuit (IC) in 1958. The number of transistors in IC chips has grown exponentially while the size of each transistor has gotten smaller and smaller. The growth of the number of transistors on a chip was projected by Intel's co-founder and then-president Gordon Moore in 1975 to double every two years [2]. Electronic devices have permeated every aspect of our lives, becoming indispensable tools. The exponentially reduced costs and the interconnectedness of these devices, facilitated by the invention of the internet, have integrated them into every conceivable tool, appliance, vehicle, and more, that shapes every aspect of our lives. The proliferation of connected devices, increasing internet usage, and the emergence of technologies such as the Internet of Things (IoT), generative AI (GenAI), and Big Data analytics are driving exponentially growing demand

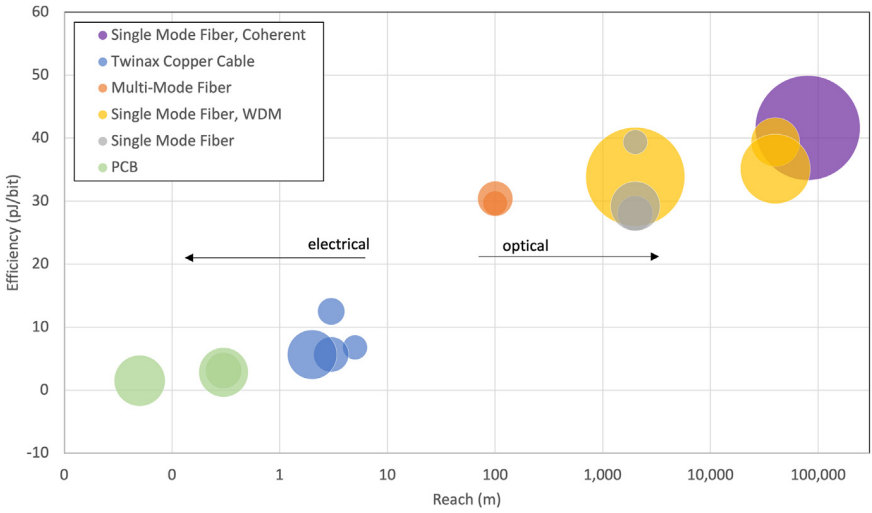


Figure 1.1: The energy per bit efficiency versus reach of the electrical and optical interconnects available today. The size of points is relative to interconnect bandwidth per system. While the reach and bandwidth of optical interconnects are superior to electrical ones, their power efficiency gap creates a challenge. Reproduced from Stone et al. (2023) [1].

for data communications. This escalating demand poses significant challenges to traditional communication networks, necessitating innovative solutions to accommodate higher data rates while reducing power consumption and costs.

This progression mirrors the historical evolution of communication technologies, including optical communications. The earliest forms of optical communications date back to ancient civilizations, where smoke, fire, or flags were used to convey signals. The use of light in free space continued into the 19th century with the introduction of limelight signal lamps in naval and ground communications. The discovery of telegraphy and radio enabled long-distance communications from the 19th century until today. Both wired and wireless electrical communications experienced exponential growth during this period but eventually encountered the physical bitrate-distance limits for long-distance communications.

The modern-era form of optical communications evolved from the invention of the first laser in 1960 [3], which was based on preceding theoretical and applied work on masers. Parallel ongoing research and development efforts on laser diodes and optical fibers enabled optical communications through confined optical fiber media. Optical fibers were manufactured with progressively reduced optical losses through process improvements, while laser diodes were made more compact and power-efficient. Alongside the use of laser diodes as optical power sources, discrete components such as optical amplifiers, modulators, and detectors were

introduced to complete the optical communication circuitry.

With the advent of public internet use in 1989 and the exponential growth that followed, optical fiber communications aligned with this upward trend. The introduction of optical amplifiers and wavelength-division multiplexing (WDM) further expanded the capabilities of optical communications across short, medium, long, and very long submarine ranges, thus heralding the emergence of optical networking. In the realm of optical communications, optical networking encompasses bandwidth and capacity management strategies within the optical frequency spectrum, as well as the integration of optical line systems into legacy networking architectures.

The early forms of optical communication components were bulky and often relied on free-space optics before significant advancements in fiber optics were achieved. As a result, the resulting circuitry was susceptible to temperature gradients, mechanical vibrations, and acoustic noises. In 1969, S. E. Miller and several colleagues at Bell Labs introduced the concept of an integrated photonic circuit, which utilized glass optical waveguides [4, 5].

1.1 A Brief History of Optical Communications

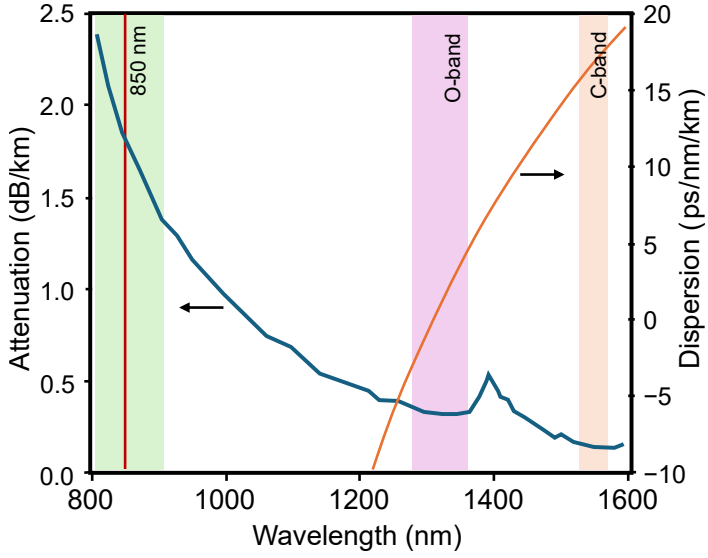


Figure 1.2: The attenuation and dispersion spectra of a typical single-mode SMF-28 type optical fiber overlayed with key optical communication band ranges. Reproduced from Hill et al. (2021) [6].

After the invention and demonstration of lasers in 1960, the proposal to uti-

lize optical fibers as transmission media for optical communications emerged in 1966 [7]. Similar to electrons in copper wires, laser light can be transmitted through optical fibers. However, early optical fibers suffered from high losses, exceeding 1000 dB/km. It wasn't until the 1970s that significant advancements were made, reducing the losses to below 20 dB/km. Concurrently, in the 1970s, continuous-wave (CW) room temperature (RT) operating GaAs lasers were also developed. These simultaneous advancements in light sources, discrete components, and optical fibers catalyzed a global effort in optical communications that spanned decades and multiple generations of development [8]. Over this period of more than four decades, the bit rate-repeater distance product (B.L) doubled every year on average.

The first generation of optical communications began with systems comprising 850 nm GaAs lasers and multimode fibers, which became commercially available in 1980. These systems operated at a bit rate of 34-45 Mbit/s and had repeater spacings of up to 10 km.

The second generation occurred with the transition of operation wavelength to the 1310 nm (O-band) range, as shown in Fig. 1.2, where optical fibers exhibited losses below 1 dB/km and near-zero chromatic dispersion. This transition was facilitated in the early 1980s by the introduction of quaternary InGaAsP lasers and detectors capable of operating in that wavelength range. Concurrently, the development of single-mode fibers significantly reduced dispersion compared to multimode fibers. By 1988, second-generation lightwave systems achieved bit rates of up to 1.7 Gbit/s with repeater spacings of 50 km.

The third generation of optical communications primarily involved a shift in the operation wavelength to 1550 nm, where fiber losses were minimal, reaching levels as low as 0.2 dB/km. This improvement in fiber loss led to an enhancement in B.L product. To overcome fiber dispersion at 1550 nm, dispersion-shifted fibers were introduced, utilizing periodic intervals of negative dispersion fiber sections to compensate for the positive dispersion at this wavelength. During this generation, optical transmission systems capable of bit rates up to 4 Gbit/s over distances exceeding 100 km were demonstrated [9]. Additionally, coherent lightwave systems were formulated and proposed, incorporating homodyne or heterodyne detection schemes [10]. Although these architectures could significantly improve the receiver sensitivity and repeater spacing, it took two generations to employ them.

The fourth generation was brought with the use of fiber amplifiers, improving the repeater spacing and the introduction of WDM, helping to scale bit rates of lightwave systems. In 1995, the data transmission on a single wavelength with 5.3 Gbit/s bit rate and 11300 km distance was reported by using erbium-doped fiber amplifiers (EDFA) [11]. For the WDM applications, the International Telecommunication Union (ITU) standardized the optical frequency channel spacing as 50-GHz and defined the low-loss wavelength range of 1530-1565 nm as C-band

(C refers to conventional). The adjacent bands are called S-band (S for short wavelength) and L-band (L for long wavelength) for the wavelength ranges of 1460-1530 nm and 1565-1625 nm, respectively. In a 2001 study, the WDM was employed in a 10.92-Tb/s transmission over 117 km, operated with 273 40-Gbit/s channels distributed in S-, C-, and L-bands [12]. The evolution of the bit-rate distance product over these four generations is shown in Fig. 1.3.

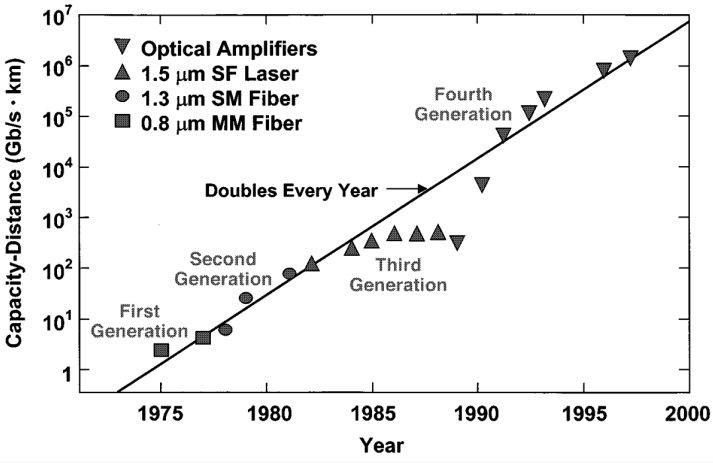


Figure 1.3: The bit rate - distance product evolution of lightwave systems over first four generations. Reproduced from Kogelnik [13].

The efforts in the fifth and future generations have mainly focused on increasing the capacity transmitted over an optical fiber. These efforts include [14]:

1. Increasing the number of optical frequency channels by reducing channel spacing for dense wavelength-division multiplexing (DWDM),

2. Extending the operation beyond the C-band into S- and L-bands by utilizing different amplification schemes including Raman amplification,

3. Enhancing the bit rate of each channel by utilizing different modulation formats, encoding and forward error correction (FEC), and employing coherent receiver architectures.

1.2 Integrated Photonics

Photonics literally means ”pertaining to photon”, the elementary quantum unit of electromagnetic fields, such as light and radio waves. It encompasses the field of

science and technology of harnessing light [15]. This field includes light generation, detection, and management through processes like guidance, modulation, attenuation, and amplification. Moreover, it encompasses any application or product that relies on manipulated light for its operation. Integrated photonics, a sub-field of photonics, involves the development of solid-state devices that combine passive or active (or both) photonic capabilities on a single substrate.

Since the conceptualization of integrating photonic components on a single substrate in 1969 [4], progress on photonic integrated circuits (PICs) has been slow compared to electronic integrated circuits, which have followed an exponential growth trajectory outlined in Moore's Law [2]. By 1977, when P. K. Tien of Bell Labs detailed the early progress on integrated photonics (then termed integrated optics) in his review paper [16], he highlighted persistent challenges faced by PICs. These included issues such as optical coupling in and out of the chip, integrating various functionalities across different material systems, and minimizing optical losses within the chip. Additionally, achieving a comprehensive suite of active and passive photonic capabilities remained a challenge due to the requirement for different material combinations.

1.2.1 Early III-V Active Photonic Components

The fundamental building blocks of an optical circuit are active elements such as light sources (e.g., light-emitting diode (LED), laser), light modulators, detectors, and passive elements like waveguides, couplers, and mirrors. More elements with different functionalities are also needed in complex optical communication systems, such as amplifiers, attenuators, multiplexers/demultiplexers, phase shifters, and so on. Before integrating all functional components on PICs, individual optical devices were invented and used as discrete components. Over different development generations, III-V based photonic platforms converged to InP substrates. InP is located approximately at the center of lattice constant and bandgap space (shown in Fig. 1.4), which makes it versatile to serve as a substrate to different ternary and quaternary III-V active materials developed with bandgap engineering.

The discovery of the first p-n junction in Si followed the observation of the photovoltaic effect in 1941 [18], which marks the date of the first solid-state based optical device and photodetection. First III-V based indium antimonide (InSb) photodetectors were developed in 1959 [19]. It took almost three decades to introduce the waveguide photodetectors, which were demonstrated in 1986 [20].

The first solid-state based optical modulators date back to 1962, demonstrated in a non-public military research study on calcite crystals used in electro-optic phase modulation employing the Pockels effect [21]. The first publicly reported solid-state optical modulators were demonstrated in 1966 on GaAs p-n junctions, where electro-absorption modulation (EAM) was achieved by employing the Franz-

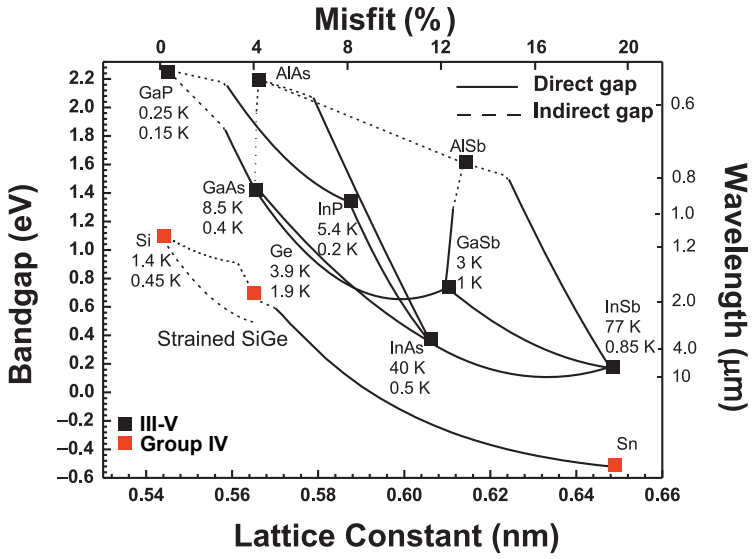


Figure 1.4: The lattice constant and the bandgap map of Si, III-V binary compounds, Ge, and Sn, labeled as black and red squares, indicating III-V compounds and group IV elements, respectively. The top lattice misfit percentage axis is referenced to the Si lattice constant. The lines between III-V binary compounds are ternary or quaternary combinations. Solid and dashed lines indicate a direct and indirect bandgap combination, respectively. The right wavelength axis is the corresponding wavelength of the bandgap axis. The numbers below each point indicate the electron and hole mobilities, in $cm^2/V.s$. Reproduced from Liu et al. [17].

Keldysh (FK) effect [22]. It took almost two decades to introduce EAM on an InP platform in 1984 [23]. The EAM exhibits a particular drawback of frequency chirping of the modulated signal. Per Kramers-Kronig relations, any changes in imaginary index (k) for EAM, also affect the real index (n) of the material, resulting phase modulation. Interferometer-based modulators were proposed to circumvent this problem [24], which incorporates phase modulators in interferometers to modulate intensity. The creation of Mach-Zehnder interferometer type modulators (MZM) was enabled by the demonstration of self-images constructed in multimode optical planar waveguides [25]. This has enabled not only the MZMs but also different passive photonic elements such as filters and waveguide couplers/splitters. The first optical interferometer-based MZM was demonstrated on the GaAs platform in 1984 [26], and later on the InP platform in 1989 [27].

Already before the conceptualization of integrated photonics, the first semiconductor lasers had emerged. A laser consists of two reflective structures creating an optical cavity and a gain media in between that is capable of enough carrier inversion to enable stimulated emission. The double heterostructure laser was initially

proposed by H. Kroemer in 1963 [28] and realized by Z. L. Alferov in 1969 [29]. It was based on an AlAs/GaAs heterostructure and achieved CW lasing at room temperature. This pioneering development earned them the Nobel Prize in Physics in 2000 [30]. The discovery of III-V based solid-state lasers was also the start of a period when a huge emphasis and effort was put on the use of advanced III-V based material systems in photonic applications, as mentioned earlier for photodetectors and modulators.

Although two cleaved facets of a semiconductor device can work as mirrors and form a Fabry-Perot cavity, this configuration does not allow such lasers to be integrated into a PIC. This limitation was addressed by a laser design proposal in 1971, which utilized the feedback of distributed Bragg gratings that reflect backward [31]. This architecture is known as a distributed feedback (DFB) laser. The first semiconductor DFB lasers were demonstrated in 1974 [32], with electrically-pumped continuous-wave room temperature operation achieved in 1975 [33]. The first longer wavelength InP-based DFB lasers were demonstrated in 1981, operating under pulsed conditions at 1.55 μm wavelength [34], and under continuous-wave operation at 1.57 μm wavelength [35].

Dingle et al. observed quantum effects in the optical absorption spectra of very thin GaAs layers sandwiched between higher bandgap AlGaAs compounds in 1974 [36]. This observation laid the foundation for quantum well lasers constructed with very thin gain media [37]. Developments in metalorganic vapor-phase epitaxy (MOVPE) growth controls and techniques further enabled high-quality growth of multiple quantum wells (MQWs) and additional functionalities [38]. The first electrically-pumped quantum well (QW) lasers operating at 77 K were demonstrated in 1977 [39], utilizing liquid-phase epitaxy (LPE). Additionally, in 1979, MOVPE was utilized to demonstrate room-temperature continuous-wave QW laser diodes [40]. Quantum confinement of carriers in QW lasers improves effective carrier inversion and reduces threshold current, temperature sensitivity, and free-carrier absorption by minimizing the active volume required. Consequently, the introduction of quantum wells in lasers dramatically improved laser performance metrics such as higher output power and lower power dissipation.

The implementation of wavelength multiplexing/demultiplexing, a technique known as wavelength-division multiplexing (WDM), has enabled the increase of optical communication bandwidth within a single channel. The development of phased array waveguides [41] paved the way for the conception of arrayed waveguide gratings (AWGs) in 1991 [42]. Subsequently, the first InP-based AWG was demonstrated in 1992 [43].

The increased use of WDM and the introduction of dense wavelength-division multiplexing (DWDM) in optical networks brought about the necessity for wavelength tunability of laser sources. Reconfigurable optical add-drop multiplexer (ROADM) architectures were introduced to optical networks in the late 1990s,

which also led to the introduction of various wavelength-tunable solutions. These solutions included DFB laser arrays, external cavity-tuned lasers, micro-electromechanical system (MEMS) tuned vertical-cavity surface-emitting lasers (VCSELs), and sampled-grating distributed Bragg grating (SG-DBR) lasers [44].

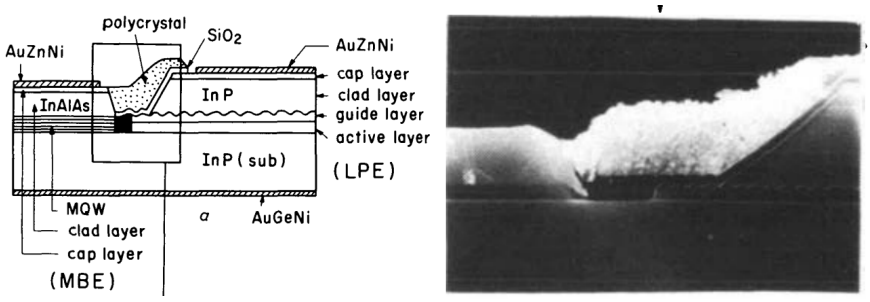


Figure 1.5: The first monolithic integration of InGaAs/InAlAs MQW modulator with an InGaAsP/InP DFB laser, reproduced from Kawamura et al. (1986) [45].

Almost a decade after Tien's review of Bell Labs' efforts, Y. Kawamura and others reported the first integrated photonics chip containing two active photonic functionalities in 1986 [45], [46]. This chip, as described in [45], comprised an InGaAsP/InP distributed-feedback laser and an InGaAs/InAlAs MQW EA modulator. The laser and modulator were grown on an InP substrate through separate epitaxial processes, and the devices were later coupled with a polycrystal, as shown in Fig. 1.5.

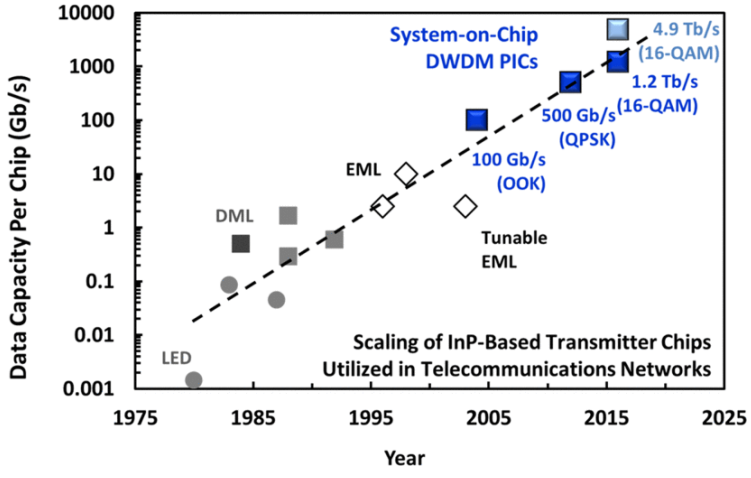


Figure 1.6: The evolution of the data capacity per InP-based transmitter PICs per year. The capacity per PIC has doubled an average of every ∼2.2 years. Reproduced from Kish et al. (2019) [47].

Accompanied by rapid advancements in both active and passive element integrations, InP-based PICs have experienced significant growth over the following years and decades. As depicted in Fig. 1.6, the evolution began with simple LED transmitters, and InP circuits continued to progress with the introduction of directly modulated lasers (DML), externally modulated lasers (EML), tunable lasers, and so forth. Over time, data rates have, on average, doubled every 2.2 years [47].

1.2.2 Dawn of Silicon Photonics

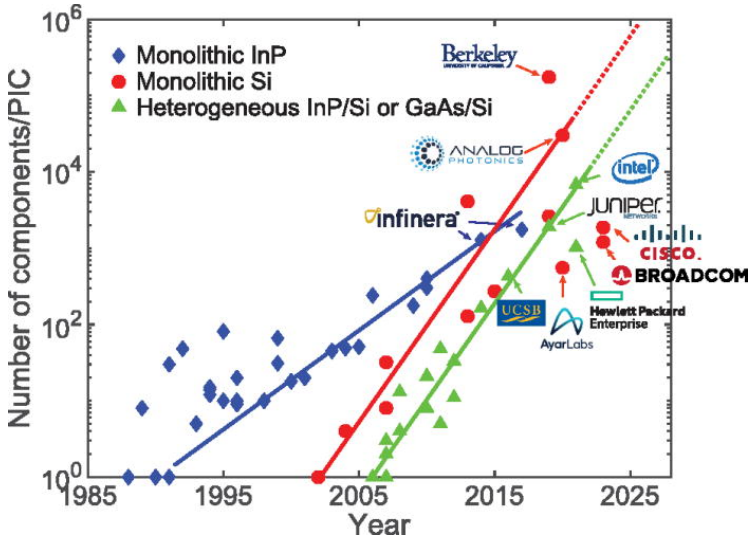


Figure 1.7: The evolution of the components per PIC over the years for different PIC platforms: InP, Si, and III-V on Si. Reproduced from Margalit et al. (2021) [48].

In 1985, R. A. Soref and J. P. Lorenzo proposed the use of silicon as the material platform for integrated photonics [49, 50]. Initially, this concept was demonstrated with rib waveguides etched on epitaxially grown intrinsic silicon on a heavily n-type doped silicon substrate. The difference in doping enabled the support of optical modes in the waveguides by leveraging the refractive index contrast between doped and undoped silicon. Subsequent studies explored various silicon-based waveguide formations, including silicon-on-sapphire (SOS) [51], silicon-on-insulator (SOI) [52], and silicon-germanium (SiGe) grown on silicon [53].

Out of these approaches, SOI prevailed in terms of mode confinement, optical losses, and versatility. Over the last several decades, SOI-based silicon photonics PIC capabilities have been significantly extended to include passive elements such as waveguides, interferometers, splitters [54], ring resonators [55], AWGs [56], polarization management devices [57], grating couplers [58], and more.

Over the years, the complexity and the number of components in each silicon PIC have rapidly grown, surpassing those of InP-based platforms, as depicted in Fig. 1.7.

The only active photonic capability of silicon at optical communication bands is modulation. Optical modulation in silicon has been achieved through various methods. Soref and Bennett formulated the free-carrier plasma dispersion effects in silicon in 1987 [59]. The earliest demonstrations of modulators in silicon utilized this effect in a free carrier injection type of operation in p-i-n diode waveguide architecture. Initially, modulation speeds were in the megahertz range [60], which were later improved to the order of gigahertz in a ring resonator architecture [61].

In 2005, the first carrier depletion type silicon modulator devices were introduced [62], employing a p-n junction waveguide where the depletion region is centered at the peak of the optical waveguide mode. These devices can achieve modulation speeds in the range of tens of gigahertz [63–65], but they require longer device lengths in the order of millimeters to achieve higher extinction ratios (ER).

Both carrier injection and depletion architectures rely on the free carrier dispersion effect, which influences the real and imaginary components of the silicon refractive index. However, it is more efficient to utilize the phase modulation effects of real index changes (Δn). Intensity modulation is then implemented either in the Mach-Zehnder interferometer (MZI) or ring resonator structure.

1.2.2.1 Extending Silicon Capabilities with Other Materials

The lack of a direct bandgap inherently limits silicon's ability to perform optical generation and amplification. Additionally, its transparency within telecom operation wavelengths also limits silicon's use as a photodetector. Therefore, various approaches have been pursued, including the integration of different material systems onto silicon, such as III-V, germanium (Ge), silicon-germanium (SiGe), barium titanate ($BaTiO_3$ or BTO) [66], lithium niobate ($LiNbO_3$ or LN) [67], graphene [68–73], and electrooptic (EO) polymers [74], among others. Among all materials, SiGe and III-V integration on silicon have received significant attention and effort over the span of decades.

Ge-on-Si and GeSi-on-Si integration have been pursued after decades-long developments on these material platforms in the electronics industry. As another group-4 element, Ge exhibits a pseudo-direct bandgap property, where the direct (Γ-valley) to indirect (L-valley) energy difference is 0.14 eV, in comparison to 2.28 eV of Si. Due to this small difference in bandgap energy, various techniques have been employed to engineer Ge's bandgap to make it a direct-gap material suitable for light generation. These techniques include the introduction of tensile strain, doping with n-type dopant materials, and/or alloying with Sn [75].

Beyond light generation efforts with Ge, Ge or SiGe materials monolithically

integrated on Si have been utilized to construct electroabsorption type modulators, either employing the Franz-Keldysh (FK) effect [76] or the quantum-confined Stark effect (QCSE) [77]. Ge has been also integrated on Si for realizing C-band and O-band photodetectors in p-i-n diode configurations [78, 79], or in avalanche photodetector (APD) architectures [80].

The active photonic capabilities of III-V based devices have prompted their integration into Si photonics platforms, primarily for light generation and amplification, but also for modulation and detection. Various methods have been explored to integrate III-V material system-based functionalities onto Si, including flip-chip bonding of pre-fabricated devices [81, 82], heterogeneous integration of externally grown III-V layers through die-to-wafer bonding [83, 84], or heteroepitaxy of III-V layers on Si, either as blanket layers [85–91] or through selective-area epitaxial growth [92–97]. The state-of-the-art monolithic III-V on Si integration approaches are detailed in Chapter 2.

Monolithic integration of III-V devices on Si in a CMOS-compatible process line can potentially offer high throughput and lower cost compared to other bonding schemes like flip-chip or die-to-wafer bonding. Various efforts have been made to monolithically integrate III-V photonic devices on large industry-scale 300-mm Si wafers [98–104]. Among all the monolithic integration approaches, III-V nanoridges grown on 300-mm Si wafers have been demonstrated to have very low defect densities, less than 1×10^{-6} cm^{-2}, the control of the waveguide geometry, and the capability to encompass desired III-V device layers.

1.2.2.2 Photodetectors on Silicon Photonics

Photodetectors (PDs) are key components in optical communications. Since the early days of integrated photonics in optical communications, photodetectors have been integrated into PICs to complete the receiver-end of optical communication circuits. Legacy III-V PIC platforms have integrated III-V photodetectors since the 1980s, operating with high responsivity and bandwidth in optical communications bands, and exhibiting low dark currents. Since the introduction of silicon photonics, significant efforts have been made to achieve similar photodetection capabilities at telecom wavelengths on silicon.

Photodetectors for optical communications have three critical performance metrics: dark current, responsivity, and bandwidth. Apart from these, there are other important metrics and factors to consider, such as platform compatibility, reliability, bias voltage, power, and operating temperature. Dark current is generated by leakage mechanisms in the material due to defects and impurities, and it is crucial in signal-to-noise ratio (SNR) limited applications. Responsivity is the ratio of photocurrent generated per optical power and formulated as:

$$R = I_{photo}/P_{opt} \tag{1.1}$$

which can be used to calculate quantum efficiency (η) of a PD:

$$\eta = Rh\nu/q \tag{1.2}$$

where h is the Planck constant, ν is the frequency of the optical signal, and q is the elementary electron charge. The bandwidths of PDs are typically limited by the resistor-capacitor (RC) constant and the carrier transit-time. The overall 3-dB bandwidth of a PD device can be calculated as [105]:

$$f_{3dB} \sim \frac{1}{2\pi}\sqrt{\frac{1}{\tau_{RC}^2 + \tau_T^2}} = \sqrt{\frac{1}{1/f_{RC}^2 + 1/f_T^2}} \tag{1.3}$$

where τ_{RC} and τ_T are RC and transit-time constants, respectively, f_{RC} and f_T are RC and transit-time bandwidths, respectively. The RC bandwidth is calculated with:

$$f_{RC} = \frac{1}{2\pi C_{PD}(R_{PD} + R_{load})} \tag{1.4}$$

where C_{PD} is the PD capacitance, R_{PD} is the PD resistance, and R_{load} is the external load resistance on the PD electrical circuit. The transit-time bandwidth is primarily driven by the carrier velocity (υ) in a given material system, which is governed by carrier mobilities (μ) and electric field (E) formed in the device to extract carriers. The transit-time bandwidth (f_T) for a given carrier transit distance (d) can be calculated with:

$$f_T = \frac{\sqrt{2}\mu E}{\pi d} \tag{1.5}$$

Silicon's transparency within telecom operation wavelengths limits its use as a PD. Therefore, different material systems and techniques have been studied to integrate PDs on silicon for various applications. These categories of PDs include: Ge [79, 106–111], GeSn [112–114], 2D [72, 115–120], and III-V [83–97] materials integrated on Si.

Germanium has a narrower bandgap than silicon, making it a potential absorption material for photodetectors operating at O- and C-band wavelength ranges. Due to the CMOS-line compatibility of germanium, various monolithic integration techniques have been implemented, and it has been widely used to construct photodetectors on silicon photonics platforms since the 2000s. State-of-the-art germanium photodetectors on silicon have exhibited high performance, including responsivities as high as 1.19 A/W at 1550 nm wavelength [109], dark current densities as low as 12.8 mA/cm^2 [110], and bandwidths as high as 265 GHz [111].

While germanium photodetectors on silicon have been demonstrated with high performances and have been utilized in current commercial silicon photonics platforms, their operation wavelength range is limited. For applications beyond the germanium absorption band edge of 1610 nm, germanium photodetectors cannot be used. Additionally, germanium photodetectors on silicon exhibit significantly

Parameter	Ge	GeSn	2D	III-V
Responsivity	High	Low	Low	Very High
Bandwidth	High	Low	High	Very High
Dark Current	High	High	Very Low	Very Low
Operation Wavelength	Limited	Extendable	Extendable	Extendable
Co-integration w/ III-V	Limited	Limited	Limited	Possible
Process Maturity	High	Low	Low	Low
CMOS-compatibility	High	Medium	Low	Medium

Table 1.1: Comparison of photodetectors based on different materials monolithically integrated on Si.

higher dark current densities compared to III-V PD devices on silicon. The integration of germanium on silicon can be further limited in cases of co-integration of III-V materials on silicon, as germanium will limit the addition of III-V based monolithic devices.

To extend the operation wavelength of germanium beyond the C-band, tin (Sn) can be added to form a germanium-tin (GeSn) alloy in bulk or QW form. GeSn on silicon has been studied as a prospective absorption material for photodetectors [112–114]. Although the operation wavelength has been extended in these studies, devices were limited in responsivity, bandwidth, and dark current performance.

In parallel, 2D materials such as graphene and metal dichalcogenides have been integrated on silicon as potential absorption materials due to their zero bandgap characteristics. Although they have been demonstrated with very low dark currents and high bandwidths, their responsivities were mostly limited [72, 115–120].

The material systems integrated on Si for photodetectors are compared in Table 1.1. In comparison with other material systems, III-V materials offer a wide design space and versatility. Desired III-V layer combinations with different bandgap characteristics can be grown for various application needs and operation wavelengths. This enables III-V based light source integration on silicon along with other active devices, such as modulators and photodetectors. The higher absorption coefficients of III-V compounds can potentially improve the responsivities of III-V photodetectors compared to germanium photodetectors. Higher carrier mobilities can further remove limits on transit time-limited bandwidths, as very high-speed unitraveling-carrier (UTC) photodetectors with 310 GHz bandwidth were demonstrated on an InP platform by Ito et al. in 2004 [121]. The epitaxial growth techniques have been tremendously improved over several decades, and the same learnings can be applied to III-V on silicon implementations for high-quality growth and low dark currents. The legacy and know-how accumulated in the III-V photonic platforms offer a large set of unprecedented opportunities to extend the capabilities of silicon photonics.

1.3 Thesis Motivation and Outline

The objective of this thesis is to enhance the capabilities of silicon photonics platforms by integrating active III-V devices. This involves pursuing the monolithic integration of III-V devices on silicon to introduce high-performance active photonic capabilities. Specifically, we study and demonstrate nano-ridge waveguide photodetectors on silicon, fabricated using aspect ratio trapping (ART) and nano-ridge engineering (NRE). Additionally, we assess the quality of the grown material of the nano-ridge waveguide devices by extracting various leakage mechanisms through elevated temperature studies. In parallel, we experiment with direct selective area growth of III-V material on an existing silicon photonics platform to achieve active modulation and photodetection capabilities directly on the same platform. This dissertation is structured into seven chapters. The current chapter, Chapter 1, has provided a detailed exploration of the historical advancements in optical communications, the III-V photonic devices, integrated photonics, and silicon photonics, as well as outlining the motivation and content of this thesis work.

Chapter 2 covers the monolithic integration of III-V on Si and the processing details of NRWPDs. It begins with an exploration of the critical challenges associated with the monolithic integration of III-V materials on silicon, including lattice and thermal expansion coefficient mismatches, as well as defect types and formation. This is followed by a detailed comparison of various monolithic integration approaches. The chapter concludes with an in-depth discussion of the steps involved in fabricating the InGaAs/GaAs NRWPD devices.

Chapter 3 focuses on the design of NRWPDs. It commences with an overview of the bulk absorption models utilized in this thesis, proceeding to discuss the geometric, optical, and electrical design steps, accompanied by simulations. The chapter concludes with the layout design of the NRWPDs and associated test structures.

Chapter 4 delves into the characterization of NRWPD devices, encompassing electrical, opto-electrical, and high-speed measurements. It culminates with a comprehensive benchmark study, comparing the NRWPDs with state-of-the-art photodetectors monolithically integrated on Si as reported in the literature.

Chapter 5 provides an extensive investigation into the leakage mechanisms of the NRWPDs to elucidate dark current performance and grown material characteristics. The study encompasses measurements at elevated temperatures and accompanying device simulations to extract different leakage mechanisms and their respective contributions to device dark currents.

Chapter 6 introduces another III-V on Si device architecture, termed wide-field grown devices, which were studied in this thesis work. The chapter briefly discusses the design, processing, and characterization of these devices, along with

reflections on why this approach encountered challenges and suggestions for potential further development.

Chapter 7 presents the conclusions drawn from this thesis work, along with perspectives and suggestions for future research directions. It provides a comparative analysis of the insights gained from both the development of high-performance NRWPDs and the investigation into low-yielding wide-field grown III-V devices on Si.

1.4 Awards and Publications

The work completed for this thesis dissertation has led to the following awards, and publications in international conferences and peer-reviewed journals.

1.4.1 Awards

1. Best student paper award (2nd place), European Conference on Optical Communication, December 2020
   For the paper: C.I. Ozdemir et al., 0.3pA Dark Current and 0.65A/W Responsivity 1020nm InGaAs/GaAs Nano-Ridge Waveguide Photodetector Monolithically Integrated on a 300-mm Si Wafer.

2. Best student paper award (1st place), IEEE Photonics Conference, September 2020
   For the paper: C.I. Ozdemir et al., InGaAs/GaAs Multi-Quantum Well Nano-Ridge Waveguide Photodetector Epitaxially Grown on a 300-mm Si Wafer.

1.4.2 Publications in International Journals and Magazines

1. **C.I. Ozdemir**, Y. De Koninck, S.K. Patra, M. Baryshnikova, B. Kunert, M. Pantouvaki, J. Van Campenhout, D. Van Thourhout, "Leakage Mechanisms of sub-pA InGaAs/GaAs Nano-Ridge Waveguide Photodetectors Monolithically Integrated on a 300-mm Si Wafer," J. Phys. D: Appl. Phys. vol. 57, no. 40, p. 405101 (2024).

2. ***(submitted)*** Y. De Koninck, C. Caer, D. Yudistira, M. Baryshnikova, H. Sar, P.-Y. Hsieh, **C.I. Ozdemir**, S.K. Patra, N. Kuznetsova, D. Colucci, A. Milenin, A.A. Yimam, G. Morthier, D. Van Thourhout, P. Verheyen, M. Pantouvaki, B. Kunert, J. Van Campenhout, "GaAs nano-ridge laser diodes fully fabricated in a 300 mm CMOS pilot line," Nature (2023).

3. Y. Kim, D. Yudistira, B. Kunert, M. Baryshnikova, R. Alcotte, **C.I. Ozdemir**, S. Kim, S. Lardenois, P. Verheyen, J. Van Campenhout, M. Pantouvaki,

"Monolithic GaAs/Si V-groove depletion-type optical phase shifters integrated in a 300 mm Si photonics platform," Photon. Res., vol. 10, no. 6, p. 1509 (2022).

4. ***(invited)*** **C.I. Ozdemir**, D. Van Thourhout, Y. De Koninck, D. Yudistira, M. Baryshnikova, N. Kuznetsova, B. Kunert, M. Pantouvaki, J. Van Campenhout, "Constructing III-V Nano-ridge Photodetectors on Silicon," Compound Semiconductor, vol. 27, no. 5, pp. 46–50 (2021).

5. ***(invited)*** **C.I. Ozdemir**, Y. De Koninck, D. Yudistira, N. Kuznetsova, M. Baryshnikova, D. Van Thourhout, B. Kunert, M. Pantouvaki, J. Van Campenhout, "Low Dark Current and High Responsivity 1020nm InGaAs/GaAs Nano-Ridge Waveguide Photodetector Monolithically Integrated on a 300-mm Si Wafer," J. Lightwave Technol., vol. 39, no. 16, pp. 5263–5269 (2021).

1.4.3 Publications in International Conferences

1. ***(invited)*** B. Kunert, D. Colucci, M. Baryshnikova, Y. Mols, R. Alcotte, D. Van Thourhout, **C.I. Ozdemir**, Y. De Koninck, M. Pantouvaki, J. Van Campenhout, A. Vais, S. Yadav, A. Sibaja-Hernandez, B. Parvais, N. Collaert, R. Langer, III/V Nano-Ridge Engineering for Device Integration on 300 mm Silicon, Compound Semiconductor Week, Sweden (2021).

2. ***(extended)*** **C.I. Ozdemir**, Y. De Koninck, D. Yudistira, N. Kuznetsova, M. Baryshnikova, D. Van Thourhout, B. Kunert, M. Pantouvaki, J. Van Campenhout, 0.3pA Dark Current and 0.65A/W Responsivity 1020nm InGaAs/-GaAs Nano-Ridge Waveguide Photodetector Monolithically Integrated on a 300-mm Si Wafer, European Conference on Optical Communication, Belgium (2020).

3. **C.I. Ozdemir**, Y. De Koninck, N. Kuznetsova, M. Baryshnikova, D. Van Thourhout, B. Kunert, M. Pantouvaki, J. Van Campenhout, InGaAs/GaAs Multi-Quantum Well Nano-Ridge Waveguide Photodetector Epitaxially Grown on a 300-mm Si Wafer, IEEE Photonics Conference, Canada (2020).

4. **C.I. Ozdemir**, S. Kim, N. Kuznetsova, A. Srinivasan, M. Baryshnikova, B. Kunert, M. Pantouvaki, G. Roelkens, D. Van Thourhout, J. Van Campenhout, Monolithic III-V Waveguide Photodetectors on Silicon, ePIXfab Silicon Photonics Summer School, Belgium (2018).

5. B. Kunert, M. Baryshnikova, Y. Mols, Y. Shi, D. Van Thourhout, N. Kuznetsova, S. Kim, **C.I. Ozdemir**, M. Pantouvaki, J. Van Campenhout, R. Langer, III-V photonic devices on Si, Joint ISTDM/ICSI 2018 Conference, Germany (2018).

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2
InGaAs/GaAs Nano-Ridges

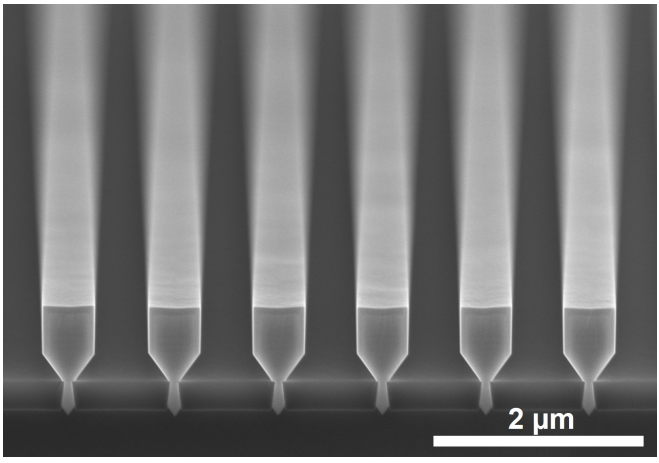

Figure 2.1: Tilted scanning electron microscopy (SEM) image of III-V nano-ridges grown on silicon [1].

Monolithic integration of III-V on silicon brings many opportunities for silicon photonics, but at the same time, it comes with its own challenges. For many years, researchers have worked on these challenges, which mainly arise from the differences between the two material systems. These differences involve the lattice constants, the thermal expansion coefficients, and the crystal structures of the materials.

In Chapter 1, we emphasized the need and importance of III-V integration on silicon. In this chapter, we detail the state-of-the-art monolithic integration methods. This includes the benefits and challenges of each method, in terms of different industrial merits. Further, we explain the growth of III-V nano-ridge devices, the main component of this thesis work. The nano-ridge growth employs two techniques: aspect ratio trapping (ART) and nano-ridge engineering (NRE). We explore the capabilities nano-ridges bring, as well as their design and other limitations within this thesis work.

2.1 Fundamental Challenges of III-V Heteroepitaxy on Silicon

Heteroepitaxy refers to the epitaxial growth of a layer on a foreign substrate, either with plastic relaxation (metamorphic growth) or without relaxation (pseudomorphic growth) [2]. Heteroepitaxy without relaxation is sustained with lattice-matching of grown layer, or with strain, or with both. Monolithic integration of III-V materials involves the heteroepitaxial growth of the III-V layers on silicon, which is a form of metamorphic growth. Compared to other integration methods employing bonding schemes, such as flip-chip or die-to-wafer bonding, III-V heteroepitaxy on Si suffers from large mismatches in lattice constants and thermal expansion coefficients, as well as differences in the crystal structures of the materials.

Fundamental differences between the two material groups, especially lattice mismatch, lead to stress formation during the growth process. After the critical layer thickness is surpassed, the built-up stress is relaxed through plastic deformations, resulting in misfit and threading dislocation defects. Any defect system in materials can cause non-radiative recombination, carrier scattering, or other inhomogeneities, leading to reduced device performance or failure. Therefore, achieving low defect densities is the primary goal of III-V heteroepitaxy on silicon.

2.1.1 Lattice Mismatch

The lattice-matched growth of various III-V compounds on III-V substrates, known as "pseudomorphic growth," is facilitated by ternary or quaternary III-V compound combinations. This method, called compound engineering, expands the design space by enabling different bandgap combinations while maintaining matched lattice constants with the III-V substrate. This design space is illustrated in Fig. 2.2. Consequently, a wide range of semiconductor devices has been realized using III-V compound engineering, demonstrating both innovative and commercial significance. However, the quality of epitaxial growth of III-V compounds on foreign substrates such as Si is severely limited due to lattice constant mismatches

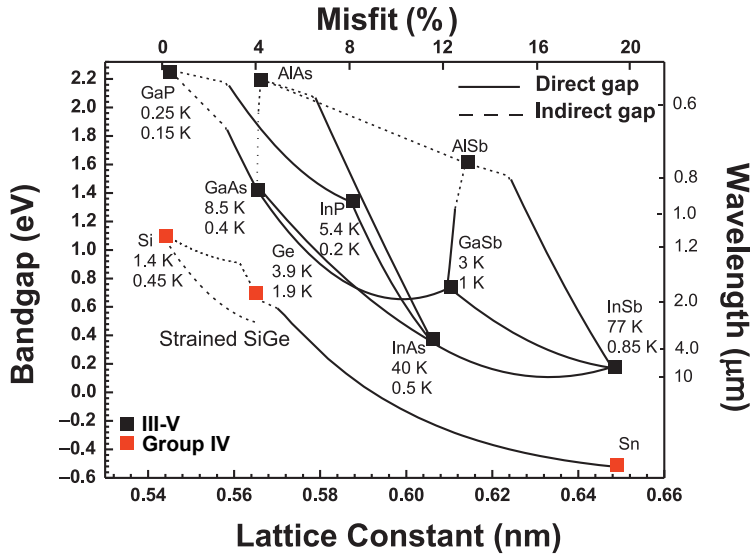

Figure 2.2: The lattice constant and the bandgap map of Si, III-V binary compounds, Ge, and Sn, labelled as black and red squares, indicating III-V compounds and group IV elements, respectively. The top lattice misfit percentage axis is referenced to the Si lattice constant. The lines between III-V binary compounds are ternary or quaternary combinations. Solid and dashed lines indicate a direct and indirect bandgap combination, respectively. The right wavelength axis is the corresponding wavelength of the bandgap axis. The numbers below each point indicate the electron and hole mobilities, in $cm^2/V.s$. Reproduced from Liu et al. [3].

between each material combination.

The lattice constant and bandgap map of Si, Ge and various III-V binary compounds are shown in Fig. 2.2. Compared to InP, Si has a smaller lattice constant of 5.431 Å, putting it away from other III-V compounds having bandgaps within standard telecom operation wavelength range of 1.3 μm to 1.6 μm. The misfit percentage shown in Fig. 2.2 can be calculated with:

$$\Delta\alpha = \frac{\alpha_{III-V} - \alpha_{Si}}{\alpha_{III-V}} \tag{2.1}$$

where α_{III-V} and α_{Si} are the lattice constants of Si and III-V compounds, respectively. A positive value of $\Delta\alpha$ will result in a compressive strain on the grown III-V layer, while a negative value will result in a tensile strain. The smaller lattice constant of Si than of most of III-V compounds result in compressive strain in most cases.

The lattice constant of ternary III-V compounds (α_{III-V}) can be calculated linearly based on the composition ratio, following Vegard's Law [4]:

$$\alpha(A_xB_{1-x}C) = \alpha(AC)x + \alpha(BC)(1-x) \tag{2.2}$$

where $\alpha(A_xB_{1-x}C)$ is the lattice constant of the $A_xB_{1-x}C$ ternary compound formed with AC and BC binaries. On the other hand, the bandgap of ternary compounds cannot always be linearly interpolated as can be observed through the bowed curves in Fig. 2.2. Therefore a second order bowing parameter should be added in the bandgap calculation:

$$E_g(A_xB_{1-x}C) = E_g(AC)x + E_g(BC)(1-x) - D_{ABC}x(1-x) \qquad (2.3)$$

where D_{ABC} is an empirical bowing parameter for the ternary combination of ABC. The bowing parameters are obtained through empirical calculations and interpolations based on different experimental results at various composition ratios [5]. The InGaAs QWs grown in the GaAs nano-ridges are targeted for composition ratios of 22% and 78% for In and Ga, respectively. Based on the equations 2.2 and 2.3, the lattice constant and bandgap of $In_{0.22}Ga_{0.78}As$ can be calculated as 5.74 Å and 1.091 eV, respectively, with D_{InGaAs} value of 0.555 [6].

2.1.2 Thermal Expansion Coefficient Mismatch

Along with the lattice mismatch, the differences in thermal expansion coefficients (CTE) challenges successful III-V growth on Si. The epitaxial growth occurring at a few hundreds of degrees above room temperature level, the device burn-in cycles, changes in operating temperatures can all bring additional material strain at the hetero-interface, resulting additional stress release via misfits and/or threading dislocations. The thermal expansion coefficients of Si, GaAs and InAs are 2.59×10^{-6} K^{-1}, 5.73×10^{-6} K^{-1}, and 4.52×10^{-6} K^{-1}, respectively. For InGaAs, the linear interpolation can be followed as in equation 2.2.

The higher thermal expansion coefficients of GaAs and InGaAs compared to Si may reduce the compressive strain due to the lattice mismatches and may even change the strain state. Fully relaxed GaAs at growth temperature deposited on Si substrates can be under tensile strain at room temperature. While lattice mismatches play the primary role in material stress, in the case of fully relaxed thick III-V buffer growth, TCE mismatch limits the maximum layer thickness. Beyond certain critical thicknesses dependent on the growth temperature, macroscopic crack formation is observed in thin III-V films grown on Si. Therefore, the critical thickness is inversely proportional to the temperature variation. For GaAs epitaxial layers grown on Si, the critical thickness is inversely proportional to the temperature variations. For the GaAs epitaxial layers grown on Si, the critical thickness is reported as 7 μm, for ΔT, the delta temperature during cooling after growth, of 575 °C. Meanwhile, for the ΔT of 725 °C, the critical thickness drops to 4.9 μm [7].

2.1.3 Anti-Phase Domains and Stacking Faults

The crystalline structures of Si and III-V compounds are different. Si, a group IV semiconductor, forms in a diamond structure, where each Si atom is bonded to four neighboring Si atoms in a tetrahedral arrangement. All bonding electrons are shared between the nuclei, resulting a non-polar material. For the III-V compounds, on the other hand, the two (or more for ternary or quaternary compounds) elements have different ionicity, resulting a polar bonds in the crystal formed in the zinc-blende structure.

The anti-phase domains (APDs) can occur any heteroepitaxial growth of polar materials on non-polar substrates. In the example of blanket growth of GaAs on planar (001) Si substrate, APDs arise from single or odd numbered steps of Si atoms on the surface as shown in Fig. 2.3. These APDs are classified as planar defects, consisting of undesired III-III or V-V bonds at the boundaries. These unusual III-III or V-V bonds create electrically charged planes and act as non-radiative recombination centers, which significantly affects the device performance.

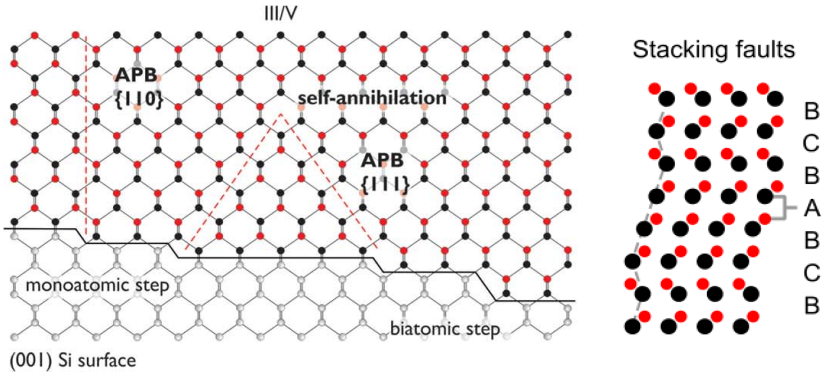

Figure 2.3: Graphical representations of anti-phase domains and stacking faults. (Left) Anti-phase domains of III-V compounds grown on (001) Si surface. Any odd numbered steps of atoms on the Si surface initiates the formation of anti-phase boundaries (APBs) between different domains, while a biatomic step does not induce any anti-phase boundary. (Right) BCBC bonding configuration is interrupted by a stacking fault resulting a bond A, deforming the ideal crystal stacking. Reproduced from Kunert et al. [8] and Du et al. [9].

Stacking faults are planar defects formed by addition or removal of one double atom $\{111\}$ plane [8]. III-V heteroepitaxy on Si is prone to the stacking faults in any case of surface damage, precipitates, or impurities on the hetero-interface. Therefore, Si surface cleaning and pre-treatment becomes very important for avoiding them.

2.1.4 Defect Types and Formation in III-V Heteroepitaxy on Silicon

Defects in semiconductors refer to any irregularities in the perfect crystal structure of the material. They can be classified as zero-, one-, two- or three-dimensional. Any singular, non-propagating point-defects, for example impurity atoms, vacancies, interstitials or anti-sites are zero-dimensional. Misfit dislocations (MD) occurring at hetero-interface and threading dislocations (TD) propagating from other defects are one-dimensional line defects. Stacking faults and anti-phase boundaries between APDs are two-dimensional planar defects. Twinned regions, grains, large precipitates, inclusions, voids, and foreign macro impurities are three-dimensional volume defects [8].

Zero-dimensional point defects are divided as intrinsic or extrinsic defects. Intrinsic point defects are vacancies or interstitials of the grown material. Extrinsic point defects are formed by any foreign impurities intentionally or unintentionally incorporated during the growth process. Improved growth techniques and precursor purities help reducing extrinsic defects. Extrinsic point defects can be also intentionally incorporated to change material properties for different applications.

MDs and TDs are classified as one-dimensional line defects. The epitaxial growth of lattice-mismatched III-V compounds on Si results in elastic strain energy. Once the pseudomorphic critical thickness, typically a few nanometers of III-V thin-film on Si, is exceeded, plastic relaxation occurs through dislocations. These dislocations can either form on the hetero-interface as MD lines or glide on the $\{111\}$ plane as TD lines. Dislocations on the top surface form TDs in a half-loop shape on the $\{111\}$ plane, then glide down to the hetero-interface and induce further MDs. Additionally, any pre-existing dislocation can also induce MDs on the hetero-interface. The formation and interaction between MDs and TDs are illustrated in Fig. 2.4 [8].

The dislocations are dynamic and can interact with each other through the growth process and the device lifetime. Individually, they can glide down, climb up, dissociate into partial dislocations, coalesce, annihilate, or repulse and multiply each other [8]. The main driving factors for dislocation dynamics are strain, stress, and temperature, which vary significantly during the growth process. Dislocation dynamics are also affected by point defects, doping, carrier injection, and illumination, which can vary widely during device formation and operational lifetime. Dislocations act as non-radiative recombination centers, contribute to carrier scattering, and induce inhomogeneities in devices, similar to other defects [2]. Therefore, dislocations can largely lead to device performance impairment, degradation, or failure over time.

The widely accepted metric for epitaxial growth quality is threading dislocation density (TDD), measured in cm^{-2}, which represents the density of threading dislocations on a unit area of epitaxial growth. TDD can be measured using

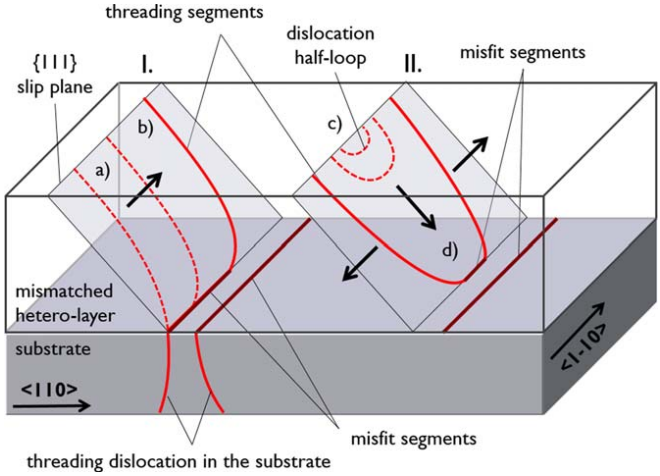

Figure 2.4: Interaction between TDs and MDs. In (I), TDs glide along MD line from (a) to (b). In (II), TD half-loop is formed starting from the TD nucleation at the surface gliding down to the hetero-interface, forming additional MDs. Any TDs in the substrate can induce further MDs and TDs in the grown layer. Reproduced from Kunert et al. [8].

different methods, including etch-pit density measurement, x-ray diffraction, and transmission electron microscopy (TEM) [9]. Commercial substrates such as Si, Ge, GaAs, and InP have very low TDD values of approximately 0 cm^{-2}, less than 3×10^2 cm^{-2}, less than 5×10^3 cm^{-2}, and less than 6×10^4 cm^{-2}, respectively [2]. These high-quality substrates have enabled the fabrication of well-performing optoelectronic devices grown with pseudomorphic epitaxy, where little to no lattice strain is involved during the growth process. However, metamorphic III-V epitaxial growth on Si has been significantly challenged by inherent lattice strain, prompting research into various epitaxial methods to reduce TDD while enabling full relaxation of the grown III-V material.

Two-dimensional planar defects can be formed with APDs and stacking faults, detailed in subsection 2.1.3. The interface of APDs is called anti-phase boundary (APB), which may create electrically charged planes. These planes act as non-radiative recombination centers and can interact with TDs. Stacking faults may exhibit a less destructive effect compared to TDs and APBs, since their atomic bonds are saturated and no dangling bonds are formed. But, their lattice distortion modifies the electronic band structure, affecting the device functionality.

2.2 Approaches for III-V Heteroepitaxy on Silicon

The epitaxial growth of III-V compounds on Si can be categorized into two main approaches: blanket growth and selective area growth (SAG). As the names sug-

gest, blanket growth involves epitaxial growth across the entire substrate surface, while SAG selectively applies epitaxy to predetermined locations on the substrate. Each approach has its own advantages and drawbacks, and both have evolved with unique growth techniques.

2.2.1 Common Defect Reduction Methods

The common defect reduction methods for both major approaches mainly focus on the Si surface preparation and structuring, III-V nucleation, and buffer layers. The use of buffer layers is implemented differently in both approaches, so it will be detailed separately in the following subsections.

The first common defect reduction method is Si surface preparation, which is crucial for high-quality III-V heteroepitaxy. This involves the removal of any foreign residues and native oxide from the surface. Various methods have been used, including thermal and chemical steps such as oxide etching to remove native oxide and re-oxidization cycles to eliminate foreign residues [10]. Another method involves silicate formation using a hot mixture of ammonium (NH_3) and nitrogen trifluoride (NF_3) to remove native oxide [11].

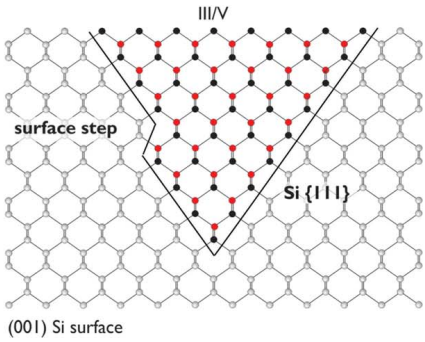

Figure 2.5: Graphical representation of III-V compound grown on {111} Si facet, where a monoatomic surface step on does not lead to an APB. Reproduced from [8]

The APBs occurring from monoatomic steps on (001) Si surface have been also targeted with different methods. These include chemical and thermal surface preparation steps to induce biatomic steps on the Si substrate surface. This was shown in [12], for a blanket growth of GaAs on (001) Si substrate with 0.15° crystal misalignment. Another approach is exposing {111} facets of Si via anisotropic etching of Si. Anisotropic etching forms a V-shape groove on Si (001) substrate, where the surfaces are {111} planes. The heteroepitaxial growth of III-V compounds on this surface cannot induce APBs, which eliminates this fundamental problem [8]. A sample III-V formation in V-grooves of Si with {111} facets is de-

picted in Fig.2.5. This method can be used in either blanket growth [13] [14] [15], or in SAG approaches [16].

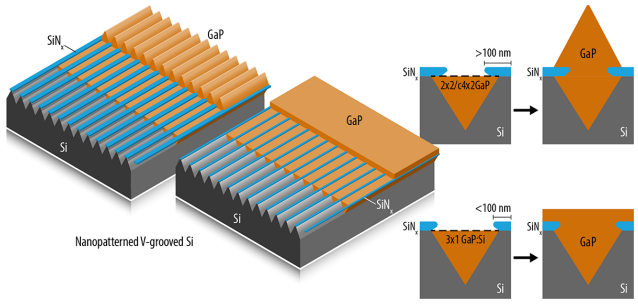

Figure 2.6: Schematics of GaP grown on V-groove Si with a $\{111\}$ diamond like SAG termination or a coalescence to a (001) flat blanket GaP surface, reproduced from [15].

2.2.2 Blanket Growth

Blanket growth refers to a uniform III-V layer epitaxy on all or a large substrate surface, where the grown material can be identified as a thin-film layer. Compared to SAG, blanket growth reduces the complexity of the growth procedures from two-/three-dimensional approach to one-dimensional. Grown material can be further etched in the consequent steps to form various device geometries, including waveguides.

For the blanket growth layers, the TDD is inversely proportional to the layer thicknesses [17]. Further increasing the grown layer thickness can reduce the defect density measured at the top of the layer. But, this approach can bring further difficulties, including the CTE mismatch induced wafer bowing and macro-crack formation described in the subsection 2.1.2, increased distance from the device functional Si substrate plane, increased material consumption, and higher fabrication costs. Therefore, the efforts in the blanket growth approach aim to reduce both defect densities and the layer thicknesses.

One approach is the increase of growth temperatures at various steps of the growth or implementing a thermal annealing after the growth steps are completed. It has been shown that the thermal annealing has reduced the TDs and APBs for a grown GaAs layer on Si [18] [19].

The utilization of buffer layers between the Si substrate and the grown III-V is one method introduced to reduce defect density. Germanium (Ge) has been used as a buffer layer for GaAs on Si blanket growth [20], offering better lattice matching conditions but increasing total thickness and introducing the Ge/GaAs interdiffusion problem. In Yu et al. [20], the interdiffusion of Ge into GaAs was suppressed by introducing an arsenide (As) prelayer. Along with the use of extrinsic buffer

layers, graded buffer layers have been studied, where the composition ratio varies in multiple steps from the least lattice-mismatched to the target composition of the III-V compound [21]. The slow variation of the lattice mismatch induces lower TDs through more relaxations via MDs between graded segments, thereby reducing TD nucleation and propagation. Graded buffer layers have also been utilized in other metamorphic growth schemes, such as Ge on Si with graded SiGe buffer segments, as shown in Figure 2.7 [2].

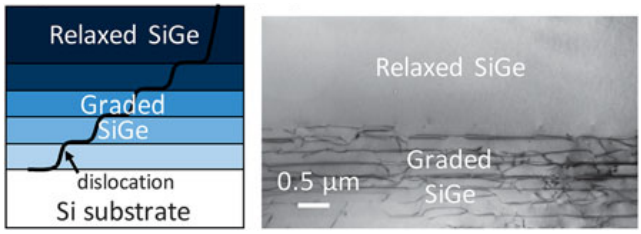

Figure 2.7: (left) Schematic, and (right) Bright-field transmission electron microscope (BF-TEM) image of compositionally graded SiGe buffer layer on Si, where the threading dislocations are effectively trapped at the mismatched SiGe layer interfaces. Reproduced from [2].

Buffer layers can be combined with defect filter layers (DFL), which are designed to filter dislocations from propagating further toward the top growth surfaces by redirecting the TD direction. One implementation of DFL is strained layer superlattice (SLS). An SLS consists of alternating material layers with different strains, often formed with QWs or QDs of compositions different from the bulk material in between. Ideally, all the SLS QWs or QDs should be pseudomorphically grown to avoid additional TDs. The strain in SLS is significant enough that any propagating TD will bend over at the SLS interfaces and may serpentine between the SLS layers, thereby reducing the total number of TDs propagating further in the growth direction. An example implementation of SLSs can be seen in Figure 2.8 [22]. In these TEM images, the filtering of TDs in the GaAs blanket layer grown on Si is achieved with InGaAs QWs. After three QWs, the grown GaAs shows a significantly reduced number of TDs. SLS-type DFLs have also been utilized in the SAG approach [23].

2.2.3 Selective Area Growth

Selective Area Growth (SAG) is a heteroepitaxial growth approach where the growth is confined to predetermined areas on the substrate. SAG offers additional strain relaxation tools and enables the evolution of growth architecture to three dimensions (3D). It also significantly improves integration with other silicon devices and platforms, including silicon photonics.The limited use of area

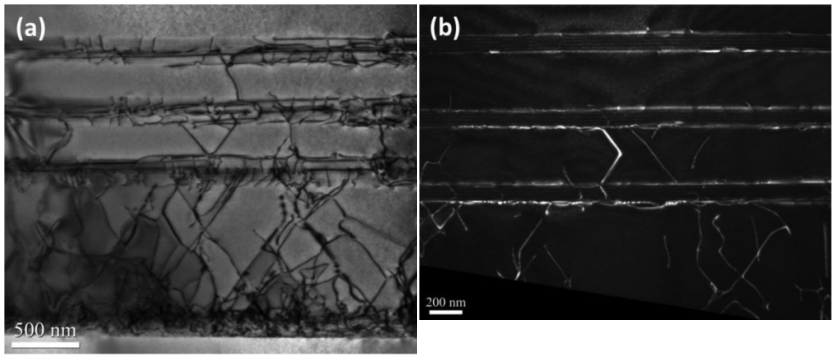

Figure 2.8: The use of InGaAs/GaAs SLSs for TD filtering in a InAs/GaAs QD laser application. (a) BF-TEM image of three layers of InGaAs/GaAs SLSs DFLs. (b) DF-TEM image of DFLs on a GaAs buffer layer and Si substrate. Reproduced from [22].

and materials enhances cost-effectiveness and extends the design space. However, SAG introduces greater complexity in controlling growth, strain, uniformity, selectivity, and structure compared to blanket growth. Growth parameters must be finely tuned to achieve the desired uniformity and selectivity. Controlling the facet evolution of the grown 3D structure is crucial for achieving the intended geometrical shape. Additionally, the smaller, confined dimensions and 3D structure of the grown material present further challenges for characterization.

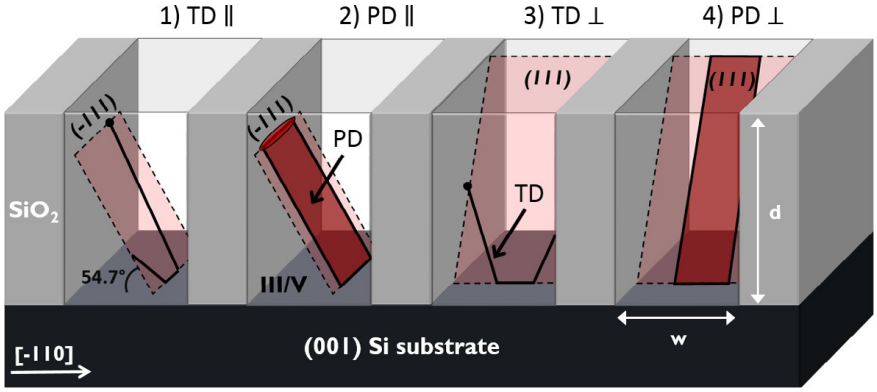

Figure 2.9: The defect trapping cases in trenches formed for the ART technique. A TD on a $\{111\}$ plane parallel (1) or perpendicular (3) to the trench orientation will have the glide arms terminated on the oxide sidewalls. A PD on a $\{111\}$ plane parallel to the trench orientation (2) will also terminate on the oxide sidewalls, given the aspect ratio is high enough. A PD on a $\{111\}$ plane perpendicular to the trench orientation (4) is not trapped in this ART configuration. Reproduced from [24].

SAG opens up a defect control method called TD necking, or more generally,

aspect ratio trapping (ART). With the ART method, epitaxial layers are selectively grown in high-aspect holes or trenches, usually formed with a patterned oxide on Si. Within the trench, TDs are propagating along the $\{111\}$ planes forming the half-loops. As shown in Fig.2.9, both TDs on $\{111\}$ planes parallel and perpendicular to the trench direction can be trapped on the oxide sidewalls. The 54.7° angle of $\{111\}$ planes with the substrate plane corresponds to an aspect ratio of 1.4. Theoretically, in a trench with an aspect ratio larger than 1.4, any TDs propagating from the hetero-interface will terminate on the oxide sidewalls [7]. The effect of the aspect ratio was presented by Kunert et al. [8], where increasing the aspect ratio from 1 to 3, and 7.5 improved the dislocation trapping, as shown in Fig.2.10. With small enough trenches, the ART method brings the capability of greatly reducing the required buffer layer thickness for the same or even more defect elimination. This will come with the advantage of avoiding TCE mismatch related limitations and the additional material stresses observed in thick blanket growths. The ART method can also be utilized with heteroepitaxial growth on V-groove patterned surfaces for APB elimination. After the ART trenches with oxide sidewalls are formed, the Si substrate can be anisotropically etched to expose $\{111\}$ facets to implement this technique.

The ART method can be identified as a vertical growth method, where the main growth continues in vertical direction. Recently, there have been other methods developed, which involve growth in lateral direction. The first, template assisted selective epitaxy (TASE) employs hollow oxide templates terminated with $\{111\}$ faceted Si [25, 26]. TASE offers laterally grown custom heteroepitaxial III-V structures, however, it requires a more complex pre-growth template preparation and limits the final device sizes. A very similar approach called lateral aspect ratio trapping (LART) grows a large area III-V membrane sandwiched between two oxide layers on a Si on insulator (SOI) platform [27–29]. LART offers easier integration with existing silicon photonics platforms on SOI due to its same plane growth at the photonic circuit level [30].

For both blanket growth and SAG approaches, there are several challenges still existing, including efficient coupling into the silicon photonics platforms, improving defect densities and device efficiencies. Each approach comes with its advantages and drawbacks. While SAG offers more tools for defect reduction, device size and geometry controls, it brings more complex growth procedures. The heteroepitaxial blanket layer growth is built on the know-how derived from homo- and pseudomorphic growths matured in the III-V devices industry, but lacks the efficient tools for defect controls and requires high thicknesses of layers, which complicates light coupling and integration with the silicon photonics platform underneath.

Recently, a new technique has been introduced, employing both blanket growth and SAG approaches, by growing III-V blanket epitaxial layers selectively in deep

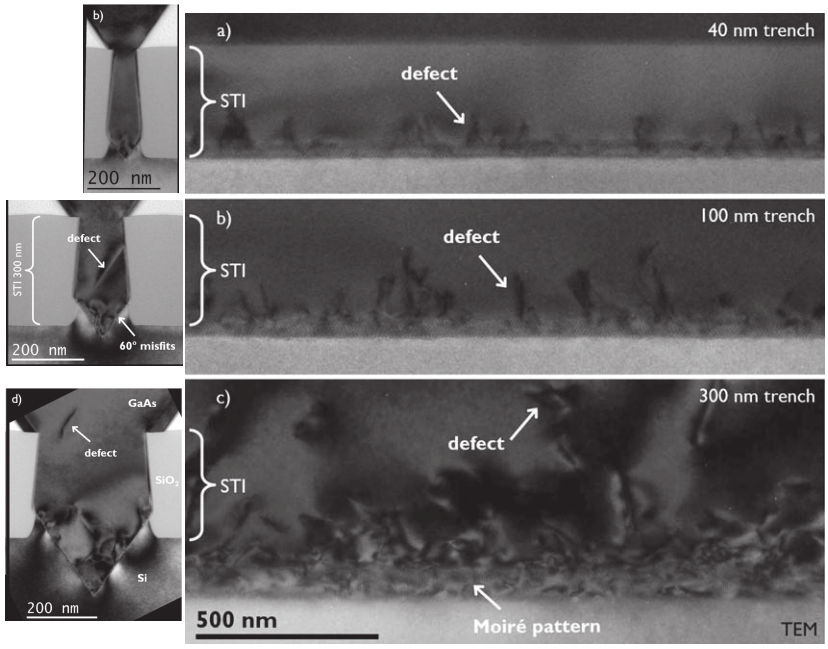

Figure 2.10: Cross-sectional and lateral bright-field (002)-order TEM images of GaAs nano-ridges grown in 300 nm deep and (a) 40 nm, (b) 100 nm, and (c) 300 nm wide trenches, having 7.5, 3, and 1 aspect ratio (AR) (height/width), respectively. Higher AR improves the defect trapping and effectively reduces the TDD. Reproduced from [8].

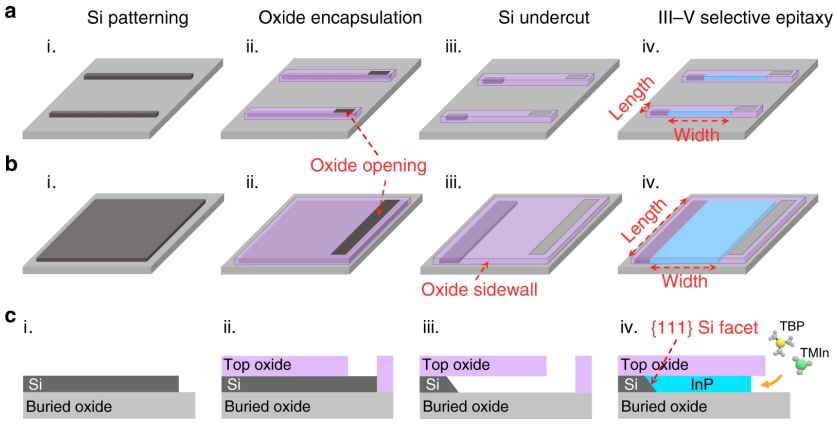

Figure 2.11: 3D schematics of InP (a) sub-micron wires and (b) membranes grown with LART; (c) cross-sectional schematic of each step. Reproduced from [28].

and large Si recesses, or 'pockets' [31]. The growth starts selectively from the

Si pockets and continues as a blanket growth towards the top of the SOI surface. During the blanket growth, various dislocation trapping methods (such as SLSs) are utilized before the growth of device functional layers, including doped GaAs and AlGaAs, active InGaAs QWs embedded with InAs QDs. The recess height and the grown layer thickness are optimized to match the active layer height with the photonic circuit level. Another similar approach starts with homoepitaxial Si growth to form sawtooth-shaped (111)-faceted Si V-grooves, which eliminate APBs at the heteroepitaxy interface [32]. The process schemes of both studies are shown in Fig. 2.12.

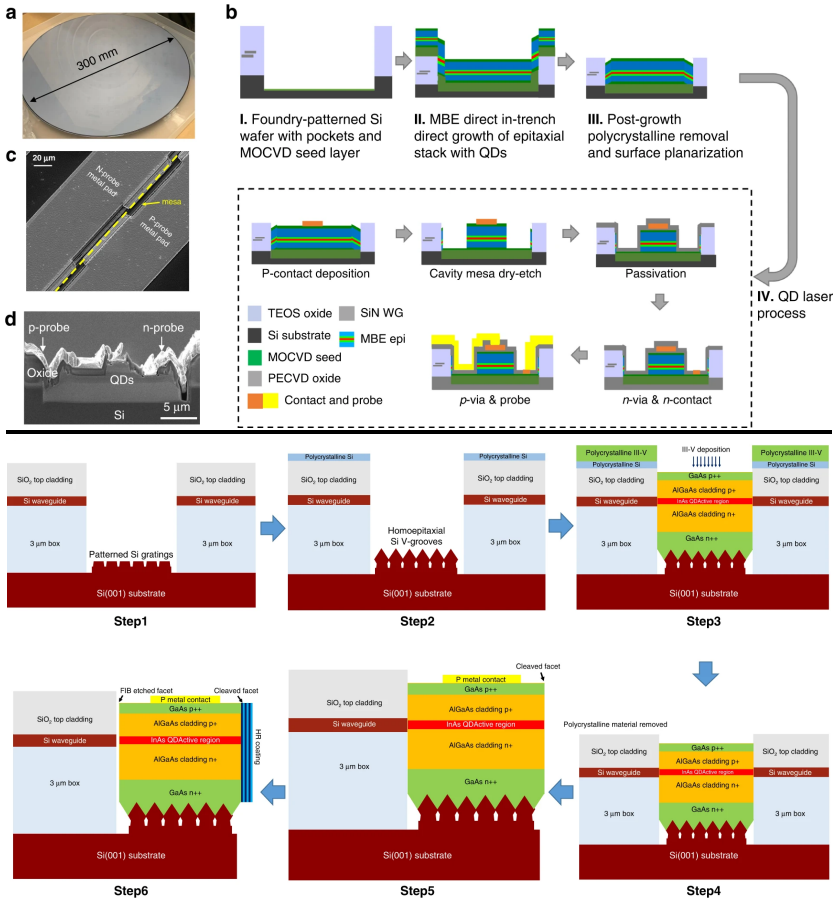

Figure 2.12: Process steps of selective hetero-epitaxial growth of III-V blanket layers in large recess pockets, (top) Shang et al. [31], (bottom) Wei et al. [32].

Nano-ridge engineering (NRE) [16] [33] [34] is a SAG technique that is utilized in this thesis work. Employing the ART on V-grooves, NRE is utilized to

continue the heteroepitaxial growth vertically to form nano-ridges. With specific growth conditions, all of the ART trenches with V-shape bottom were filled with grown III-V compound. For GaAs nano-ridges reported by Kunert et al. [16], towards the top of the trench the V-shape of the bottom disappears due to reflow of the GaAs seed layer. Once the grown layer reaches the top of the trench, the growth continues to form the nano-ridges. Depending on the growth conditions, including temperature and precursor ratios, various nano-ridge crystal geometries can be achieved as shown in Fig.2.13 [33]. The grown GaAs nano-ridge was measured to be fully relaxed based on x-ray reciprocal space map (RSM) metrology [16]. Apart from GaAs, the NRE method has also been utilized to grow InP [35], GaSb [34], and InGaAs [36]. Different III-V compounds can be incorporated pseudomorphically during the nano-ridge growth process, including QWs, for various device applications. NRE enables also the incorporation of dopants during the growth process for the device junction formation, and capping layers for the surface passivation.

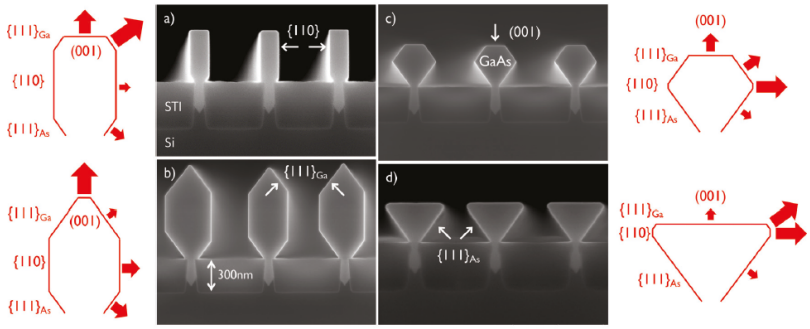

Figure 2.13: NRE enables various cross-sectional geometries of grown structures. Different geometrical profiles achieved with different growth parameters applied during nano-ridge epitaxy. Cross-sectional scanning electron microscopy (SEM) images of GaAs nano-ridges with different profiles, and the corresponding sketches indicating the different growth rate hierarchies applied for achieving these geometries. Reproduced from [33].

2.3 InGaAs/GaAs Nano-Ridge Device Manufacturing

The nano-ridge (NR) devices that are studied in this thesis work are fabricated by combining the ART and the NRE methods. The NR devices are fully grown in imec's 300-mm complementary metal-oxide semiconductor (CMOS) pilot line.

The manufacturing of the NR devices starts with a 300-mm Si (001) substrate. For a p-i-n type of diode device formation and better electrical connectivity, the

Si substrate is initially doped with a blanket ion implant step. The phosphorus ion implant step is targeting a peak n-type doping concentration of 1×10^{19} cm^{-3}.

For the formation of nano-trenches, a CMOS method called shallow-trench isolation (STI) is used. STI is typically employed to isolate different CMOS modules with narrow oxide trenches. In a typical STI process, silicon is dry etched to form isolation trenches, and these shallow trenches are filled with oxide. In the case of NR manufacturing, the STI trenches are designed to be large enough to form Si ridges in between. The ratio of the open Si surface to the total area is kept between 9% to 10% [16]. The nano-trenches are patterned with widths of 60, 80, 100, 120, and 150 nm to observe the aspect ratio effects on the NRs. After oxide planarization, a Si wet-etch step is carried out to form the oxide nano-trenches using tetramethylammonium hydroxide (TMAH), resulting in a V-shaped trench bottom with exposed $\{111\}$ facets of Si, as shown in Fig. 2.18. As discussed in subsection 2.2.1, starting the heteroepitaxial growth on $\{111\}$ Si facets aims to avoid APBs. Due to STI dry etching, the Si ridges have non-vertical sidewalls, narrowing towards the top of the substrate. The narrowing trench width towards the top of the trench further helps in defect trapping.

Next, the epitaxial growth is performed by metal organic vapor phase epitaxy (MOVPE) in a 300-mm deposition chamber. During the growth process, different group-III and -V precursors are applied, such as tertiarybutyl arsine (TBAs), trimethylindium (TMIn), triethylgallium (TEGa), and trimethylgallium (TMGa) [16]. Starting with the n-type doped GaAs layer on the $\{111\}$ Si facets, the nano-trench is filled with epitaxially grown GaAs. The target doping concentration is about 1×10^{19} cm^{-3} for the n-type GaAs layer. The defects initiated at the GaAs/Si hetero-interface are effectively confined inside the trenches [8], dependent on the aspect ratio of the nano-trenches [34].

The n-type doped GaAs layer is grown further outside of the nano-trench and begins to form the desired rectangular waveguide shape by employing the NRE growth technique. The subsequent GaAs layer grown out of the trenches has a misfit defect density below 1×10^{6} cm^{-2} [34], serving as a fully relaxed buffer for the pseudomorphic growth of active layers on the top. After the n-type doped GaAs, the growth continues with an intrinsic (or unintentionally doped (UID)) GaAs layer. The growth controls are further adjusted to progress the rectangular waveguide profile. Inside the i-GaAs layer, the active region consists of three $In_{0.22}Ga_{0.78}As$ quantum wells (QWs) with a targeted thickness of 10 nm each. The thickness, separation, and the number of QWs are optimized based on the pseudomorphic growth conditions and the desired device operation. Preferably, the QWs are placed in the center of the waveguide for higher optical mode overlap, as will be discussed in Chapter 3.

The NR growth continued with a p-type doped GaAs layer, with the target doping concentration of 1×10^{19} cm^{-3}. As the last epitaxial growth step, the In-

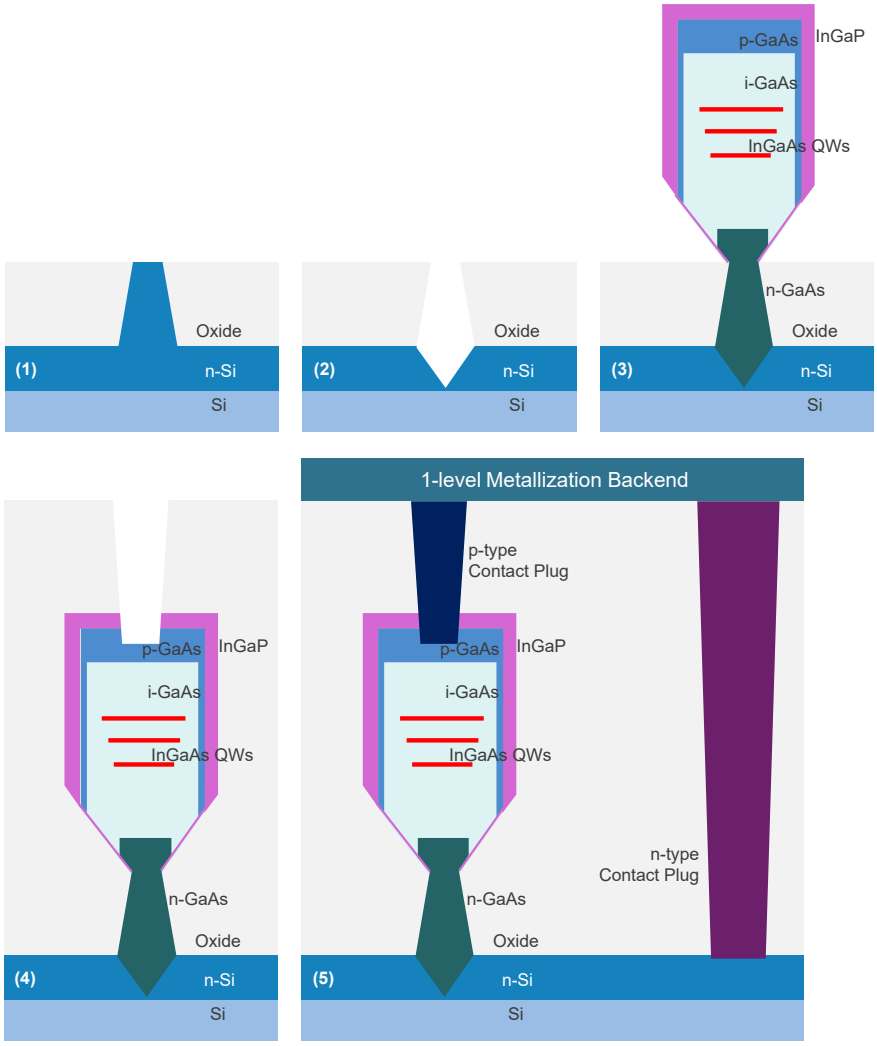

Figure 2.14: Fabrication steps of the InGaAs/GaAs NR devices. (1) Oxidation STI process to form Si ridges to be etched. (2) Anisotropic wet etching of Si to form the nano-trenches with V-shape bottom. (3) Epitaxial growth of NRs with the ART and the NRE methods. (4) Oxide filling, planarization and oxide/InGaP/GaAs etching for the top metal contact access. (5) Metal plug depositions for anode and cathode contacts, and the single layer back-end CMOS standard Cu damascene metallization. Reproduced from [37].

GaAs/GaAs NR is capped with a lattice-matched $In_{0.49}Ga_{0.51}P$ layer to passivate the GaAs surfaces [38] [39]. As InGaP has a higher bandgap, it offers a physical and electrical blocking layer prohibiting carriers escaping and recombining at the surface defects on the NR/oxide boundary. Finally, nano-ridges with a rectangular

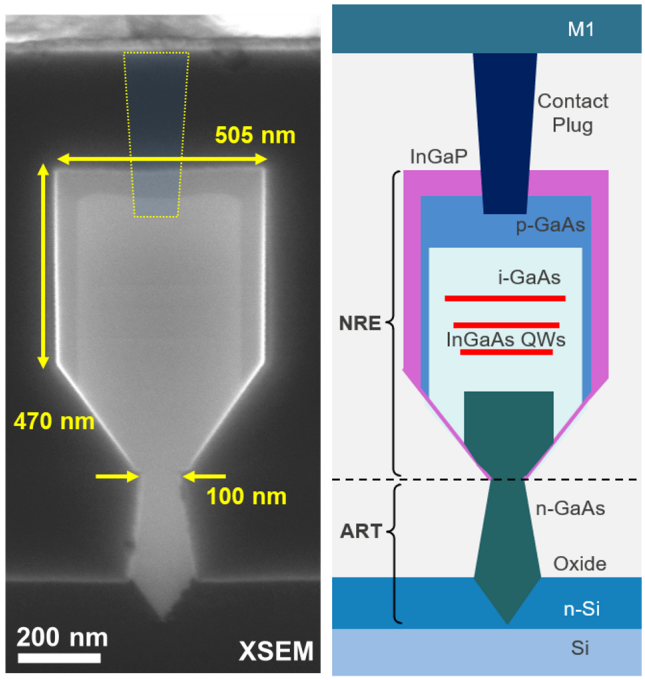

Figure 2.15: (left) Cross-sectional scanning electron microcopy (XSEM) image of a GaAs nano-ridge with three InGaAs QWs. (right) Schematic description of the nano-ridge cross-section. Reproduced from [37].

waveguide shape at the top portion are achieved above the nano-trenches, with a final nano-ridge waveguide height of 470 nm and a width of 505 nm for the 100 nm trench width devices as shown in Fig. 2.15.

The oxide filling is completed after the free standing NR is formed. The conformal oxide filling does not have a planar top surface due to NR structures. Hence, an oxide planarization step is performed with a chemical-mechanical polishing (CMP) step. After the oxide filling and planarization, the top oxide layer and the InGaP layer underneath are locally etched to form with a plug array pattern. Tungsten contact plugs are deposited to electrically contact the top p-type doped GaAs layer. The pitch between the plugs is varied from 0.6 μm to 4.8 μm.

The bottom n-GaAs layer is connected through the n-doped Si substrate to another set of tungsten contact plugs. The fabrication is completed using a standard CMOS Cu damascene metallization processing. The different process steps are shown in Fig. 2.18. A schematic cross-section and a cross-section scanning-electron microscopy (XSEM) image of the final nano-ridge device are shown in Fig. 2.15. The 3D schematic of a NR device and its anode/cathode connections

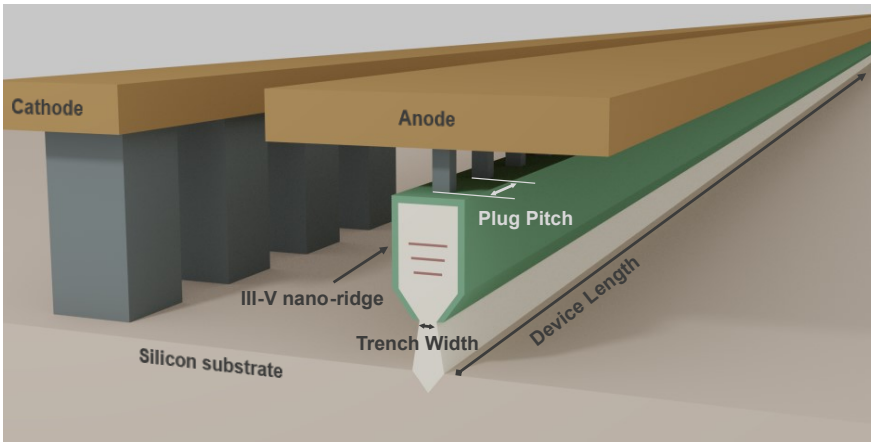

Figure 2.16: 3D representation of InGaAs/GaAs NR devices, reproduced from [1].

are depicted in Fig. 2.16.

After the fabrication of the NR devices is completed, photoluminescence (PL) measurements are carried out. The PL response show a peak emission wavelength at 1040 nm and a band-edge at 1110 nm, confirming the target indium composition of 22% and the thickness of the quantum wells in InGaAs/GaAs MQW stack (Fig. 2.17).

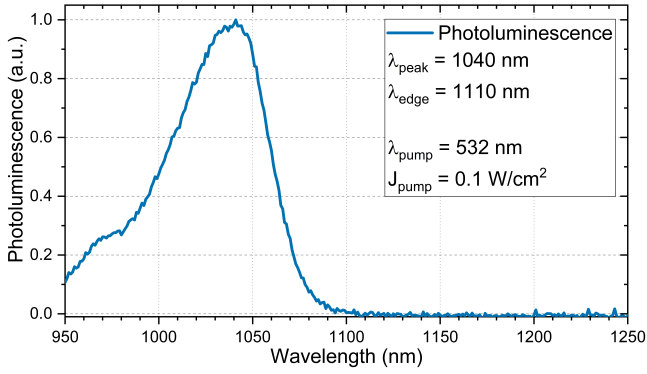

Figure 2.17: Photoluminescence spectrum of the InGaAs/GaAs quantum wells of nano-ridges, pumped with 532 nm 15 kHz pulsed laser with 0.1 W/cm^2 intensity.

In a side study, an additional fin structure is added on the InGaAs/GaAs NR devices. The fin is epitaxially grown in a second growth step. The goal is to optically isolate the top p-contact plugs from the optical mode center, and enable a higher p-type GaAs doping at the top, to further improve the p-contact resistivity.

Before the second growth step, the InGaP layer is locally etched, similar as for the p-contact etching, but with a different mask enabling a larger opening. The second growth step continued to form the p-type doped GaAs fin. The rest of the process steps are similarly followed to form the metal contacts as shown in Fig. 2.18.

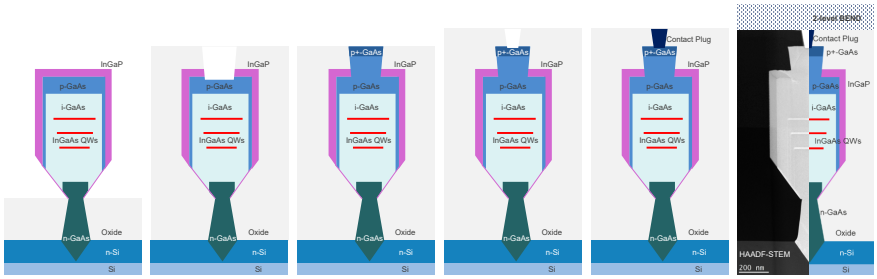

Figure 2.18: Fabrication steps of the InGaAs/GaAs NR devices with regrown p-GaAs fin. (1) Epitaxial growth of NRs using the ART and NRE methods. (2) Oxide filling, planarization, and oxide/InGaP/GaAs etching to form the p-GaAs fin template. (3) Regrowth of p-GaAs. (4) Oxide filling, planarization, and oxide/InGaP/GaAs etching for top metal contact access. (5) Deposition of p-type and n-type metal plugs, and 2-level back-end CMOS standard Cu damascene metallization. (6) Final device cross-section figure overlaid with a HAADF-STEM image. Reproduced from [40].

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3

Design of InGaAs/GaAs Nano-Ridge Waveguide Photodetectors

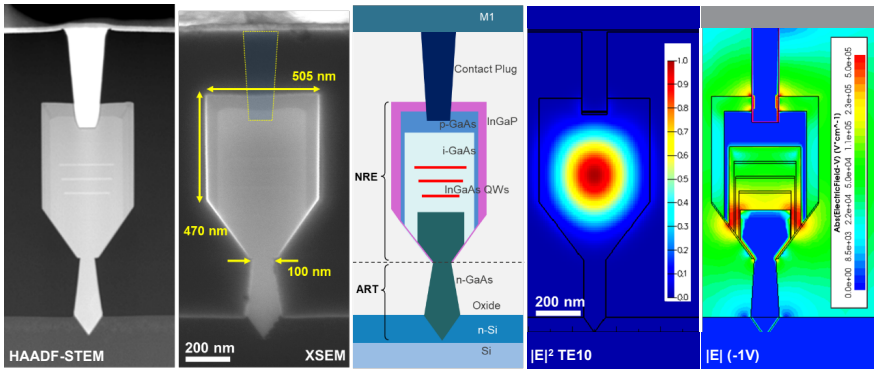

Figure 3.1: Cross-sectional figures of III-V nano-ridges grown on silicon. (left to right) High-angle annular dark-field scanning transmission electron microscopy (HAADF-STEM), cross-sectional scanning electron microscopy (XSEM), schematic, simulated optical mode profile, simulated E-field profile.

This chapter will cover the design of InGaAs/GaAs nano-ridge waveguide photodetectors (NRWPDs). It begins with modeling the absorption of the InGaAs compound concerning its composition. The indium composition design space is limited by the epitaxial growth constraints of the bulk GaAs nano-ridges (NR).

Nevertheless, the absorption model provides insight into the best operable wavelength ranges for specific indium composition rates. The chapter then explores other design space variations, such as the trench width, which alters the size of the nano-ridges. These design space variables were studied in different simulation groups, including optical, electrical device, and opto-electrical co-simulations. Lastly, the chapter covers the layout design, which accommodates the design of experiments (DOEs) based on these design space variables.

3.1 Bulk InGaAs Absorption Model

Interband absorption occurs when light is absorbed by any material, and a photon with sufficient energy excites an electron in the valance band into the conduction band, creating an electron-hole pair. The optical absorption coefficient α (1/cm) is the ratio of the number of photons absorbed per unit volume over the number of injected photons per unit area.

The absorption coefficient changes with respect to the absorbed photon energy, or in other terms, the wavelength or the frequency of the light. The spectral dependence of the absorption coefficient can be calculated as [1]:

$$\alpha_0(\hbar\omega) = C_0|\hat{e}\cdot\mathbf{p}_{cv}|^2\rho_r(\hbar\omega - E_g) \tag{3.1}$$

where

$$C_0 = \frac{\pi e^2}{n_r c\epsilon_0 m_0^2\omega} \tag{3.2}$$

and

$$\rho_r(\hbar\omega - E_g) = \frac{1}{2\pi^2}\left(\frac{2\mathbf{m_r}^*}{\hbar^2}\right)^{3/2}(\hbar\omega - \mathbf{E_g})^{1/2} \tag{3.3}$$

where

$$\frac{1}{m_r^*} = \frac{1}{m_e^*} + \frac{1}{m_h^*} \tag{3.4}$$

$|\hat{e}\cdot\mathbf{p}_{cv}|^2$ is the momentum matrix element. In the equation for C_0, e is elementary charge, n_r is the real part of the refractive index, ϵ_0 is the vacuum permittivity, m_0 is the electron rest mass, and ω is the frequency. In the equation for $\rho_r(\hbar\omega - E_g)$, $\mathbf{m_r}^*$ is the reduced effective mass, $\hbar$ is the reduced Planck constant, and $\mathbf{E_g}$ is the effective bandgap.

From equation 3.1, the absorption coefficient with respect to frequency is dependent on the momentum matrix element and joint (or reduced) density of states. The momentum matrix element denotes the electron-photon interaction. This component in the α_0 calculation gets different values for bulk and quantum well geometries since the electron-photon interaction in QWs is polarization-dependent

due to carrier confinement. For bulk materials, the matrix element is isotropic and given as [1]:

$$|\hat{e}\cdot\mathbf{p}_{cv}|^2 = \frac{m_0}{6}E_P \tag{3.5}$$

where E_P is the Kane's model energy parameter. E_P values for different composition rates of InGaAs can be calculated based on different experimental findings given in Table 3.1 [2]. The ternary parameters for InGaAs alloys are calculated with the InAs and GaAs binary compound parameter values and a bowing parameter (D). For an arbitrary parameter A, the calculation for $In_xGa_{1-x}As$ can be:

$$A(In_xGa_{1-x}As) = A(InAs)x + A(GaAs)(1-x) - D_{InGaAs}x(1-x) \tag{3.6}$$

All parameters related to the absorption model of InGaAs are listed in Table 3.1, with GaAs and InAs values and InGaAs bowing parameter, D_{InGaAs}.

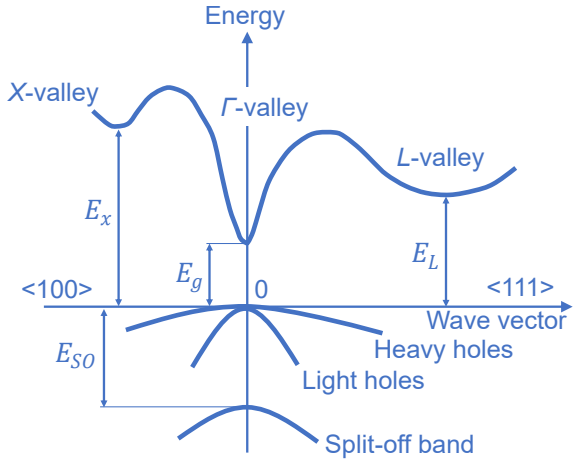

Figure 3.2: Schematic of InGaAs band diagram. Reproduced from [3].

The joint density of states component $\rho_r(\hbar\omega - E_g)$ of the absorption coefficient calculation is the summation of the different excitation cases between the different hole and conduction bands depicted in Fig.3.2. For direct bandgap materials such as GaAs, InAs, and InGaAs, the lowest bandgap value occurs at the Γ valley, where separate heavy hole (HH), light hole (LH), and split-off (SO) valence bands exist. Therefore, ρ_r for the Γ valley is calculated separately for each transition case and added in the absorption coefficient calculation as:

$$\rho_{\mathbf{r}} = \rho_{r,LH} + \rho_{r,HH} + \rho_{r,SO} \tag{3.7}$$

where

$$\rho_{r,LH}(\hbar\omega - E_g) = \frac{1}{2\pi^2}\left(\frac{2m_{r,LH}{}^*}{\hbar^2}\right)^{3/2}(\hbar\omega - E_g(E_\Gamma - E_{LH}))^{1/2} \tag{3.8}$$

$$\rho_{r,HH}(\hbar\omega - E_g) = \frac{1}{2\pi^2}\left(\frac{2m_{r,HH}{}^*}{\hbar^2}\right)^{3/2}(\hbar\omega - E_g(E_\Gamma - E_{HH}))^{1/2} \quad (3.9)$$

$$\rho_{r,SO}(\hbar\omega - E_g) = \frac{1}{2\pi^2}\left(\frac{2m_{r,SO}{}^*}{\hbar^2}\right)^{3/2}(\hbar\omega - E_g(E_\Gamma + \Delta_{SO}))^{1/2} \quad (3.10)$$

and

$$\frac{1}{m^*_{r,LH}} = \frac{1}{m^*_e} + \frac{1}{m^*_{LH}} \quad (3.11)$$

$$\frac{1}{m^*_{r,HH}} = \frac{1}{m^*_e} + \frac{1}{m^*_{HH}} \quad (3.12)$$

$$\frac{1}{m^*_{r,SO}} = \frac{1}{m^*_e} + \frac{1}{m^*_{SO}} \quad (3.13)$$

The bandgap variations of HHs and LHs represented by E_{HH} and E_{LH}, respectively, arise from any type of strain. For a fully relaxed material, these can be taken as zero.

The absorption coefficients of bulk InGaAs calculated for 18% to 22% In compositions are shown in Fig.3.3. The curves show a minimum absorption of 5000 1/cm for the 950 to 1050 nm wavelength range and a high dependence on the In composition. The extinction coefficient (k), the imaginary component of the complex refractive index, can be calculated from the absorption coefficient (α) with:

$$\alpha = \frac{4\pi k}{\lambda} \quad (3.14)$$

The absorption coefficient model of InGaAs can be further extended to include the strain, quantization, and excitonic effects. An extensive theory of the interband absorption of InGaAs/GaAs quantum wells can be found in Micallef (1993) [4].

3.2 Nano-Ridge Design Overview

In section 2.3 of the previous chapter 2, the manufacturing steps of InGaAs/GaAs nano-ridge devices were covered. The devices in this thesis use GaAs as the bulk material of the waveguide structure and InGaAs as the quantum well (QW) material for active absorption. This choice enables synergies with other types of active devices being developed on the same platform, such as optically pumped lasers [5] and electrically pumped lasers [6]. The inclusion of QWs also enables the design and co-integration of advanced modulator devices, such as quantum-confined Stark effect (QCSE) type electro-absorption modulators (EAM) or phase modulators (PM).

Parameters	InAs	GaAs	$\mathbf{D_{InGaAs}}$
$\mathbf{E_g^{\Gamma}[eV]}$	0.417	1.519	0.477
$\mathbf{E_g^{X}[eV]}$	1.433	1.981	1.4
$\mathbf{E_g^{L}[eV]}$	1.133	1.815	0.33
$\mathbf{\Delta_{SO}[eV]}$	0.39	0.341	0.15
$\mathbf{m_e^*(\Gamma)}$	0.023	0.063	0.0091
$\mathbf{m_{hh}^*}$	0.41	0.51	$\sim$0
$\mathbf{m_{lh}^*}$	0.026	0.082	$\sim$0
$\mathbf{m_{SO}^*}$	0.15	0.15	0
$\mathbf{E_P[eV]}$	21.5	28.8	-1.48

Table 3.1: Material parameters used in absorption coefficient model calculations. Values retrieved from [3], [2]. InGaAs bowing parameter, D_{InGaAs}, is used as in $A(In_xGa_{1-x}As) = A(InAs)x + A(GaAs)(1-x) - D_{InGaAs}.x(1-x)$.

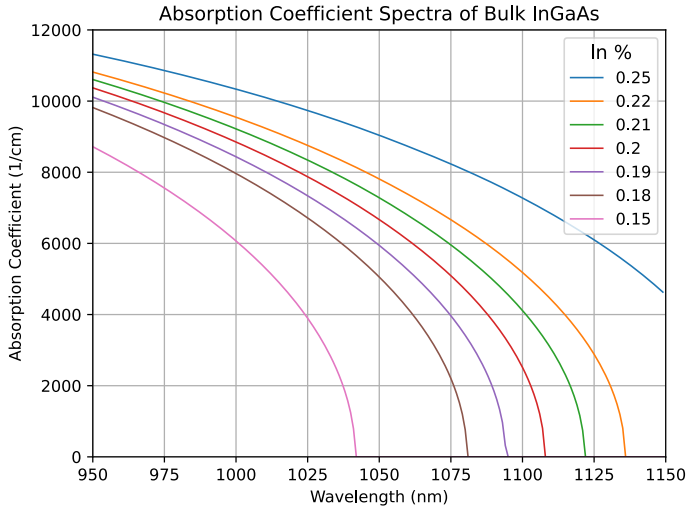

Figure 3.3: Calculated bulk absorption coefficient spectra of InGaAs for various In compositions.

Earlier studies to form waveguides from the nano-ridges grown on silicon resulted in the final rectangular cross-section structure shown in Fig. 2.15. This cross-section consists of the bottom trench area buried in an STI oxide, an over-

grown, free-standing pentagonal nano-ridge on top. It is electrically connected via n-type Si at the substrate, and a tungsten plug contacted at the top. Different numbers of InGaAs QWs were studied, ranging up to 7 of them [7], and 3 QWs were found to be ideal regarding QW uniformity, strain, and growth quality. In order to preserve growth uniformity, the nano-ridge device regions are surrounded by uniform nano-ridge arrays with 80 nm trench width. This allowed growth uniformity to be sustained across 300-mm wafers, eased subsequent oxide deposition, planarization, and metallization steps, and reduced the loading effects during the III-V nano-ridge growth. Loading effects can influence the nano-ridge formation and geometry, and the open/masked area ratio governs the loading effects. Therefore, the ART trench width (TW) size impacts the size of the nano-ridge that is grown in the subsequent growth process, and the nano-ridge size can be controlled through this width. An example of the effect of TW on the nano-ridge size can be seen in Fig.3.4. As described in section 2.3, the ART trench portion of the nano-ridges traps the threading dislocations and parallel planar defects. The n-type GaAs growth is further extended after the trench is filled to ensure that any defects trapped in the trench are contained in the doped GaAs region. This allows the leakage through defects to be minimized in the intrinsic region of the p-i-n junction. This is critical, both for both light detection and for light generation.

Geometrical Parameters	**Values for Various Trench Widths (nm)**				
	60 nm	**80 nm**	**100 nm**	**120 nm**	**150 nm**
Plug Height	320	290	300	285	250
Plug Width	90	90	90	90	90
Plug Depth	120	120	120	120	120
Ridge Width	414	455	505	530	665
Ridge Height	480	470	470	480	445
Funnel Height	215	235	265	275	335
Trench Width	60	80	100	120	150
Trench Height	260	260	260	260	260
Trench Depth into Si	75	85	95	100	125

Table 3.2: The geometrical size values for different trench width nano-ridge devices. The funnel stands for the funnel-like bottom portion of the waveguide portion.

In earlier optically pumped lasing studies on GaAs nano-ridges, passivation of the nano-ridge by an InGaP layer effectively improved the photoluminescence response [8]. Therefore, the InGaP passivation is also implemented in this thesis work.

Although different coupling schemes are envisioned for the monolithically in-

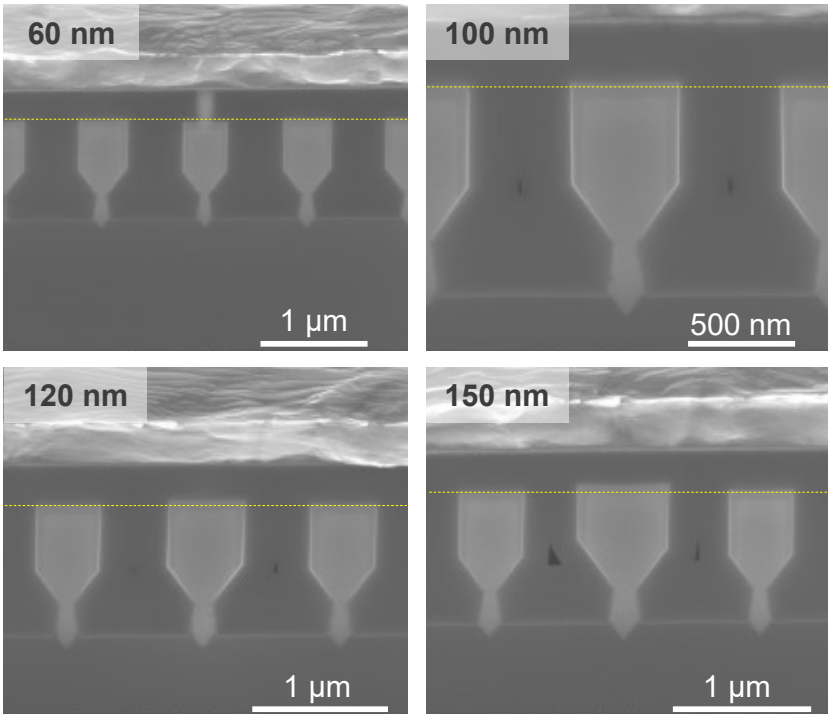

Figure 3.4: Cross-sectional SEM images of nano-ridge devices with different trench widths. The nano-ridge sizes change with the trench width value. Horizontal markers are put for comparison with the dummy nano-ridges with 80 nm trench width put in between different devices.

tegrated III-V nano-ridges [9], the characterization of the photodetector devices in this thesis work was carried out through edge coupling on a cleaved facet of the devices. Therefore, the design layouts were formed to be compatible with the cleaving separation and aimed to maximize the measurable devices per cleave line. Free space coupling into the cleaved edge was also simulated with the finite-difference time-domain (FDTD) method.

In summary, the design space variables for the NRWPDs studied in this thesis can be listed as:

- QW placement within the nano-ridge
- Trench width size
- Device length
- P-contact plug density

3.3 Simulations for NRWPD Design

The simulations for the NRWPD design include separate optical and electrical device simulation sets and opto-electrical co-simulations. The simulation efforts initially started with 2D optical mode simulations for the waveguide design and 2D electrical device simulation for the diode junction design. Later, more extensive simulations were carried out to estimate the edge coupling efficiency and the metal contact losses. Opto-electrical co-simulations allowed to predict the DC and AC photocurrent. The detailed simulation results on high-speed response and leakage mechanisms are covered in the chapters 4 and 5.

3.3.1 Optical Simulations

3.3.1.1 Waveguide Mode Simulations

The mode simulations of nano-ridge waveguide devices were completed for 2 dimensional (2D) cross-sections of the devices. For this purpose, Ansys Lumerical MODE finite difference eigenmode solver software was utilized [10].

The waveguide modes of the nano-ridge devices were simulated using the Ansys Lumerical finite difference eigenmode solver [10]. The cross-sections with and without p-contact plugs were studied separately. The dimensions and QW placement were taken from experimental TEM cross-sections. The bottom trench portion of the nano-ridge was simplified and kept fully vertically as opposed to the tie-shape of real devices.

The simulation wavelength was 1020 nm. GaAs and InGaAs (22% In) complex refractive indices (n,k) were calculated from Adachi [11]. The rest of the material values were taken from the built-in material database of Lumerical MODE, constructed from Palik [12].

For this structure, the fundamental TE mode confinement in the area of the three InGaAs QWs Γ_{QW} is calculated at $\approx 8.2\%$.

Simulation Results TE10	NR without plug	NR with plug
Effective Index	3.27	3.23
Loss (dB/μm)	0.311	0.866
99% Absorption Length (-20 dB)	64.3 μm	23.1 μm

Table 3.3: The 2D optical mode simulation results for 100 nm trench width NRWPD.

Table 3.3 summarizes the simulation results for a 100 nm trench width device. The absorption length ranges between 23.1 μm and 64.3 μm for the cross-section with and without the metal contact plug. The majority of the optical loss in the no-plug case occurs due to the absorbing InGaAs QWs, but the loss increases more

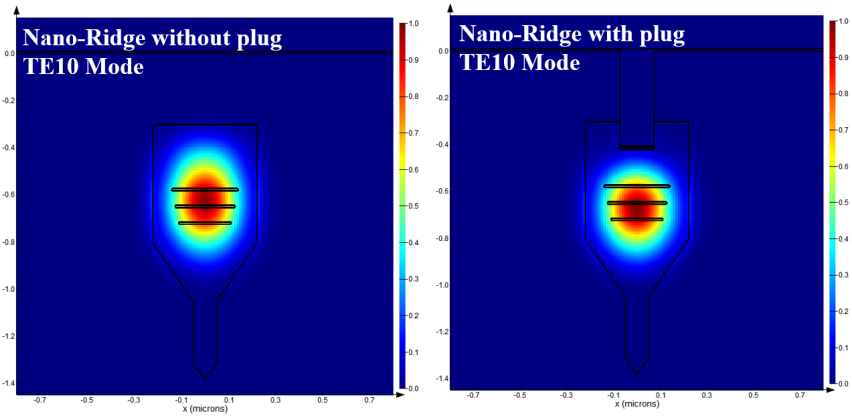

Figure 3.5: The 2D $|E|^2$ optical mode of fundamental TE mode of the nano-ridge cross-section with (right) and without (left) p-type contact plug. 100 nm trench width nano-ridge geometry. Linear color scale.

than twice for the 2D cross-section with plug. This indicates the strong optical losses due to the top metal contact plug.

3.3.1.2 Edge Coupling Simulations

The fiber edge coupling measurements of the NRWPDs bring additional coupling loss that must be calculated to understand the photodetector device performance clearly. Therefore, the coupling was simulated through a 3-dimensional finite-difference time-domain (FDTD) simulation [13].

The simulated structure consisted of the elongated profile of the NRWPD devices of different geometries formed by different trench widths, listed in Table 3.2. The NRWPD portion of the simulated structure consisted of Si and oxide cladding but no other loss element, including QWs and metal contact plugs, in order to focus only on the passive coupling losses. The other portion of the simulation structure consisted of air with a planar Gaussian source. The edge coupling opto-electrical measurements of NRWPD devices described in chapter 4 were to be completed with a lensed fiber with a Gaussian beam waist of 2.0 μm. The Gaussian source in the free space portion of the structures was focused on the facet of the device, with TE-like polarization and 2.0 μm beam waist. A mode expansion monitor was added 2 μm after the device facet to measure transmitted power in the first 10 lowest-order eigenmodes of the nano-ridge waveguide structure. The transmitted power in the modes after the first 10 eigenmodes was found to be ignorably small. The total transmission was calculated by adding the total power transmitted in these 10 eigenmodes and dividing by the Gaussian source power. The best-coupled mode was found to be the fundamental TE mode, while some of

the higher-order modes were also coupled into the PD waveguide. The simulation structure and calculated transmission are given in Fig. 3.6.

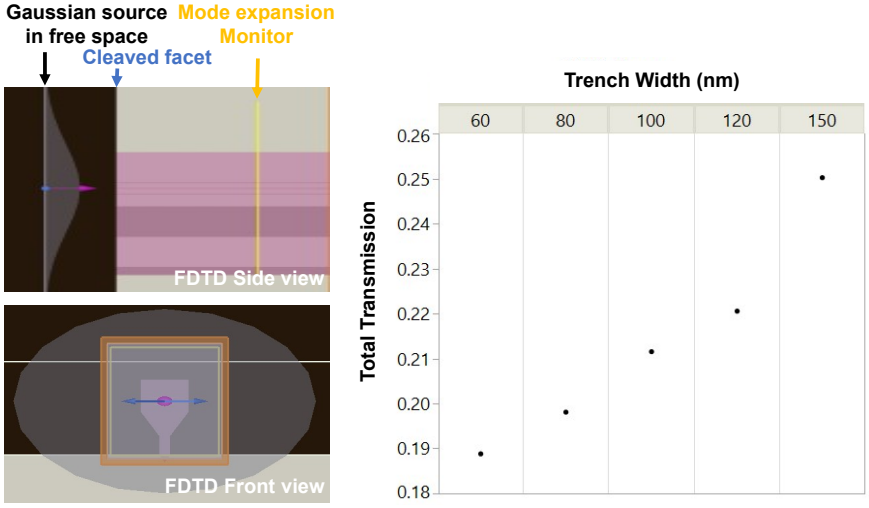

Figure 3.6: The setup and results of 3D FDTD simulations for free space edge coupling into the NRWPD devices. (left) The 3D FDTD simulation setup with side and facet front views, showing the Gaussian source in free space, the device facet, simulation mode expansion monitor and device cross-section. (right) The coupling results are given in Transmission ratio for different device trench width geometrical values.

The coupling efficiency is inferred from the transmission ratio calculated in this 3D FDTD simulation. As expected, the efficiency increases for increasing trench width, or the overall size of the nano-ridge. The coupling efficiencies range from 19% to 25% as shown in Fig. 3.6.

3.3.1.3 Contact Plug Density Simulations

The top p-contact plugs of the nano-ridges were optimized to have proper connectivity to the p-type doped region. The plugs were integrated as in a standard CMOS via process and consisted of a few nanometers of adhesion layers and tungsten as the main body material. Although minimally invasive into the device structure, their proximity was close enough that it perturbs the device's performance.

The simulations on the effects of the contact plug pitch were completed in a 3D FDTD simulation constructed in Ansys Lumerical FDTD software [13]. The structure consisted of a 4.8 μm portion of uniform nano-ridge of 100 nm trench width geometry, including only the metal plugs as lossy material. The 3D nano-ridge waveguides were excited with the fundamental TE mode source placed at the center of a zeroth plug. The transmission was calculated after 4.8 μm distance with a power monitor, while the plug array pitch between the two cross-sections varied

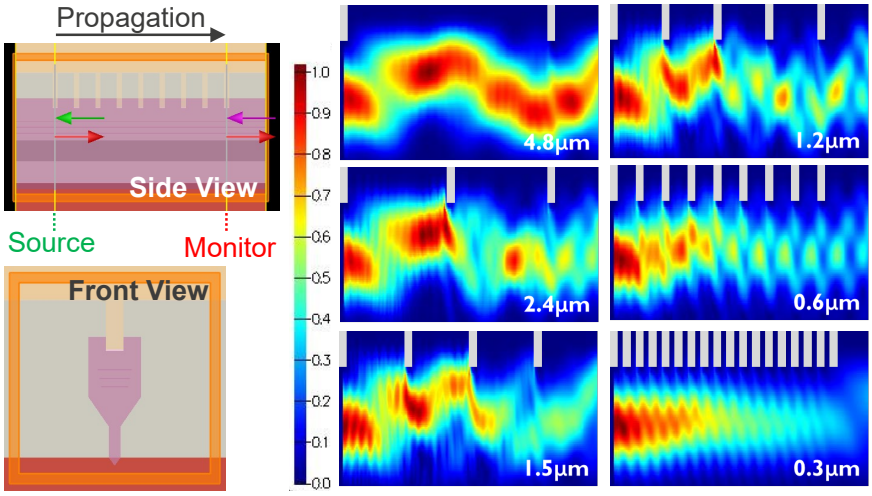

Figure 3.7: 3D FDTD simulations for calculating p-contact plug effects. (left) Side and front view of constructed simulation structure in Lumerical FDTD. (right) Side view of 2D power distribution at center for different p-contact plug pitches, grey plug shapes externally added for clarity [14].

at 0.3 μm, 0.6 μm, 1.2 μm, 1.5 μm, 2.4 μm, and 4.8 μm. A secondary power screen was placed along the waveguide's centerline to observe the propagating power distribution and the interaction with the metal plugs. The simulation setup and the 2D power distribution along a longitudinal cross-section for each plug pitch value are shown in Fig. 3.7.

The attenuating effect of the metal contact plugs can be seen in Fig. 3.7. The 0.3 μm plug pitch clearly shows a strong attenuation of the optical power, while the transmission improves for the lower plug densities. The 4.8 μm plug pitch case also exhibits a resonance-like behavior where the cross-sectional optical power profile follows a low-loss path, avoiding the metal plug and further reducing the optical losses. The numerical results of the plug density simulations are further elaborated in chapter 4 along with the measured PD device performance values.

3.3.2 Device Simulations

The electrical device simulations were completed on the 2D cross-section of the NRWPDs. For these simulations, the Sentaurus Device software [15] was utilized.

The initial device simulations were utilized to validate the device operation in terms of carrier transport, electric field formation, and electrostatic behavior. This was useful since the nano-ridge epitaxial layers were grown vertically and horizontally at different rates, resulting in a complex junction structure.

The 2D simulation structure was formed by using the Sentaurus Structure Ed-

itor software with various sets of material properties for each sub-layer. The mesh size was reduced at critical volumes (e.g., InGaAs QWs) and interfaces (e.g., GaAs/Si, GaAs/InGaAs, GaAs/InGaP, GaAs/oxide, InGaP/oxide). The simulation model was derived from the built-in p-n junction model, where the p- and n-type contacts are set as lumped element anode and cathode, respectively. The simulation included the mobility, recombination, optics, and heterointerface physics models.

The device simulation starts with the equilibrium potential and charge distribution solution. For this, the software iteratively solves the electrostatic potential equation of the Poisson (Eq. 3.15), electron (Eq. 3.16) and hole (Eq. 3.17) charge conservation equations as below [15]:

$$\nabla \cdot (\epsilon \nabla \phi + \overrightarrow{P}) = -q(p - n + N_D - N_A) - \rho_{trap} \tag{3.15}$$

$$\nabla \cdot \overrightarrow{J_n} = q(R_{net,n} - G_{net,n}) + q\frac{\partial n}{\partial t} \tag{3.16}$$

$$-\nabla \cdot \overrightarrow{J_p} = q(R_{net,p} - G_{net,p}) + q\frac{\partial p}{\partial t} \tag{3.17}$$

where ϵ is the electrical permittivity, ϕ is the electrostatic potential, $\overrightarrow{P}$ is the ferroelectric polarization, q is the elementary electronic charge, n and p are the electron and hole densities, N_D and N_A are the concentration of ionized donors and acceptors, respectively, ρ_{trap} is the charge density contributed by traps and fixed charges, $R_{net,n(p)}$ and $G_{net,n(p)}$ are the electron (hole) net recombination and generation rates, respectively, and $\overrightarrow{J_{n(p)}}$ is the electron (hole) current density. Later, depending on the simulation setting, the lumped element bias was ramped with set step periods, and these equations were solved on the mesh points recursively until errors went below set limits. Ramping steps are initially set and further reduced during the simulation ramping to avoid convergence errors.

The addition of more models increases the simulation complexity and chances of convergence failures. So, there is no single device simulation routine that can cover all possible effects and conditions. While the core material parameters, electrostatic potential, electron and hole conservation models are kept, different simulation models can be turned on and off for different analyses. In the case of AC response simulations, the primary structure was ramped to the desired bias voltage first, and later, the AC response calculation was continued. For the AC response calculation, a small signal model was applied at defined electrical device ports for a defined frequency range. The resulting admittance and capacitance values were recorded for each frequency point measured, from which the S11 response can be calculated. For the optical AC response simulations, the optical generation model

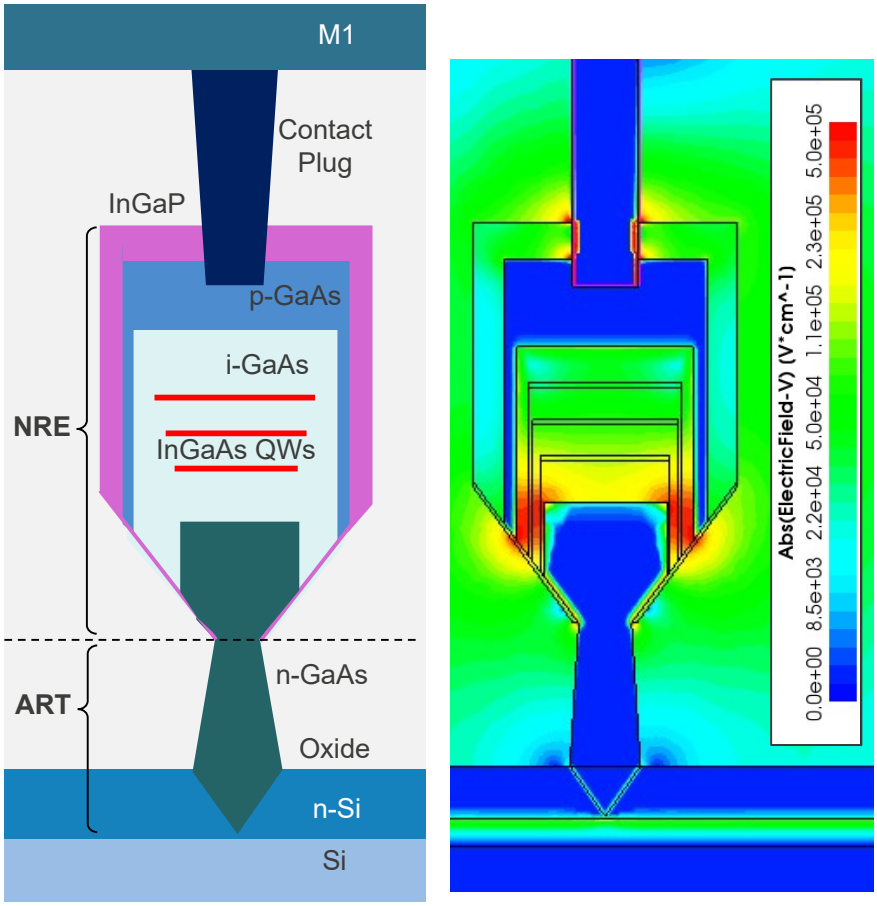

Figure 3.8: The NRWPD cross-sectional schematic (left) and absolute E-field profile (right) at -1 V bias, calculated with Sentaurus Device software, arcsinh color-scaled in the range of 0 *to* 5×10^5 *V/cm [14].*

was treated as a device port, and the small signal admittance and capacitance on the anode and cathode nodes were recorded for S21 response calculations.

The preliminary electric field distribution of the NRWPD devices at -1 V bias is shown in Fig. 3.8. The intrinsic GaAs volume, consisting of active InGaAs QWs, exhibits an electric field of more than 50 kV/cm and up to 500 kV/cm at the bottom side portions. This indicates successful junction formation, enabling efficient photocurrent extraction from the active volume during photodetection.

The detailed device simulations on high-speed AC responses and S-parameter extraction of the devices are given in chapter 4 along with the high-speed measurements. The dark current device simulations are given in chapter 5. For the

wide-field grown InGaAs devices on silicon, the simulations are given in chapter 6.

3.3.3 Opto-Electrical Co-Simulations

The simulation efforts on the optical and electrical device characteristics of the nano-ridge photodetector devices were separately elaborated in previous sections. Each physical domain characteristic was found satisfactory for the device implementation and further fabrication. Yet, there are still more critical performance metrics that cannot be extracted individually from these simulation efforts. These metrics include, for example for photodetectors, the responsivity and the operation bandwidth of the devices. While quick estimations are viable for simple 1D layered photonic devices, for more complex device structures like nano-ridges, the opto-electrical co-simulations are a necessity.

There are several commercial simulation packages capable of opto-electrical co-simulations, such as Ansys Lumerical or Sentaurus software packages. For the Sentaurus Device software used in this thesis work, the RSoft optical simulation products [16] are offered for co-simulation studies. Although this co-simulation scheme offers complementing 3D FDTD simulations and device simulations, the 2D co-simulation required additional effort for data compatibility since both tools had different output and input data structures. The steps ensuring data compatibility and the opto-electrical simulation flow are illustrated in Fig. 3.9.

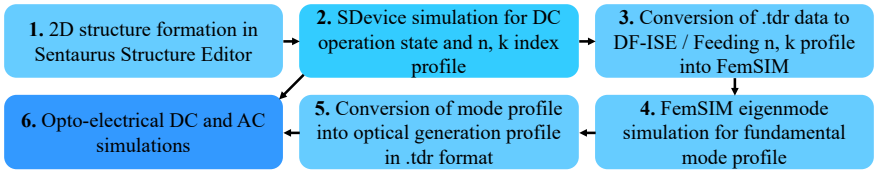

Figure 3.9: Flowchart of the opto-electrical simulation structure.

As shown in Fig. 3.10, the preliminary opto-electrical co-simulations demonstrate the carrier generation profile used as the input for device simulation, which is comparable with the fundamental optical mode profile. The DC optical current generation at -1 V bias indicates successful carrier collection paths for both holes and electrons. Particularly for holes, the p-type doped GaAs sidewalls aid in collecting the generated carriers at the edges of the InGaAs QWs. For electrons, the proximity of the overgrown n-type GaAs region assists in carrier collection.

The high-speed opto-electrical response of the NRWPD devices is detailed in chapter 4 along with the high-speed electrical simulations and measurements.

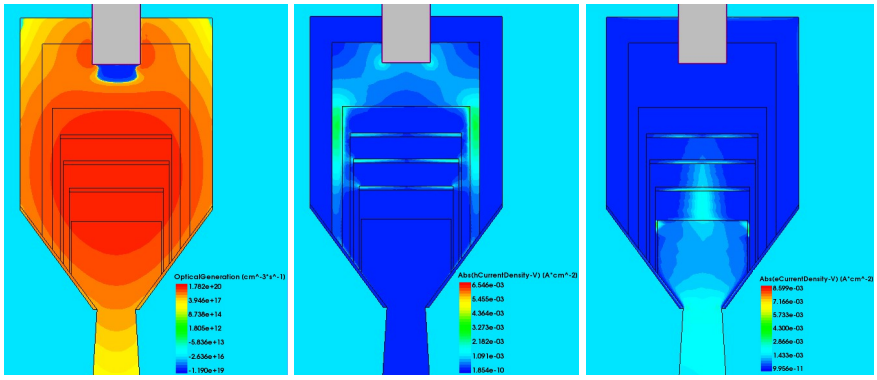

Figure 3.10: (left) Optical generation ($1e^{-11}$ $W/\mu m$ power density) profile (in arcsinh scale) generated from RSoft FemSIM mode solver and fed into Sentaurus Device, 1×10^{-11} W total power, 1 μm assumed 2D simulation depth. (middle and right) Hole and electron current density of generated carriers from InGaAs at -1 V bias voltage, according to the imported optical generation profile.

3.4 Layout Design

The mask layout design of the nano-ridge devices is based on the design space constraints detailed in the previous sections and the fabrication/processing boundaries set for the monolithic III-V growth on the 300-mm Si CMOS pilot line of imec. Within these boundaries, the design of experiments was constructed, and the layout was designed to be compatible with the measurement settings. The layout design was completed with the IPKISS software package [17].

The III-V nano-ridge growth is sensitive to growth area density on the large area of a 300-mm Si substrate. Any local selective-area density change may result in variations in nano-ridge geometrical shape and growth quality due to loading effects. Therefore, dummies with a uniform density of 8-10% were placed between contacted devices on the layout. All nano-ridge orientations were kept on a single axis to improve uniformity. The Si contact plugs were placed at 13 μm distance to satisfy minimum nano-ridge uniformity and metal routing needs.

For characterization of the NRWPD device, different device sites were designed, including sites for edge coupling, AC characterization, surface illumination, and for PL and electrical metrology.

3.4.1 Design of Experiments for Edge Coupling

A design of experiments (DOE) whereby the trench width, length, and p-contact plug density were varied as described in Table 3.4 was set up.

The NRWPD devices were planned to be measured with edge coupling after

Design Parameter	Unit	Site A	Site B
Length	μm	500	5, 20, 45, 95, 120
Plug Pitch	μm	0.6, 1.2, 2.4, 4.8	0.3, 0.6, 1.5
Trench Width	nm	60, 80, 100	60, 80, 100, 120, 150

Table 3.4: NRWPD device design parameters for the edge coupled measurement sites.

cleaving one end of the devices. Devices with different parameters were laid out vertically and aligned on an imaginary cleave line. The device groups were placed with a 100 μm period to accommodate standard probing array access. This enables automated and semi-automated electrical probing to be completed efficiently, with fewer probe landings.

In site A, only one side of the cleaved die is used for long devices. In site B, both ends with electrical pads allow use of both sides after cleaving. To save mask space, nano-ridges were horizontally shifted to fit different device lengths, which are split by cleaving, as shown in Fig. 3.11.

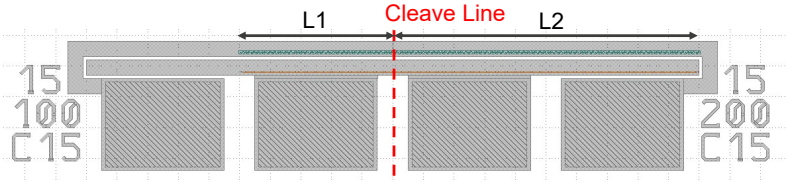

Figure 3.11: A sample of edge coupled measurement site NRWPD device cell layout design.

3.4.2 Design of Experiments for AC Characterization

The devices described in the previous section are helpful for high-density device screening with edge coupling, after a single cleaving. However, due to high capacitance of the metal routing, AC parameter extraction is difficult. Therefore, a separate cell was designed for AC parameter extractions.

The nano-ridges in AC characterization site were placed on the same axis as in other device sites. Their n-contact plug arrays were formed with the same separation to the nano-ridges. The metal pads were drawn with an octagonal shape to reduce sharp edges and separated by 100 μm distance for a standard ground-signal (GS) probe. The nano-ridge length was kept constant at 148 μm, while the trench widths and metal contact lengths were varied. Table 3.5 lists the design parameters for this site. The site also included 'open' and 'short' type calibration cells for each metal contact length. In the 'open' cell the nano-ridge was removed. In the 'short' cell the pads were shorted with the Si contact plugs.

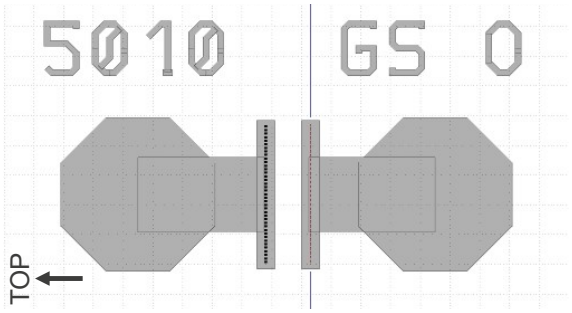

Figure 3.12: NRWPD AC characterization layout design, the image is rotated, and the top side of the wafer is marked.

Design Parameter	Unit	AC Characterization Site
Trench Width	nm	60, 80, 100, 120, 150
Contact Length	μm	20, 50, 100
Length	μm	500
Plug Pitch	μm	0.3

Table 3.5: AC characterization site device design parameters.

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4

Characterization of InGaAs/GaAs Nano-ridge Waveguide Photodetectors[1]

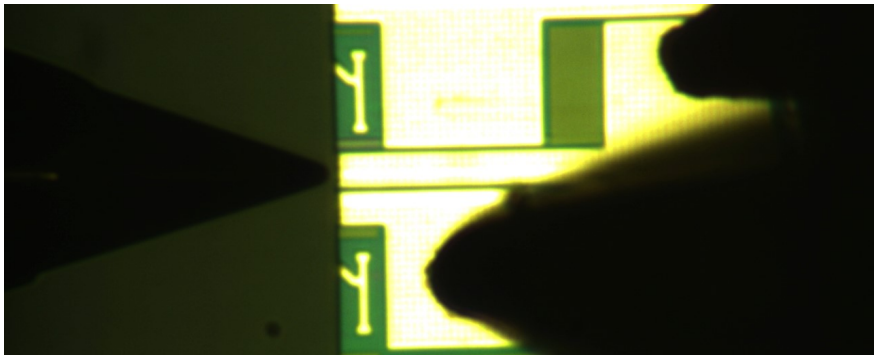

Figure 4.1: Edge-coupling into nano-ridge waveguide photodetectors with a lensed fiber.

This chapter will cover the characterization of the nano-ridge waveguide photodetector devices. It begins with the current-voltage (I-V) characterization of the devices, providing the first glimpse into their dark current characteristics. A comprehensive study on leakage mechanisms is provided in Chapter 5. The chapter then proceeds with opto-electrical characterization, where devices are illuminated

[1] Some of the content of this chapter was published in Ozdemir et al., "Low Dark Current and High Responsivity 1020nm InGaAs/GaAs Nano-Ridge Waveguide Photodetector Monolithically Integrated on a 300-mm Si Wafer," J. Lightwave Technol., vol. 39, no. 16, pp. 5263–5269 (2021).

through edge coupling. Subsequently, high-speed measurements and complementary simulations are presented. Finally, the chapter concludes with a benchmark study comparing the most recent monolithically integrated photodetector devices on Si.

4.1 Electrical Measurements

4.1.1 Methods

After the wafer-scale fabrication of the devices described in Chapter 2, two sets of samples were prepared by cleaving dies to form optical facets for optical edge coupling. Devices from two distinct sites were prepared, A and B, as described in chapter 3, which contain designs with p-contact plugs on different pitch distances along the waveguide, as well as different device lengths, as described in Table 3.4. Site A had NRWPD devices of up to 500 μm length. The pitches of the p-contact plugs to the p-GaAs layer are 0.6 μm, 1.2 μm, 2.4 μm, and 4.8 μm. Site B contained NRWPD device lengths from 5 μm to 120 μm, with p-contact pitch values of 0.3 μm, 0.6 μm and 1.5 μm. The actual length of the measured devices depended on the precision of the cleaving position, which had a variability of about ± 4 μm.

The electrical measurements were completed on two different tools. The first one is a 24-pin automated waferscale prober with a Keysight 3858A Digital Multimeter. The latter has a noise floor of 1 pA. The noise floor is dependent on the measured level range and settling time. The second tool is a 2-probe force/sense semi-auto prober tool with Keysight B1500A Semiconductor Device Analyzer, with noise floor measured at 5 fA. Measurements on both stations have given different dark current responses since most of the dark currents measured were noise-limited. This behavior is further discussed in Chapter 5.

4.1.2 Results

The dark and light current-voltage (I-V) response of the NRWPDs of site A (Table 3.4) with length 500 μm and various p-contact plug pitches is shown in Fig. 4.2.

The I-V characterization of devices from site A reveals p-i-n diode behavior with more than 6 orders of magnitude rectification (Fig. 4.2). Measured forward-bias dark currents depend on p-contact plug pitch due to variance in contact resistivity.

The dark current distributions of a large set of devices at -1 V and -2 V are given in Fig. 4.3, where the distributions are grouped with respect to the trench widths of the devices. The median dark current is below 1 pA level for all devices, and no dependence on the trench width has been found. The tool's noise floor limit of 1 pA limited a better characterization of the dark currents.

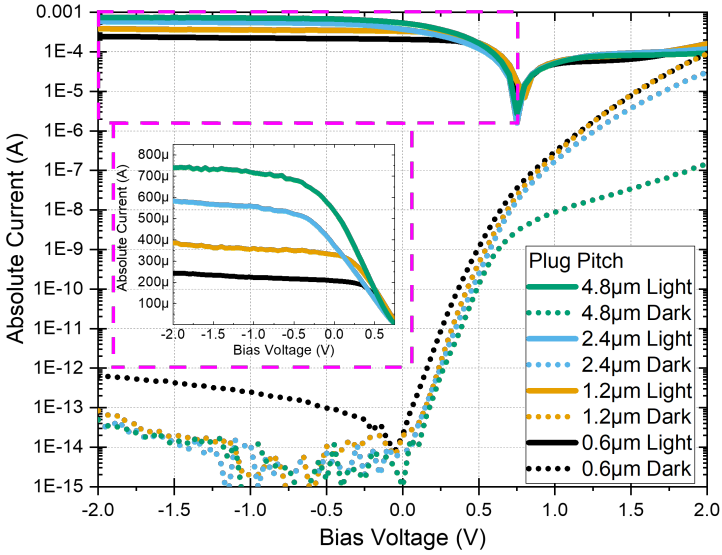

Figure 4.2: Dark and light I-V response of 500 μm long NRWPDs with various p-contact plug pitches.

The dark currents of nano-ridge devices are expected to increase with increasing trench widths since defect trapping becomes less effective with lower aspect ratios of the trench. A subset of devices in Site A with a trench width of 100 nm are further measured with a Keysight B1500A Semiconductor Device Analyzer having a noise floor at 5 fA. These devices were the longest and the widest NRWPDs available. The dark current distributions at -1 V and -2 V are given in Fig. 4.4. These devices exhibited a very low dark current, with a median value of 0.05 pA at -2 V. The median dark current at -1 V was observed to be around the noise floor of the measuring tool.

No clear dependence is observed between the contact plug pitch and reverse dark current. Taking into account the 505 nm width (as measured on SEM images) and 500 μm length of the NRs in site A, this corresponds to an equivalent dark current density of $1.98 \times 10^{-8} A/cm^2$ at -2 V, which is the lowest reported dark current for III-V photodetectors monolithically grown on Si. Table 4.2, which can be found in section 4.4, compares the dark current densities measured for the photodetectors monolithically grown on Si, using different material stacks. In this benchmarking, it is important to note that the NRWPD devices listed in the table have a higher bandgap than many other reported devices.

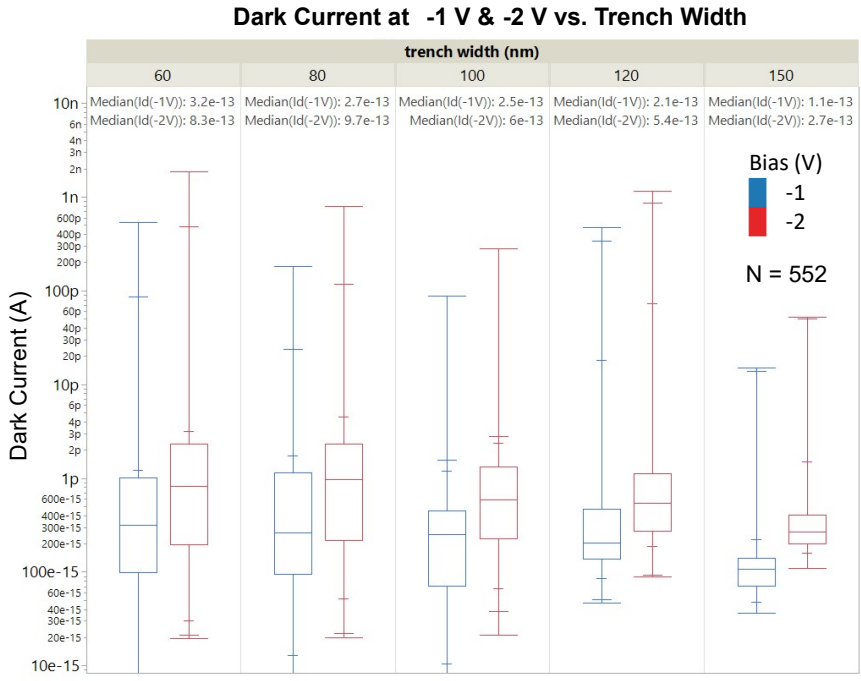

Figure 4.3: Dark current distributions per trench width. The measurements were done with the Keysight 3858A Digital Multimeter, where the noise floor is 1 pA.

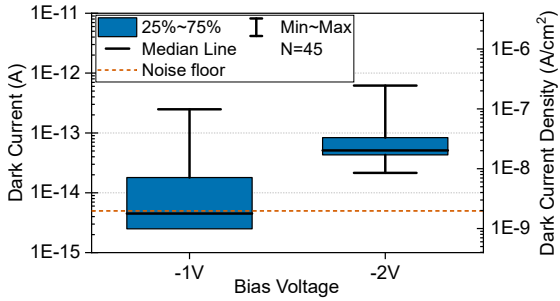

Figure 4.4: Dark current distributions at -1 and -2 V of 100 nm trench width devices in site A measured with Keysight B1500A Semiconductor Device Analyzer, which has the noise floor at 5 fA.

4.2 Opto-Electrical Measurements

4.2.1 Edge Coupling Setup

The NRWPD devices from sites A and B were measured after cleaving them at the designated cleaving lines. Later, devices were optically accessed by coupling a high-index (HI-1060) lensed fiber with metalized and tapered tip, and 2.0 μm mode field diameter (MFD). For DC opto-electrical characterization of the NRW-PDs, a single-mode continuous wave (CW) Fabry-Perot (FP) laser with 1020 nm wavelength was used. The laser output was fed into a fiber polarization controller, then a FC/APC (Fiber Connector, Angled Physical Contact) to FC/PC (Fiber Connector, Physical Contact) patch cord, and finally into the lensed fiber. The optical power at the tip of the lensed fiber was measured in each measurement run with an optical power meter (ThorLabs PM100D) set at the laser wavelength. The nominal power at the tip of the lensed fiber was measured as $\sim +7.0$ dBm. $(+/-1\%)$ (5.01 mW $+/-0.06$ mW). The overall setup is described in Fig. 4.5.

The DC opto-electrical measurement setup consisted of two motorized 6-axis optical device alignment stages with X, Y, and Z translational and pitch, yaw, and roll rotational controls. The cleaved sample with the array of NRWPD devices at the edge was placed in the center of a stationary stage, while the lensed fiber and the electrical probes were placed on the two motorized stages. The fiber was actively aligned based on the measured device's light current read out at the source measure unit (SMU) connected via electrical probes. During the alignment procedure, the fiber was rotationally aligned at a distance, and later, the fine alignment was completed on 3 translational axes while the fiber tip approached the die edge facet. Once the measurement on a single device was completed, the fiber and probe groups were moved away, and the alignment procedure was restarted on the next NRWPD device. The procedure was automated with a Python script for a single cleaved die with more than 100 NRWPD devices. Fig. 4.6 shows the measurement setup and alignment schematic.

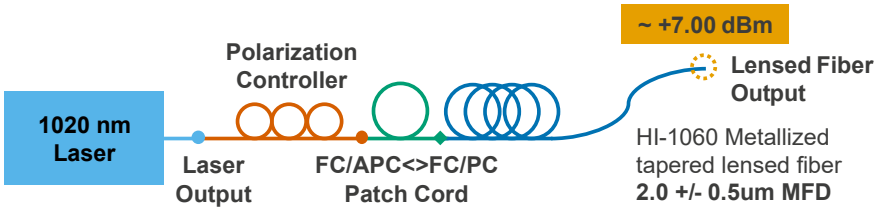

Figure 4.5: The optical train scheme for the edge coupling measurements of NRWPD devices.

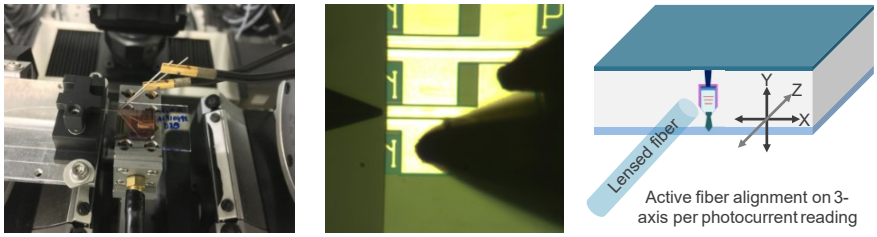

Figure 4.6: Edge coupled measurement. (left) The measurement setup. (middle) Top view on the measured device accessed with the electrical probes and lensed fiber on the edge. (right) Schematic description of the fiber alignment at the edge.

4.2.2 Results

The currents measured with light injection were 8 to 10 orders of magnitude higher than the measured dark currents, as shown in Fig. 4.2 of current-voltage (I-V) measurements. The measured currents at reverse bias were higher than those at forward bias, which may be related to a more efficient carrier collection.

With the nominal optical power, the light currents are in the range of 100 μA to 800 μA and show a clear dependency on the contact plug pitch, as shown in Fig. 4.7 for 100 nm trench width devices. As discussed in chapter 3, section 3.3.1, the close proximity of the top contact plugs of the NRWPDs is expected to contribute strongly to the optical losses of the device, affecting the performance. The collected light currents increase with longer top contact plug pitches (lower plug densities).

The external and internal responsivities, as well as the power and length dependencies, are further detailed in the following subsections.

4.2.2.1 External Responsivities

The photocurrents of NRWPD devices were calculated by subtracting measured dark currents from light currents. The extracted photocurrents were further used to calculate the external and internal responsivities.

The fiber-referred external responsivities were calculated from the ratio of photocurrent to the measured fiber-tip power. As given in Fig. 4.8, the median levels of external responsivities range between 0.017 to $\sim$0.14 A/W across different trench widths and plug pitches of the devices. The cross-sectional size of the devices increases with the trench width. Therefore, the larger trench-width devices exhibit higher responsivities. The external responsivities also correlate strongly with the plug pitch parameter. In the group of 100 nm trench-width NRWPDs, for the shortest contact pitch of 0.3 μm, the median fiber-referred responsivity of the NRWPDs is $\sim$0.03 A/W for 1020 nm wavelength at -1 V bias. It increases to $\sim$0.14 A/W for 4.8 μm plug pitch.

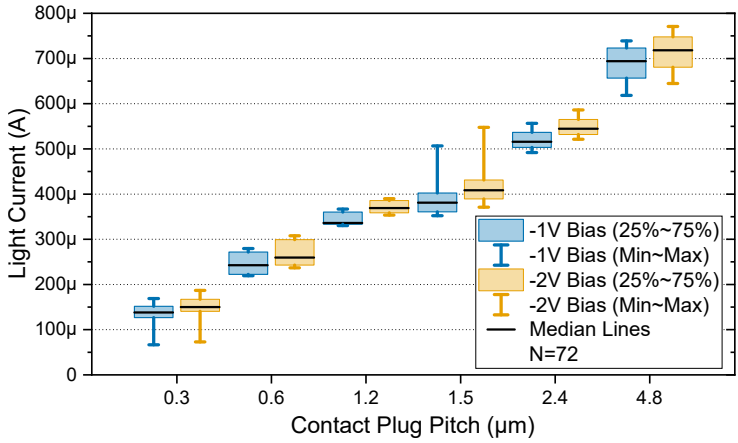

Figure 4.7: Light current distributions per contact plug pitch of 100 nm trench width NRWPDs.

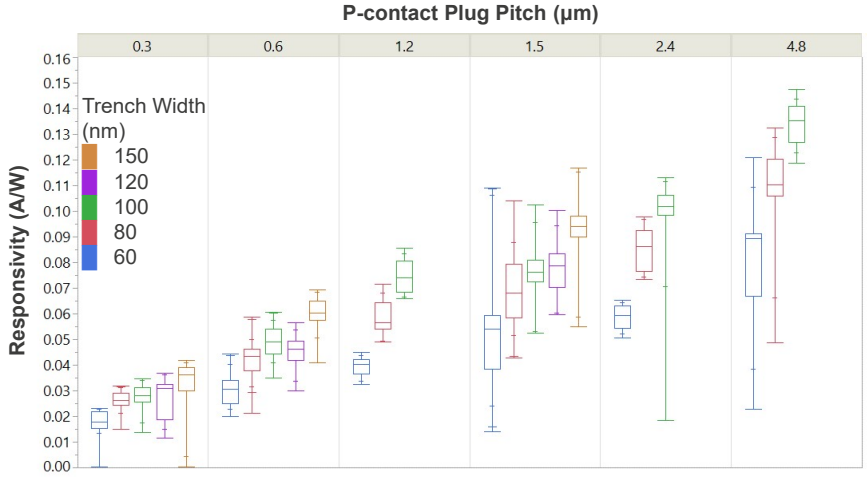

Figure 4.8: Fiber-referred external responsivities at −1 V bias.

4.2.2.2 Coupling-corrected Internal Responsivities

The mismatch between the mode profiles of the fundamental TE mode of the NR-WPDs (with the MFD of ∼0.42 μm for 100 nm trench-width devices) and the focused beam of the lensed fiber (with the MFD of ∼2.0 μm) introduces a coupling loss that needed to be taken into consideration for the calculations of the internal responsivities. The coupling efficiencies ($\eta_{coupling}$) were previously calculated in chapter 3, section 3.3.1, by utilizing finite-difference time domain (FDTD) simula-

tions in 3D. The total coupling efficiencies were calculated for different NRWPD geometries. The calculated coupling efficiencies range from 19% to 25% as given in Fig. 3.6. The coupled power (P_c), the internal responsivity (R_{int}) and the internal quantum efficiency (η_{int}) were then calculated with the following formulas 4.1,4.2, 4.3:

$$P_c = P_{out,lensedfiber} \times \eta_{coupling} \tag{4.1}$$

$$R_{int} = (I_{light} - I_{dark})/P_c \tag{4.2}$$

$$\eta_{int} = R_{int}\hbar\omega/e \tag{4.3}$$

where $\hbar$ is the reduced Planck constant, ω is frequency and e is electron charge. Based on formulas 4.2 and and 4.3, the internal responsivities and corresponding internal quantum efficiencies are calculated for both device sites A and B, at -1 V bias.

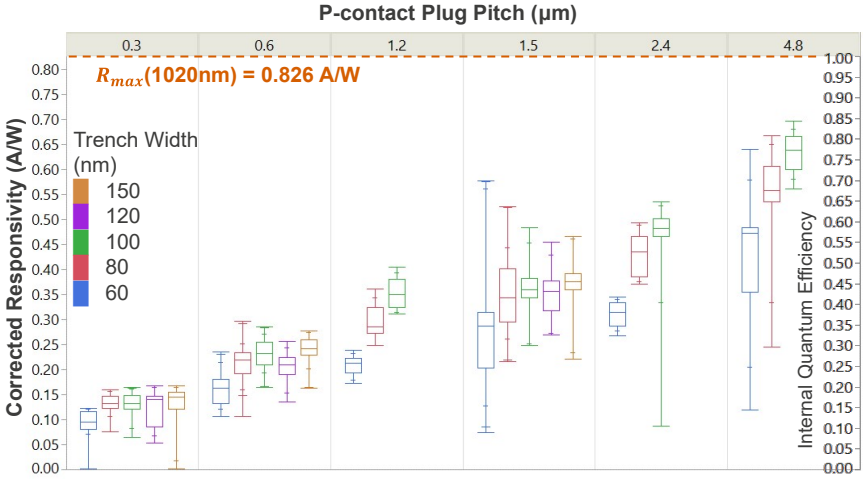

Figure 4.9: Coupling corrected internal responsivities at -1 V bias.

While the effects of cross-section geometry are reduced with the coupling correction, the larger trench-width devices still exhibit higher internal responsivities. A clear dependence was found on the metal plug pitch parameter, which governs the top metal contact density. An inverse relation is found between the devices' responsivity and the metal losses these plugs induce. The median coupling-corrected internal responsivities ranged between 0.10 to 0.65 A/W for -1 V bias. Taking into account that the theoretical maximum responsivity (R_{max}) is 0.826 A/W at 1020 nm wavelength and equation 4.3, this range corresponds to 12% to 79% internal quantum efficiencies.

For a further analysis of the losses induced by the metal plugs, a subset of the 100 nm trench-width NRWPD devices' responsivities were compared with the transmission data obtained from the 3D FDTD simulations in chapter 3, subsection 3.3.1.3. The calculated transmission values are reported in Fig. 4.10 (grey lines). The internal responsivity levels follow this p-contact plug pitch dependence, suggesting that the drop in the internal responsivities for smaller contact pitch values is linked to the loss induced by the optical absorption at the metal contacts. This result also helps us differentiate the responsivity-reducing mechanisms of the NRWPD devices and can help further improve the performance in the future.

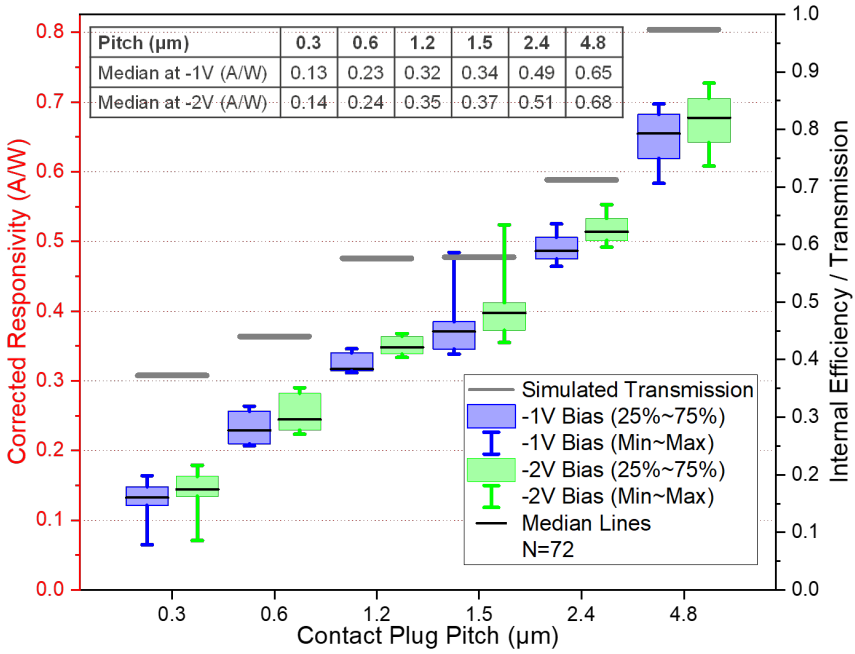

Figure 4.10: Distribution of the responsivity for different biases and p-contact plug pitches of devices from sites A and B excited with nominal input power. Site B data excluded devices shorter than the corresponding absorption lengths. (grey bars) Simulated transmission values for different p-contact plug pitches, scaled to the right vertical axis. (inset) Table of median responsivity values.

4.2.2.3 Input Power Dependence

The linear response of the NRWPD responsivity was validated experimentally. A subset group of 100 nm trench-width NRWPDs with 0.3, 0.6, 1.5 μm p-contact plug pitches in Site B were measured at input power levels less than the nominal power level of (5.01 mW $+/-$0.06 mW). The measured device lengths were

longer than the calculated absorption lengths.

The measured photocurrents vs. fiber-referred input power responses and their linear fittings are shown in Fig. 4.11. The photocurrents were plotted against the optical input powers applied. The points were linearly fitted according to their plug pitch and applied bias voltages. The linear fit slope falls within the corresponding ranges of the responsivities reported in Fig. 4.8. The figure demonstrates a linear response, with no signs of saturation.

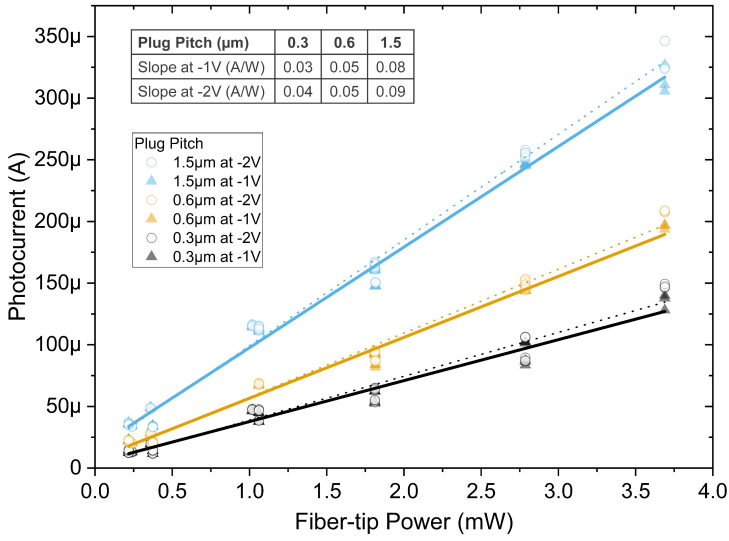

Figure 4.11: Photocurrent vs. fiber-referred power of the devices in site B that are longer than the absorption length. Grouped and linearly fitted for each bias voltage and contact plug pitch. (inset) Table of linear fitting slopes for each case.

4.2.2.4 Length Dependence

The absorption coefficients and lengths of NRWPD devices can be extracted from measurements on shorter devices. For this study, another subset of NRWPD devices with shorter lengths from site B was measured. This subset included the devices with 0.3, 0.6, 1.5 μm p-contact plug pitches and 5, 20, 45, 95, 120 μm lengths.

The length dependent responsivity can be written with an exponential saturation formula based on the Beer-Lambert law:

$$R(x[um]) = R_{sat}(1 - e^{-\alpha x}) \tag{4.4}$$

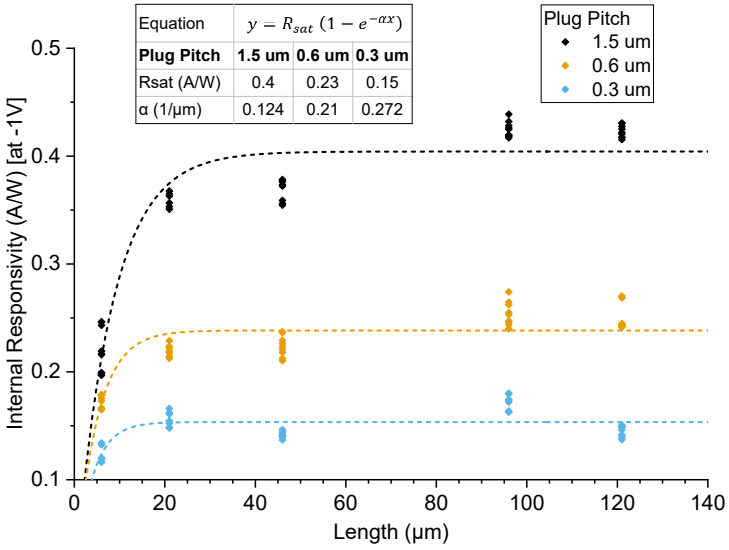

Figure 4.12: Internal responsivity vs. length at -1 V of devices measured at nominal input power in site B. Data points are grouped with respect to contact plug pitch. Fitting is based on an exponential saturation formula based on the Beer-Lambert Law. Both absorption coefficients and maximum responsivities were observed to be dependent on the contact plug pitch. (inset) Table with fitting equation and extracted parameters of R_{sat} and α absorption coefficient.

where R_{sat} is the maximum responsivity and α ($1/\mu m$) is the absorption coefficient. The absorption coefficient can be separated as:

$$\alpha = \alpha_{MQW} + \alpha_{metal} + \alpha_{FCA} \tag{4.5}$$

where α_{MQW}, α_{metal}, α_{FCA} are the MQW, metal, and free carrier absorption coefficients, respectively. Measured internal responsivities of the short-length devices in site B at -1 V are fitted with this equation (Fig. 4.12). The results reveal the contact plug pitch dependence of both maximum responsivity (R_{sat} of the fitting) and extracted total absorption coefficient α. Based on the fitted α values for different plug densities, an absorption coefficient of 0.088 $1/\mu m$ is found for the nano-ridges without p-contact plugs (α_{MQW} + α_{FCA}). This is in good agreement with the MQW modal absorption (α_{MQW}) of 0.072 $1/\mu m$ of fundamental TE mode, calculated in optical mode simulations. The absorption coefficient of 0.088 $1/\mu m$ results in a 99% absorption length as 53 μm. Beyond this length, all the input light is assumed to be absorbed. This absorption length gets shorter for higher plug densities due to metal losses.

4.3 High Speed Performance

The dynamic response of p-i-n photodetectors is typically limited by the resistor-capacitor (RC) constant and the carrier transit time. The overall 3-dB bandwidth of a device can be written as [1]:

$$f_{3dB} \sim \frac{1}{2\pi}\sqrt{\frac{1}{\tau_{RC}^2+\tau_{transit}^2}} = \sqrt{\frac{1}{1/f_{RC}^2+1/f_{transit}^2}} \tag{4.6}$$

Our study of the NRWPD's high-speed performance was limited due to the lack of a lightwave component analyzer (LCA) compatible with the NRWPD operating wavelength at 1020 nm. The measurements therefore were limited to S11 response measurements for extracting the RC bandwidth. In addition, simulation studies were carried out on the opto-electrical AC response for extracting carrier bandwidth and improving the RC bandwidth with modifications of the device cross-section.

4.3.1 Opto-electrical Simulations for Transit Time Calculations

For NRWPDs, the simulations suggest that carriers generated in the InGaAs MQW region experience electric fields of ~50 kV/cm and attain drift velocities of 0.8×10^7 cm/s [2] and 1.0×10^7 cm/s [3], for electrons and holes respectively. Considering transit lengths smaller than 200 nm in the intrinsic region of the NRWPD, a back-of-envelope calculation gives the carrier transit time-related bandwidth exceeding 100 GHz. It is not expected to be a limiting factor for the high-speed performance of NRWPDs. To verify this calculation and observe carrier dynamics at the device cross-section opto-electrical co-simulations were completed.

The opto-electrical co-simulation method described in chapter 3, subsection 3.3.3, was utilized to calculate the carrier transit time bandwidth of the NRWPD devices. First in the simulation, the device cross-section was biased at -1 V at steady state. Later, the optical generation in the InGaAs MQW region was perturbed in an AC small-signal analysis method up to 1 THz frequency as $G^{opt} + \delta G^{opt} e^{i\omega t}$, where $\omega = 2\pi f$ and δG^{opt} is the small signal perturbance amplitude. For each defined frequency step, the device output current perturbation response (δI_{dev}) was recorded in the forms of optical conductance G_{opt} (not to be confused with the optical generation denoted above with G^{opt}) and optical capacitance C_{opt} responses by the simulation software as [4]:

$$G_{opt} = \frac{Re[\delta I_{dev}(f)]/q}{\delta P^{tot}\lambda/hc} \tag{4.7}$$

$$C_{opt} = \frac{1}{\omega}\frac{Im[\delta I_{dev}(f)]/q}{\delta P^{tot}\lambda/hc} \tag{4.8}$$

For the high-speed response of optically-generated carrier collection, we are interested in the absolute output current perturbation response ($|\delta I_{dev}|$) per frequency. But this value is embedded in the optical conductance G_{opt} and capacitance C_{opt} responses of the software tool, hence it needs to be calculated externally. $|\delta I_{dev}|$ can be extracted through absolute admittance. The absolute photo-admittance response is calculated with:

$$|Y| = \sqrt{G^2 + B^2} \tag{4.9}$$

where

$$B = 2\pi f C \tag{4.10}$$

which gives:

$$|Y_{opt}(f)| = \frac{\delta I_{dev}(f)/q}{\delta P^{tot}\lambda/hc} \tag{4.11}$$

Suppose the frequency-dependent photo-admittance is normalized to the DC zero-frequency response. In that case, the output becomes the normalized frequency response of the device to the optical generation perturbation in the MQW volume, which can be given as:

$$\Delta Y_{opt}(f) = \frac{|Y_{opt}(f)|}{|Y_{opt}(0)|} = \frac{\delta I_{dev}(f)}{\delta I_{dev}(0)} \tag{4.12}$$

Scaling in log scale, the 3-dB drop point gives the carrier bandwidth response of the device cross-section. As shown in Fig. 4.13, the photocurrent response of 100 nm trench width NRWPD device has 3-dB bandwidth of ∼155.4 GHz.

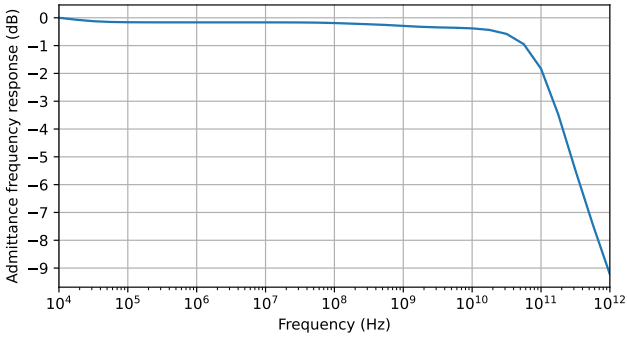

Figure 4.13: The simulated photo admittance frequency response of 100 nm trench width NRWPD device cross-section simulated at −1 V DC bias voltage. The device simulation measured the frequency response at the anode/cathode pair while the photocurrent generation in MQW was perturbed. This response gives the simulated carrier transit time response of the device.

4.3.2 High Speed Electrical Measurements

The S11 response of the NRWPD devices was measured using a 50 GHz vector network analyzer (VNA) (Keysight N5225A PNA Microwave Network Analyzer) in a 1-port configuration to assess the RC bandwidth. Prior to each measurement group, the VNA was calibrated with tool- and probe-specific open/short/load samples. These measurements were carried out on a non-cleaved device where RF pads with and without NRWPD devices were available, as specified in chapter 3, subsection 3.4.2. Cross-sections of these devices are given in Figs. 4.14, 4.15.

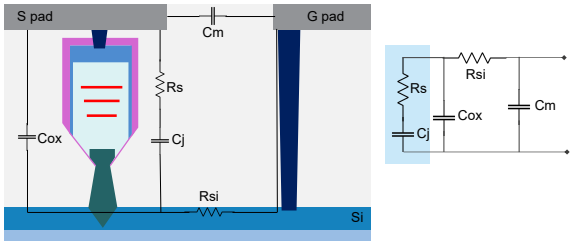

Figure 4.14: Equivalent NRWPD circuit model for high-speed analysis.

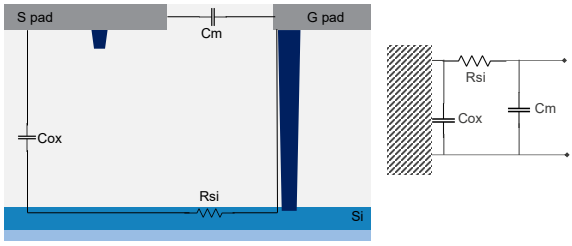

Figure 4.15: Open circuit condition where NRWPD devices are removed for Cox, Rsi, and Cm extraction.

The open circuit measurement helps to decouple the external pad effects and accurately extract device series resistance (R_s) and junction capacitance (C_j). Metal capacitance (C_m), silicon resistance (R_{Si}), and oxide capacitance (C_{ox}) are extracted from the open reference cross-section configuration. With those parameters, the circuit model fitting, with an R-square of 0.996, on the NRWPD's S11 response gives the estimated series resistance (R_s) and junction capacitance (C_j). The S11 response and the fitting are given in Fig. 4.16.

For an NRWPD device with 0.3 μm contact plug pitch and 150 μm length at -1 V bias, we find nominal values of C_j = 91 fF and R_s = 884 Ohm, respectively, resulting in an intrinsic RC-limited opto-electrical bandwidth of 1.9 GHz. Overall fitting ranges for 0.3 μm contact plug pitch devices are given in Table 4.1. Based on a ~23 kOhm ($\pm$ 10%) contact resistance per plug obtained from transfer length

Parameter	Unit	Min	Typical	Max
C_{ox}	fF	102	122	162
C_m	fF	17	22	33
R_{Si}	Ohm	56	72	86
C_j	fF	55	91	105
R_s	Ohm	760	880	2300
f_{RC}	**GHz**	**1.1**	**1.9**	**2.5**

Table 4.1: Extracted high-speed circuit parameter values

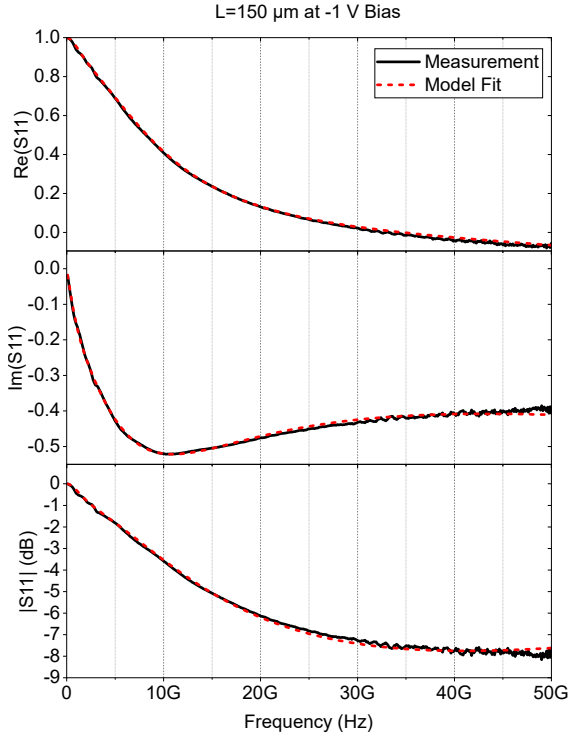

Figure 4.16: Sample AC fitting, S11 response of a 150 μm long NRWPD at -1 V bias and fitting based on the simplified equivalent circuit.

method measurements ($\sim 3.41 \times 10^{-6}$ Ohm.cm^2 contact resistivity for $\sim$90 nm of plug width and $\sim$30 nm plug depth into the p-type doped GaAs), this extrapolates to 1.1 GHz for the 4.8 μm contact plug pitch case.

4.3.3 Electrical RC Simulations

A strong potential exists for higher bandwidth operation in future NRWPD devices. The junction capacitance can be reduced in the next generation devices by carefully optimizing the device cross-section and eliminating the p-doped GaAs sidewalls. The optimization of the contacting and p-type doping profile can reduce the series resistance.

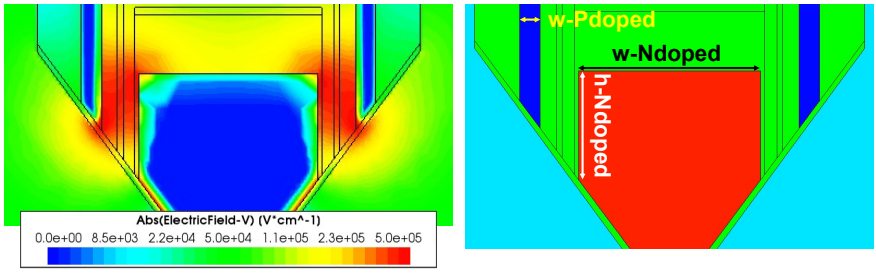

Figure 4.17: (left) Simulated E-field response at −1 V zoomed in the bottom portion of the nano-ridge where the field is localized. (right) Denotation of size parameters given in Fig. 4.18, applied in the AC simulations for R_s and C_j.

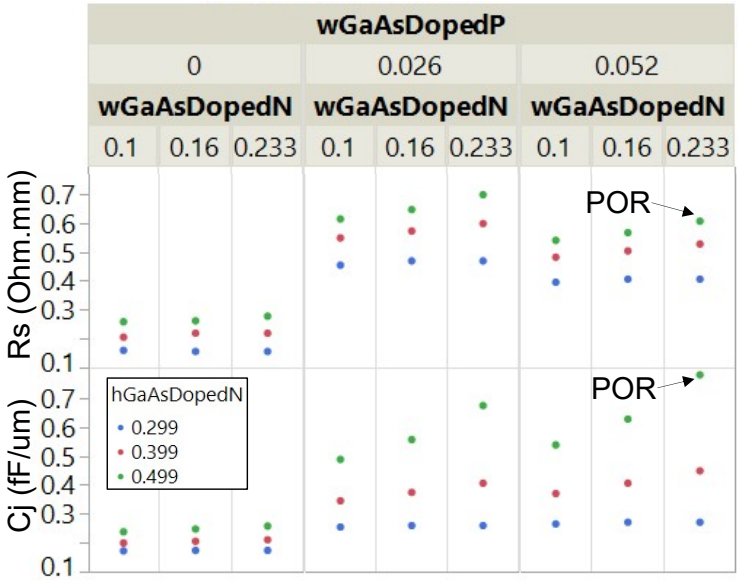

Figure 4.18: Series resistance and junction capacitance found in RC optimization simulations.

In order to numerically characterize these future design changes, a set of device

simulations was completed to explore the effects of cross-sectional dimensions on the RC parameters. As seen in the device simulation results in Fig. 4.17, the extreme localization of the E-field at the bottom side intrinsic GaAs region suggests the p-doped GaAs sidewalls critically increasing the junction capacitance (C_j). Along with the p-doped GaAs sidewall width (denoted as *"GaAsDopedP"* in the simulation results Fig. 4.18), the n-doped GaAs region width (*"wGaAsDopedN"*) and height (*"hGaAsDopedN"*) were also modified around the point of reference (POR) values of measured devices. The POR values were found approximately from the scanning spreading resistance microscopy (SSRM) measurements on NRWPD devices with 100 nm trench width.

The p-doped sidewalls have the greatest impact on the RC response of the devices. As shown in Fig. 4.18, reducing the sidewall thickness to 0 improves the junction capacitance and series resistance by approximately 2.5 times and 2 times, respectively. Removing the p-doped GaAs sidewalls allows for a more uniform distribution of the electric field in the active volume, effectively redistributing the carrier mobility paths and reducing the series resistance and junction capacitance. In the best-case scenario of the simulation parameter space, where the n-doped volume width is 100 nm and the height is 300 nm, and the p-doped sidewalls are removed, the $R_s \cdot C_j$ product is reduced by approximately 20 times, extending the RC bandwidth of the NRWPDs to approximately 38 GHz.

4.4 Benchmark to Other Monolithic Photodetector Devices Grown on Si

In this section, the NRWPD devices are benchmarked with respect to Ge and III-V materials-based photodetector devices monolithically integrated on Si. The other integration approaches mentioned in Chapter 2, such as flip-chip bonding of prefabricated devices [5], or heterogeneous integration of externally grown III-V layers through die-to-wafer bonding [6] [7], have different III-V stack construction and integration schemes that make it challenging to have a fair comparison with the monolithic approach.

The benchmark study considered bias voltage (V_{op}), operation wavelength (λ_{op}), device bandwidth (BW_{op}), responsivity (R), quantum efficiency (η), and dark current density (J_{dark}). The reported parameters are given in Table 4.2.

The germanium-based monolithically grown photodetectors reported by H. Chen et al. in 2016 [8] attained 0.93 A/W responsivity and 67 GHz bandwidth at -1 V bias and 1310 nm wavelength, while the dark current density was reported at 3.4×10^{-2} A/cm^2. The selective-area grown bulk Ge was placed on top of a Si/poly-Si waveguide where a p-i-n junction was formed.

III-V material-based PD studies listed in Table 4.2 can be divided according to

Ref.	Year	Mat.	V_{op} (V)	λ_{op} (nm)	BW_{op} (GHz)	R (A/W)	η	J_{dark} (A/cm^2)
[8]	2016	Ge	-1	1310	67	0.93	88%	3.4×10^{-2}
[9]	2017	III-V	-1	1250	2.3	0.9	89%	0.8×10^{-4}
[10]	2018	III-V	-3	1310	5.5	0.08	7%	1.3×10^{-4}
[11]	2018	III-V	-3	1550	9	0.79	63%	8.0×10^{-4}
[12]	2019	III-V	-1	1300	N\A	0.26	25%	3.5×10^{-7}
[13]	2020	III-V	-5	1310	2.3	0.234	22%	6.6×10^{-5}
[14]	2020	III-V	-3	1550	28	0.27	22%	1.0×10^{-1}
[15]	2020	III-V	-2	850	N\A	0.17	34%	4.5×10^{-7}
[16]	2020	III-V	-1.5	1346	25	0.4	37%	1.4×10^{0}
[17]	2020	III-V	-2	1346	25	0.68	47%	2.8×10^{0}
[18]	2020	III-V	-0.5	1550	N\A	1.06	85%	3.3×10^{-2}
[19]	2020	III-V	-1	1020	N\A	0.25	30%	1.4×10^{-5}
[20]	2021	III-V	-1	1310	40	0.8	32%	1.1×10^{-2}
[21, 22]	2022	III-V	-1	1310	52	0.4	16%	4.8×10^{-4}
[23]	2022	III-V	-1	1320	70	0.2	19%	4.8×10^{-2}
[24, 25]	'20,'21	III-V	-2	1020	1.9	0.68	**83%**	**1.9×10^{-8}**

Table 4.2: The benchmark of dark current densities and other performance metrics of photodetectors monolithically integrated on Si. The results detailed in this chapter are summarized in the last row.

the growth approach: blanket layer or selective-area epitaxy. Of these integration methods, monolithic integration based on selective-area growth arguably has the most potential for enabling the highest integration throughput and the lowest cost.

The blanket growth study of Y. Wan et al. in 2017 [9] comprised a buffered GaAs growth on V-grooved Si, with InAs/InGaAs quantum dots (QDs) as active media, achieving 0.9 A/W responsivity, 2.3 GHz bandwidth at -1 V bias and 1250 nm wavelength, with J_{dark} of 0.8×10^{-4} A/cm^2. The buffered blanket InAs/InGaAs QD PD growth of D. Inoue in 2018 [10] achieved 0.08 A/W responsivity, 5.5 GHz bandwidth at -3 V bias and 1310 nm wavelength, with J_{dark} of 1.3×10^{-4} A/cm^2. The top illuminated p-i-n (or PIN) and modified uni-traveling carrier (MUTC) PDs of K. Sun et al. in 2018 [11] were blanket grown on Si with InGaAs/InAlAs/InP active stack achieved 0.79 A/W responsivity, 9 GHz bandwidth at -3 V bias, and 1550 nm wavelength, with J_{dark} of 8.0×10^{-4} A/cm^2. Another GaAs blanket growth on V-grooved Si as buffer layer for InAs/InGaAs QD PDs of J. Huang et al. in 2019 [12], achieved 0.26 A/W responsivity at -1 V bias and 1300 nm wavelength, with very low J_{dark} of 3.5×10^{-7} A/cm^2. The InAs QD avalanche photodetectors (APDs) of B. Chen et al. in 2020 [13] grown with blanket GaAs buffer on V-grooved Si, achieved 0.234 A/W responsivity, 2.3 GHz bandwidth at -5 V bias and 1310 nm wavelength, with J_{dark} of 6.6×10^{-5} A/cm^2.

The high-speed waveguide MUTC PDs of K. Sun et al. in 2020 [14], were blanket grown with buffer layer and InGaAs/InAlGaAs active III-V stack, and achieved 0.27 A/W responsivity, 28 GHz bandwidth at -3 V bias and 1550 nm wavelength, with J_{dark} of 1.0×10^{-1} A/cm^2. GaAs p–i–n photodetectors blanket grown on 300-mm Si wafers of H. Mehdi et al. in 2020 [15], achieved 0.17 A/W responsivity at -2 V bias and 850 nm wavelength, with J_{dark} of 4.5×10^{-7} A/cm^2.

The InGaAs p-i-n PDs selective-area laterally grown with template-assisted selective epitaxy (TASE) of S. Mauthe et al. in 2020 [16], [17] achieved 0.4 A/W and 0.68 A/W responsivities, 25 GHz bandwidth, and 1.4×10^{0} A/cm^2 and 2.8×10^{0} A/cm^2 of J_{dark} at -1.5 V and -2 V biases, respectively, and at 1310 nm wavelength.

Another selective-area growth of III-V photodetectors on Si was reported by Y. Xue et al. in 2020 [18], where aspect ratio trapping (ART) was utilized for the growth starting on V-grooved Si SAG templates. The PDs constructed with InGaAs/InP MQW active stack achieved 1.06 A/W responsivity at -0.5 V bias and 1550 nm wavelength, with J_{dark} of 3.3×10^{-2} A/cm^2.

Our earlier study on NRWPDs with top regrown p-GaAs fin in 2020 [19] achieved 0.25 A/W responsivity at -1 V bias and 1020 nm wavelength, with J_{dark} of 1.4×10^{-5} A/cm^2.

Y. Xue et al. in 2021 [20] and 2022 [21], [22], utilized a lateral growth technique employing TASE and ART methods for a p-i-n InGaAs PD device with InP buffer on silicon-on-insulator (SOI) substrate. The early standalone PD device in 2021 [20] achieved 0.8 A/W responsivity, 40 GHz bandwidth at -1 V bias and 1310 nm wavelength, with J_{dark} of 1.1×10^{-2} A/cm^2. Their later effort on Si waveguide integration of the III-V PD grown on Si with the same method [21], [22], achieved 0.4 A/W responsivity, 52 GHz bandwidth at -1 V bias and 1310 nm wavelength, with J_{dark} of 4.8×10^{-4} A/cm^2.

P. Wen et al. in 2022 [23] further extended the lateral growth with TASE efforts of S. Mauthe et al. [16], [17] by growing the PD stack perpendicular to incoming Si waveguide direction. They employed an n-InP/i-InGaAs/p-InP/p-InGaAs active stack and achieved 0.2 A/W responsivity, 70 GHz bandwidth at -1 V bias and 1320 nm wavelength, with J_{dark} of 4.8×10^{-2} A/cm^2.

The comparison given in Table 4.2 shows that no single study offers the best performance in all metrics for III-V PDs grown on Si. While P. Wen et al. [23] showed the highest bandwidth of 70 GHz, their responsivity was limited at 0.2 A/W. [18] reported the highest responsivity of 1.06 A/W while their study lacked the bandwidth analysis and direct Si waveguide integration approach. As the best compromise, Xue et al.'s work in 2022 [21] offered high performances in all performance metrics and direct Si waveguide integration. Compared with other works, our study resulted in the record-low dark current density of III-V photodetectors monolithically grown on Si. With an internal quantum efficiency of 79%

and a responsivity of 0.65 A/W, it has significant performance. As a drawback, the operation at a non-telecom wavelength of 1020 nm and limited bandwidth due to high RC time constant show that NRWPD devices have room for improvement.

4.5 Conclusion

We reported high-quality InGaAs/GaAs MQW p-i-n nano-ridge waveguide photodetectors, monolithically integrated in a 300-mm Si pilot line through selective-area epitaxial growth with aspect-ratio trapping and nano-ridge engineering. At 1020 nm wavelength, the photodetectors with the lowest contact density exhibit an internal responsivity of 0.65 A/W or 79% internal quantum efficiency. A detailed analysis of the responsivity dependence on device length and metal contact pitch and a good correlation with simulation models are reported.

In addition, a record-low dark current density of 1.98×10^{-8} A/cm^2 is reported at -1 V bias, illustrating the high material quality of the InGaAs/GaAs structures as well as the effective InGaP passivation. Finally, initial RF measurements and electric-field simulations suggest that the bandwidth in current devices is predominantly limited by the RC constant and is estimated to be 1.1 - 1.9 GHz. In summary, this work illustrates the potential of the III-V nano-ridge epitaxy concept to integrate high-quality III-V waveguide devices directly on Si.

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5

Leakage Mechanisms of InGaAs/GaAs Nano-ridge Waveguide Photodetectors[1]

5.1 Introduction

In the previous chapter, the nano-ridge waveguide photodetectors (NRWPD) were shown to exhibit extremely low dark currents, smaller than 1 pA at room temperature [1]. These extremely low dark currents are promising for many photonic applications, offering better sensitivity and lower power consumption. However, the actual leakage mechanisms dominating the performance of these devices have not been explored yet. In addition, like many other photonic devices, III-V devices monolithically grown on Si will be required to operate at elevated temperatures [2], especially when the photonic integrated circuits (ICs) are integrated with high-performance electronics. The degradation of device performance due to defects then becomes an issue. Higher defect densities resulting from the metamorphic growth of III-V devices on Si make these devices susceptible to additional leakage mechanisms at higher operating temperatures. Therefore, it is crucial to study the leakage behavior of monolithically grown III-V devices at elevated temperatures to validate the epitaxial growth quality. An early understanding of the leakage behavior will also help ensure such devices' reliability and longevity under extreme conditions. In addition, these studies will enable the development of noise

[1] Some of the content of this chapter was published in Ozdemir et al., "Leakage Mechanisms of sub-pA InGaAs/GaAs Nano-Ridge Waveguide Photodetectors Monolithically Integrated on a 300-mm Si Wafer," J. Phys. D: Appl. Phys. (2024).

Design Parameter	Unit	Reported Device Parameters
Plug pitch	μm	0.3,0.6,1.5
Waveguide width	nm	490
Waveguide height	nm	540
Trench width	nm	100
Trench height	nm	300
Device length	μm	100

Table 5.1: Geometrical parameters of devices studied in this work.

mitigation strategies and further optimized designs for high-performance devices.

In this study, we measured the dark current at elevated temperatures and correlated these measurements with numerical simulations using technology computer-aided design (TCAD) simulations [3] to resolve the dominant leakage mechanisms. In the simulation, we included different leakage models, including both surface and bulk related Shockley-Read-Hall (SRH) recombination, Auger recombination, and radiative recombination. SRH recombination through deep defects in the bulk III-V volume contributes significantly to the total dark current. Under reverse bias, however, the effect of surface recombination is shown to remain limited. Under forward bias, on the other hand, surface leakage at the unpassivated bottom side surfaces becomes significant. Overall, the NRWPD devices exhibit excellent dark current performance, also at high temperatures, with median dark currents of 0.1 nA at 195 °C and -1 V bias. Backpropagating the TCAD leakage model to room temperature, where the device measurements are limited by the noise floor of the measuring tools, suggests the real dark currents can be as low as 0.01 pA.

5.1.1 Studied Subset Device Properties

The study on the dark currents and leakage mechanisms of NRWPD devices detailed in this chapter was completed on a subset of devices with the parameters given in Table 5.1. The study was based on 100 nm trench-width NRWPDs with 100 μm length. The 100 μm-long devices from site B described in Chapter 3 have p-contact plug pitches of 0.3, 0.6, and 1.5 μm. The 100 nm trench width and 100 μm length were picked as the design reference based on the responsivity performance of NRWPDs, detailed in Chapter 4. InGaAs/GaAs MQW NRWPD devices from 13 different dies (39 devices in total) were characterized in this study.

5.2 Experimental Results

5.2.1 Photoluminescence Measurements

Initially, the PL spectrum and the peak-emission time-resolved PL signal (tr-PL) were measured. Figure 5.1 shows a photoluminescence (PL) spectrum taken at room temperature under surface illumination. The peak emission wavelength at 1030 nm and the band-edge at 1110 nm confirm the target QW composition of $In_{0.22}Ga_{0.78}As$ and thickness of 10 nm were attained. The Si PL peak is not observed at this low pump intensity. The inset of Figure 5.1 shows the time-resolved PL signal (tr-PL) at 1030 nm wavelength together with a fit to a one-term exponential model [4]:

$$I_{tr-PL}(t) = A \cdot e^{\frac{-(t-t_0)}{\tau_{PL}}} \tag{5.1}$$

We found $\tau_{PL} \cong 1.95$ ns. Both the PL-spectrum and the tr-PL trace were taken under pulsed illumination at 532 nm wavelength, with a 15 kHz repetition rate and $<$1 ns pulse duration. The pump intensities were 0.3 W/cm^2 and 0.03 W/cm^2, respectively (Hamamatsu C12350-11).

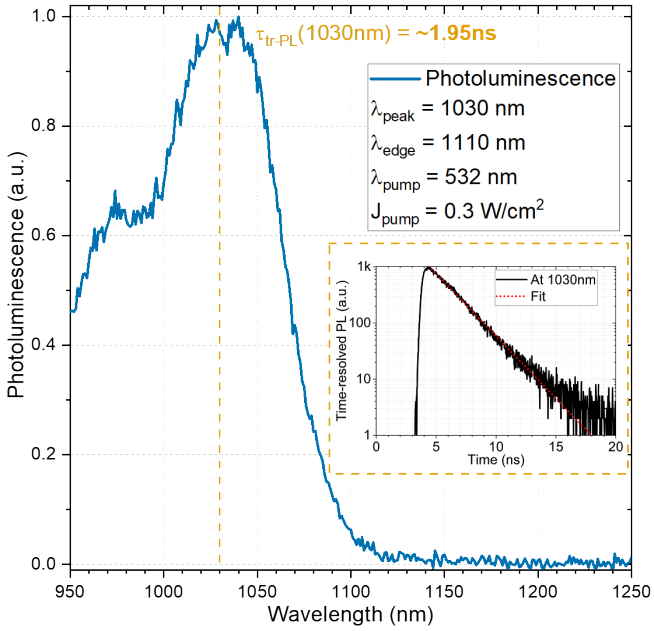

Figure 5.1: Photoluminescence of the quantum wells, pumped with 532 nm, 15 kHz pulsed laser with 0.3 W/cm^2 intensity. The secondary peak around 975 nm is from the E2-H2 transition. (inset) Time-resolved photoluminescence response at 1030 nm and one-term exponential fitting, logarithmic scale.

5.2.2 Dark Current-Voltage Measurements at Elevated Temperatures

The current-voltage (I-V) response of a p-i-n diode allows extraction of crucial device performance metrics such as the series resistance, the diode rectification, the leakage current at various bias voltages, the activation energy, and the diode ideality factor. I-V measurements at elevated temperatures furthermore enable the analysis of the detailed leakage current characteristics and extraction of activation energies [5], [6].

InGaAs/GaAs MQW NRWPD devices from 13 different dies (39 devices in total) were electrically characterized using a 300-mm wafer prober. The measurements were completed on 2 different electrical characterization tools (1. Keysight 3858A Digital Multimeter, 2. Keysight B1500A Semiconductor Device Analyzer) for the temperature ranges of 25 °C to 125 °C, and 135 °C to 195 °C, respectively.

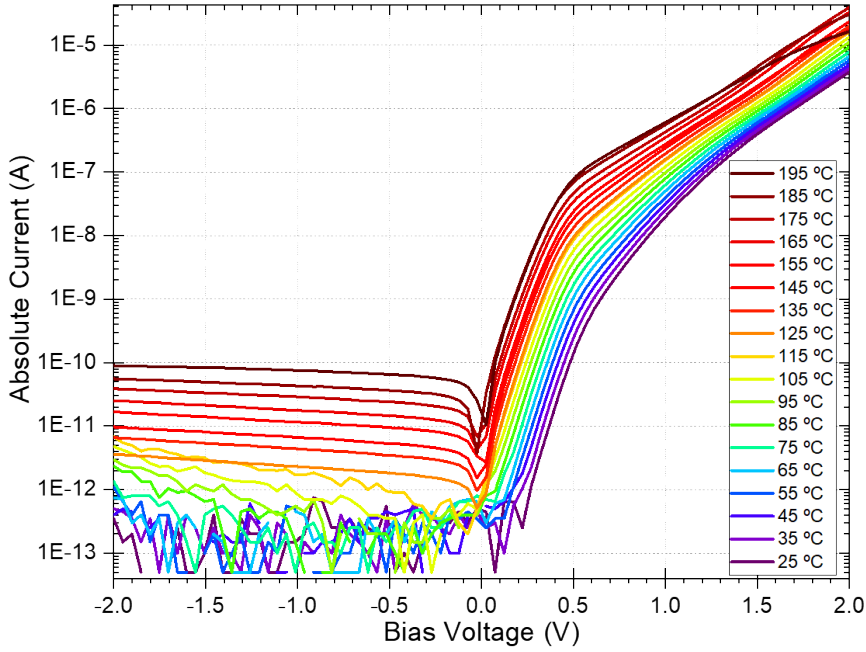

Figure 5.2: Dark current-voltage response of a 100 μm long NRWPD device at ambient temperatures varying from 25 °C to 195 °C.

The typical I-V response of a 100 μm long device is shown in Fig. 5.2. At 25 °C, a rectification of more than 6 orders of magnitude was observed between -2 and $+2$ V, indicating a p-i-n diode behavior. For temperatures below 105 °C, the dark current measurements under reverse bias were limited by the 1 pA noise floor

of the measuring tool (Keysight 3858A Digital Multimeter). Above 105 °C, the leakage current started to increase. This behavior is also visible in Fig. 5.3, which shows the dark current statistics for all measured 100 μm long devices (at -1 V bias). The effects of p-contact plug pitch variations were found to be negligible at both reverse and forward subthreshold bias ranges.

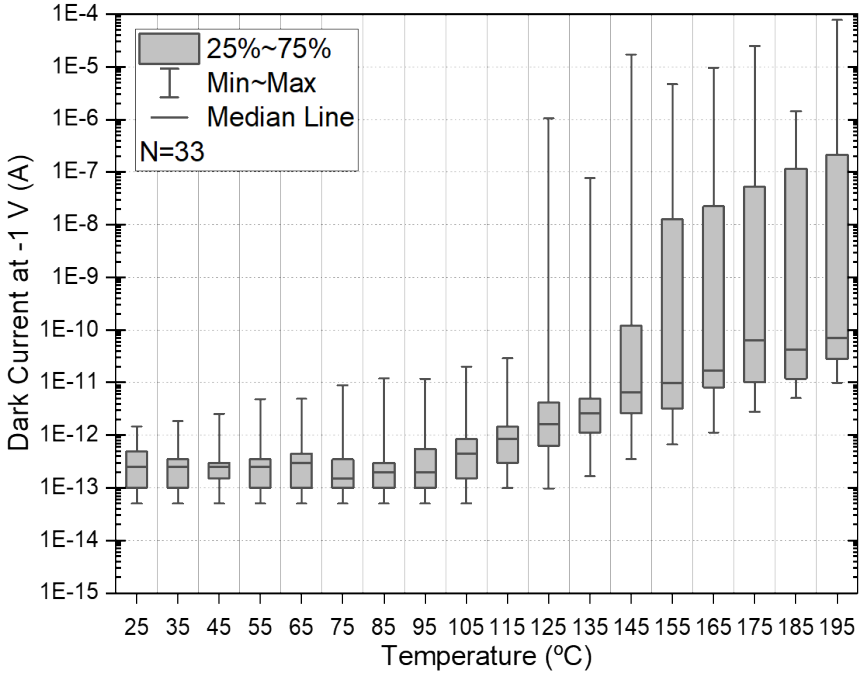

Figure 5.3: Dark currents measured at -1 V bias point of 100 μm long devices (N=33) at varying ambient temperatures from 25 °C to 195 °C. The noise floor of the measurement tool is reported as 1 pA.

5.2.2.1 Parameter Extractions

In the case of recombination-dominated leakage currents, the activation energies at different bias voltages can be extracted through the following formula [5], [7]:

$$I_{dark} = CT^{3/2}e^{-E_a/kT}(e^{qV_a/2kT} - 1) \tag{5.2}$$

where C is a constant, E_a is the activation energy, V_a is the bias voltage, and k is the Boltzmann constant. For a given bias voltage, this formula gives the Arrhenius

relation:

$$E_a \propto \frac{\ln(I_{dark}/T^{3/2})}{1/kT} \tag{5.3}$$

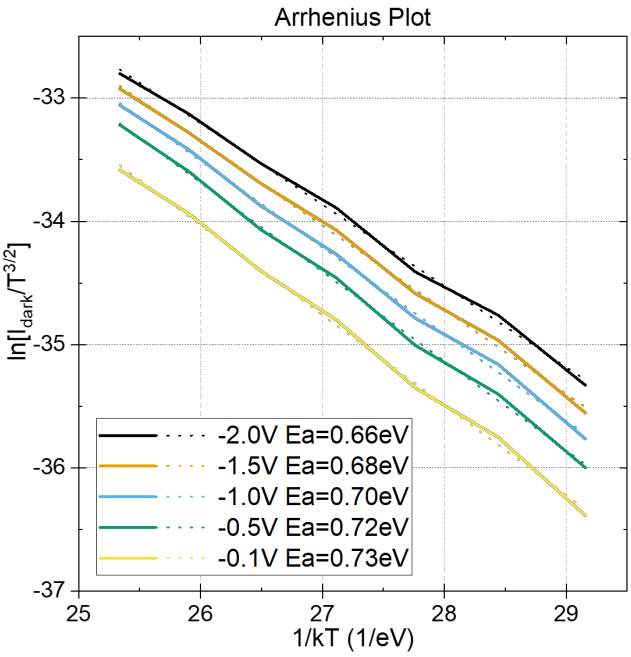

Figure 5.4: Arrhenius plot of nano-ridge waveguide photodetector devices at various reverse bias points.

Fig. 5.4 shows that the activation energies extracted at reverse bias voltages varying from -2.0 to -0.1 V range from 0.66 eV to 0.73 eV. The fact that $E_a \sim E_g/2$, with $E_g \cong 1.43$ eV [8] the bandgap of GaAs, points towards SRH recombination as the dominant recombination mechanism [9].

The ideality factor (η) of the p-i-n diode was extracted from the forward subthreshold bias region ($0.0 - 0.5$ V) of the I-V curves at different temperatures, following the simplified relation [10]:

$$J_F \propto e^{qV_a/\eta kT} \tag{5.4}$$

where J_F is the forward bias current density. For the whole temperature range between 25 °C and 195 °C, the ideality factors ranged between 1.81 to 2.11 as shown in Fig. 5.5. The ideality factor near the value of 2 indicates recombination-dominated currents in this bias region [10].

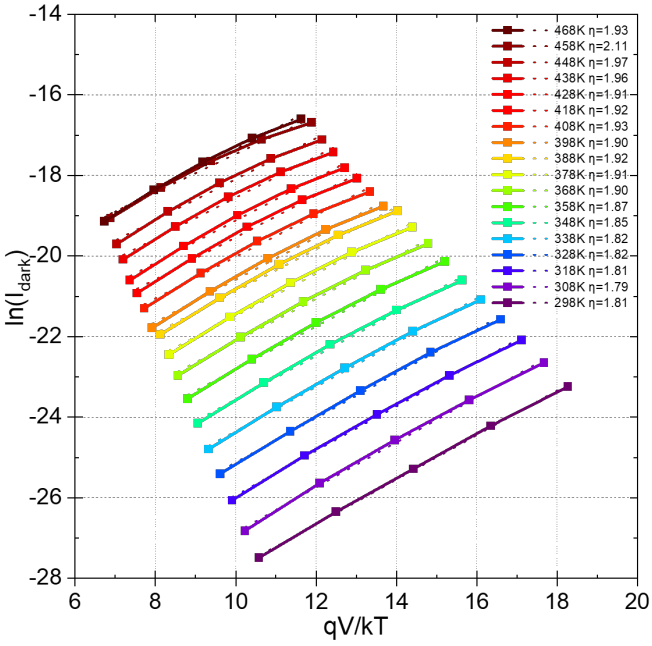

Figure 5.5: Extraction of the ideality factor (η) from the forward subthreshold bias region current response at ambient temperatures from 25 °C (298 K) to 195 °C (468 K).

5.3 Modeling

5.3.1 Theoretical Overview of Studied Models

The devices were modeled using the Sentaurus Device software [3]. For simulating the PL response, a cross-section without top contact plugs was used (Fig. 5.6a). For simulating the full electrical behavior also, the contact plugs were taken into account (Fig. 5.6b). Based on the activation energy and ideality factor extracted in the previous section, we focused on recombination-driven leakage currents and, in particular, on SRH recombination. The volume and surface SRH recombination are implemented in Sentaurus Device TCAD through the following formulas, respectively [3]:

$$R_{BulkSRH,net} = \frac{np - n_{i,eff}^2}{\tau_p(n + n_1) + \tau_n(p + p_1)} \tag{5.5}$$

$$R_{SurfSRH,net} = \frac{np - n_{i,eff}^2}{(n + n_1)/s_p + (p + p_1)/s_n} \tag{5.6}$$

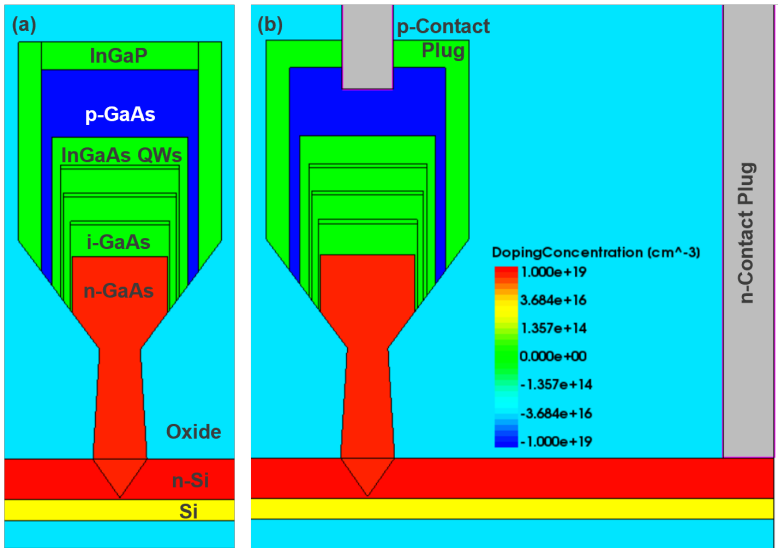

Figure 5.6: 2D cross-sections for (a) PL simulations & (b) Electrical simulations. Coloring indicates the doping concentration.

with:

$$n_1 = n_{i,eff} exp\left(\frac{\Delta E_{trap}}{kT}\right) \tag{5.7}$$

$$p_1 = n_{i,eff} exp\left(\frac{-\Delta E_{trap}}{kT}\right) \tag{5.8}$$

where ΔE_{trap} is the energy level difference between the modeled defects and the intrinsic levels, n and p are the electron and hole densities, respectively, $n_{i,eff}$ is the effective intrinsic density, τ_n and τ_p are the electron and hole SRH lifetimes, respectively, s_n and s_p are the electron and hole surface recombination velocities, respectively, k is the Boltzmann constant, and T is temperature [3].

In addition to the SRH recombination models, radiative and Auger recombination models were included in the simulations, described respectively as [3]:

$$R_{Radiative,net} = B \cdot (np - n_{i,eff}^2) \tag{5.9}$$

$$R_{Auger,net} = (C_n n + C_p p) \cdot (np - n_{i,eff}^2) \tag{5.10}$$

where B is the radiative recombination coefficient, and C_n and C_p are the electron and hole Auger coefficients, respectively.

Model	Subcomponents	Parameter	Value					Unit	Reference
SRH Bulk	Main	$\tau_{SRH,GaAs}$	0.1[‡]	0.33	1	3.3	10	33[†]	ns	-
		$\tau_{SRH,InGaAs}$	3.2[‡]	2.7	2.6	2.5	2.5	2.5[†]	ns	Sim.
	Temperature Dependence	α	-1.5						-	[11]
SRH Surface	GaAs/Oxide	$S_{GaAs/Oxide}$	1×10^6 (PL simulation) $5 \times 10^5 - 1 \times 10^7$ (electrical simulation)						cm/s cm/s	[12] [12]
		ΔE_{trap}	-0.3						eV	[13]
	InGaP/Oxide	$S_{InGaP/Oxide}$	5×10^4						cm/s	[14]
Auger	GaAs	C_{GaAs}	1×10^{-30}						cm^6/s	[15]
	InGaAs	C_{GaAs}	1×10^{-29}						cm^6/s	[16]
Radiative	GaAs	B_{GaAs}	7.2×10^{-10}						cm^3/s	[15]
	InGaAs	B_{GaAs}	3×10^{-10}						cm^3/s	[15]

Table 5.2: TCAD model studied parameters

5.3.2 Photoluminescence Modeling

The tr-PL response was simulated using the structure shown in Fig. 5.6a, with the parameter values as listed in Table 5.2. Due to the limited conformity of the InGaP passivation layer at the bottom side oblique surfaces, GaAs is assumed to be exposed to oxide at these surfaces in the modeling. With ∼20% total reflection between air to oxide to InGaP and an assumed 100% quantum efficiency, the experimental excitation intensity of 0.03 W/cm^2 was implemented in the simulation as a constant carrier generation in the top InGaP and p-doped GaAs layers with a rate of 2×10^{21} 1/s/cm^2 for a pulse duration of 1 ns. Following this carrier generation step, the transient radiative recombination response in the InGaAs MQW layers was recorded assuming the InGaAs QWs transient radiative response is comparable with the measured tr-PL response of the InGaAs MQWs at 1030 nm. The SRH lifetimes of GaAs and InGaAs were scanned from 0.1 ns to 33 ns (with half-decade steps) to observe the effects on the InGaAs MQW PL lifetime. The transient response of the radiative recombination in the InGaAs QWs was fitted with the following formula to extract the according PL lifetime:

$$U(t) \propto U_0 e^{-\frac{t}{\tau_{radiative}+\alpha\tau}} \tag{5.11}$$

where α is a correction factor obtained through tr-PL measurements as 0.14. The PL lifetimes obtained from this scan are shown in Fig. 5.7. The PL lifetime is observed to be dependent mostly on $\tau_{SRH,InGaAs}$, where $\tau_{SRH,InGaAs}$ is tightly constrained to the range 2.5−3 ns for the ∼2 ns measured τ_{PL}. The extracted τ_{PL} is less sensitive to $\tau_{SRH,GaAs}$, which was varied from 0.5 to 33 ns in the simulation. The dependence of PL lifetimes on $\tau_{SRH,InGaAs}$ can be attributed to localized carriers in InGaAs QW volumes during this event. The SRH lifetime pairs ($\tau_{SRH,GaAs}$ & $\tau_{SRH,InGaAs}$) resulting in an extracted τ_{PL} equal to the measured PL lifetime of 1.95 ns are listed in Table 5.2. Using these as input, we carried out a second set of simulations, focusing on the leakage currents.

5.3.3 Electrical Modeling

For the electrical modeling, we used the structure of Fig. 5.6b, with model parameter values as listed in Tables 5.1 and 5.2, and swept the bias voltage from −2 V to +0.5 V, at different temperature points ranging from between 25 °C and 195 °C.

Initially, we explored the effects of bulk SRH lifetime pairs calculated in the first set of tr-PL simulations, listed in Table 5.2, at 165 °C. This temperature point was a good compromise between the temperature (105 °C) where the dark current first increases above the noise level and the maximum measurement temperature (195 °C) (Fig.4). To visualize trends in the large measured and simulated datasets easily, the dark currents at −1 V and +0.25 V bias points are plotted in Fig. 5.8. The −1 V bias point is the center of the measured negative bias voltage range of

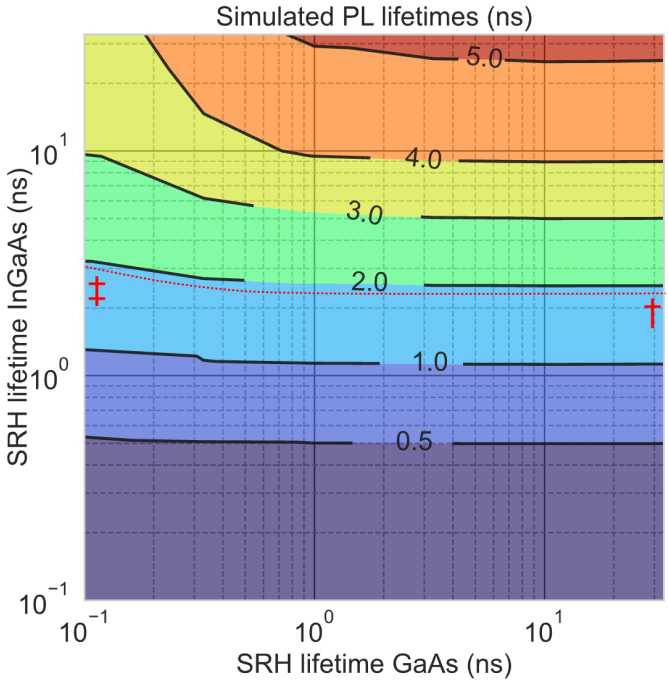

Figure 5.7: Simulated PL lifetime contours extracted from the InGaAs QW volume radiative recombination time decay response in PL simulations with varying SRH lifetimes of GaAs and InGaAs (0.1 to 33 ns). Experiments corresponding SRH lifetime pairs along ∼1.95 ns PL lifetime are listed in Table II. The two extremities of the group of parameters used in the electrical simulations are marked with † and ‡ respectively.

the device. The +0.25 V bias point is in the subthreshold forward bias regime, where the recombination-driven conduction mechanism was observed through the ideality factor analysis.

In Fig. 5.8, the measurement data is indicated by black squares, while the simulations are plotted using colored symbols. Different color groups represent a different surface recombination velocity of the GaAs/oxide surface ($S_{GaAs/Oxide}$). Within each color group, $\tau_{SRH,GaAs}$ and $\tau_{SRH,InGaAs}$ are varied following the values provided in Table 5.2 (with the first and last pairs marked with the † and ‡ symbols, respectively). We notice that, for these simulated data points the leakage currents increase for both reverse and forward biasing when $\tau_{SRH,GaAs}$ increases. This indicates a stronger dependence on $\tau_{SRH,GaAs}$ for the leakage currents, compared to the tr-PL simulation response of the devices, where the effect of $\tau_{SRH,InGaAs}$) is more prominent. The electrical simulations with $\tau_{SRH,GaAs}$ values above 1 ns are close to the measured median dark currents at the reverse

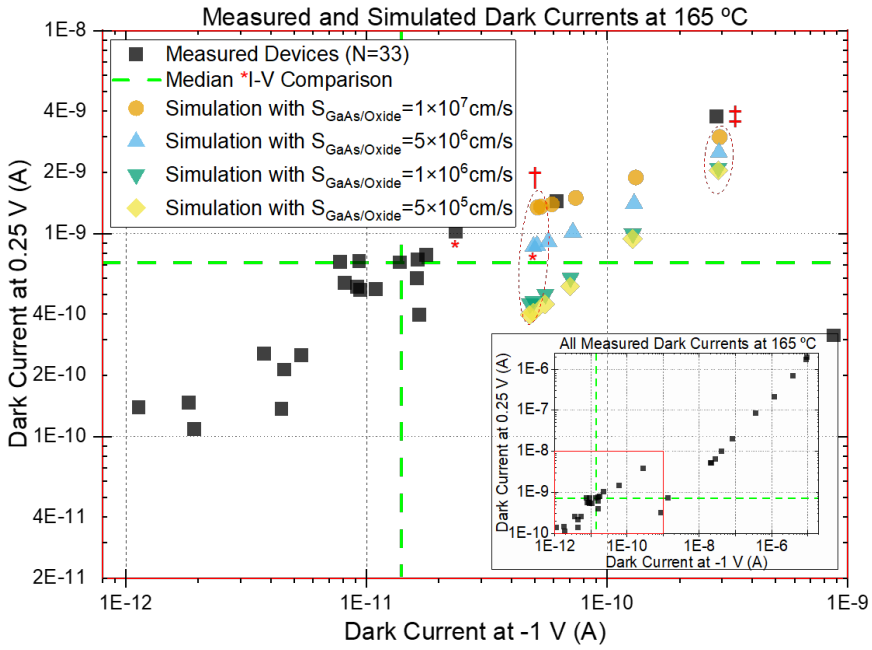

Figure 5.8: Comparison of measured (black) and simulated (colored) devices of 100 μm length, at −1 V and +0.25 V bias points. The main panel shows a subset of the results as marked by the red frame in the inset, which shows all 33 measured devices. The median point of the measurements is marked by the green dashed lines. Simulation results are colored according to the different applied surface recombination velocities, $S_{GaAs/Oxide}$, ranging from 5×10^5 to 1×10^7 cm/s. Each coloured simulation group has $\tau_{SRH,GaAs}$ and $\tau_{SRH,InGaAs}$ pairs as listed in Table 5.2, where the first and last pairs are marked with † and ‡. The $*$ symbol refers to data points for which the detailed current-voltage response is plotted in Fig. 5.11.

and forward biases. The recombination-limited minority-carrier lifetime can be calculated with the dislocation density (N_d) as [17], [18]:

$$\frac{1}{\tau} = \frac{1}{\tau_{max}} + \frac{\pi^3 D_{min} N_d}{4} \tag{5.12}$$

where D_{min} is the minority-carrier diffusion coefficient and τ_{max} is the maximum lifetime without dislocations. For an electron diffusion coefficient of 78 cm^2/s [17], and a misfit defect density below 1×10^6 cm^{-2} (measurement limited) [19], equation 5.12 gives a recombination-limited minority-carrier lifetime above 1 ns, correlating well with our experimental results.

While both the reverse and forward leakage currents of the NRWPD are sensitive to $\tau_{SRH,GaAs}$, the measured forward leakage currents are observed to be

higher than our initial simulation results for $S_{GaAs/Oxide}$ of 1×10^6 cm/s. Therefore we extended the simulation by sweeping the GaAs/oxide surface recombination velocity $S_{GaAs/Oxide}$ over the range $5 \times 10^5 - 1 \times 10^7$ cm/s [12], assuming a surface defect trap displacement level of -0.3 eV [13]. Fig. 5.8 shows that the forward leakage currents are more dependent on the surface recombination variations than the reverse leakage current response. The GaAs/oxide surface at the bottom sidewalls of the NRWPD is close to the side i-GaAs volumes where the intrinsic thickness of the active volume is the shortest. Therefore, the GaAs/oxide surface defects provide a short path to the majority carriers diffusing at forward bias and increase the leakage current via majority carrier recombination at the surface defects.

The leakage current contributions from Auger and radiative type recombination mechanisms for the given model parameters were observed as negligible compared to the SRH-type mechanisms in the bias range of the simulations. The leakage current contributions from the InGaP/oxide surface SRH were also found to be negligible, since the bandgap of InGaP is higher than GaAs, limiting carrier diffusion into the InGaP region. Also, the reported surface recombination velocity of the InGaP/oxide surface is smaller than that of the GaAs/oxide surface, as listed in Table 5.2. Further, there is no clear dependence observed between the top p-contact plug density and the leakage behaviour of the devices, as contributions from this variation were found negligible in the I-V responses at the reverse and subthreshold bias ranges.

The electrical simulations are further expanded to all measured temperature points from 25 °C to 195 °C with the simulation parameters given in Table II. The resulting leakage currents at -1 V are compared with the measured leakage currents of 100 μm long devices in Fig. 5.9. The temperature response of the simulated devices is found to follow the same trend as the measured devices for dark currents above the noise floor of the measurement tool ($>$1 pA). A breakdown of the recombination mechanisms at different temperatures (Fig. 5.10) reveals a strong contribution from InGaAs and GaAs bulk SRH for both reverse and forward bias voltages, while GaAs/Oxide Surface SRH type recombination contributes at forward bias at higher temperatures.

The simulated leakage currents deviate from the measured leakage currents at temperatures below 55 °C, suggesting the real leakage currents are below the measurement limit, with a difference of more than 1-order. The comparison of the I-V responses of a measured and a simulated device is shown in Fig. 5.11, representing the two datasets marked by a $*$ symbol in Fig. 5.8. The strong correlation between the measured and simulated I-V profiles, both in reverse and forward bias regimes, is observed. This shows the proposed model describes the experimental results well.

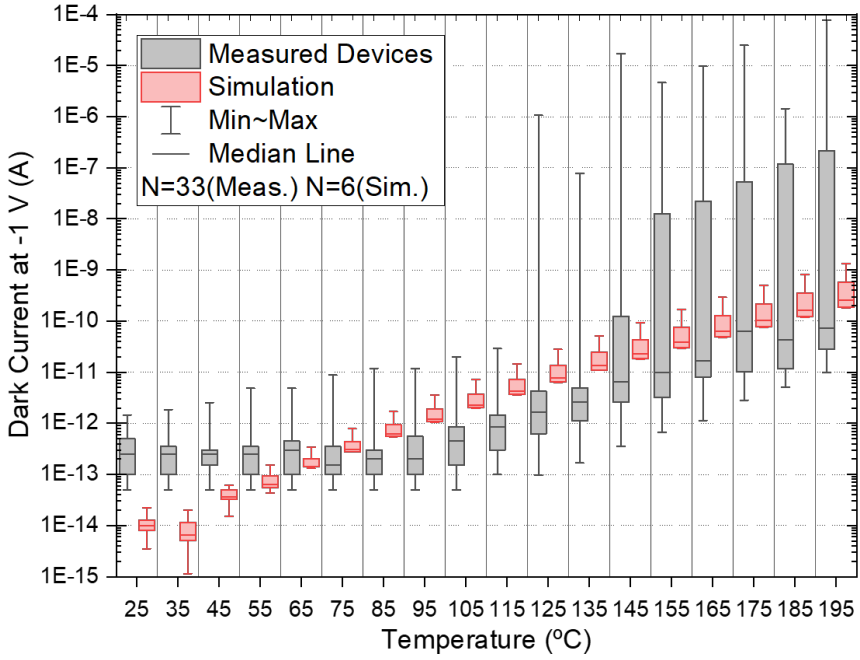

Figure 5.9: Dark currents measured at -1 V bias point of 100 µm long devices (grey, N=33). Simulated dark current responses at SRH lifetime pairs listed in Table 5.2 with 1×10^6 cm/s GaAs/Oxide surface recombination velocity (red, N=6). Grouped at varying ambient temperatures from 25 °C to 195 °C. The noise floor of the measurement tool is reported as 1 pA.

5.4 Conclusion

We reported a comprehensive study of the dark current behavior measured for InGaAs/GaAs MQW nano-ridge photodetector devices monolithically grown on Si. At room temperature the measured dark current is noise-limited, asserting the high material quality. The dark current was measured at elevated temperatures and correlated to TCAD models to reveal the different leakage current components relevant to the devices. The main contribution was found to be SRH-type non-radiative recombination, both in the bulk InGaAs QW and GaAs volumes. At the GaAs/Oxide surface, SRH-type recombination plays a role at subthreshold forward bias voltages. Backpropagating the device model to room temperature suggests the actual dark current to be around 0.01 pA at -1 V bias, more than one order of magnitude below the measured levels, which were limited by the noise level of the experimental setup. For ambient temperatures as high as 195 °C, devices exhibited median dark currents below 0.1 nA, showing the promise of these photodetector devices for a wide range of applications, including interconnects,

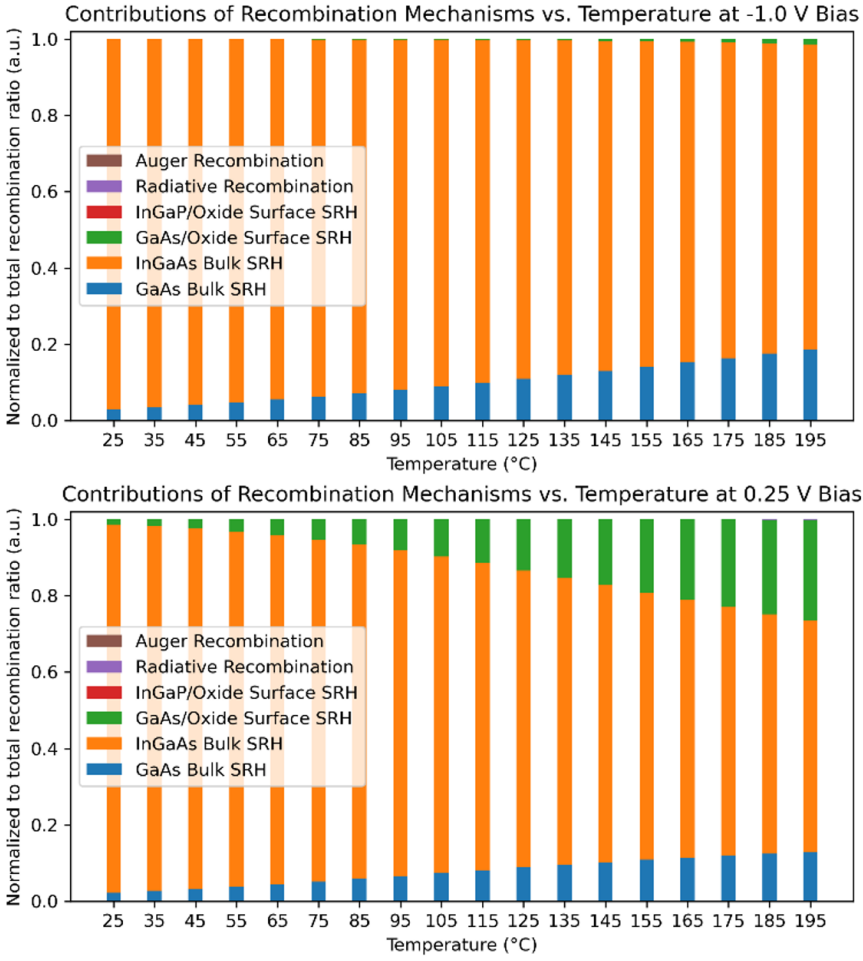

Figure 5.10: Normalized ratios of different recombination mechanisms at -1 V and $+0.25$ V biases, simulated at temperatures from 25 °C to 195 °C, with $\tau_{SRH,GaAs}$ of 3.3 ns, $\tau_{SRH,InGaAs}$ of 2.5 ns and $S_{GaAs/Oxide}$ of 1×10^6 cm/s. Auger, Radiative and InGaP/Oxide Surface SRH recombination mechanisms are found ignorably small for both bias voltages.

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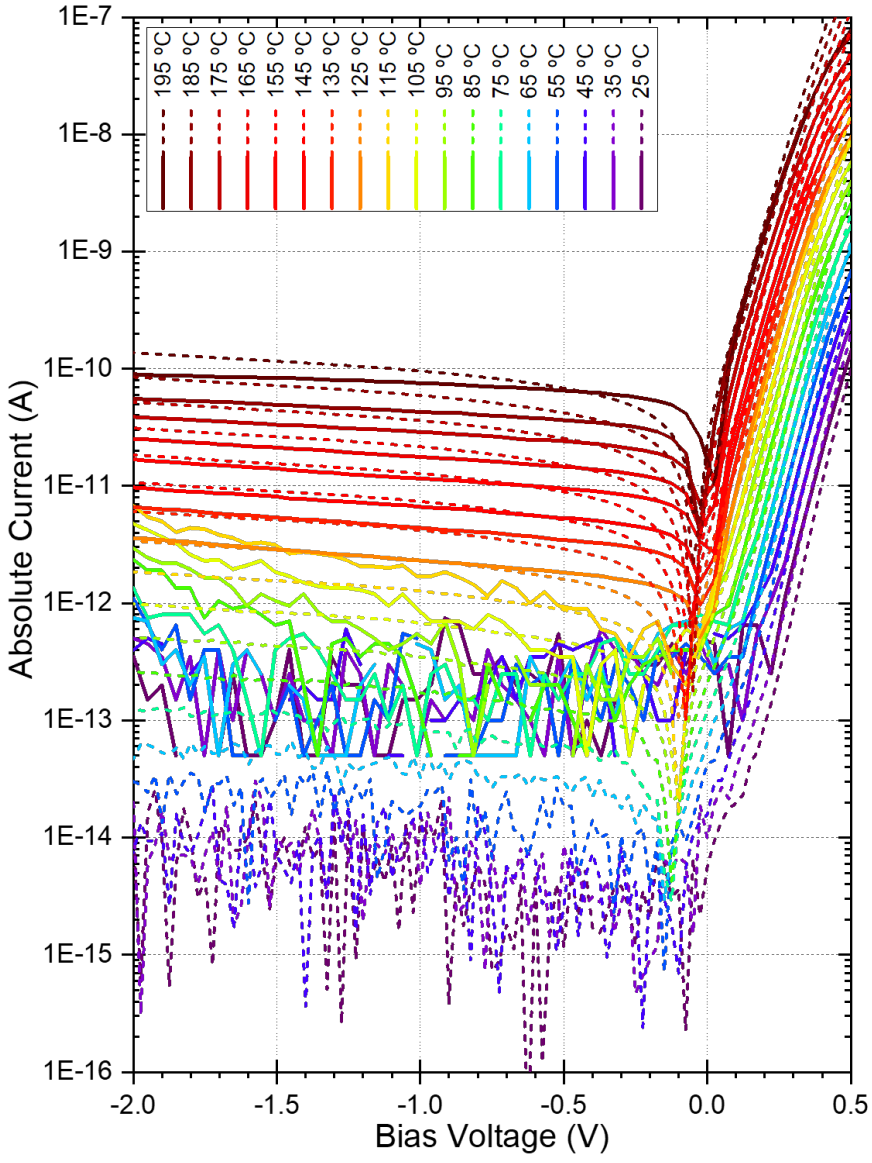

Figure 5.11: Measured (solid lines) and simulated (dashed lines) dark current-voltage response of a 100 μm long NRWPD device at ambient temperatures varying from 25 °C to 195 °C. The two datasets are marked with the ∗ symbol in Fig. 5.8. 1×10^6 *cm/s GaAs/Oxide surface recombination velocity was applied in the simulation group.*

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6

Wide-Field Grown InGaAs Devices on Silicon

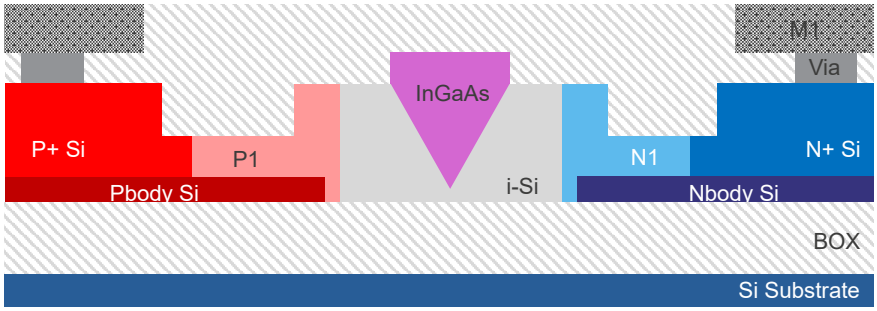

Figure 6.1: Scheme of wide-field grown InGaAs device on silicon.

6.1 Introduction

In this chapter, we will switch to a monolithic approach, different from nano-ridges grown with the ART and NRE methods. Wide-field growth refers to the selective area growth of III-V active material on Si on open areas defined by oxide windows. Compared with the monolithic nano-ridge waveguide growth approach, the wide-field growth offers direct integration with an existing Si photonics platform. It

also avoids direct metal contact on III-V volumes when the metal connections are established on Si, similar to Ge lateral p-i-n (LPIN) photodetectors [1].

Heteroepitaxial growth of InGaAs has tremendous potential for electro- absorption type active photonic applications on Si in the C- and L-band telecom wavelength ranges. It offers (1) wavelength extendibility of the devices beyond the Ge band-edge limit, (2) bandgap tunability in a wide range between the GaAs and InAs bandgaps, and (3) a sharper band-edge of the material compared to the Ge band-edge, enabling better capabilities for Franz-Keldysh type electro-absorption modulation (EAM). The advantages of InGaAs are described in Fig. 6.2.

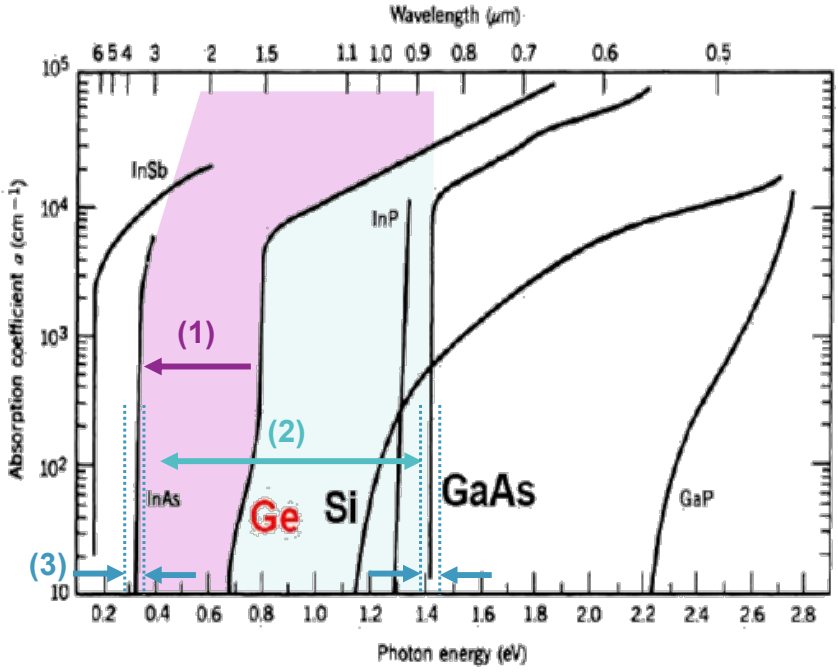

Figure 6.2: Advantages of InGaAs absorption coefficient spectrum in comparison with Ge. Overlayed descriptive figures on the spectra graph from [2]. The advantages are marked as (1) wavelength extendibility, (2) bandgap tunability, (3) sharper band-edge.

The wide-field growth approach was trialed for binary III-V GaAs for phase modulation [3], and ternary InGaAs for electro-absorption modulation and photodetection applications. While GaAs wide-field phase modulators offered some benefits over Si-based phase modulators, InGaAs wide-field devices, which we will detail in this chapter, suffered from material composition inhomogeneities and resulted in very limited device performance.

This chapter covers the design, simulations, fabrication, opto-electrical char-

acterization, and results of the wide-field grown InGaAs devices.

6.2 Wide-Field Device Design and Simulations

6.2.1 Design Constraints

The wide-field grown InGaAs devices were planned to be trialed on an existing Si photonics platform mask set with an existing EAM design site. The site contains shallow-etched wide Si rib waveguides with various lengths, p-/n-type doping windows to construct a Si p-i-n junction, p-/n-plus doping windows, via plugs, and metal pads for electrical access to the device. This study consisted of a mask respin for III-V window and P1/N1 level doping masks. The III-V active volume was intended to be placed in the intrinsic region of the p-i-n junction. This design site consists of two replicates (sites A and B) of waveguide groups with different lengths and widths. The size parameters of these sites are given in Table 6.1. Among the parameters listed in Table 6.1, waveguide width (WW), body type doping intrinsic width (BIW), and the device lengths were fixed in the platform and were not included in the design space of this study. The III-V growth window width (35W) and the final intrinsically doped Si width (IW) were studied and parameterized through mask reworks.

Parameter [Unit]	**Site**	**Values**			
Waveguide Width (WW) [nm]	A,B	700	900	1100	1300
Body Intrinsic Width (BIW) [nm]	A,B	250	450	650	850
III-V window Width (35W) [nm]	A,B	250	250	250	250
Intrinsic Width (IW) [nm]	A	0	200	400	600
	B	300	300	300	300
Device Length [μm]	A,B	9	19	41	79

Table 6.1: Size parameters of InGaAs wide-field grown devices

6.2.2 Optical Mode Simulations

The optical mode simulations were completed with Ansys Lumerical MODE software [4], in a similar way as described in chapter 3 for the nano-ridge waveguide devices. The optical simulations were done for all waveguide widths listed in Table 6.1. The fundamental mode profiles of the edge cases with widths 0.7 μm and 1.3 μm are shown in Fig. 6.4. The simulations were completed at target wavelength of 1.55 μm with a 250 nm III-V window width, 50 nm III-V overgrowth height, and the $In_{0.53}Ga_{0.47}As$ compound with the corresponding absorption coefficient.

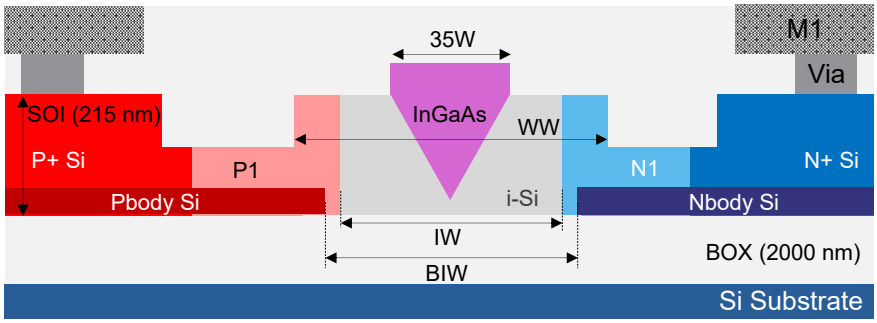

Figure 6.3: Cross-section with design parameters of the proposed InGaAs on silicon modulator.

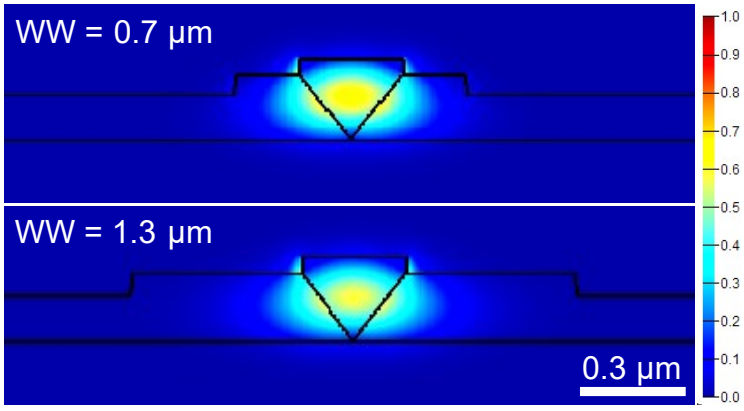

Figure 6.4: Optical mode simulations of 2D cross-sections of 0.7 μm and 1.3 μm WW InGaAs wide-field devices on silicon, simulated with 1.55 μm wavelength excitation and $In_{0.53}Ga_{0.47}As$ composition.

The simulations show that the fundamental TE mode is well confined in the V-shaped InGaAs active volume for all WW cases, with no signs of higher-order mode interference.

6.2.3 Si Waveguide Doping Design

The bandgap of InGaAs is lower than that of Si. Therefore, forming a high electric field for effective photocarrier collection is essential. The intrinsic width of the Si waveguide governs the photocurrent collection efficiency from the active III-V volume via junction electric field, and the junction capacitance. The fixed doping windows of P-/N-plus and P-/N-body type dopings bring a challenge for custom optimization of the final IW of the waveguide.

The second challenge arises from the free-carrier absorption (FCA) of Si,

which is directly affected by the doping levels and the volume of the doped region. The selected IW also governs the volume of the doped region. The doping level influences the series resistance of the junction and the junction potential. All in all, there is a trade-off between optical loss, responsivity, and bandwidth of such InGaAs on Si photodiode, governed by the doping levels and IW.

In a short TCAD device simulation study to observe the effects of waveguide doping levels on RC bandwidth, a 2D structure with WW = 0.7 μm and IW = 0.3 μm was used. The simulation showsa peak of the RC bandwidth at the waveguide doping concentration of 1×10^{18} cm^{-3}. To assess the effects of FCA, three nominal doping concentration levels were chosen in the design matrix as 5×10^{17} cm^{-3}, 1×10^{18} cm^{-3}, and 1×10^{19} cm^{-3}. For intended doping concentration levels and IW separation, the P1/N1, P-/N-body, and P-/N-plus windows' doping energy and dose settings were optimized by using Synopsys Sentaurus Process [5] TCAD software. The optimized doping conditions are given in Table 6.2.

Doping	**Type**	**Body**		**P1/N1 (2-step)**		**Plus**	
		Energy	Dose	Energy	Dose	Energy	Dose
cm^{-3}	P/N	keV	cm^{-2}	keV	cm^{-2}	keV	cm^{-2}
5×10^{17}	N	140	$1.2e13$	50/140	$2.5e12$	30	$3e15$
	P	48	$1.2e13$	20/48	$2.5e12$	10	$3e15$
1×10^{18}	N	140	$4.5e13$	50/140	$2.5e12$	30	$3e15$
	P	48	$4.5e13$	20/48	$2.5e12$	10	$3e15$
1×10^{19}	N	140	$4.5e14$	50/140	$3e11$	30	$3e15$
	P	48	$4.5e14$	20/48	$3e11$	10	$3e15$

Table 6.2: Doping settings optimized through process simulations for waveguide doping concentrations of 5×10^{17} *cm^{-3},* 1×10^{18} *cm^{-3}, and* 1×10^{19} *cm^{-3}.*

The doping settings and profiles obtained through process simulations were further fed into the device simulations to observe the junction formation and electric field distributions, shown in Fig. 6.5. For the device simulations, the InGaAs region had an n-type doping concentration of 1×10^{16} cm^{-3} to simulate non-intentional doping during the III-V material growth. For WW = 0.7 μm, the electric field is highly confined in the III-V volume, with a maximum level of 100 kV/cm. For WW = 1.3 μm, the electric field is more distributed due to the wider intrinsic width, while within the III-V volume, the electric field reaches 25 kV/cm. There is also a pinching of the electric field observed in this case, where the peak of the electric field appears outside of the III-V region.

The obtained doping profiles for different WW and doping levels were later fed into an optical mode simulation to assess the optical losses due to the dopant-induced FCA. A lossless equivalent of the InGaAs material was used for this simulation. Fig. 6.6 provides a comparison of the optical loss cross-sections. In this

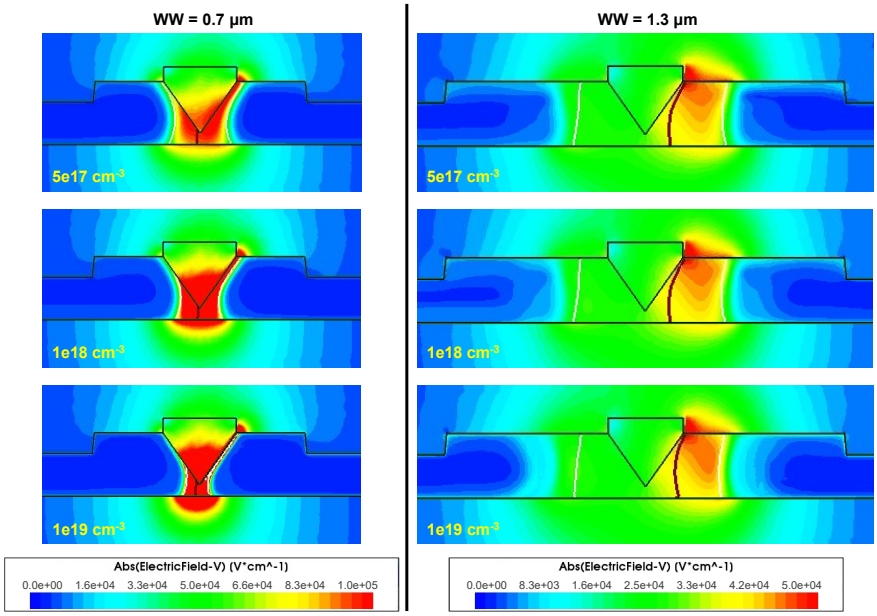

Figure 6.5: Electric field distributions of WW = 0.7 μm and WW = 1.3 μm InGaAs wide-field devices on silicon. The doping profiles were obtained with process simulations where the doping settings in Table 6.2 were applied. The edges of the depletion region (intrinsic volume) are represented with white contour lines, and the junction is represented with a red contour line.

figure, WWs of 0.7 μm and 1.3 μm were compared, of which the intrinsic widths are 250 nm and 850 nm, respectively. The FCA values calculated for the fundamental TE modes in these waveguide cross-sections are given in Table 6.3. As expected, an increase in the doping concentration increases the FCA losses. Likewise, the widening of the waveguide and the intrinsic width towards the WW of 1.3 μm effectively reduces the FCA losses.

Doping (cm^{-3})	**FCA (dB/cm)**			
	0.7 μm	0.9 μm	1.1 μm	1.3 μm
5×10^{17}	7.82	5.26	3.20	1.80
1×10^{18}	28.51	16.36	8.90	4.63
1×10^{19}	384.63	198.04	99.90	49.38

Table 6.3: Free carrier absorption values obtained through optical mode simulations on the doping profiles extracted from the process simulations, for different waveguide widths of 0.7 μm, 0.9 μm, 1.1 μm, and 1.3 μm.

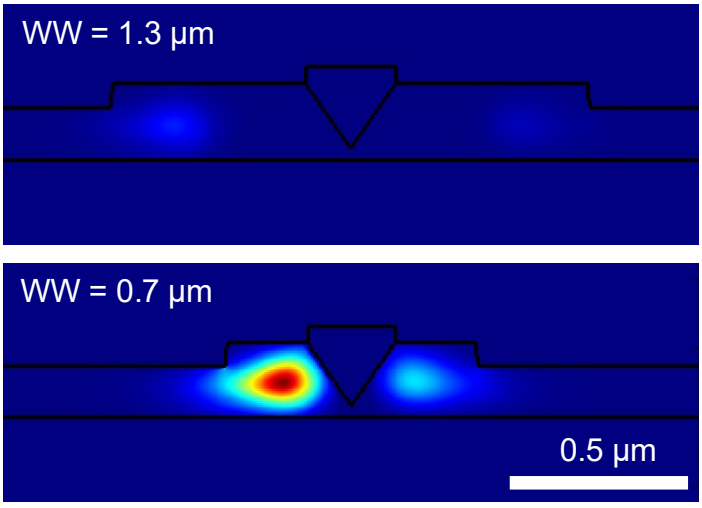

Figure 6.6: Free carrier absorption profiles of waveguides with width of 0.7 μm and 1.3 μm, doped with the settings of 1×10^{19} cm^{-3} doping concentration. Both profiles are normalized to the same colormap values.

6.2.4 Si WG to III-V/Si WG coupling simulations

The trial site for the InGaAs wide-field devices on the Si photonics platform consists of two normal-incidence grating couplers for in/out optical access to the device site, connecting ridge waveguides, and a shallow-etched rib waveguide device site. The shallow-etched rib waveguide section consists of non-etched Si areas on both sides for electrical access, as shown in Fig. 6.3. In addition to the two different Si WG cross-sections, the III-V/Si wide-field waveguide device introduces the third different waveguide cross-section and the coupling challenge between the three cross-sections. To ensure a proper transition of the III-V/Si device section with respect to the abrupt ridge to rib Si WG transition, a set of 3D finite-difference time-domain (FDTD) simulations was carried out using the Ansys Lumerical FDTD software [6].

Initially, the Si ridge to rib waveguide transition, the starting point of the active device section, was constructed with existing maskset parameters for WW = 0.7 μm. Later, the InGaAs volume with the V-groove bottom profile was constructed using a lossless $In_{0.53}Ga_{0.47}As$ equivalent material. The device was excited in the Si ridge waveguide with the fundamental TE mode at 1.55 μm wavelength. The transmission of the fundamental TE-mode was calculated by two power monitors placed right after the excitation source and 10 μm after the Si waveguide transition. The InGaAs volume was translated within ± 500 nm distance to the Si waveguide transition point, and the transmitted optical power was recorded. The

3D simulation scheme and the calculated transmission values are shown in Fig. 6.7.

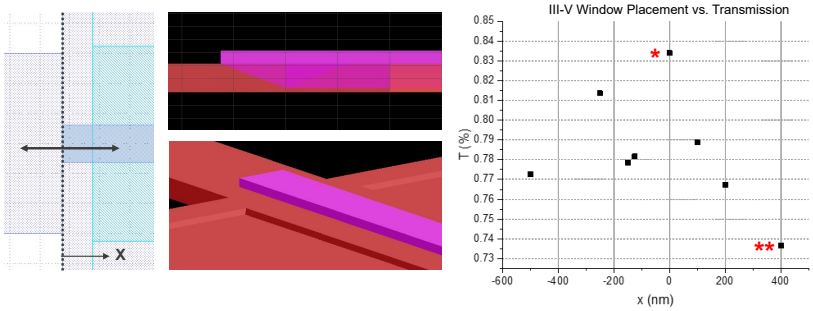

Figure 6.7: The 3D simulations in FDTD for coupling efficiency of Si to III-V/Si waveguide transition, per III-V growth window placement on the ridge to rib Si WG transition. The waveguide width is 0.7 μm.

As shown in Fig. 6.7, placing the III-V growth window edge at the ridge to rib transition point gave the highest transmission value of approximately 84%. As an example, the E_y and $|E|$ field distributions of the transition point placement (x = 0 nm) and 400 nm into the rib region placement (x = +400 nm) are given in Fig. 6.8. The figure demonstrates that in the +400 nm case, more light scatters out of the waveguide at the ridge-to-rib Si waveguide transition.

6.2.5 Layout

The mask layout design of the wide-field grown InGaAs on Si devices was completed on the aforementioned preexisting Si photonics mask set, where grating couplers, ridge and shallow-etched rib waveguides, metal pads, and vias were defined. The device length, waveguide width, and body-type doping intrinsic width were already defined in this area, as listed in Table 6.1. In this respin of the mask set, the III-V window, P1 and N1 type doping masks were redesigned.

As shown in Table 6.1, the 35W was set to 250 nm for all device sites. This maximizes the III-V volume while providing a sufficient safety margin (>10 nm) at the bottom of the SOI layer to avoid any over-etching of the V-groove opening and exposing the buried oxide surface.

This design of experiment (DOE) of IW, defined by the P1/N1 doping windows, was divided into two equivalent sites of A and B. In Site A, IWs were progressively increased from 0 nm to 600 nm by increasing WW, following the trend of BIW distributions for different WWs. The DOE in site A aims to study the effect of changing IW on device performance. In site B, IW is kept at 300 nm to provide enough intrinsic volume for 250 nm III-V placement. The DOE of

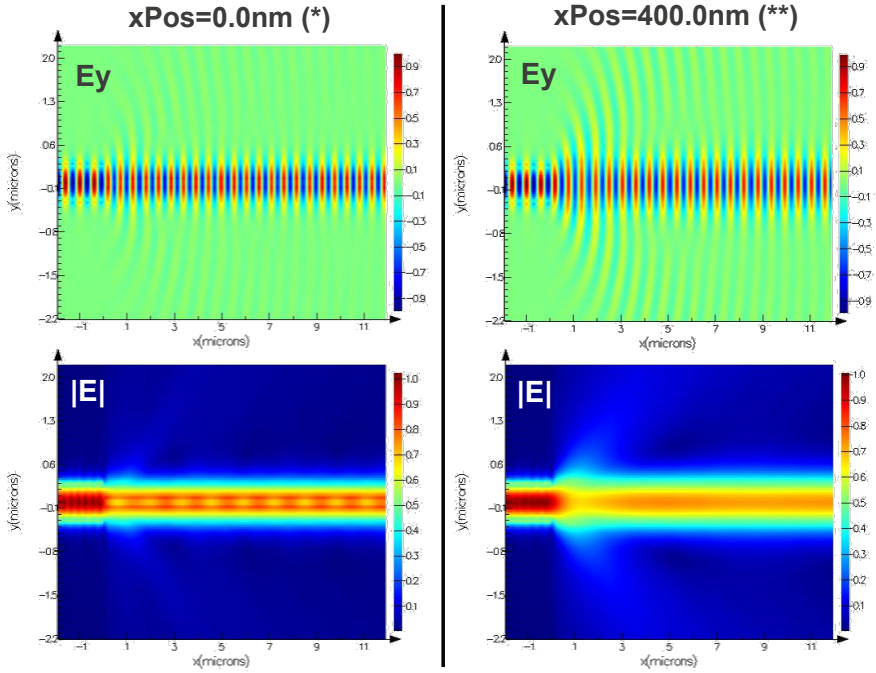

Figure 6.8: E_y and $|E|$ distributions of x=0 nm and x=+400 nm 35W placement cases.

site B is intended to study the effects of carrier transport on different widths of Si waveguides on the high-speed performance of the devices.

In addition to the EAM device site design, the layout also included additional process and electrical metrology sites, as well as dummy III-V windows to ensure the III-V growth uniformity.

6.3 Wide-Field Device Fabrication

The wide-field grown InGaAs devices on Si were fabricated in the pilot CMOS line of imec's 300-mm foundry. The process steps included imec's 300-mm Si photonics platform fabrication steps [7], with additional steps for incorporating the III-V wide-field devices. The GaAs-based device fabrication steps were previously covered by Y. Kim et al. [3].

The fabrication steps are outlined in Fig. 6.9. The process began with a 300-mm SOI substrate with 215 nm thick SOI on a 2-μm thick buried oxide. The top Si layer was used to form the Si waveguide and other passive elements, and served as the substrate for III-V material growth. The ridge and shallow-etched rib waveguides were patterned with dry-etching of 220 nm and 70 nm depths of top

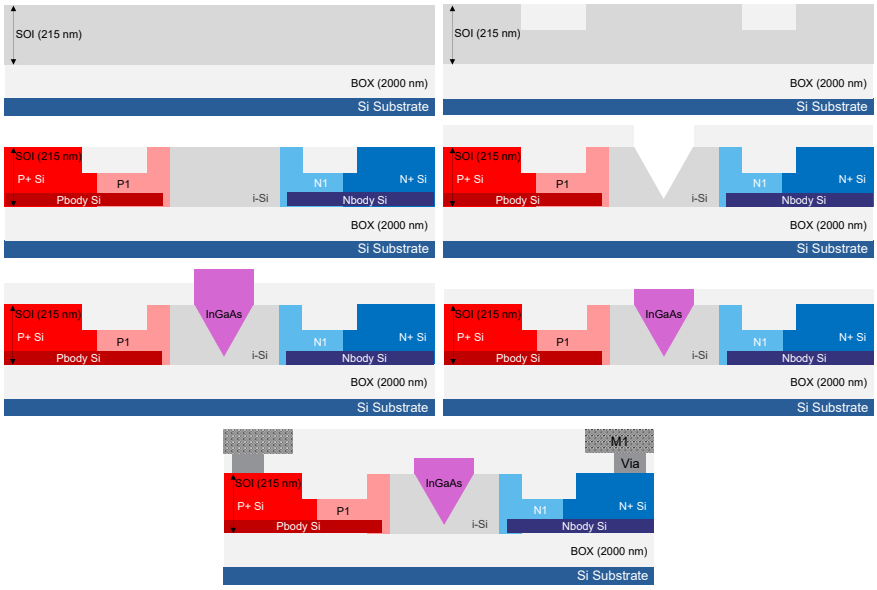

Figure 6.9: The process steps of wide-field grown InGaAs device on silicon.

surface, respectively [7]. After patterning the passive elements, the surface was planarized using an oxide cladding and a chemical-mechanical polishing (CMP) step. The SOI was then doped in several steps for the body, P1/N1, and P-/N-plus type doping, with the separate doping windows and parameters listed in Table 6.2. Following the doping steps, the III-V growth window was created with a dry-etched oxide template, and the V-groove in Si was formed by anisotropic wet etching of Si in the center of the waveguides. Selective-area epitaxial growth of InGaAs on Si was completed in 2 main stages of seed and overgrowth, both with the metalorganic vapor-phase epitaxy (MOVPE) process. After InGaAs growth, excess InGaAs was planarized with another CMP step. Lastly, electrical access to the devices was established using standard CMOS Ni-silicide and tungsten contact plugs, and contact pads were formed with a standard Cu damascene metallization process.

The InGaAs epitaxial growth was completed in two steps. The first step involved growing a seed layer to accommodate the strain from lattice mismatch, allowing it to be managed by misfit dislocations (MD) within a thin layer. In the subsequent overgrowth step, the majority of the InGaAs active volume was grown on the fully relaxed seed layer. This two-step growth method has been applied in several heteroepitaxial growth studies [8], including the III-V on Si nano-ridges covered in previous chapters [9].

The composition of the bulk $In_xGa_{1-x}As$ growth is targeted for (1) EAM and

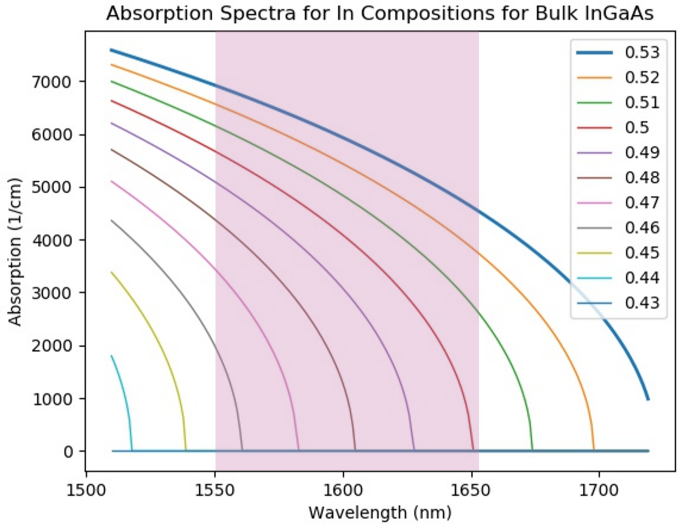

Figure 6.10: Calculated absorption spectra in the vicinity of 1550 nm wavelength for bulk $In_xGa_{1-x}As$ material with various In composition rates.

(2) photodetection applications at a 1550 nm Si passives operation wavelength. The grating couplers of the EAM site, where the wide-field grown InGaAs devices were initially studied, had a target wavelength of 1600 nm, operable within $\pm$50 nm from that target. InGaAs compositions with band-edges within this wavelength range are found to range from 46% to 50% of In, as calculated through the bulk InGaAs absorption model covered in subsection 3.1 of chapter 3. The absorption spectra near the 1550 nm wavelength are shown in Fig. 6.10. In this first study, four composition rate targets are defined. One composition design split is selected at 46% of In to evaluate EAM device characteristics, while the other three design splits are chosen with higher In composition rates to assess growth uniformity and the effects on photodetection performance. The final In rate targets are defined as 46%, 50%, 55%, and 60%.

The composition of the epitaxially grown materials was verified after each growth step using inline X-ray diffraction analysis (XRD). Upon completion of all epitaxial growth steps, a scanning transmission electron microscopy (STEM) sample was obtained from a sister process development wafer with a targeted composition of 46% In, as illustrated in Fig. 6.11. The high-angle annular dark field (HAADF) image displays various color contrasts within the InGaAs, indicating composition inhomogeneity. The higher-order bright-field (BF (220)) image reveals strain fields throughout the InGaAs volume, alongside composition inhomogeneity. Additionally, the annular bright-field (ABF) image shows distributed stacking faults and threading dislocations across the grown volume.

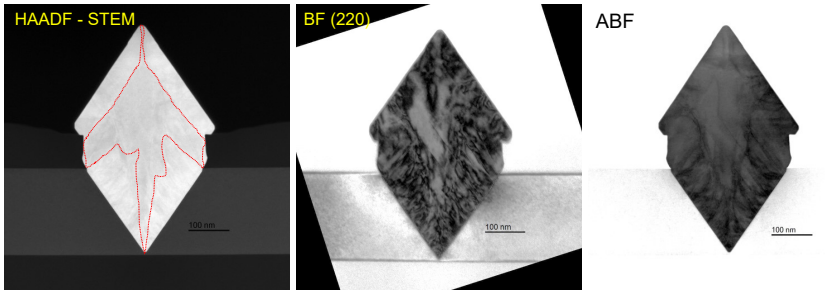

Figure 6.11: Scanning transmission electron microscopy images of wide-field grown InGaAs with different settings (HAADF - high-angle annular dark field, BF (220) - bright-field at the higher order of (220), ABF - annular bright-field).

Further analysis with energy dispersive X-ray spectroscopy (EDS), conducted alongside STEM metrology, is presented in Fig. 6.12. EDS enables the material characterization by extracting elemental composition. Scans were performed for all three elements: Ga, In, and As. The EDS STEM images for In and Ga reveal three distinct regions with different InGaAs compositions, with the In composition rate ranging between 30% and 60% at various locations. The region (3) marked in Fig. 6.12 can be disregarded as it will be removed in the subsequent CMP step, used to planarize the InGaAs volume above the oxide layer. However, regions (1) and (2) persist in the final device cross-section. The EDS scan confirms the inhomogeneity of the InGaAs composition across the device cross-section.

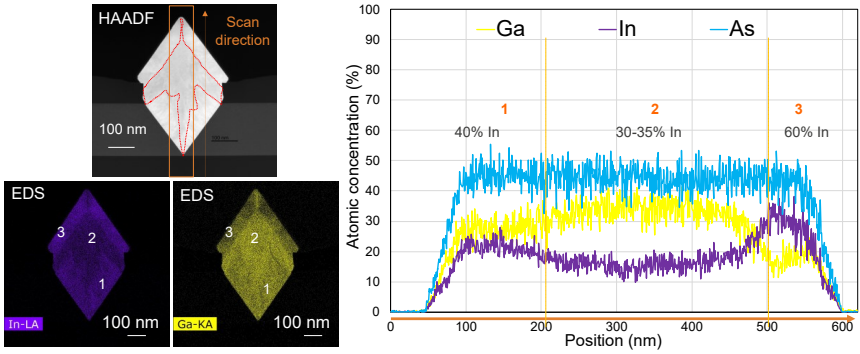

Figure 6.12: Energy dispersive x-ray spectroscopy (EDS) on wide-field grown InGaAs with 46% In composition target.

6.4 Opto-Electrical Characterization and Results

The opto-electrical characterization of the wide-field grown InGaAs on Si devices was conducted using an automated wafer-scale prober equipped with optical fiber probes and electrical probes. Each device unit on the DOE site includes a reference waveguide with in & out grating couplers identical to those on the device path, and electrical connections to the device, as illustrated in Fig. 6.13.

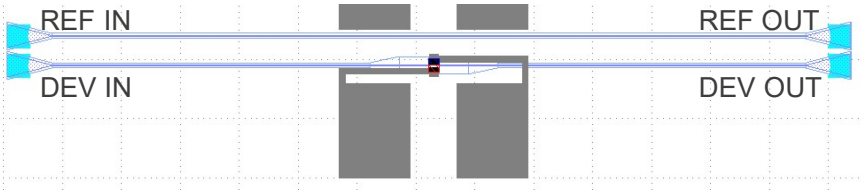

Figure 6.13: Layout of individual device cell.

The transmission spectra were initially measured for the reference waveguide. Subsequently, they were measured for the device optical path at various device bias voltages. An example of a transmission spectrum taken between 1570 nm and 1630 nm wavelength is depicted in Fig. 6.14. These spectra were later utilized to extract the device insertion loss (IL) for a given bias voltage using the following equation:

$$IL(\lambda)[xV] = T_{ref}(\lambda) - T_{dev}(\lambda)[xV] \tag{6.1}$$

where $IL(\lambda)[xV]$ represents the insertion loss at wavelength λ for a bias voltage of x volts, $T_{\text{ref}}(\lambda)$ is the transmission through the reference waveguide at wavelength λ, and $T_{\text{dev}}(\lambda)[xV]$ is the transmission through the device waveguide at wavelength λ and bias voltage x.

Design Parameter	**Values**
In % (XRD reading)	46% (**#0**), 50% (**#1**), 55% (**#2**), 60% (**#3**)
Si Doping	1×10^{19} cm^{-3}
Waveguide Width (WW)	0.7 μm
III-V Width (35W)	250 nm
Intrinsic Width (IW)	$\sim$ 0 nm
Lengths	9, 19, 41, 79 μm

Table 6.4: Reported device design parameters.

While the transmission spectra for a significant portion of the design space were successfully measured, several design variants exhibited unexpected spectrum profiles such as flats, loss peaks, valleys, and more. These anomalies may

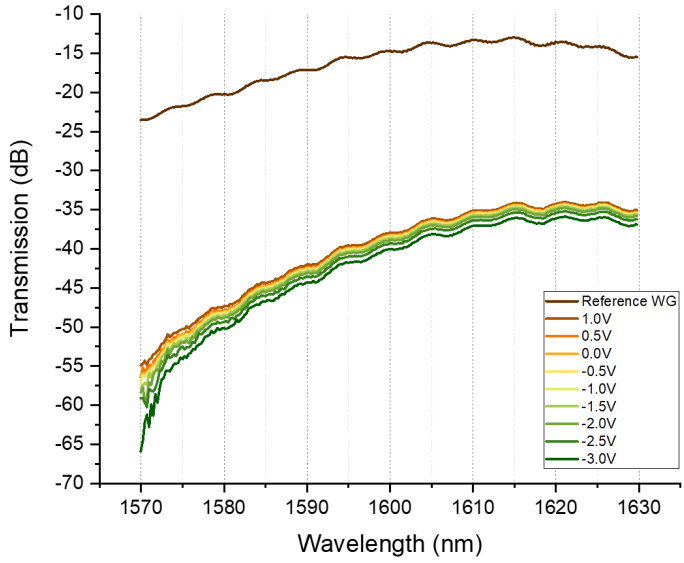

Figure 6.14: Example of a transmission spectra measurement with reference waveguide spectra at 1570 - 1630 nm wavelength range.

be attributed to measurement errors, multimoding, or scattering. Therefore, the remaining opto-electrical characterization results are reported only for the subset of the design space defined in Table 6.4.

First, the ILs of the devices were calculated from the transmission spectra measurements for all InGaAs composition design variants listed in Table 6.4. A sample IL spectrum at 0 V bias is provided in Fig. 6.15 for different In composition rates marked as #0, #1, #2, and #3 corresponding to 46%, 50%, 55%, and 60% In composition rates, respectively. As shown in Fig. 6.15, the ILs for all In composition variants decrease towards the red edge, but there is no sharp band-edge behavior, indicating the inhomogeneities of the InGaAs material composition.

The insertion losses of the devices WW = 0.7 μm, measured at 1629 nm (red edge of the measured spectral range) were linearly fitted per corresponding device lengths to extract coupling loss (dB) and propagation losses (dB/μm). The measured ILs and fits are given in Fig. 6.16. The extracted coupling and propagation losses are given in Table 6.5.

The dark currents of the subset of devices defined in Table 6.4 are around 1 μA at -1 V bias voltage, and no significant dependence on In % and length was observed. The distributions are depicted in Fig. 6.17. The level of dark current is sufficiently low for practical applications.

The intended EAM operation of the wide-field grown InGaAs nano-ridges is

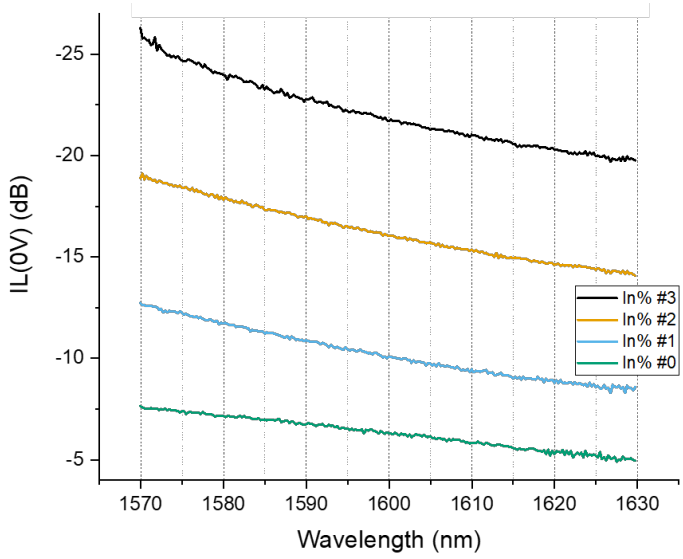

Figure 6.15: Example of a measured insertion loss spectra of varying In % devices with WW of 0.7 μm and length of 19 μm.

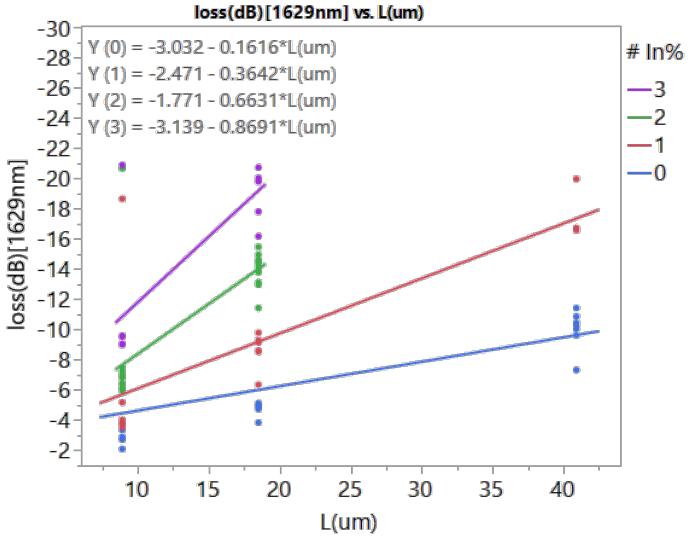

Figure 6.16: Insertion loss (dB) measured at 1629 nm wavelength compared with lengths and grouped with target In % composition.

based on the Franz-Keldysh (FK) effect [10]. The presence of a strong electric field tilts the energy band profile of a material, inducing more tunneling effects in

In # (target %)	Coupling Loss (dB)	Propagation Loss (dB/μm)
#0 (46%)	-3.0	-0.16
#1 (50%)	-2.4	-0.36
#2 (55%)	-1.7	-0.66
#3 (60%)	-3.1	-0.86

Table 6.5: Coupling loss (dB) and propagation loss (dB/μm) extracted for different In composition rate samples measured at 1629 nm.

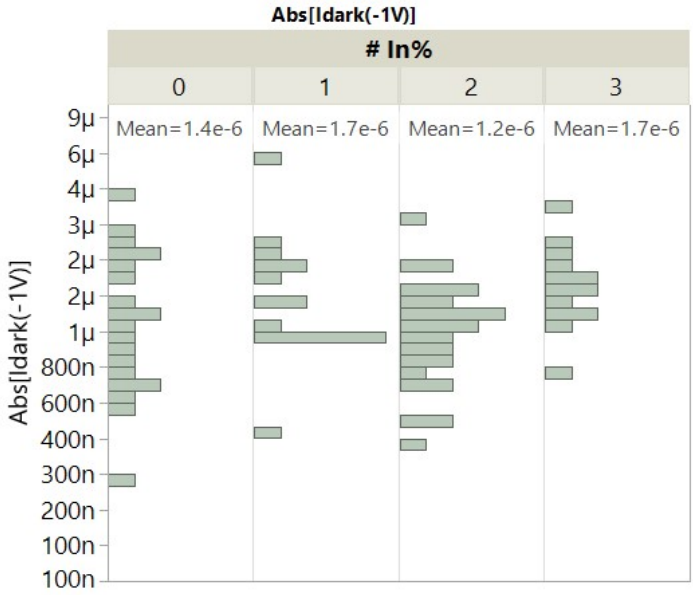

Figure 6.17: Dark current distribution per different In composition rates at -1 V.

the vicinity of the absorption band edge. Under the tunneling effect, the electron and hole wavefunctions extend into the band gap with a tail. This results in below-bandgap optical excitation of carriers, thereby extending the absorption band-edge of the material. Due to the superposition of both wave functions, constructive and destructive interference can occur at different photon energy points, causing the absorption band-edge extension also starts to exhibit an oscillatory profile [11]. By modulating the electric field, the absorption edge tail can be manipulated to create an EAM-type active device.

The modulation performance was characterized by extinction ratio (ER) measurements. The ER is calculated as follows:

$$ER_{xV}(\lambda)[dB] = IL_{xV}(\lambda)[dB] - IL_{0V}(\lambda)[dB] \tag{6.2}$$

where $IL_{xV}(\lambda)$ represents the insertion loss at wavelength λ for a bias voltage of x volts, and $IL_{0V}(\lambda)$ represents the insertion loss at wavelength λ for zero bias voltage.

For the subset of reported devices, the majority of the ERs fall below 1 dB. Considering the high insertion losses of the devices, the figure of merit (FOM) for EAM (calculated by the ratio of ER to IL) is determined to be 0.13 at the maximum level. This FOM is one order of magnitude less than that of a typical Si-Ge based EAM and two orders of magnitude less than that of III-V based EAMs [12].

Fig. 6.18 shows an example of ER and IL spectra (top), measured at -1 V, -2 V, and -3 V bias points. While the IL increases with the increased reverse bias voltage, the spectra do not exhibit the sharp increase or oscillations characteristic for the Franz-Keldysh effect. This can be attributed to the inhomogeneity of the InGaAs composition, which smears the absorption band-edge across the wavelength range of interest. The low EAM performance can also be attributed to the defects in the InGaAs volume, which can result in free carriers screening the electric field within the depletion region, reducing the effective electric field in the active volume.

In the bottom graph of Fig. 6.18, the I-V characteristics of the same device reveal high dark currents at reverse bias, increasing from approximately 1 μA to above 100 μA as the bias voltage changes from -1 V to -3 V. These high dark currents can also explain the increase in the insertion loss due to FCA effects.

Also the photodetection performance of the wide-field grown InGaAs devices was found to be inferior. The majority of the devices exhibited responsivities of less than 0.1 A/W, compared to the theoretical maximum of 1.25 A/W at this wavelength range. The low PD performance can also be attributed to high defectivity in the active InGaAs volume, which significantly increases dark currents and photocarrier recombination. The screening effect can also play a role in reducing the photocarrier extraction efficiency. A sample of dark and light I-V curves is provided in Fig. 6.19, where the light I-V curve converges with the dark I-V curve at higher reverse bias voltages, indicating that the device becomes dark current limited.

6.5 Discussion and Observations

The wide-field grown InGaAs devices on Si were pursued to integrate III-V active materials directly onto silicon photonics platforms at the circuit layer. Compared to other integration mechanisms, this approach avoids the need for additional coupling schemes. In contrast, nano-ridges grown on Si still require a coupling modality to redirect the optical path to the Si level. Additionally, the wide-field grown method offers easy integration into a standard Si photonics process flow, enabling electrical contacting through the Si. Moreover, it provides versatility as different

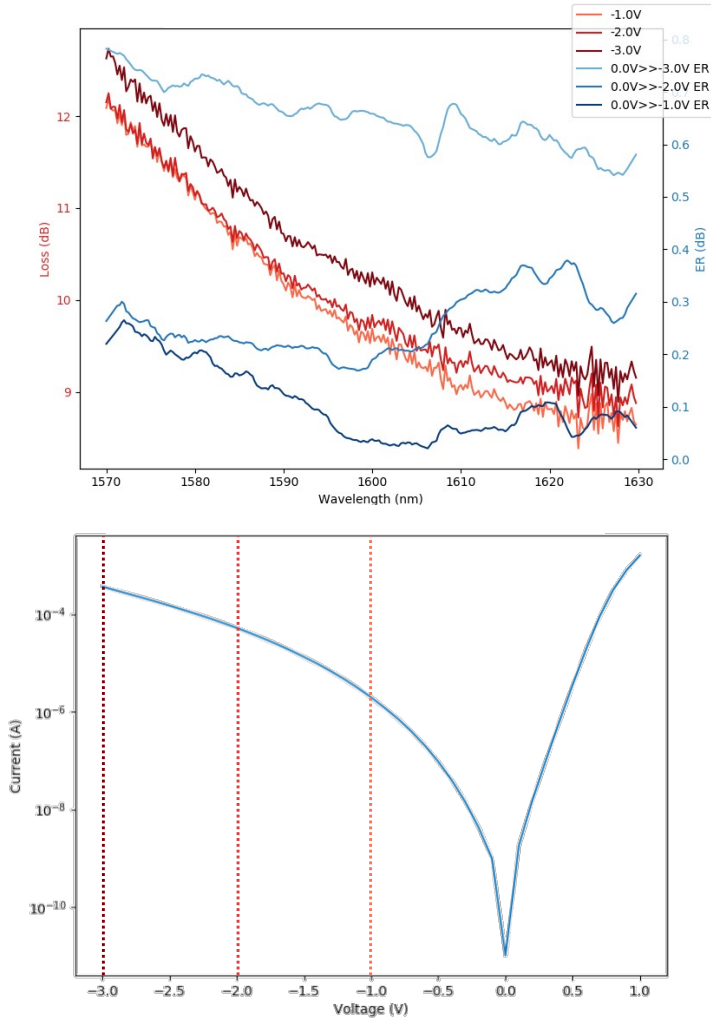

Figure 6.18: (top) Extinction ratio spectra calculated for different bias points, example of a device of 50% target In composition rate and 19 μm length. (bottom) Dark current I-V of the device above, exhibiting high dark currents at -2 V and -3 V bias points.

III-V active material combinations can potentially be grown on the same wafer.

Unfortunately, in this early trial, device performance was limited by the quality of the grown material. This strongly emphasizes the importance of material quality, as all critical active device performance metrics depend on it. It has been shown that more exhaustive growth studies are required to achieve sufficient material quality and homogeneity while keeping defect densities low.

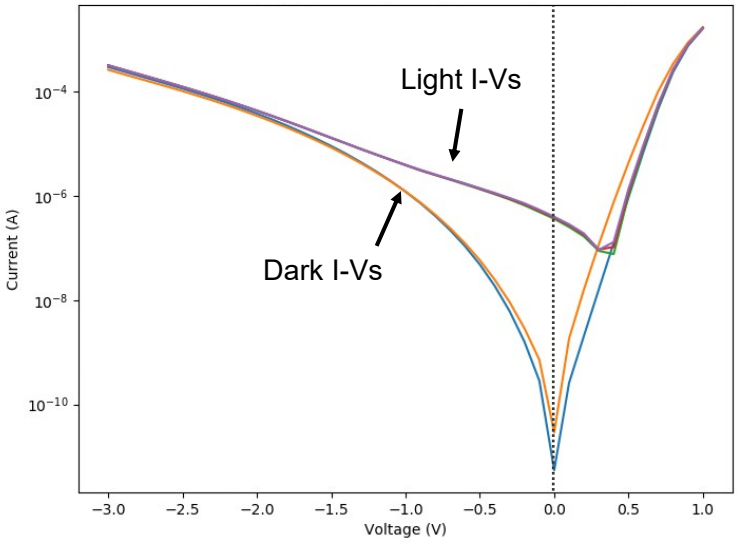

Figure 6.19: Dark and light I-V characteristics of a sample InGaAs wide-field grown device of 50% target In composition rate and 19 μm length.

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7

Conclusion and Perspectives

Silicon photonics has emerged as a highly versatile photonics platform that has grown from the know-how in the electronics industry and has advanced its capabilities exponentially in the last decades. Both passive and active capabilities of silicon photonics have been studied on multiple avenues of research and development all around the world. While the passive losses have been reduced dramatically and more and more components have been integrated on a single chip, silicon's inherent limitation in performing all active photonic functions due to its indirect bandgap remains. In order to enable all photonic capabilities, various research groups have pursued integrating different material systems on silicon. Among these material systems, III-V materials stand out for their complete active photonic capabilities and their foundational role in shaping the photonics era.

In this doctoral study, our principal aim was to enhance the active photonic capabilities of silicon photonics platforms by monolithically integrating III-V devices. Specifically, we demonstrated InGaAs/GaAs multi-quantum well (MQW) nano-ridge waveguide photodetectors (NRWPD) grown on silicon. These were grown using specialized growth techniques known as aspect ratio trapping (ART) and nano-ridge engineering (NRE). Furthermore, we evaluated the growth quality through an exhaustive examination of the leakage mechanisms associated with these devices. Concurrently, we conducted trials involving the direct selective area growth of III-V material on a silicon photonics platform to achieve active modulation and photodetection directly on the same platform. We subsequently evaluated and compared the performance of these devices with that of the NRWPD devices.

7.1 Nano-Ridge Waveguide Devices on Silicon

In Chapter 2, we detailed various monolithic III-V growth techniques on Si. We compared these state-of-the-art approaches with ART and NRE. Additionally, we provided an explanation of the process steps and details involved in fabricating III-V nano-ridge waveguide devices.

In Chapter 3, we delved into the design of NRWPD devices, detailing the design steps and boundaries, comprehensive optical and electrical simulations, and the layout design.

In Chapter 4, we reported on our devices: high-quality $In_{0.20}Ga_{0.80}As$/GaAs MQW p-i-n nano-ridge waveguide photodetectors. These devices were monolithically integrated in a 300-mm Si pilot line through selective-area epitaxial growth with aspect-ratio trapping and nano-ridge engineering. At a wavelength of 1020 nm, the photodetectors with the lowest contact density exhibited an internal responsivity of 0.65 A/W, 79% internal quantum efficiency. We provided a detailed analysis of the responsivity dependence on device length and metal contact pitch, demonstrating a good correlation with simulation models.

Moreover, we reported a record-low dark current density of 1.98×10^{-8} A/cm^2 at -1 V bias, highlighting both the high material quality of the InGaAs/GaAs structures and the effectiveness of InGaP passivation. Additionally, initial RF measurements and electric-field simulations indicated that the bandwidth of current devices was primarily limited by the RC constant, estimated to be in the range of 1.1 to 1.9 GHz. In summary, our findings in Chapter 4 demonstrate the first III-V nano-ridge waveguide photodetectors grown on Si and underscore the potential of the III-V nano-ridge epitaxy concept to integrate high-quality III-V waveguide devices directly onto Si.

In Chapter 5, we presented a comprehensive study of the dark current behavior of InGaAs/GaAs MQW nano-ridge photodetector devices monolithically grown on Si. Our initial measurements revealed that at room temperature, the measured dark current was noise-limited, indicating the high material quality of the devices. By conducting measurements at elevated temperatures and correlating them with TCAD models, we identified various leakage current components relevant to the devices. The primary contribution was attributed to Shockley-Read-Hall (SRH) type non-radiative recombination, occurring both in the bulk InGaAs quantum well and GaAs volumes. Additionally, we observed SRH-type recombination at the GaAs/oxide surface under subthreshold forward bias voltages. Extrapolating our device model to room temperature, we estimated the actual dark current to be around 0.01 pA at -1 V bias, more than one order of magnitude below the measured levels, which were limited by the noise level of the experimental setup. Furthermore, even at elevated ambient temperatures of up to 195 °C, our devices exhibited median dark currents below 0.1 nA, demonstrating their potential for a

wide range of applications beyond interconnects, for example sensing, and imaging.

7.1.1 Perspectives on Future Nano-Ridge Waveguide Devices on Silicon

Although the NRWPD devices presented in this dissertation exhibit high responsivity and record-low leakage currents, there are several gaps to be filled for the intended use of these devices and commercialization. These main gaps include, but are not limited to:

- Extension of the operation wavelength to the telecom bands of O-band or C-band,
- Increase of overall OE bandwidth,
- Realization nano-ridge to Si waveguide coupling,
- Co-integration with other types of active nano-ridge devices,
- Improvements in design and material quality for field operation performance and reliability.

The operation wavelength of the devices reported in this dissertation was limited to 1020 nm. In contrast, industry-standard Si photonics platforms for communications and interconnects operate at either the O-band range of 1260 nm to 1360 nm or the C-band range of 1530 nm to 1565 nm. Ongoing efforts have aimed to extend the operation wavelength of nano-ridge devices beyond this early demonstration with $In0.20Ga0.80As$/GaAs MQWs. These efforts include growing GaSb as a nano-ridge bulk layer to extend nano-ridge platform capabilities [1] and utilizing higher In composition ratio MQWs of $In0.45Ga0.55As$ grown in $In0.25Ga0.75As$ bulk nano-ridges to demonstrate optically pumped O-band nano-ridge lasers [2], [3].

Our study has shown that the early NRWPD devices exhibit limited bandwidth performance due to the high RC constants of the devices. High junction capacitance (C_j) and series resistances (R_s) were shown to particularly occur due to the p-doped layers grown on the sidewalls of the i-GaAs bulk portion. As shown in device simulations in Chapter 4, subsection 4.3.3, the removal of these p-doped GaAs sidewalls improves both C_j and R_s. Furthermore, improvements in p-contact plugs and the doping concentration of the p+ doped layer for contacts can further reduce R_s [4]. Additionally, parasitic capacitance can be further reduced by decreasing contact pad sizes, increasing the pad to Si thickness ratio, or isolating the nano-ridge growth Si area by etching the Si in a nano-ridge on SOI configuration.

While this dissertation successfully demonstrates the growth of nano-ridge devices on Si, a crucial challenge persists regarding the coupling of optical modes in nano-ridges positioned above the Si layer. A prior theoretical study outlined evanescent coupling schemes from nano-ridges to Si waveguides on a 350 mm thick SOI configuration [5]. However, these evanescent coupling methods may necessitate longer nano-ridges than needed. Therefore, alternative butt-coupling approaches employing low-temperature plasma-enhanced chemical vapor deposition (PECVD) deposited silicon nitride (SiN) or polycrystalline silicon (poly-Si) regrown layers could be explored for achieving efficient coupling in shorter nano-ridge devices on Si.

The nano-ridges have been successfully demonstrated as both photodetectors and lasers on the same platform [6]. However, while a single III-V stack can serve different active capabilities, each active device architecture necessitates specific configurations of III-V layers for optimal performance. For instance, a laser may require MQWs or quantum dots grown within the nano-ridge, while a photodetector could benefit from a more compact configuration with the active material filling the entire bulk volume. On the other hand, a nano-ridge-based electro-absorption modulator (EAM) might demand tighter control over band-edge characteristics compared to a nano-ridge laser's gain media. Similarly, a Mach-Zehnder modulator (MZM) constructed with carrier-depletion nano-ridge phase shifters may require non-absorbing III-V active material, contrasting with the active layers needed for nano-ridge lasers and photodetectors. Given these varying device combinations, separate nano-ridge growths are necessary for each device, highlighting the need for further advancements in monolithic III-V growth and III-V passivation with oxide studies. Following the growth of a particular type of nano-ridge device, it must be passivated. Subsequently, a new nano-ridge area will be designated, and the second set of nano-ridges will be grown while preserving the integrity of the first set. This process will be iterated until all desired device architectures are grown on the same substrate. Notably, the implementation of this procedure warrants a comprehensive study to evaluate the reliability and performance of the initially grown nano-ridges after the passivation and subsequent growths.

Our study on the leakage mechanisms of the nano-ridges in Chapter 5 has revealed exceptional material quality, characterized by extremely low dark currents and consequently low defect densities. While the extraction of single-point dark current behavior at elevated temperatures provides valuable insights, future efforts should prioritize industry-standard reliability studies on nano-ridges. While there have been several initial reliability studies on $In0.20Ga0.80As/GaAs$ nano-ridges [7, 8], further research is needed to enhance device capabilities for high-temperature field operations and to determine the industry-standard Failure Rate (λ) measured in Failure In Time (FIT) units. FIT is a reliability metric representing the number of unit failures per billion hours. Additionally, λ is used to calculate

the Mean Time To Failure (MTTF), expressed as $MTTF = 1/\lambda$.

7.2 Wide-Field Grown Devices on Silicon

The wide-field grown InGaAs devices on Si aim to directly integrate III-V active materials onto silicon photonics platforms at the circuit layer. This approach offers a shortcut compared to other integration mechanisms, as it eliminates the need for additional coupling schemes. In contrast, nano-ridges grown on Si still require a coupling modality to redirect the optical path to the Si level. Additionally, the wide-field grown method facilitates easy integration into a standard Si photonics process flow, allowing for electrical contacting through Si. Moreover, it provides versatility, as different III-V active material combinations can potentially be grown on the same wafer.

Unfortunately, in this early trial of InGaAs devices detailed in Chapter 6, device performance was limited by the quality of the grown material. The insertion loss spectra did not exhibit sharp band-edges for the targeted EAM demonstration with 47% In composition; instead, the insertion loss was smeared throughout the spectra. The grown material exhibited ternary compound composition inhomogeneities, confirmed by scanning transmission electron microscopy (STEM) with energy dispersive X-ray spectroscopy (EDS) metrology. Additionally, the devices showed low performance for photodetection, limited by dark current, indicating high defect densities.

This study underscores the crucial significance of material quality, as all critical active device performance metrics depend on it. It has been demonstrated that more exhaustive growth studies are necessary to achieve sufficient material quality and homogeneity while maintaining low defect densities. This study represents a significant first step in establishing the low-end reference for the material quality of InGaAs wide-field grown devices on Si and emphasizes once again why material quality is paramount for high-performance devices.

Future studies on wide-field grown devices should emphasize epitaxial growth uniformity and effective defect reduction. The defect reduction for the heteroepitaxial III-V growths in Si was previously shown with a relaxation seed layer [9]. In their study in 2017, Li et al. demonstrated GaAs seed layers in Si V-grooves for the strain reduction of GaSb growth, and ”defect-necking” with the oxide layers at the top edges of V-grooves, where the seed layer misfit defects are trapped. Beyond the required epitaxial growth studies, the wide-field grown devices will offer quick integration on existing silicon photonics platforms, and the studies on them have continued for the wide-field grown GaAs phase shifters [10, 11].

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