FACULTY OF ENGINEERING
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Integrated Photonic Modulators Based on Graphene and Other 2D-Materials for Optical Interconnects

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A decade ago, the idea of pursuing a challenging PhD and successfully completing it seemed impossible to me. I doubted my ability to publish data in reputable journals or to produce a thesis akin to a book in English. However, the journey of life has proven to be unexpectedly fascinating. Despite the fears and confusion that accompanied me, it led me step by step to where I am today. Throughout my studies, I have not only acquired knowledge but also forged numerous friendships and connections, all of which have consistently reaffirmed my decision to pursue a PhD. If I could turn back time, I would undoubtedly choose to embark on this journey again, particularly in the position I find myself in now.

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List of Acronyms

3D	3Dthree-dimension
2D	2Dtwo-dimension
AI	AIArtificial Intelligence
ALD	ALDAtomic Layer Deposition
BHF	BHFBuffered Hydrofluoric Acid
BPS	BPSBand Pass Filter
BOX	BOXBuried Oxide
BTO	BTOBarium Titanate
CDF	CDFCumulative Distribution Function
CMOS	CMOSComplementary Metal-Oxide-Semiconductor
CMP	CMPChemical Mechanical Polishing
CNIT	CNITConsorzio Nazionale Interuniversitario per le Telecomunicazioni
CVD	CVDChemical Vapor Deposition
DLG	DLGDual Single-Layer Graphene
DoE	DoEDesign of Experiment
DUT	DUTDevice Under Test
EBL	EBLElectron Beam Lithography

EAM	EAMElectro-Absorption Modulator
EDFA	EDFAErbium-Doped Fiber Amplifier
EO	EOElectro-Optic
EME	EMEEigenMode Expansion
EPD	EPDEndpoint Detection
ERM	ERMElectro-Refraction Modulator
ER	ERExtinction Ratio
ETM	ETMElectro-Transmission Modulator
FET	FETField-Effect Transistor
FK	FKFranz-Keldysh
FOM	FOMFigure of Merit
FSR	FSRFree Spectral Range
FWHM	FWHMFull Width at Half-Maximum
GOG	GOGGraphene-Oxide-Graphene
GOS	GOSGraphene-Oxide-Silicon
GRA1	GRA1Bottom (First) Graphene Layer
GRA2	GRA2Top (Second) Graphene Layer
hBN	hBNHexagonal Boron Nitride
HSQ	HSQHydrogen Silsesquioxane
IEA	IEAInternational Energy Agency
ICP	ICPInductively Coupled Plasma
IL	ILInsertion Loss

LN	LNLithium Niobate
LCA	LCALightwave Component Analyzer
LIDAR	LIDARLight Detection and Ranging
MDB	MDBMeasurement-Dependent Behavior
MD	MDModulation Depth
MMI	MMImulti-mode interference
MOSFET	MOSFETMetal-Oxide Field-Effect Transistor
MPM	MPMMicrowave Photonics Modulator
MZIs	MZIMach-Zehnder Interferometer
MZM	MZMMach-Zehnder Modulator
NP	NPNeutrality Point
NIR	NIRNear-Infrared
OES	OESOptical Emission Spectroscopy
PD	PDPhotodetector
PIN	PINP-doped/Intrinsic/N-doped
PL	PLPhotoluminescence
PM	PMPhase Modulator
PMMA	PMMAPoly-Methyl Methacrylate
PMD	PMDPre-Metal Dielectric
poly-Si	poly-SiPoly-Silicon
PNA	PNAPerformance Network Analyzer
PN	PNP-doped/N-doped
PRBS	PRBSPseudorandom Binary Sequence

QAM	QAMQuadrature Amplitude Modulation
Q-factor	Q-factorQuality Factor
QCSE	QCSEQuantum-confined Stark effect
RIE	RIEReactive Ion Etching
RM	RMRing Modulator
RR	RRRing Resonator
SOS	SOSSilicon/Oxide/Silicon
SEM	SEMScanning Electron Microscope
SHG	SHGSecond-Harmonic Generation
SLG	SLGSingle-Layer Graphene
SMF	SMFSingle-Mode Fiber
SOI	SOISilicon-On-Insulator
STI	STIShallow Trench Isolation
TE	TETransverse Electric
TMDC	TMDCTransition Metal Dichalcogenide
TP	TPTransmission Penalty
TLM	TLMTransfer Length Measurement
TMA	TMATri-Methylaluminium
VNA	VNAVector Network Analyzer
XTEM	XTEMCross-sectional Transmission Electron Microscope

List of Publications

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Samenvatting

De afgelopen decennia is de alomtegenwoordige invloed van het internet alleen maar toegenomen. Mensen besteden alsmaar meer tijd aan verschillende online-activiteiten, zoals video kijken, online winkelen, sociale media-interacties en het gebruik van AI. Deze digitale transformatie heeft ons dagelijks leven aanzienlijk verrijkt. Datacenters spelen hierbij een cruciale rol en vormen de ruggengraat die dit digitale tijdperk ondersteunt. In 2016 voorspelde Cisco, een groot telecommunicatiebedrijf, dat het datacenterverkeer in 2021 20,6 ZB/jaar zou bedragen. Deze voorspelling anticipeerde echter niet op de wereldwijde uitbraak van Covid-19, die de manier waarop mensen werken en leven dramatisch veranderde. Tijdens deze uitdagende periode werd de afhankelijkheid van internet voor virtuele vergaderingen, contact met familie en werken op afstand steeds groter. Daardoor werd het toch al urgente probleem van het escalerende dataverkeer alleen nog maar verergerd.

Geconfronteerd met een ongekende toename van datageneratie en -consumptie worstelen datacenters met een groot aantal nieuwe uitdagingen, waarvan de belangrijkste de noodzaak is om het energieverbruik te beperken. Het duizelingwekkende energieverbruik komt voornamelijk voort uit het uitgebreide aanbod aan computerapparatuur en bijbehorende koelsystemen. De continue werking en koeling van deze machines vertalen zich in een aanzienlijke behoefte aan elektrisch vermogen. Dit was de aanleiding om optische interconnecties te gaan onderzoeken als alternatief voor traditionele elektrische dataconnecties. Optische verbindingen bieden een hogere bandbreedte en lagere latentie in vergelijking met conventionele elektronische verbindingen, waardoor een snellere en efficiëntere gegevensoverdracht mogelijk wordt en signaalverlies wordt tegengegaan. Naast deze voordelen qua performatie, sluit de adoptie van optische verbindingen aan bij de bredere doelstelling van het verbeteren van de energie-efficiëntie in datacentra en krachtige computersystemen, en draagt zo bij aan een duurzaam technologisch landschap.

Siliciumfotonica is een geavanceerde technologie die de adoptie van optische verbindingen in board-to-board- en chip-to-chip-verbindingen mogelijk maakt. Door gebruik te maken van bestaande CMOS-fabricageprocessen kunnen silicium gebaseerde fotonische circuits in heel hoge volumes en met hoge betrouwbaarheid worden gefabriceerd. Binnen dit innovatieve domein wordt een breed scala aan optische componenten en circuits rechtstreeks op siliciumsubstraten gedefinieerd, waardoor optische en elektronische functionaliteiten naadloos op één chip kunnen worden

geïntegreerd. Op dit moment zijn heel wat verschillende passieve en actieve bouwblokken beschikbaar binnen dit platform. Desalniettemin blijven er verschillende uitdagingen. Zo is het realiseren van de 'ideale' elektro-optische (EO) modulator, met een grote aan-uit verhouding (ER), laag insertieverlies (IL), hoge snelheid en laag stroomverbruik nog altijd moeilijk. De modulator heeft idealiter een compacte voetafdruk en een lage stuurspanning, zodat het compatibel is met CMOS (complementaire metaaloxide halfgeleider)-schakelingen. Bovendien moeten modulatoren die gebruikt worden in systemen met hoge integratiedichtheid betrouwbaar, reproduceerbaar en compatibel zijn met bestaande CMOS-productietechnieken. Het tegelijkertijd voldoen aan al deze criteria blijkt een uitdaging te zijn voor pure op silicium gebaseerde modulatoren die afhankelijk zijn van het relatief zwakke plasma-dispersie-effect. Om deze beperkingen te overwinnen heeft recent onderzoek zich intensief gericht op de integratie van niet-silicium materialen, waaronder germanium, III-V halfgeleiders, polymeren en 2D materialen, met silicium platforms.

Van de verschillende benaderingen heeft grafeen veel aandacht gekregen vanwege zijn uitzonderlijke elektrische en optische eigenschappen. Op grafeen gebaseerde elektro-absorptiemodulatoren (EAM's) zijn een veelbelovende alternatief voor bestaande siliciummodulatoren, waarbij gebruik wordt gemaakt van de breedbandige en afstembare lichtabsorptie van grafeen in combinatie met de intrinsieke ultrahoge mobiliteit. In het afgelopen decennium hebben op grafeen gebaseerde EAM's verschillende voordelen laten zien ten opzichte van pure siliciummodulatoren. Hiertoe behoren een optische bandbreedte van meer dan 180 nm, een uitstekende temperatuurtolerantie van meer dan 30°C, een hoge snelheid van meer dan 40 Gbps en een laag energieverbruik van ongeveer 112 fJ/bit. Met name de DLG-structuur (dual single-layer graphene) heeft de afgelopen jaren aan populariteit gewonnen. Deze DLG EAM biedt niet alleen sterkere modulatie, maar zorgt ook voor compatibiliteit met verschillende golfgeleiderplatforms. Daarom is de integratie van een DLG-structuur op SiN-golfgeleiders en silicium-slotgolfgeleiders in verschillende artikelen onderzocht.

Om het gebruik van grafeengebaseerde componenten in praktische toepassingen te overwegen is het echter noodzakelijk om een schaalbaar pad richting grootschalige productie met een hoge betrouwbaarheid tegen lage kosten te demonstreren. Eerder onderzoek gebruikte vaak kleine coupons of niet schaalbare grafeen depositiemethodes, i.p.v. volledig CMOS-compatibele integratietechnologie. De belangrijkste uitdagingen draaien om de lithografieprocessen, de grafeeninkapseling en de contacten. Dit is de primaire focus van hoofdstuk r̃ef{chap:inline_SLGEAM}. Het onderzoek maakt specifiek gebruik van enkellaags grafeen elektro-absorptiemodulatoren als testvehikel, waarbij integratie op waferschaal wordt aangetoond in een 300mm CMOS pilootlijn. Door drie kritische processtappen te optimaliseren en een CMOS-compatibele speciale integratieaanpak te implementeren, is de yield van het proces beter dan 95% en zijn de prestaties vergelijkbaar met die van CVD-grafeen gebaseerde componenten gedemonstreerd in laboratoriumomgevingen. De kennis uit dit

onderzoek kan worden uitgebreid tot een geavanceerde bibliotheek van op grafeen gebaseerde opto-elektronische apparaten, waaronder modulatoren, fotodetectoren en sensoren. Deze vooruitgang legt de basis voor de industriële toepassing van op grafeen gebaseerde fotonica-apparaten.

Een andere voorwaarde om op grafeen gebaseerde componenten in praktische toepassingen te gaan gebruiken, is het demonstreren van prestaties die vergelijkbaar en beter zijn dan die van de beste siliciummodulatoren. Om een snellere cyclus van ontwerp-fabricage-testen toe te laten spitsen we ons toe op lab-gebaseerde fabricage, op kleinere coupons. Ons onderzoek concentreerde zich op het potentieel van dubbele enkellaags grafeenmodulatoren (DLG), waaronder elektro-absorptiemodulatoren (EAM's), Mach-Zehnder-modulatoren (MZM's) en Ringmodulatoren (RM's). Dankzij een zorgvuldig ontwerp en integratie vertonen onze DLG EAM en MZM een FOM (Figure-of-Merit) van respectievelijk 8,9 dB en 27,6 dBV bij een stuurspanning van 2 V. Deze prestaties overtreffen andere state-of-the-art modulatoren op basis van grafeen en zijn vergelijkbaar met Si en Ge modulatoren die gebruik maken van respectievelijk het plasmadispersie en Franz-Keldysh (FK) effect. Om de prestaties van de modulator verder te verbeteren, integreren we DLG in slotgolfgeleiders, waardoor de opsluiting van het licht in de grafeenlagen wordt verbeterd. Apparaten met slotgolfgeleiders vertonen een superieure modulatie-efficiëntie (0,038 dB/μm/V en 0,079 Vcm) in vergelijking met apparaten met stripgolfgeleiders. De FOM in onze huidige EAM's en MZM's overtreft echter niet onze eigen op strip-golfgeleiders gebaseerde apparaten. Door middel van uitgebreide simulaties, onderzoeken we de tradeoffs geassocieerd met het gebruik van slotgolfgeleiders en stellen we een pad voorop voor slot waveguide-gebaseerde modulatoren als het superieure platform voor het realiseren van high-performance modulatoren.

In de wereld van 2D materialen is grafeen een prominente speler, maar een overvloed aan atomaire dikke materialen binnen deze uitgebreide familie blijft grotendeels onaangeroerd. De laatste studie in dit proefschrift onderzoekt MoS_2, een 2D-materiaal met een bandgap, voor de realisatie van fasemodulatoren met lage verliezen. Met behulp van drie verschillende structuren bestuderen we het potentieel ervan. D.m.v. de integratie van een dubbele enkellaags MoS_2 structuur op een silicium golfgeleider laten we met succes een MZM zien met een indrukwekkende modulatie-efficiëntie van ongeveer 1 Vcm en een opmerkelijke FOM_{pm} van 6 dBV. De uitstekende elektro-optische prestaties van op MoS_2 gebaseerde modulatoren positioneren hen als geduchte spelers in het veld, overtreffen andere op 2D gebaseerde modulatoren en doen het zelfs beter dan op silicium gebaseerde apparaten.

Concluderend kan gesteld worden dat de gezamenlijke inspanningen die in dit proefschrift beschreven worden aanzienlijk bijdragen aan de vooruitgang van ons begrip en gebruik van 2D materialen in fotonische chips. Dit werk draagt aanzienlijk bij tot ons begrip van deze materialen en maakt de weg vrij tot wijdverspreide adoptie ervan in toekomstige communicatiesystemen.

Summary

In recent decades, the pervasive influence of the Internet has become increasingly apparent as people dedicate more of their time to various online activities, such as video watching, online shopping, social media interactions, and leveraging AI assistance. This digital transformation has significantly enriched our daily lives. Amidst this dynamic landscape, data centers emerge as the heroes of the digital age, serving as the essential infrastructure backbone that steadfastly supports our data-driven world. In 2016, Cisco, a major telecommunications company, predicted that data center traffic would reach 20.6 ZB/year by 2021. However, this forecast did not anticipate the global outbreak of Covid-19, which dramatically altered the way people work and live. During this challenging period, the reliance on the Internet for virtual meetings, connecting with family, and remote work intensified, exacerbating the already pressing issue of escalating data traffic.

In the face of this unprecedented surge in data generation and consumption, data centers grapple with a myriad of new challenges, foremost the imperative to curtail power usage amid the relentless growth in data volume. The staggering energy consumption primarily arises from the extensive array of computing equipment and associated cooling systems. The continuous operation and cooling demands of these machines translate into a substantial electricity supply requirement. Consequently, the exploration of optical interconnects as a superior alternative to traditional electrical interconnects emerges as a compelling and pivotal research focus. Optical interconnects present a solution by offering elevated bandwidth and reduced latency compared to conventional electronic interconnects, facilitating accelerated and more efficient data transfer while mitigating signal degradation. Beyond these performance benefits, the adoption of optical interconnects aligns with the broader objective of enhancing energy efficiency in data centers and high-performance computing systems, contributing to a sustainable and streamlined technological landscape.

Silicon photonics is a cutting-edge technology facilitating the adoption of optical interconnects in board-to-board and chip-to-chip connections. Leveraging existing CMOS fabrication processes, silicon photonics is well-suited for high-yield, high-volume production at a low cost. Within this innovative domain, a diverse range of optical components and circuits are defined directly onto silicon substrates, seamlessly integrating optical and electronic functionalities on a single chip. Con-

sequently, various silicon-based passive and active optical components have been extensively explored and now widely deployed. Nevertheless, several challenges remain. As an example, achieving an ideal electro-optic (EO) modulator, requiring key characteristics such as a large extinction ratio (ER), low insertion loss (IL), high speed, and low power consumption, is still difficult. The device ideally should feature a compact footprint and a low driving voltage, ensuring compatibility with CMOS (complementary metal-oxide-semiconductor) circuitry. Moreover, modulators employed in high-integration density systems must demonstrate reliability, reproducibility, and compatibility with existing CMOS manufacturing techniques. Meeting all these criteria simultaneously proves challenging for pure silicon-based modulators reliant on the relatively weak plasma dispersion effect. To overcome these limitations, recent research has intensely focused on the integration of non-silicon materials, including germanium, III-V semiconductors, polymers, and 2D materials, with silicon platforms.

Among various approaches, graphene has garnered considerable attention owing to its exceptional electrical and optical characteristics. Graphene-based electro-absorption modulators (EAMs) are proposed as promising alternatives to high-speed silicon modulators, leveraging graphene's broadband and tunable light absorption, coupled with its intrinsic ultra-high mobility. Over the past decade, graphene-based EAMs have showcased several advantages over pure silicon modulators. These include a broadband optical bandwidth exceeding 180 nm, excellent temperature tolerance surpassing 30°C, high-speed operation capability exceeding 40 Gbps, and low power consumption of approximately 112 fJ/bit. Notably, the dual single-layer graphene (DLG) structure has gained popularity in recent years. This DLG EAM not only offers stronger modulation but also ensures compatibility with various waveguide platforms. Consequently, the integration of a DLG structure onto SiN waveguides and silicon slot waveguides has been explored in several papers.

However, for graphene devices to be used in practical applications, it is imperative to demonstrate a scalable path for large-scale manufacturing with high yield at a low cost. Previous literature often utilized small coupons or non-scalable graphene supplies, lacking fully CMOS-compatible integration technology. Key challenges revolve around lithography processes, graphene encapsulation, and contacts. This constitutes the primary focus and accomplishment detailed in Chapter 3. The study specifically employs single-layer graphene electro-absorption modulators as a test vehicle, achieving wafer-scale integration in a 300mm pilot CMOS foundry environment. By optimizing three critical processing steps and implementing a CMOS-compatible dedicated integration approach, the device yield surpasses 95%, exhibiting performance metrics comparable to those of CVD graphene devices demonstrated in laboratory settings. The knowledge derived from this study has the potential to extend to a sophisticated library of graphene-based optoelectronic devices, including modulators, photodetectors, and sensors. This advancement lays the foundation for the industrial adoption of graphene-based photonics devices.

Another key requirement for graphene-based photonics devices to be used in prac-

tical applications is to demonstrate competitive performance comparable to state-of-the-art devices. To achieve this, our study focuses on laboratory-based devices with small coupons allowing for rapid fabrication. Our exploration centers on the potential of dual single-layer graphene (DLG) modulators, encompassing electro-absorption modulators (EAMs), Mach-Zehnder modulators (MZMs), and Ring modulators (RMs). With meticulous design and integration, our DLG EAM and MZM exhibit a figure of merit of 8.9 dB and 27.6 dBV, respectively, at a driving voltage of 2 V. This performance surpasses other state-of-the-art graphene-based modulators and is comparable to Si and Ge devices utilizing the plasma dispersion and Franz-Keldysh (FK) effect, respectively. To further enhance device performance, we integrate DLG onto slot waveguides, enhancing mode confinement in the graphene layers. Slot waveguide-based devices exhibit superior modulation efficiency (0.038 dB/µm/V and 0.079 Vcm) compared to strip waveguide-based devices. However, the figure of merit in our current EAMs and MZMs does not surpass our own strip-based devices. Through comprehensive simulations, we elucidate the tradeoffs associated with using slot waveguides and propose the path for slot waveguide-based devices as the superior platform for realizing high-performance modulators.

In the realm of 2D materials, graphene has been a prominent player, yet a plethora of atomic-thick materials within this extensive family remains largely untapped. The final study in this thesis delves into the exploration of MoS_2, a 2D material with a bandgap, specifically for low-loss phase modulators. Employing three distinct structures, we study its potential, and with the incorporation of a dual single layer MoS_2, we successfully showcase a MZM boasting an impressive modulation efficiency of approximately 1 Vcm and a remarkable figure of merit (FOM_{pm}) of 6 dBV. The outstanding electro-optic performance of MoS_2-based modulators positions them as formidable contenders in the field, surpassing other 2D-based modulators and even outperforming silicon-based devices.

In conclusion, the collective endeavors detailed in this thesis significantly contribute to the progression of our comprehension and utilization of 2D materials in photonic devices. These advancements not only deepen our understanding but also set the stage for the widespread integration of these materials into the fabric of next-generation communication technologies, propelling innovation and fostering transformative changes in the field.

1

INTRODUCTION

1.1 Optical Interconnect

In the contemporary digital landscape, our world is undergoing a remarkable transformation, driven by the relentless surge in data generation and consumption. Today, the ease with which people can seamlessly share, create, and consume information across a multitude of social media platforms is nothing short of astounding. To put this digital frenzy into perspective, consider the staggering statistics of 2022: every passing minute witnesses the posting of 1.7 million comments on Facebook, the sharing of 66,000 photos on Instagram, and the initiation of 5.9 million searches on Google (Figure 1.1) [1]. The global volume of data forecasted to be generated, recorded, duplicated, and utilized in 2022 amounts to 97 zettabytes, with projections indicating a surge to 181 zettabytes by 2025. [32].

However, this era of information abundance has taken an exponential leap when Artificial Intelligence (AI) enters the stage. With its unparalleled prowess in enhancing efficiency, automation, personalization, and decision-making, AI has seamlessly integrated into our daily lives, spanning various domains. From revolutionizing communication and entertainment to making significant inroads in healthcare, finance, and transportation, AI has the potential to reshape the way we live and interact with our surroundings. In the not-so-distant future, we might envision a world where surgeries can be performed without human hands and where trans-

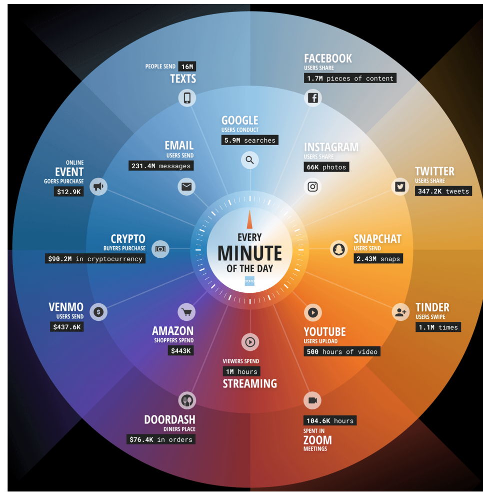

Figure 1.1: The infographic depicts the volume of data generated by the Internet every minute in 2022, highlighting specific social activities, taken from [1].

portation no longer relies on human drivers, thanks to the advent of smart AI-based ecosystems.

In this dynamic landscape, data centers stand out as the unsung heroes of the digital age. Operating behind the scenes, they constitute the invisible backbone infrastructure that diligently supports our data-driven world. Data centers provide the critical framework required to store, process, and transmit this colossal volume of data efficiently and securely. As our world continues to evolve in the era of data and AI, data centers remain indispensable in enabling the seamless flow of information and the realization of our digital aspirations.

Faced with an exponential increase in data generation and consumption, data centers meet a number of new challenges. The primary one of these is the need to reduce power consumption while the volume of data handled continues to grow. According to the International Energy Agency (IEA), data centers currently consume more electricity than entire nations. Furthermore, the forecast suggests that this staggering demand could more than triple by 2030, rocketing to an astonishing 752 terawatt-hours [33].

The extraordinary magnitude of energy consumption stems primarily from the vast array of computing equipment—ranging from thousands to millions of units—incessantly engaged in the processing and storage of data. At the same time, data centers produce a lot of heat. To prevent overheating and make sure the equipment stays at the right temperature, data centers use cooling systems including things like air

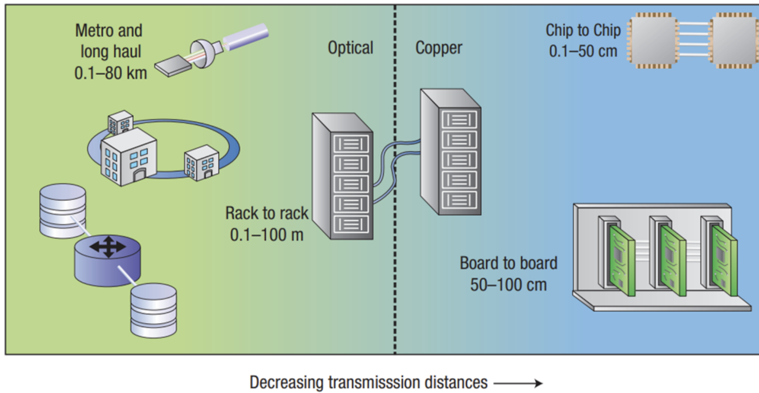

Figure 1.2: The adoption of communication technology, distinguishing between optical and electrical approaches, as a function of transmission distance. Taken from [2]

conditioning and industrial cooling units. The relentless operation and cooling of these machines necessitates a substantial supply of electricity. The imperative of swiftly transferring, storing, and processing vast volumes of data, all while maintaining exceptionally low power consumption (less than 1 picojoule per bit), has emerged as the driving force behind the advancement and adoption of optical interconnects as a superior alternative to their electrical counterparts.

In transitioning to optical interconnects, it is essential to assess their state and discern the advantages they offer over their electrical counterparts. As highlighted in a Figure 1.2, optical interconnects via fiber optics have firmly established their dominance in long-distance connections, while electrical interconnects remain prevalent for shorter distances [2]. In the realm of rack-to-rack interconnections, a judicious fusion of both technologies often takes precedence, strategically harmonizing their attributes to optimize performance and operational efficiency.

However, the landscape is evolving rapidly, primarily propelled by the exponential surge in data traffic. Electrical interconnects, especially over shorter spans, are grappling with formidable integration challenges [34–36]. Efforts to accommodate more wires within confined spaces have led to the reduction of wire width, consequently elevating resistance. Although increasing wire height appears to be a potential solution, it introduces a delicate trade-off, as it concurrently escalates capacitance and invites unwanted signal coupling [37]. These collective challenges conspire to limit the speed and overall quality of electrical interconnects [38–41].

In this context, optical interconnects emerge as a promising avenue for addressing these impediments, offering the potential for reduced signal loss, higher bandwidth, lower energy consumption, and minimal crosstalk [42, 43]. The community's ob-

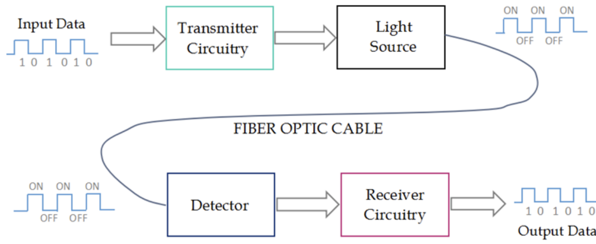

Figure 1.3: Schematic representation of an electro-optical interconnect, where electrical signals are converted into optical signals by a transmitter and transported using a light source. Upon reaching the destination, the optical signals are detected by a detector and subsequently converted back into electrical signals by a receiver.

jective is to push the boundaries of optical performance and pave the way for the seamless integration of optical I/O directly into servers, enabling board-to-board and chip-to-chip connectivity. This advancement holds the promise of revolutionizing data center and high-speed communication infrastructures, addressing key challenges while unlocking new realms of speed and efficiency.

1.2 Silicon Photonics

1.2.1 Introduction

Optical communication links comprise three essential components: transmitters, communication channels, and receivers as shown by Figure 1.3. These links begin with the creation of a data stream in the electrical domain, which is then converted into an optical signal by a transmitter equipped with a laser and/or a modulator. The modulated optical signal is subsequently transmitted from one location to another through various communication channels, including air, and optical fiber. Upon reaching its destination, the optical signal is reconverted into an electrical signal by an optical receiver, employing a photodetector (PD) and often necessitating the use of an amplifier.

Silicon photonics is a cutting-edge technology that seamlessly combines silicon-based materials with integrated circuit manufacturing techniques to engineer devices and systems for manipulating and transmitting data via light [44] (see Figure 1.4. Leveraging established CMOS fabrication processes, silicon photonics is now poised for cost-effective, high-volume production with exceptional yields [3]. Within this pioneering domain, a wide array of optical components and circuits is

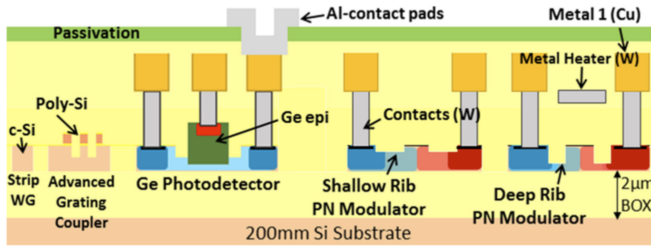

Figure 1.4: Schematic cross-section of imec's silicon photonics platform, highlighting its fundamental passive and active components. Taken from [3].

directly etched onto silicon substrates, facilitating the seamless fusion of optical and electronic functionalities on a single chip. This advancement opens up a new frontier for expanding the horizons of optical input/output, enabling the potential of board-to-board and chip-to-chip connectivity.

One of the key advantages of silicon photonics lies in its ability to produce silicon waveguides on a sub-micron scale, which can effectively guide light and serve as the communication channel [44]. This capability is instrumental in enhancing the functionality of integrated circuits, including the design of filters and interferometers, as will be discussed in upcoming sections. Beyond its role in passive components, silicon materials are crucial in the evolution of active devices, like modulators, which we will explore further in subsequent sections.

1.2.2 Mach-Zehnder Interferometers

The Mach-Zehnder Interferometers (MZIs) hold a prominent place in optical circuits and serves as the fundamental building block for several other optical devices, including modulators, switches, and filters. A schematic representation of this device is shown in Figure 1.5. The MZI is essentially a passive waveguide structure that accomplishes the task of splitting an incoming optical signal into two separate arms, which are later recombined [44]. In this thesis, we employ 2x2 MZIs, featuring multi-mode interference (MMI) couplers to facilitate the division and recombination of the propagating signal [44]. The recombination of these paths results in an interference pattern. This pattern is created by the constructive and destructive interference of light waves that have traveled different distances in the two arms of the interferometer.

A complete description of an MZI hinges on two critical components: the coupler and the changes in absorption and phase that occur during propagation along each

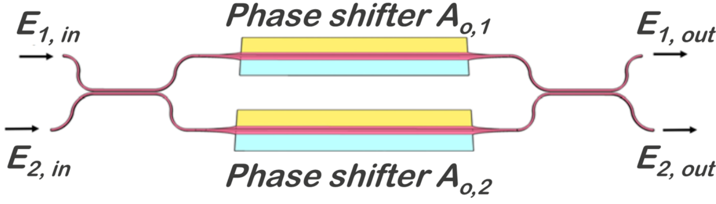

Figure 1.5: Schematic for a 2x2 Mach-Zehnder interferometer [4].

of the arms. The coupler is characterized by its transmission and cross-coupling coefficients, denoted as "t" and "k" which define the distribution of the electric field between the through and cross ports. The through port pertains to cases where the transmission occurs along the same channel as the input signal, whereas the cross port relates to scenarios where the output crosses over to the other channel. The behavior of an 2x2 MZI can be effectively modeled in terms of input and output electric fields, as detailed in reference [44].

$$\begin{bmatrix} E_{1,out} \\ E_{2,out} \end{bmatrix} = \Phi_{c,1} \begin{bmatrix} A_{0,1} & 0 \\ 0 & A_{0,2} \end{bmatrix} \Phi_{c,2} \begin{bmatrix} E_{1,in} \\ E_{2,in} \end{bmatrix} \tag{1.1}$$

$$\Phi_c = \begin{bmatrix} t & -jk \\ -jk & t \end{bmatrix} \tag{1.2}$$

$$A_{0,x} = A_0 \exp{(-\frac{1}{2}\alpha_x L_x)} \sin{(\omega T - \phi_x)} \tag{1.3}$$

where Φ_c is an ideal loss-less 2×2 transfer matrix and t and k satisfy the following equation:

$$|t^2| + |k^2| = 1 \tag{1.4}$$

L represents the propagation length of the arm, while $A_{0,x}$ characterizes the change in amplitude of the electric field, incorporating the power attenuation coefficient, α. Additionally, ϕ denotes the phase of the electric field, and ω stands for the angular frequency, and T signifies time [45].

Given the remarkably high optical frequencies at play, our observations are confined to the time-averaged attributes of these waves. Therefore, it becomes crucial to replace all terms in the equation1.1 with their corresponding time-averaged

equivalents. By employing trigonometric identities and incorporating these time-averaged transformations, we can articulate the transmission parameters from input 1 to output 1 (T_{11}) and output 2 (T_{12}) as follows:

$$T_{11} = \frac{A_0^2}{2}(\exp(-\alpha_1 L_1)t^4 + \exp(-\alpha_2 L_2)k^4 \\ - 2t^2k^2 \exp\left(-\frac{1}{2}\alpha_1 L_1 - \frac{1}{2}\alpha_2 L_2\right)\cos(\phi_2 - \phi_1)) \tag{1.5}$$

$$T_{12} = \frac{(A_0 tk)^2}{2}(\exp(-\alpha_1 L_1) + \exp(-\alpha_2 L_2) \\ + 2\exp\left(-\frac{1}{2}\alpha_1 L_1 - \frac{1}{2}\alpha_2 L_2\right)\cos(\phi_2 - \phi_1)) \tag{1.6}$$

In this thesis, our primary focus lies on utilizing an unbalanced MZI, characterized by different propagation lengths (ΔL) for each arm. This specific configuration readily allows for the observation of a wavelength-dependent interference pattern at the output. The free spectral range (FSR) can be determined:

$$FSR = \frac{\lambda^2}{n_g \Delta L} \tag{1.7}$$

where λ is the wavelength and n_g is the group index. The relationship with effective index is shown as follows:

$$n_g = n_{eff} - \lambda \frac{d(n_{eff})}{d(\lambda)} \tag{1.8}$$

1.2.3 Ring resonators

The Ring Resonator (RR), characterized by its closed-loop waveguide, is a pivotal component with a wide range of applications of sensors [46–49] and filters [50–52] in photonics. Its exceptional capability to precisely control and manipulate light underscores its significance in contemporary optical systems [53]. A noteworthy feature is the compact size of ring resonators, typically just a few micrometers in dimension. This compactness enables high-density volume integration, in stark contrast to the relatively larger footprint of MZIs which often span sub-centimeter ranges. A schematic representation of this device is shown in Figure 1.6.

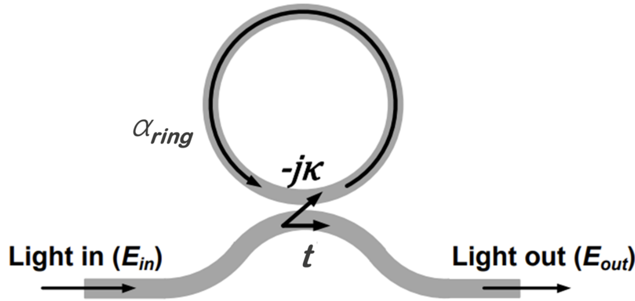

Figure 1.6: Schematic for a ring resonator.

The ring resonator comprises two essential components: a ring waveguide and a bus waveguide, strategically positioned in close proximity to facilitate light coupling. The interaction between these waveguides can be succinctly described using two key parameters: α_{ring} and t. Firstly, the single-pass transmission coefficient α_{ring} signifies the proportion of light lost during propagation in the ring. It factors in all sources of loss, including absorption and scattering [53]. Secondly, there is t, known as the 'through' coefficient, which quantifies the relationship between the input optical field and the output optical field.

Additionally, another vital parameter presented in Figure 1.6 is k, the coupling coefficient. This parameter defines the ratio between the input optical field and the optical field coupled to the ring waveguide. Notably, when light couples to the ring waveguide, a 90 degree phase-shift occurs, and therefore, the coupling coefficient is generally expressed as $-jk$. Assuming lossless coupling, and in adherence to the conservation of energy, the relationship between t and k can be expressed as equation 1.4.

Upon the introduction of light into the bus waveguide, a segment of the optical field couples with the ring waveguide, providing loss and a phase shift within a single cycle. Upon completing its circuit within the ring, a part of the optical field couples with the output of the ring resonator, while the remaining portion embarks on another orbit. This cyclical progression unfolds infinitely, and the output optical field can be articulated as follows:

$$\begin{aligned}\frac{E_{out}}{E_{in}} &= t - k^2\alpha_{ring}\exp(-j\phi) \\ &\quad [1 + t\alpha_{ring}\exp(-j\phi) + (t\alpha_{ring}\exp(-j\phi))^2 + \dots]\end{aligned} \tag{1.9}$$

In this equation, we use the notations E_{in} and E_{out} to represent the input and output

optical fields, respectively. The phase (ϕ) within the ring waveguide is expressed as $\frac{2\pi n_{eff} L}{\lambda}$, with L representing the circumference of the ring waveguide, and n_{eff} signifying the effective index of the waveguide. The ratio of the transmitted and incident optical field and transmission in the bus waveguide can be written as:

$$\frac{E_{out}}{E_{in}} = \frac{t - \alpha_{ring} \exp(-j\phi)}{1 - t\alpha_{ring} \exp(-j\phi)} \tag{1.10}$$

$$T_{bus} = |\frac{E_{out}}{E_{in}}|^2 = \frac{t^2 + \alpha_{ring}^2 - 2t\alpha_{ring} \cos(\phi)}{1 + t^2\alpha_{ring}^2 - 2t\alpha_{ring} \cos(\phi)} \tag{1.11}$$

Resonance within the ring waveguide manifests when the condition $\phi = 2m\pi$ is met for any integer m, aligning with the in-phase requirement characteristic of the ring waveguide. This resonance criterion can be expressed as:

$$m\lambda_{res} = n_{eff} L \tag{1.12}$$

where m is the modal integer and λ_{res} is the resonance wavelength.

Resonances in optical systems are commonly evaluated using the quality factor (Q-factor), a measure of the resonance's sharpness. The Q-factor is expressed as:

$$Q = \frac{\lambda_{res}}{FWHM} \tag{1.13}$$

where FWHM represents the full width at half maximum. This factor provides insights into the efficiency of energy storage within the cavity and its ability to sustain oscillations. A higher Q factor indicates a sharper resonance, enabling the cavity to store energy for an extended period. However, this also implies a longer time for light to exit the ring, leading to increased photon lifetime. This prolonged photon lifetime can, in turn, limit the operational speed of the device. The Q-factor can be correlated with the cavity photon lifetime(τ_{cav}).

$$\tau_{cav} = \frac{\lambda_{res}}{2\pi c} Q \tag{1.14}$$

The 3dB bandwidth due to photon lifetime (f_{cav}) and overall EO bandwidth ($f_{overall}$) is given by [54]:

$$f_{cav} = \frac{1}{2\pi\tau_{cav}} \tag{1.15}$$

$$(\frac{1}{f_{overall}})^2 = (\frac{1}{f_{cav}})^2 + (\frac{1}{f_{RC}})^2 \quad (1.16)$$

where f_{RC} is the bandwidth limited by the RC delay.

1.2.4 Silicon based modulators

Silicon-based modulators primarily exploit the plasma dispersion effect, utilizing variations in free carrier concentrations to induce changes in the refractive index [44, 55]. This approach opens the door to exploring the electro-optic (EO) effect, a phenomenon in which the optical properties of a material respond to a varying electric field [45]. When exploiting this phenomenon to control optical losses along a straight waveguide, it gives rise to the development of electro-absorption modulators (EAM) designed for information transmission. Conversely, achieving modulation in the effective refractive index often requires the assistance of an interferometer to translate the index changes into alterations in amplitude. Devices incorporating an interferometer structure for this purpose are referred to as electro-refraction modulators (ERM). [44]. Pure silicon modulators relying solely on the plasma dispersion effect are inherently weak, rendering them unsuitable for efficient electro-absorption modulation. Consequently, the integration of interferometric devices, such as Mach-Zehnder interferometers (MZI) and ring resonators (RR), to form electro-refraction modulators is a typical approach for enhancing the performance of silicon-based modulators. These devices are commonly referred to as Mach-Zehnder modulators (MZM) and ring modulators (RM).

Three primary methods are employed to introduce changes in free carrier concentration within silicon material: (a) Injection [5, 6, 56–58], where minority carriers are introduced by forward biasing a p-doped/intrinsic/n-doped (PIN) silicon junction. (b) Accumulation [7–9, 59–61], which involves the accumulation of majority carriers across a silicon/oxide/silicon (SOS) capacitor. (c) Depletion [10–12, 62–64], which majority carriers are depleted by reverse biasing a p-doped/n-doped (PN) junction.

Early silicon modulators relied on carrier injection to electrically control carrier concentrations [6, 56, 65]. This type of modulator offers high modulation efficiency [6, 22, 56]. However, carrier injection-based modulation is constrained by the slower diffusion process and the recombination time of the injected electron-hole pairs, limiting its operational speed [5, 22, 57]. Figure 1.7 shows the schematic of a carrier injection device in a MZM [5] and RM [6], employing an embedded PIN junction for modulation. Compared to MZMs, RMs, with their reduced device dimensions, offer significant size advantages.

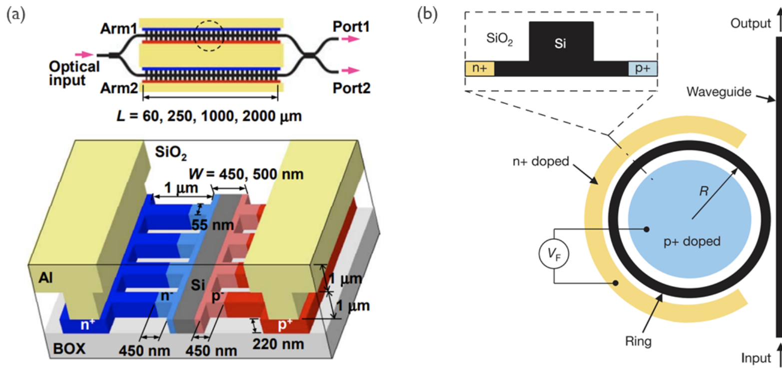

Figure 1.7: Schematic of Si carrier injection modulator integrated on a (a) MZI and (b) RR, taken from [5] and [6], respectively.

To enhance the speed of modulators, a novel approach known as the accumulation modulator, based on the SOS capacitor structure embedded in a silicon waveguide, has been introduced [59]. This modulator, which no longer relies on carrier diffusion, achieved data transmission rates of up to 1 Gbps with a bandwidth exceeding 1 GHz [59], quite remarkable at the time of its introduction. Since then, this type of modulator has garnered widespread attention and exploration [7–9, 60, 61].

The typical structure of an accumulation modulator involves a thin insulating gate oxide layer sandwiched between a poly-silicon (poly-Si) layer on top and crystalline silicon (c-Si) at the bottom, as depicted in Figure 1.8. This structure is relatively straightforward to construct, involving the deposition of poly-Si on SOI after the formation of the gate oxide. Consequently, the gate oxide plays a pivotal role in the performance of accumulation modulators, as it needs to balance the trade-off between modulation efficiency, speed, and signal loss [7].

State-of-the-art accumulation modulators have demonstrated impressive capabilities, achieving high-speed data transmission of 40 Gbps [60] and a remarkable modulation efficiency of 0.16 Vcm, with low optical loss of 3.5 dB/mm [61], typically at around a 1310 nm wavelength. Recent advancements have brought about the introduction of accumulation modulators employing a c-Si/oxide/c-Si configuration in both vertical [9] and horizontal [8] directions, aimed at enhancing design flexibility and integratability while minimizing optical loss.

Depletion modulators are the predominant approach for implementing plasma dispersion-based phase modulation, and a typical representation of this modulator is shown in Figure 1.9. They offer several advantages over other modulation types, including low loss and low capacitance. The low capacitance characteristic enables high-speed operation, often exceeding 40 Gbps [10, 12, 62, 63]. However, this

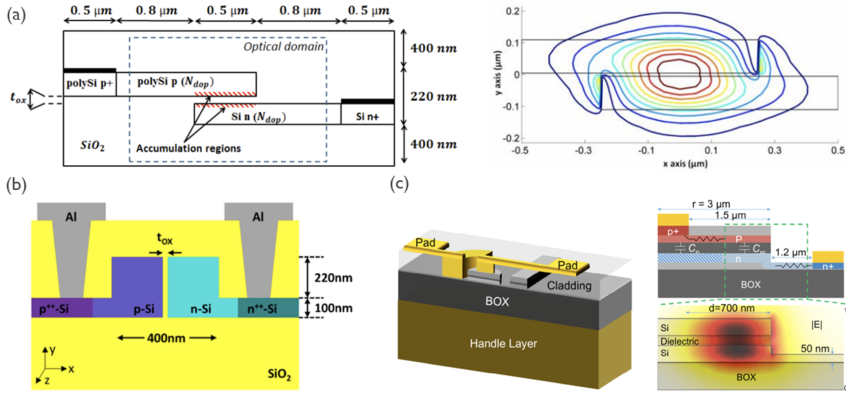

Figure 1.8: Schematic of Si carrier accumulation modulator integrated on (a) a MZI with vertical poly-Si/oxide/c-Si structure (left) and field distribution plot of the TE mode (right), (b) a MZI with horizontal c-Si/oxide/c-Si configuration, and (c) a RR with c-Si/oxide/c-Si configuration, taken from [7], [8], and [9], respectively.

relatively low capacitance limits the modulation efficiency, necessitating longer device lengths (typically >1 mm) to achieve a pi phase shift compared to other modulator types.

The drawback of this increased device length extends beyond a larger footprint; it also transforms the device from a lumped element into a distributed one. Consequently, a traveling wave electrode is indispensable to ensure rapid and precisely timed carrier depletion, enabling high-speed modulation of the optical signal [10, 11, 62] (see Figure 1.9). To strike the right balance between modulation efficiency, speed, and minimal optical loss, various research efforts have focused on enhancing the carrier profile [11, 64] and adopting different device structures [12, 62, 63].

One example of the former idea is constructing a vertical PN junction, as illustrated in Figure 1.9 (b). This approach increases the overlap between the depletion region and the optical field, resulting in improved modulation efficiency (ranging from 0.8 to 1.86 Vcm). The device in Figure 1.9 (c) combines both methods of improvement by using a vertical carrier profile and a RR structure. This configuration supports the highest modulation efficiency (0.52 Vcm) among depletion modulators and can reach speeds of up to 64 Gbps. However, this improvement comes at the cost of high optical loss (approximately 90 dB/cm). The trade-off between efficiency, speed, and loss is a recurring challenge in this field.

To overcome these limitations, the integration of non-silicon materials such as germanium [66–69], $LiNbO_3$ (LN) [70,71], $BaTiO_3$ (BTO) [72,73], polymer [74–

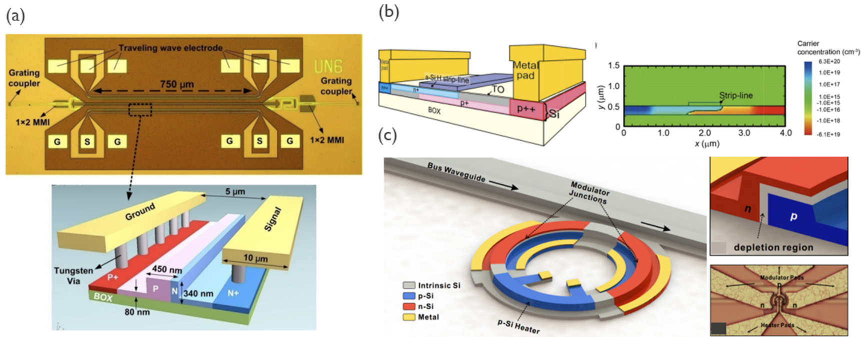

Figure 1.9: Schematic of Si carrier depletion modulator integrated on a MZI with (a) horizontal and (b) vertical carrier profile, taken from [10], and [11], respectively. (c) Schematic of Si carrier depletion modulator integrated on a RR, taken from [12]

76], and III-V semiconductors [77–80] with silicon platforms has been intensively studied in recent years. The main results for ERMs and EAMs with different materials are summarized in Table 1.1 and Table 1.2, respectively.

1.3 2D Materials: Graphene and Beyond

1.3.1 Introduction

2D materials, short for two-dimensional materials, refer to a class of substances consisting of extremely thin layers, typically just one or a few atoms in thickness. These materials are often composed of a single layer of atoms arranged in a two-dimensional lattice structure, as opposed to the three-dimensional (3D) arrangement seen in most bulk materials. This unique structural characteristic gives 2D materials remarkable properties and behaviors that set them apart from their 3D counterparts.

Graphene, a one-atom-thick sheet of carbon atoms arranged in a hexagonal lattice, was and still is the most famous member of the family of 2D materials. However, it was not always a widely accepted idea. In fact, for many years, it was believed to be a theoretical construct, too delicate and elusive to exist in the physical world. The scientific community was initially skeptical about the practical realization of this remarkable material. The turning point came in 2004 when two scientists, Andre Geim and Konstantin Novoselov, at the University of Manchester in the United Kingdom, succeeded in isolating and characterizing a monolayer of graphene [19]. Their groundbreaking achievement involved a simple yet ingenious method: they used ordinary adhesive tape to peel thin layers from a piece of graphite. This

Table 1.1: Summary of state-of-the-art electro-refraction modulators. FOM_{PM} stands for the Figure of merit for phase modulators.

ERMs	Effect	Wavelength	$V_\pi L$	$Loss$	FOM_{PM}	BW	Bit rate
[Unit]	-	$[nm]$	$[Vcm]$	$[dB/cm]$	$[dBV]$	[GHz]	[Gbps]
Si [5]	Injection	≈1550	0.274	53	14.5	12.5	25
Si [58]	Injection	≈1550	2	27.8	55.6	37	70
Si [7]	Accumulation	1550	0.28-0.69	49-60	15-33.8	5.6-22.4	-
Si [61]	Accumulation	1300	0.16	35	5.6	-	25
Si [12]	Depletion	≈1280	0.52	90	46.8	50	64
Si [81]	Depletion	1550	1.5	27	40.5	-	112
$LiNbO_3$ [70]	Pockels	1550	2.2	8.3	18.26	70	100
$BaTiO_3$ [72]	Pockels	1550	0.2	6.5	1.3	2	25
Polymer [76]	Pockels	1550	1.44	2.2	3.17	68	200
Polymer [75]	Pockels	1550	0.099	72	7.13	70	100
III-V [77]	Accumulation	≈1550	0.047	19.4	0.91	0.1	-
III-V [78]	Accumulation	≈1550	0.09	26	2.34	2	32
III-V [79]	Depletion + FK	1527	0.12	28	3.36	-	-

Table 1.2: Summary of state-of-the-art electro-absorption modulators. ER, IL, TP, and BW stand for extinction ratio, insertion loss, transmission penalty, and bandwidth respectively. Please note that the TP value is calculated based on the given V_{pp}. FK stands for Franz-Keldysh effect and QCSE represents Quantum-confined Stark effect.

EAMs	Effect	Wavelength	V_{pp}	ER	IL	TP	BW	Bit rate
[Unit]	-	$[nm]$	$[V]$	$[dB]$	$[dB]$	$[dB]$	[GHz]	[Gbps]
GeSi [67]	FK	1566	$\gtrsim$4	7.5	10.6	14.46	56	56
Ge [68]	FK	1615	2	4.6	4.9	9.76	>50	56
Ge [69]	FK	1605	3	14.2	5.7	8.88	>67	80
GeSi [66]	QCSE	$\approx$1300	2	5.2	7.6	12.17	50	60
III-V [80]	QCSE	1300	2.2	>10	4.8	<8.27	>67	50

discovery marked the birth of graphene and changed the course of material science.

Since Geim and Novoselov's pioneering work, graphene has become the focal point of extensive research worldwide. Scientists, engineers, and innovators have delved into its extraordinary properties and explored its potential applications in fields ranging from electronics and energy to materials science and beyond. In 2010, just six years after their groundbreaking work, Andre Geim and Konstantin Novoselov were awarded the Nobel Prize in Physics for their remarkable discovery of graphene. Their achievement marked a historic moment as they became the first Nobel laureates in the field of graphene research. The Nobel Committee's recognition highlighted the revolutionary impact of this single layer of carbon atoms.

Graphene's success opened the door to a fascinating family of two-dimensional materials. Beyond graphene, other 2D materials, such as transition metal dichalcogenides (TMDs) like molybdenum disulfide (MoS_2), have attracted significant attention. These materials offer a vast playground for researchers, promising innovative solutions in a wide range of applications, from electronics and photonics to quantum technologies and beyond [20].

1.3.2 Graphene properties

In graphene, the carbon atoms are sp^2 hybridized, forming strong σ bonds within the plane of the material as shown in Figure 1.10. Simultaneously, out-of-plane π bonds give rise to delocalized π electrons both above and below the atomic plane [82–84]. The robust σ bonds play a vital role in maintaining the structural integrity of graphene's hexagonal lattice, ensuring exceptional mechanical stability and resilience. Consequently, graphene exhibits remarkable physical properties, including extraordinary tensile strength (with an intrinsic tensile strength exceeding 130 GigaPascals), exceptional stiffness (Young's modulus of approximately 1 TeraPascal), and outstanding thermal and corrosion resistance [11, 85–89]. At the same time, its one-atom-thick structure contributes to its extraordinary lightness and remarkable flexibility.

Conversely, the π bonds within graphene are instrumental in shaping its electronic and optical characteristics. The unhybridized p-orbitals of each carbon atom, perpendicular to the σ bonds, overlap to create π bonds. These π bonds give rise to a delocalized π-electron cloud above and below the atomic plane, establishing a unique electronic band structure known as a Dirac cone (refer to Figure 1.10 (c)) [83]. At specific points in the two-dimensional hexagonal Brillouin zone, denoted as the K and K' points, the valence and conduction bands intersect. This intersection results in a linear energy dispersion, forming a conical structure within the band

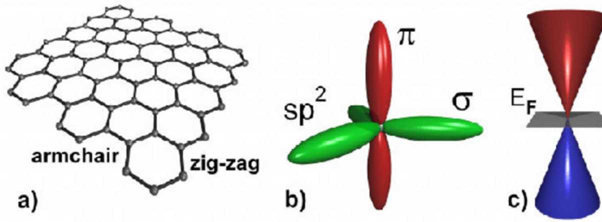

Figure 1.10: (a) 2D hexagonal lattice, (b) bonding and (c) band diagram of graphene, taken from [13].

diagram. The gapless band structure and the linear energy dispersion of electrons and holes near the Fermi level results in extraordinary electrical conductivity. Indeed, graphene is one of the most exceptional electrical conductors known, with reported mobility greater than 100,000 cm^2/Vs [90–93].

Furthermore, graphene demonstrates a notable ambipolar field effect, permitting the adjustment of its electrical characteristics [19]. Applying avoltage modifies the carrier concentration, shifting the Fermi level. Notably, a peak in resistivity corresponds to the Fermi level coinciding with the Dirac point, where the density of states significantly decreases [19]. Interestingly, this does not lead to zero conductivity but rather a minimum conductivity of approximately $\approx 4e^2/h$ was observed [94]. In practical situations, the observed phenomenon is commonly attributed to the inhomogeneous distribution of electron and hole puddles induced by substrate disorder, resulting in variations in the Fermi level across the material [95]. Even under ideal conditions such as a perfect vacuum where disorder is absent, the persistence of thermal fluctuations and quantum mechanical effects ensures that the conductivity of graphene near the Dirac point does not approach zero [94].

The unique electronic band structure of graphene also results in distinctive optical properties that are particularly appealing for photonic applications [96]. Despite its single-atom thickness, graphene exhibits an optical absorption of roughly 2.3$\%$ under perpendicular light incidence within visible spectrum as shown by Figure 1.11) [97, 98]. This absorption is approximately 50 times higher than that of GaAs with the same thickness. This strong absorption can be harnessed and enhanced when integrated with photonic waveguides as shown in Figure 1.11 (c). In such cases, the interaction of light with graphene is controlled by waveguide length and mode overlap with the material. Another remarkable optical property is graphene's broad optical bandwidth [94, 99, 100]. Due to its lack of a bandgap, graphene can absorb light across a wide range of wavelengths, spanning from the visible to the infrared, encompassing the typical optical fiber communication

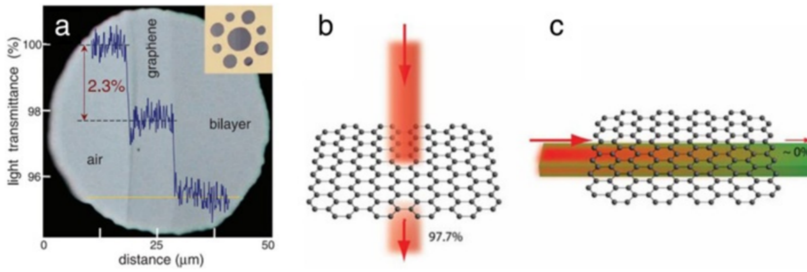

Figure 1.11: (a) Pristine graphene exhibits an optical absorption of approximately 2.3% within the visible wavelength range. (b) Single-layer graphene achieves an optical absorption of around 2.3% for vertically incident light. (c) Integration of graphene with a waveguide allows control over the interaction of light with graphene, determined by waveguide length and mode overlap with the material. Taken from [14].

bandwidth (1300-1600 nm). When coupled with its tunability and high mobility, graphene emerges as an excellent candidate for applications in high-speed optoelectronic devices.

1.3.3 TMDC properties

Transition metal dichalcogenides (TMDCs) are a family of 2D materials, characterized by a structure in the form of MX_2 compounds, where M represents a transition metal (e.g., Mo, W, Re) and X signifies a chalcogen (e.g., S, Se, Te). These compounds feature a hexagonal lattice structure, with a single layer of transition metal atoms sandwiched between two layers of chalcogen atoms (see Figure 1.12). This unique arrangement results in a stable and robust framework, providing exceptional properties and functionalities.

One notable distinction between TMDCs and graphene lies in their bandgap properties. TMDCs exhibit a bandgap, which makes them particularly promising for electronic applications [101–103]. A fascinating feature is that the bandgap of TMDCs is thickness-dependent (see Figure 1.12(b)) [104–106]. In bulk MoS_2, for instance, an indirect bandgap transition from the maximum of the valence band to the conduction band is observed, with a predicted bandgap of 1.2 eV. However, as the thickness of MoS_2 films decreases, the bandgap increases, reaching approximately 1.8 eV for monolayer structures. In monolayers, the transition from the valence band to the conduction band becomes direct, in contrast to the indirect transition observed in bulk semiconductors.

In electronic applications, TMDC films offer several advantages due to their atom-

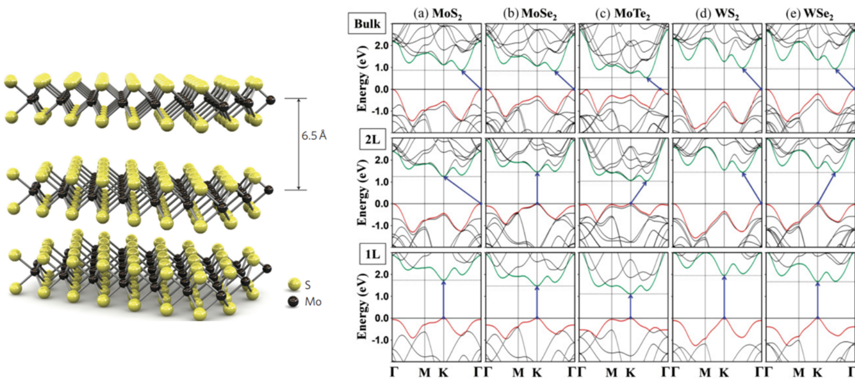

Figure 1.12: (Left) Schematic structure of MoS_2, taken from [15]. (Right) Band structures of TMDCs from the bulk to double-layer, and single-layer, taken from [16]

ically thin nature and semiconducting properties. They have the potential to outperform silicon (Si) as the channel material for ultra-scaled field-effect transistors (FETs) as shown in Figure 1.13 [107–110]. Theoretical studies have shown that the mobility of TMDC materials remains high, exceeding 200 cm^2/Vs even for single-layer films [15, 111]. This surpasses the mobility of thinned-down conventional bulk Si [112]. Moreover, TMDC-based FETs exhibit reduced short-channel effects, resulting in improved transistor performance [105, 113, 114]. These transistors typically offer a high on/off ratio with lower leakage current, contributing to enhanced energy efficiency [15, 108–110]. Lower power consumption is achieved when the transistor is in the off state, reducing wasted power.

In photonics applications, TMDCs' considerable bandgap in the visible and near-infrared (NIR) range (1–2 eV) positions them optimally for various optoelectronic applications [115–117]. The direct bandgap transition in TMDCs enables efficient absorption and emission of photons, making them attractive for light-emitting and photodetector devices. TMDCs are also recognized for their strong light-matter interaction [17, 29, 118, 119]. Combined with significant tunability through external parameters such as strain, electric fields, and chemical doping, they can be employed for highly efficient modulators operating in both visible and NIR wavelengths as shown in Figure 1.13 [17, 29, 120]. Furthermore, TMDCs can display nonlinear optical effects, including second-harmonic generation (SHG) and Kerr nonlinearities [121–124]. These effects are critical for various applications, including frequency doubling and all-optical signal processing. Overall, the optical properties of TMDCs make them highly attractive for applications in LEDs, photodetectors, sensors, light modulators, and other optoelectronic devices, offering versatility and adaptability across different spectral ranges and functionalities.

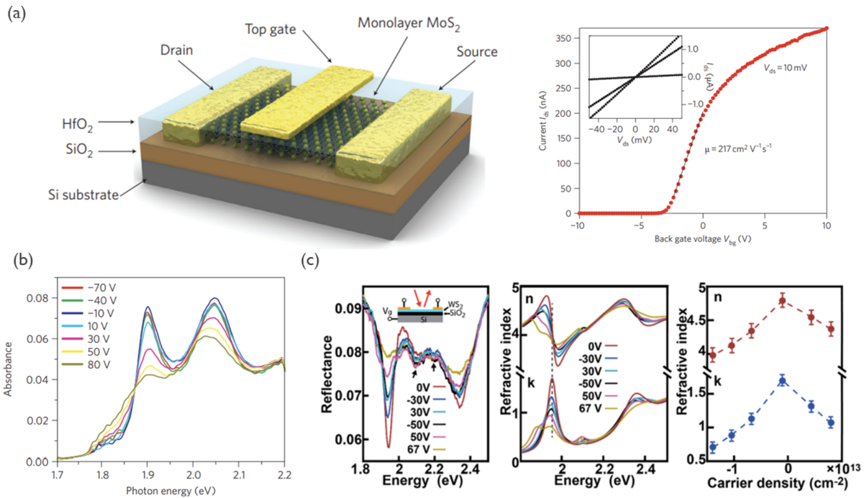

Figure 1.13: (a) Schematic structure of single layer MoS_2 transistor with over 200 cm^2/Vs mobility, taken from [15]. EO response of (b) MoS_2 and (c) WS_2 around their excitonic peaks, taken from [17], and [18], respectively.

1.3.4 Production techniques

In 2004, Geim and Novoselov pioneered the revolutionary technique of micromechanical exfoliation, leading to the successful isolation of the first monolayer of graphene as shown in Figure 1.14 [19, 94]. This innovative method relies on the simple use of adhesive scotch tape to overcome the relatively weak interlayer Van der Waals bonds present in graphite. Because this process lacks chemical interactions, the monolayer graphene obtained through micromechanical exfoliation boasts remarkable crystallinity and maintains its structural integrity. In fact, it has been reported to achieve the highest quality crystalline graphene, characterized by impressive room temperature mobility of approximately 180,000 cm^2/Vs [91]. However, it's essential to note that the size of graphene produced using this approach is inherently limited, typically reaching only a few micrometers in diameter. Consequently, this size limitation makes it less suitable for large-scale industrial applications.

Beyond graphene, micromechanical exfoliation has also successfully produced monolayers of other 2D materials [125–130], significantly expanding the method's utility. One remarkable advantage of micromechanical exfoliation, particularly in the realm of research, is the ability to stack distinct exfoliated flakes to construct heterostructures (see Figure 1.14) [20, 131–134]. These heterostructures serve a dual purpose as both encapsulation layers and platforms for designing novel

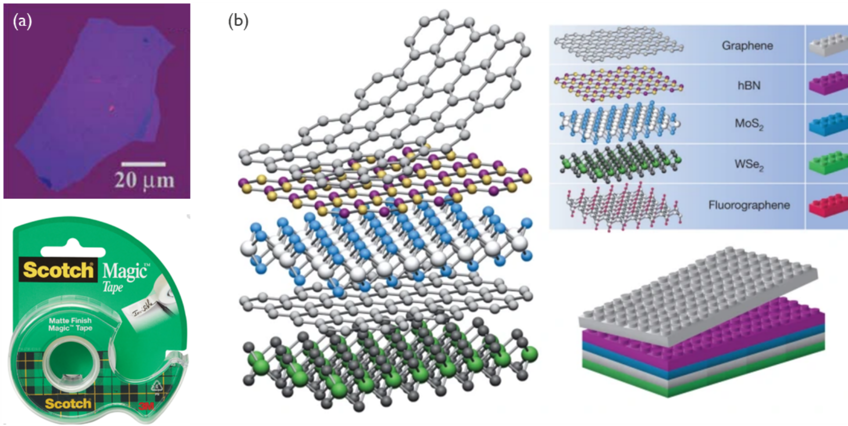

Figure 1.14: (a) Monolayer graphene produced through micromechanical exfoliation, taken from [19]. (b) Schematic representation of 2D material-based heterostructures constructed with building blocks of 2D materials, taken from [20].

materials with unique functionalities. The high quality and intrinsic properties of materials obtained through micromechanical exfoliation establish an exceptional foundation for the in-depth exploration of fundamental 2D material properties.

In order to utilize 2D materials in industrial applications, it is imperative to demonstrate their viability for large-scale manufacturing and integration. Chemical Vapor Deposition (CVD) emerges as a pivotal solution to bridge this gap. In contrast to top-down techniques like mechanical exfoliation, which are confined by material dimensions, CVD provides a cost-effective bottom-up approach, enabling the large-scale synthesis of 2D materials with a high degree of uniformity and quality (see Figure 1.15). In this thesis, all the 2D materials used for device fabrication, including graphene and MoS_2, are obtained through CVD growth.

The growth of CVD graphene involves the utilization of hydrocarbon precursors, such as methane (CH_4), as the carbon source, and catalysts like Cu, Pt, and Ni as the growing substrates [135, 136]. When the precursor is introduced into the chamber, the carbon source undergoes dissociation into carbon atoms at elevated temperatures (over 900 Celsius degree). These carbon atoms then dissolve into the catalyst and precipitate at the metal-substrate interface, arranging themselves into a hexagonal lattice structure. As more carbon atoms precipitate, the nucleation sites of graphene grow into larger domains that eventually connect to form polycrystalline films. It has been observed that a rapid cooling rate is crucial for suppressing the formation of multiple layers, thereby achieving single-layer graphene on Ni. In the case of catalysts like Cu and Pt, the growth process is similar, but the mechanism differs. Due to their significantly lower carbon solubility, the growth process resembles a

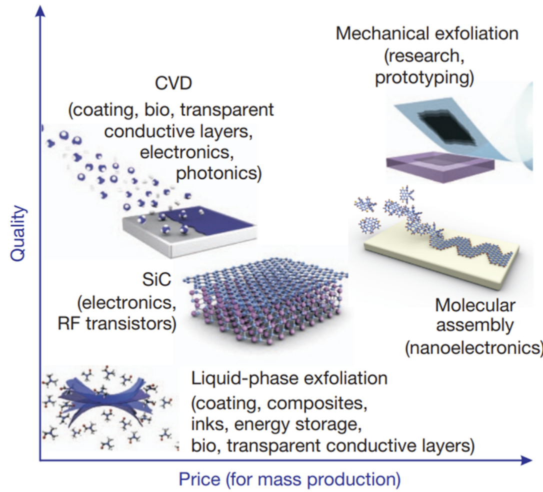

Figure 1.15: Various graphene production techniques, with considerations for the quality of the resulting graphene and the associated production costs. Taken from [21]

self-limiting mechanism that automatically results in single-layer graphene on Cu or Pt catalysts.

Precise control over parameters such as precursor concentration, growth temperature, chamber pressure, and growth time is necessary to optimize the quality of the grown graphene. Typically, the mobility of CVD graphene is predominantly limited by defects and boundaries within the polycrystalline films. Consequently, optimizing the substrate to yield single-crystal graphene has become a popular approach for obtaining high-quality graphene. Today, single-crystal graphene with millimeter-scale dimensions has been successfully achieved, boasting a demonstrated mobility exceeding 7000 cm^2/Vs [93, 137, 138].

The CVD method is a versatile technique that can also be employed for the growth of TMDCs. The process commences with the careful selection of precursor gases tailored to the specific TMDC of interest. For instance, in the case of MoS_2, commonly utilized precursors encompass molybdenum hexacarbonyl ($Mo(CO)_6$) and sulfur (S) sources like hydrogen sulfide (H_2S) or sulfur hexafluoride (SF_6). These precursor gases are instrumental in providing the molybdenum (Mo) and sulfur (S) atoms required for the growth of MoS_2 on various substrates, including silicon dioxide (SiO_2), sapphire, or other insulating materials.

The growth process initiates with the elevated temperature causing the release of Mo and S atoms from the precursor gases. Subsequently, these liberated Mo and S atoms diffuse on the substrate surface, forming nucleation sites. These nucleation

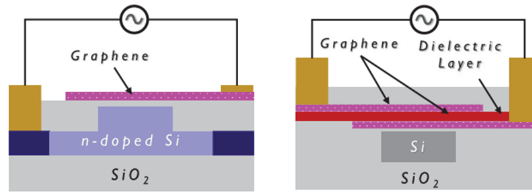

Figure 1.16: Two predominant structures of graphene (2D materials) based photonic devices, taken from [22].

sites serve as the foundational units for the growth of MoS_2. As additional Mo and S atoms adhere to these nucleation sites, MoS_2 layers progressively develop. The growth happens both horizontally and vertically. It's imperative to maintain precise control over growth conditions, encompassing factors like temperature, pressure, and precursor flow rates, to attain the desired MoS_2 layer quality.

Remarkably, recent advancements in the field have seen the successful demonstration of single-crystal monolayer MoS_2 with sizes exceeding 300 micrometers and decent mobilities >50 cm^2/Vs [139]. Furthermore, the CVD method is not confined to MoS_2 alone; it can be effectively employed to grow other members within the TMDC family, including $MoTe_2$ [140], WS_2 [141], WSe_2 [142], and $MoSe_2$ [143]. This versatility in TMDC growth using the CVD technique underscores its significance in the development of 2D materials for various applications.

1.4 2D-Materials Based Modulators

To create a 2D materials-based optical modulator, the integration of 2D materials on waveguides is a common approach. This method leverages the evanescent tail of the optical wave to facilitate the interaction between 2D materials and light. By employing a capacitor structure to control the gating of the 2D material sheets, it becomes possible to modulate the absorption and phase of the 2D materials, effectively converting electrical signals into optical signals. Two predominant structural designs have been widely adopted, as illustrated in Figure 1.16 [22].

The first design is the single-layer 2D-oxide-silicon structure, where a gate oxide is sandwiched between a doped silicon waveguide and a single 2D layer. The second design, known as the 2D-oxide-2D structure, involves two individual layers of 2D material separated by a gate oxide layer, forming a capacitor integrated on top of an undoped waveguide. This two-layer configuration can be implemented on any type of waveguide, such as for example silicon nitride waveguides, therefore greatly

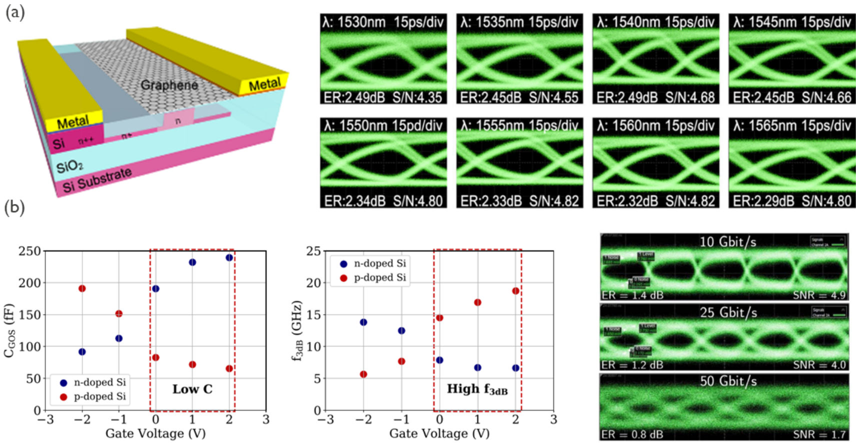

Figure 1.17: (a) A 3D schematic and eye properties at 10 Gbps of the single-layer graphene EAM, utilizing a planarized SOI substrate. Taken from [23]. (b) Investigating the impact of capacitance on 3dB bandwidth and demonstrating a 50 Gbps performance for a single-layer EAM, adopt from [24].

enhancing its flexibility and eliminating the need for Si ion implantation.

1.4.1 Electro-absorption modulators

The one-layer structure was employed first in 2011. These early devices achieved a modulation depth of 0.1 $dB/\mu\, m$ and an EO bandwidth exceeding 1 GHz [144]. Notably, they exhibited broad operation capabilities, spanning from 1.35 to 1.6 $\mu\, m$ wavelength. Subsequent research by Hu et al. and Alessandri et al. focused on optimizing this device type [23, 24]. Compared to the initial demonstration, they both adopted a silicon-on-insulator (SOI) substrate as the platform for silicon photonics fabrication, as visually detailed in Figure 1.17. In addition, they implemented chemical mechanical polishing (CMP) to enhance the surface flatness and uniformity, enabling the transfer of the graphene layer with improved quality.

Hu et al. achieved remarkable results, demonstrating a 10 Gb/s operational speed across all measured wavelengths and excellent temperature tolerance, with performance maintained up to 50°C, and predicting functionality at even higher temperatures (175°C) [23]. Furthermore, Alessandri et al. identified device capacitance and resistance as key limiting factors in achieving higher speeds. By using p-doped silicon instead of n-doped silicon, they showcased a state-of-the-art single-layer graphene (SLG) EAM with a remarkable 20 GHz EO bandwidth and an impressive 50 Gbps operational speed (see Figure 1.17) [24].

While SLG EAMs offer admirable performance, they are constrained by intrinsic losses and limited absorption modulation caused by the doped silicon layer. Consequently, the dual single-layer graphene (DLG) structure has gained substantial popularity due to its potential for improved modulation performance and expanded electro-optical (EO) bandwidth. This is especially pronounced when the mobility of 2D materials exceeds that of silicon. The presentation of the first DLG EAM occurred in 2012 when Liu et al. successfully demonstrated a modulation depth of 0.16 dB/µm with a 1 GHz EO bandwidth [145]. They also identify avenues for further enhancement.

In 2016, Dalir et al. achieved a significant milestone by experimentally demonstrating DLG EAMs with an astonishing 35 GHz EO bandwidth [25]. They accomplished this by relocating the DLG beneath an amorphous waveguide, resulting in a planar surface, as depicted in Figure 1.18, which significantly improved material conductivity and contacts. However, it's worth noting that due to the requirement of large peak-to-peak driving voltage, they were unable to display an open eye diagram. In 2019, Giambra et al. achieved a remarkable breakthrough by showcasing the first high-speed DLG EAM with a 50 Gbps open eye diagram and an EO bandwidth of 29 GHz [26], as illustrated in Figure 1.18. This extraordinary modulation speed was made possible by utilizing high-quality single-crystal CVD-grown graphene. Their prediction suggested that the modulation depth could be also improved to 0.137 dB/µm for such high-mobility graphene. However, the demonstration was limited by the breakdown voltage of the dielectric layer.

Finally, in 2021, Agarwal et al. overcame this challenge by adopting a 2D-3D combined dielectric layer for the gate oxide [146]. This innovative structure harnessed the superior properties of two-dimensional hexagonal boron nitride (hBN) to preserve the ultra-high quality of the exfoliated graphene layer, while employing high dielectric constant hafnium oxide (HfO_2) in between hBNs to facilitate the application of higher voltages. The result was a state-of-the-art DLG EAM with a modulation depth of 0.177 dB/µm, a 39 GHz EO bandwidth, and an impressive 40 Gbps operational speed.

1.4.2 Electro-refraction modulators

Although graphene-based EAMs have achieved a superior performance, the limited capability for phase modulation has hindered their use for generating complex modulation formats, such as quadrature amplitude modulation (QAM). Consequently, there has been a concerted effort in studying graphene-based phase modulators. A significant milestone in this domain was achieved by Sorianello et al. in 2018, as illustrated in Figure 1.19 [27], with the demonstration of the first graphene-based

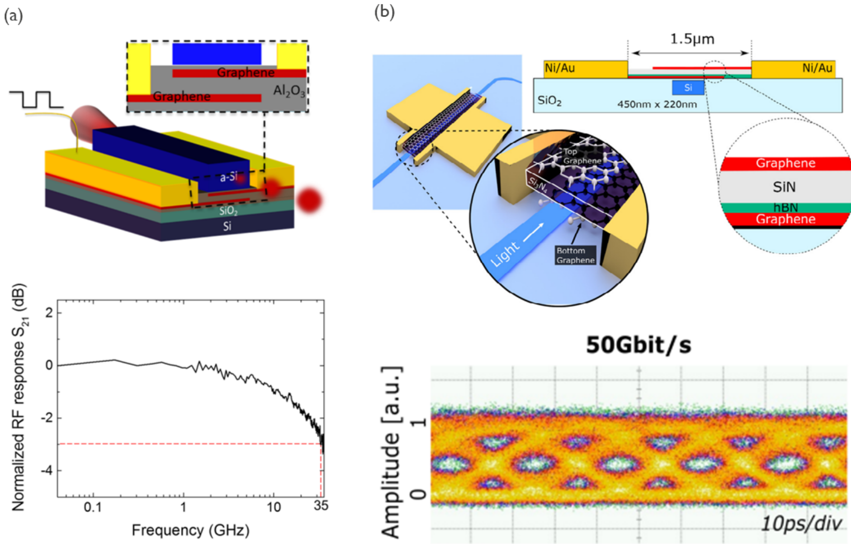

Figure 1.18: The high speed performance demonstrated by double-layer EAMs, adopt from [25, 26].

MZM boasting gigahertz bandwidth. This device, employing a SLG structure, achieved an impressive modulation efficiency of 0.28 V·cm. Notably, it exhibited a 5 GHz EO bandwidth and an open-eye diagram at 10 Gbps, demonstrating error-free transmission over a 50 km single-mode fiber (SMF).

A noteworthy demonstration of a graphene-based RM was reported by Phare et al. in 2015, as depicted in Figure 1.19 [28]. They constructed a dual-layer graphene (DLG) capacitor on Si_3N_4 waveguides, revealing a remarkable 22 Gbps open-eye diagram and a 30 GHz EO bandwidth. The utilization of Si_3N_4 waveguides, characterized by a low thermo-optic coefficient, in combination with the relatively low quality factor of the ring resonator, rendered the modulator robust to thermal effects. In a quest for increased energy efficiency, Heidari et al. introduced an ultra-low-power graphene-based optical modulator in 2022 [147]. By incorporating a Bragg reflector waveguide, they harnessed enhanced light-matter interaction, resulting in reduced capacitance and an impressive EO bandwidth of 60 GHz. Remarkably, this modulator demonstrated a minimal power consumption of only 2.25 $fJbit^{-1}$.

Apart from graphene, the integration of other two-dimensional materials, such as TMDCs, has proven to be valuable when incorporated into silicon-based waveguides, resulting in remarkable phase modulators operating at telecommunication wavelengths. In 2020, Datta et al. conducted pioneering research by employing a

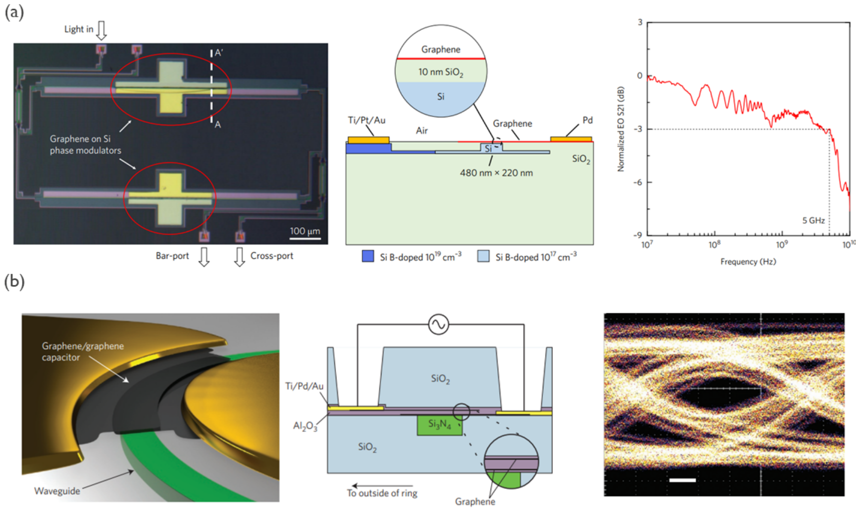

Figure 1.19: The schematic and speed performance of graphene-based electro-refraction modulator, integrated on a (a) MZI and (b) RR, respectively, adoped from [27] and [28].

RM and ionic liquid to precisely measure the real and imaginary components of the refractive index change in WS_2 [29]. Their findings indicated that the doping-induced phase change relative to the change in absorption ($|\Delta\ n/\Delta\ k|$) for WS_2 was approximately 125, a significantly higher value compared to other materials commonly used in silicon photonic modulators.

Leveraging this insight, they proceeded to construct a low-loss Mach-Zehnder modulator based on a WS_2-oxide-ITO capacitor integrated on Si_3N_4 waveguides [29]. This innovative device stands out for its minimal insertion loss and modulation efficiency (approximately 0.8 Vcm). These characteristics make it a compelling platform for a wide range of applications, including but not limited to LIDAR, phased arrays, optical switching, and quantum and optical neural networks, where low-loss, high-performance optical modulation is imperative.

1.5 Research Objectives

Electro-optical modulators are foundational components within high-capacity optical communication and high-performance computing systems. An ideal electro-optical modulator must exhibit a set of critical characteristics, including a substantial extinction ratio, minimal insertion loss, high operational speed, and low power consumption. Furthermore, it is desirable for the device to maintain a compact footprint

Table 1.3: Summary of state-of-the-art 2D material-based modulators. ER, IL, TP, and BW stand for extinction ratio, insertion loss, transmission penalty, and bandwidth respectively. Please note that the TP value is calculated based on the given V_{pp}. FOM_{PM} stands for the Figure of merit for phase modulators.

Structure	Polarization	V_{pp}	ER	IL	TP	BW	Bit rate
[Unit]	[-]	$[V]$	$[dB]$	$[dB]$	$[dB]$	[GHz]	[Gbps]
SLG EAM [144]	TM	4	4	-	-	1.2	-
SLG EAM [23]	TM	8	5.2	3.8	8.37	5.9	10
SLG EAM [24]	TM	6	6.5	4.2	8.3	14.2	50
DLG EAM [145]	TM	6	6.5	4	8.11	1	-
DLG EAM [25]	TM	25	2	0.9	8.23	35	-
DLG EAM [26]	TE	9	3	20	26	29	50
DLG EAM [146]	TM	7	4.4	7.8	12.7	39	40
DLG RING [28]	TE	10	15	12.5	15.6	30	22
Structure	Polarization	Wavelength	$V_{\pi}L$	$Loss$	FOM_{PM}	BW	Data rate
[Unit]	[-]	$[nm]$	$[Vcm]$	$[dB/cm]$	$[dBV]$	[GHz]	[Gbps]
SLG MZM [27]	TE	1550	0.28	236	66	5	10
WS_2-ITO MZM [29]	TE	1550	0.8	135	108	0.33	-

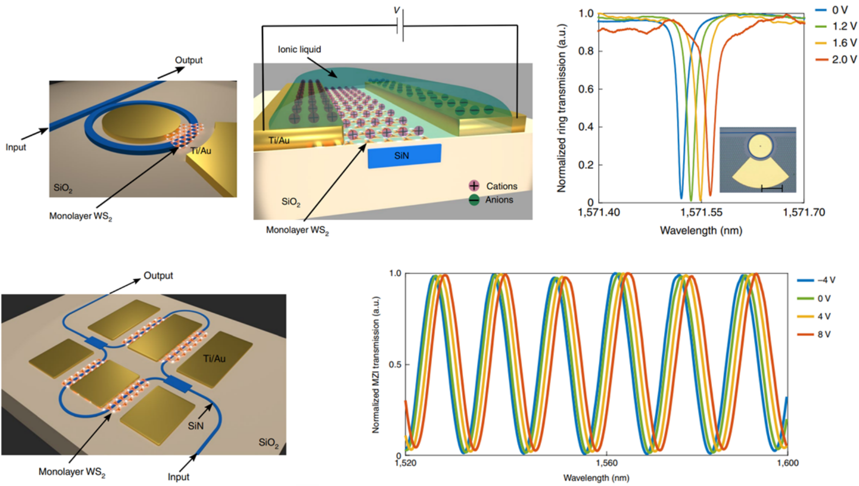

Figure 1.20: The schematic of a high-performance phase shifter at C-band wavelength based on WS_2 integrated on (top) ring resonator and (bottom) Mach-Zehnder interferometer, providing a low-loss platform for telecommunication application. Taken from [29].

and demand a low driving voltage, aligning seamlessly with CMOS circuitry. In addition, modulators used in high-integration density systems need to demonstrate reliability, reproducibility, and compatibility with existing CMOS manufacturing techniques.

It is challenging to meet all these criteria simultaneously using pure silicon-based modulators. Silicon's relatively weak plasma dispersion effect makes it less efficient for straight-waveguide coupled electro-absorption modulators, necessitating the use of MZI and RR. Nonetheless, MZI-based modulators exhibit large footprints, while ring modulators suffer from the limited optical bandwidth and high sensitivity to temperature. To overcome these limitations, researchers have turned their attention to alternative non-silicon materials, with 2D materials emerging as a particularly promising avenue.

Given their exceptional electrical and optical properties, graphene and other 2D materials are well-suited for high-performance, high-speed EO modulators, a fact substantiated by a decade's worth of empirical evidence within the literature. The central question driving this thesis is as follows:

"Can 2D material-based photonic devices be adopted in industry for the next generation of data communication and telecommunications applications?"

Answering this question necessitates a deep understanding of the current challenges faced by graphene and 2D material-based photonic devices. Most of these de-

vices found in the literature are typically fabricated in laboratory environments, utilizing processes like e-beam lithography, metal lift-off, and contact metals that are not inherently compatible with CMOS technology. To integrate graphene and 2D materials effectively into real-world systems, it is imperative to demonstrate competitive device performance, achieve consistent results, ensure reliability, and establish a clear path for large-scale manufacturing with high yield at minimal cost. Consequently, establishing a robust integration process within a complete CMOS fabrication environment becomes paramount in the initial stages of industry adoption.

The second aspect of addressing the core question revolves around the performance of graphene and 2D material-based devices. Can they outperform devices based on other materials? How can we leverage the inherent advantages of graphene and 2D materials to further enhance device performance? To enhance device performance, we have chosen to focus on optimizing graphene and 2D material-based modulators, involving parameters design, waveguide design, and material selection. Ultimately, our objective is to experimentally and theoretically demonstrate the potential of graphene and 2D material-based modulators, thereby providing a compelling response to the central question outlined above.

It is essential to note that the entirety of the work was conducted at imec in Leuven. The wafer-scale graphene utilized in fab-based devices was generously provided by Graphenea, while the graphene and MoS_2 used in lab-based devices were grown in-house at imec.

1.6 Thesis overview

Chapter 1 serves as a foundational introduction, delving into the realm of optical interconnects and the ever-evolving field of silicon photonics. The chapter explicates the underlying principles of modulators and introduces the exciting domain of two-dimensional (2D) materials. Additionally, it highlights the latest developments in electro-absorption and electro-refraction modulators, setting the stage for the research objectives outlined in this thesis.

Chapter 2 undertakes an extensive simulation-based exploration to unravel the performance characteristics of diverse graphene-based modulators. The investigation encompasses a thorough examination of how design parameters influence device performance, offering valuable insights for the chapters to come. This chapter also elucidates the characterization methods that will be employed in subsequent chapters.

Chapter 3 embarks on a practical journey, initially selecting single-layer graphene electro-absorption modulators as test vehicle and establish their wafer-scale integration in a 300mm pilot CMOS foundry environment. Following this successful integration, the chapter explores three distinct paths to enhance device performance, building upon the established integration process.

Chapter 4 takes a deeper dive into laboratory-based experimentation, concentrating on the comparative analysis of strip and slot waveguide-based double-layer graphene modulators. Within this chapter, we delve into the performance evaluation of three major modulator types, namely EAM, MZM, and RM. Furthermore, we explain the impact of design parameters on slot waveguide-based graphene modulators and highlight the pathway to surpass the performance of strip waveguide-based devices.

Chapter 5 introduces the realm of MoS_2-based phase modulators. The chapter explores three distinct structures of MoS_2-based MZMs, unlocking the potential of this material in facilitating low-loss, high-efficiency phase shifting capabilities.

2

MODELLING AND CHARACTERIZATION

In this chapter, we explore the theoretical potential of graphene-based modulators and explain the experimental methods used to characterize devices in this dissertation. In the first half of this chapter, the commercial software $Lumerical^{TM}$ is used to model two main architectures for realizing integrated graphene modulators. Changes in the refractive index are discussed. Afterwards, we consider the frequency response and explore the trade-off throughout the device's design, in which a number of crucial parameters are investigated. Finally, the effect of background doping on the graphene layer are studied. These findings may help on paving the way toward realizing high-performance and high-speed modulators based on graphene. In this chapter's second section, electro-optical and electrical characterization techniques are described. They are used to evaluate the electro-optical performance of modulators and assess the quality of 2D materials.

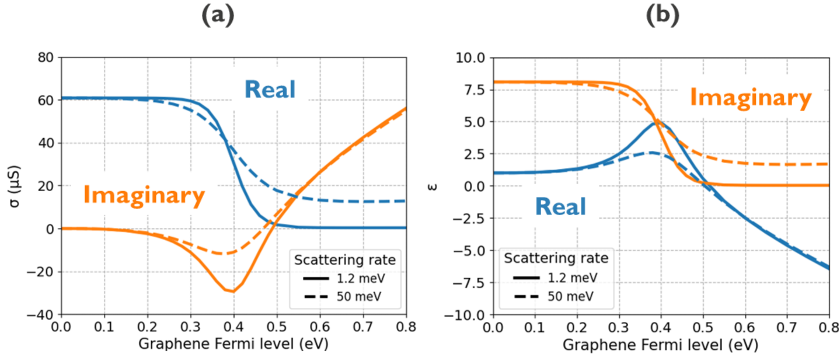

Figure 2.1: Simulated real and imaginary part of (a) graphene surface conductivity σ and (b) dielectric constant ϵ as a function of E_F at 1550 nm wavelength for graphene with Γ = 1.2 and 50 meV. The oxide thickness (d_{ox}) and background relative permittivity (ϵ_r) are 0.7 nm and 1, respectively.

2.1 Optical and electrical modelling of graphene modulators

In this section, we simulate graphene-based devices using the surface conductivity model in Lumerical MODE solutions. Based on the equations described in this section, the theoretical frequency response is computed. The trade-offs that occur during the design of a device are studied so that devices with a desired performance can be developed.

2.1.1 Modelling of graphene

Due to graphene's atomic thickness, it is usually described using the surface conductivity model rather than the volumetric permittivity model. The model is developed from Kubo's formula [148], taking both interband and intraband transitions into account. The following equations are dependent on the light's angular frequency (ω), graphene's intraband scattering rate (Γ), temperature (T), and Fermi-level (E_F) [149]:

$$\sigma(\omega, \Gamma, T, E_F) = \sigma_{inter}(\omega, \Gamma, T, E_F) + \sigma_{intra}(\omega, \Gamma, T, E_F) \tag{2.1}$$

$$\sigma_{intra}(\omega, \Gamma, T, E_F) = \frac{-iq^2}{\hbar^2 \pi(\omega + i2\Gamma)} \int_0^\infty \xi(\frac{\partial f_d(\xi)}{\partial \xi} - \frac{\partial f_d(-\xi)}{\partial \xi})\, d\xi \tag{2.2}$$

$$\sigma_{inter}(\omega,\Gamma,T,E_F) = \frac{iq^2(\omega+i2\Gamma)}{\hbar^2\pi}\int_0^\infty (\frac{f_d(-\xi)-f_d(\xi)}{(\omega+i2\Gamma)^2-4(\xi/\ \hbar)^2})\,d\xi \quad (2.3)$$

$$f_d(\xi) = \frac{1}{exp((\xi-E_F)/(k_BT))+1} \quad (2.4)$$

where q is the elementary charge, $\hbar$ is the reduced Planck constant and k_B is Boltzmann constant. ξ is the energy distribution and f_d is the Fermi-Dirac distribution.
Interband transitions relate to the movement of carriers from the valence band to the conduction band or vice versa, which is strongly dependent on the incident light's energy (E_{wl}) and the graphene E_F. Inter-band transitions are being suppressed when $E_F > E_{wl}/2$ and forbidden due to Pauli blocking. For instance, a wavelength of 1550 nm corresponds to a photon energy of roughly 0.8 eV, hence Pauli blocking occurs when $E_F >$0.4 eV. Intraband transitions, on the other hand, relate to movement within the same band and depend on graphene's scattering rate due to the conservation of momentum [150]. Γ can be translated to the scattering time (τ) by the following formula:

$$\tau = \frac{\hbar}{\Gamma} \quad (2.5)$$

Figure 2.1(a) shows the real and imaginary components of graphene's surface conductivity at 1550 nm wavelength for Γ = 1.2 and 50 meV, corresponding to 0.54 ps and 0.013 ps, respectively, according to the Equation 2.5. These outcomes were derived from a surface conductivity model in Lumerical MODE. From the surface conductivity, we can calculate a more traditional dielectric constant for graphene by introducing two additional parameters: the thickness (d_{ox}) and the background relative permittivity (ϵ_r). For graphene, only the in-plane components of the electromagnetic field are significant, and the equation can be rewritten as follows:

$$\epsilon_{||}(\omega,\Gamma,T,E_F) = \epsilon_r + i\frac{\sigma(\omega,\Gamma,T,E_F)}{\epsilon_0\,\omega\,d_{ox}}\ and\ \epsilon_\perp = \epsilon_r \quad (2.6)$$

Figure 2.1(b) depicts the real and imaginary components of graphene's dielectric constant, which were obtained from Figure 2.1 (a) assuming a thickness of 0.7 nm and a value of ϵ_r=1. When E_F is more than 0.2 eV, varying scattering rate values result in dramatically different dielectric constants.

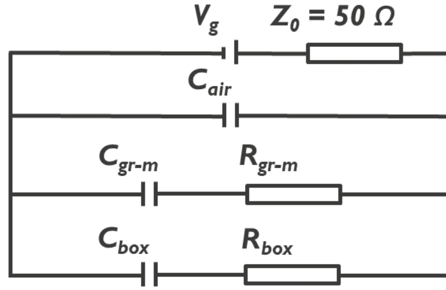

Figure 2.2: Equivalent electrical circuit model of graphene (2D)-based modulator. In the model, C_{gr-m} represents the capacitance of the graphene-based device, while R_{gr-m} represents the total resistance of the graphene-based device, combining the contact and sheet resistance of the structure. C_{air}, C_{box}, and R_{box} denote the capacitance between the metal pads, the capacitance of the silicon substrate, and the resistance of the silicon substrate, respectively. V_g and Z_0 represent the driving voltage and impedance.

2.1.2 Devices Performance Metrics

We may now modulate the surface conductivity and, subsequently, the complex refractive index [149, 151] by sweeping the graphene Fermi-level, resulting in both amplitude and phase modulation. Typically, the Fermi-level of graphene is modulated and controlled by applying a gate voltage across the capacitor. The relationship between E_F and the applied voltage is not linear, and can be found from [152]:

$$|V - V_{Dirac}| = \frac{e}{C_{eq}} \frac{1}{\pi} (\frac{E_F}{\hbar v_F})^2 + n_{layer} \frac{|E_F|}{e} \tag{2.7}$$

where V_{Dirac} is the voltage of graphene's Dirac point, v_F is the Fermi velocity of carriers in graphene, n_{layer} is the number of graphene layers present in the device (normally 1 or 2) and C_{eq} is the equivalent capacitance of the device, including the quantum capacitance of graphene [153, 154]. In such a scenario, the performance of an amplitude and phase modulator can be simulated and assessed with the gate voltage applied. For phase modulators, the change in phase ($\Delta\,\phi$) can be computed in terms of the change in effective index ($\Delta\,n_{eff}$) as indicated by the following equation. The crucial metric for assessing the effectiveness of phase modulation is $V_\pi\,L$, as defined in the subsequent equation:

$$\Delta\,n_{eff} = \frac{\lambda}{2\pi\,L}\,\Delta\,\phi \tag{2.8}$$

$$V_\pi L = \frac{\Delta V}{\Delta \phi} \pi L \ ; \ \Delta V = V_{pp} \tag{2.9}$$

where λ is the wavelength. The figure of merit of phase modulators (FOM_{pm} in a unit of dBV) includes the loss of device and is defined as:

$$FOM_{pm} = V_\pi IL \ = \ V_\pi L \alpha_{loss} \tag{2.10}$$

where α_{loss} is propagation loss of the device. The smaller the FOM_{PM}, the more efficient the phase modulator. For amplitude modulators, optical insertion loss (IL) and extinction ratio (ER) per unit length at a certain voltage range (V_{pp}) are determined based on the following equations:

$$IL = \frac{P_{in}}{P_1} \ ; \ ER = \frac{P_1}{P_0} \tag{2.11}$$

Where P_{in} (in a unit of W) represents the input optical power, P_1 (in a unit of W) represents the high output power and P_0 (in a unit of W) represents the low output power. Utilizing the figure of merit (FOM_{EAM}), transmission penalty (TP) at specific V_{pp}, all these details can be taken into account and fairly compared between modulators. The TP is defined as :

$$FOM_{EAM} = TP\,[dB] = -10\, log_{10} \frac{P_1 - P_0}{2P_{in}} \tag{2.12}$$

The lower the TP, the better the performance, allowing for reduced overall optical loss in optical networks.

In addition to optical performance metrics, the frequency response is also a critical parameter to evaluate the performance of the devices. The -3dB bandwidth of a device is rigorously defined as the frequency range over which the magnitude of the device's transfer function decreases to 70.7% (1/$\sqrt{2}$) of its maximum value, reflecting the point at which the power transfer is reduced by half or -3dB relative to the peak value. This measure is crucial in characterizing the frequency response and speed capabilities of electronic systems. [155]. The dominant parameter that restricts the 3-dB frequency response for graphene-based devices is the RC delay in the corresponding circuit depicted in Figure 2.2. C_{dv} is the capacitance of the graphene modulator, whereas R_{dv} is its overall resistance. C_{air}, C_s, and R_s are all parasitic components, standing for the capacitance between metal pads, the parasitic capacitance of the SOI substrate, and the parasitic resistance of the SOI substrate, respectively. The intrinsic electrical bandwidth of the device can be calculated by:

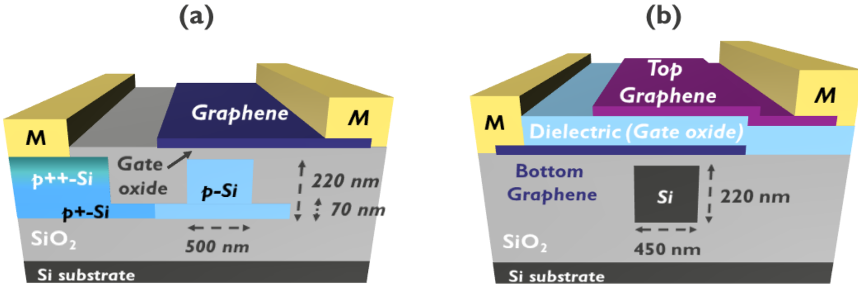

Figure 2.3: Schematic cross-section of (a) single-layer (SLG) and (b) dual-single-layer (DLG) graphene modulator on SOI substrate. A thickness of 5 nm SiO_2 and 10 nm Al_2O_3 are considered respectively for the gate oxide in the SLG and the DLG architecture.

$$3 - dB\ bandwidth = \frac{1}{2\pi R_{dv} C_{dv}} \tag{2.13}$$

In this thesis, we found out that the driver impedance has a great impact on the 3-dB bandwidth when analyzing experimental data. The impedance (50 Ω) needs to be taken into account. Therefore, the equation can be further expressed as:

$$3 - dB\ bandwidth = \frac{1}{2\pi (R_{dv} + 50) C_{dv}} \tag{2.14}$$

2.1.3 Modelling of single layer graphene and dual single layer graphene

There are two prominent architectures of graphene modulators as shown in Figure 2.3. The first one is the single layer graphene-oxide-silicon (GOS) structure. The doped silicon waveguide (p-Si) and graphene sandwich the gate oxide to form a capacitor structure. One side of the waveguide is partially patterned to create a rib structure, allowing for electrical contacting through a 70 nm silicon slab layer. Three doping steps are carried out, to minimize the contact and sheet resistance of the Si layers, without considerably increasing the optical loss in the waveguides. In later simulations, carrier concentrations of 1.5×10^{18}, 3×10^{19} and 1×10^{20} cm^{-2} are taken into account for $p - Si$, $p^{+} - Si$ and $p^{++} - Si$, respectively. To enable high-speed performance, we follow the finding in our previous publication [24] and select p-type doping for our silicon layers. Another architecture is the graphene-oxide-graphene (GOG) device, in which two individual graphene layers are separated by a dielectric layer and form the capacitor on top of a passive

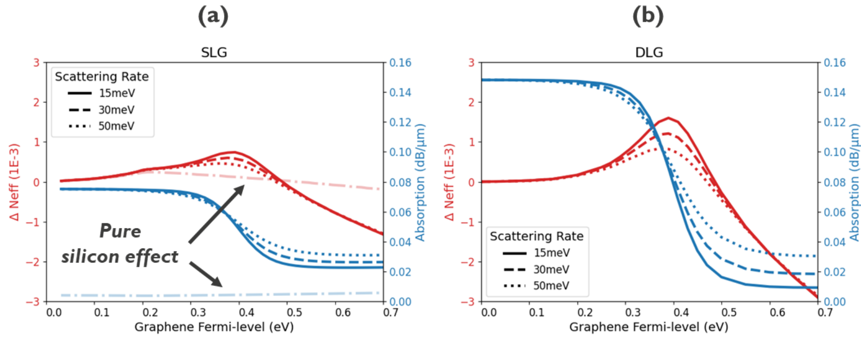

Figure 2.4: Simulated absorption (blue curves) and effective index change (red curves) of (a) SLG and (b) DLG as a function of graphene Fermi-level at TE mode and 1550 nm wavelength, for graphene with Γ = 15, 30, 50 meV. The light red and blue curves also demonstrate the modulation of absorption and effective index for pure silicon.

waveguide. Due to the presence of two layers of graphene and the absence of doped silicon, the GOG EAM allows a larger extinction ratio and smaller insertion loss, as will be shown below. Moreover, the GOG stack has the ability to be incorporated on various waveguide types, such as SiN waveguides and slot waveguides, hence expanding its application.

In this thesis, Lumerical, a commercial finite difference solver, is used to simulate the modulation of absorption and phase for both structures. As shown in Figure 2.3, the waveguide widths (W_{wg}) for devices with single layer graphene (SLG) and dual single layer graphene (DLG) are 500 and 450 nm, respectively. The overlap area of the DLG is 750 nm. All simulations were conducted at a wavelength of 1550 nm and a temperature of 300 K. The CHARGE solver in Lumerical was used to calculate the carrier distribution in the doped silicon. The layers of graphene were modeled as intrinsic, with no background doping. The effect of background doping on the graphene layer will be presented and discussed in a subsequent section. During the simulation, the graphene layer can be divided into two distinct regions: gated and ungated. The zone where the graphene Fermi level E_F can be modified is the gated region, whereas the ungated sections always have the same and unchanged E_F. The gated region in the SLG is determined by the width of the doped-Si waveguide, whereas the gated region in the DLG is determined by the overlap region between the top and bottom graphene. Figure 2.4 depicts a simulation for a SLG and a DLG in terms of Δn_{eff} and absorption as a function of graphene E_F for three scattering rate values. In the SLG, the modulation of the silicon through the plasma dispersion effect [55] is also taken into account. Both structures demonstrate that the absorption can be reduced and minimized when E_F is greater than 0.55 eV, which corresponds to the suppression of interband

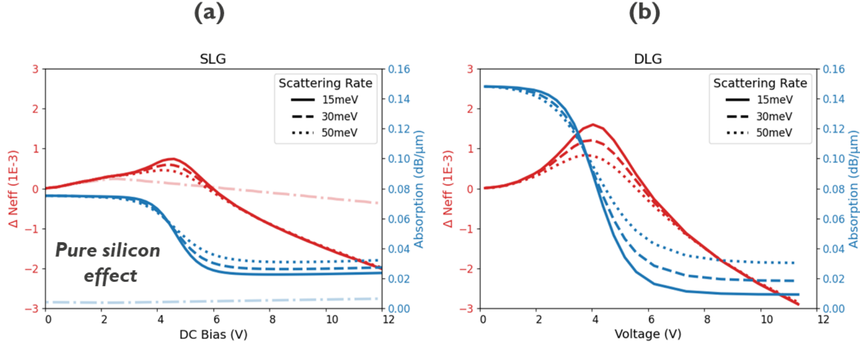

Figure 2.5: Simulated absorption (blue curves) and effective index change (red curves) of (a) SLG and (b) DLG as a function of DC bias at TE mode and 1550 nm wavelength, for graphene with Γ *= 15, 30, 50 meV. A dielectric constant of 7.8 is considered for* Al_2O_3 *in DLG architectures. Graphene's quantum capacitance is also taken into account by assuming initial carrier doping and impurity carriers of* 0 *and* 8×10^{11} cm^2 *[30], respectively.*

transitions caused by Pauli blocking. By raising the graphene E_F from 0 to 0.7 eV, an amplitude modulation of 0.053, 0.049, and 0.044 dB/μm is achieved in SLG devices, whilst 0.139, 0.130, and 0.118 dB/μm are accomplished in DLG devices for graphene with Γ = 15, 30, and 50 meV. Regarding the change in effective index, the values first rise and then fall, causing the peak to occur at $E_F \approx$ 0.4 eV. To enable pure phase modulation, $E_F >$0.5 eV is considered as the optimal operating area in which the optical loss of the device is constant and minimal.

To figure out the exact voltage required to move the Fermi-level of graphene, Eq. 2.7 and a dielectric constant of 7.8 for 10 nm Al_2O_3 in DLG are used. This high-k dielectric features an equivalent oxide thickness (EOT) of 5 nm, which is the thickness of a silicon oxide layer that provides the same capacitance density as a high-k material. For SLG devices, a 5 nm SiO_2 gate oxide is considered, and the Lumerical CHARGE solver is utilized to precisely monitor the charge profile under various biases. Figure 2.5 depicts the outcome for both architectures. Consequently, the amplitude modulation efficiency was calculated using 2V peak-to-peak voltage (V_{pp}), giving 0.021, 0.018, and 0.015 $dBum^{-1}V^{-1}$ in the SLG and 0.047, 0.039, and 0.031 $dBum^{-1}V^{-1}$ in the DLG for graphene with Γ = 15, 30, and 50 meV, respectively.

As illustrated in Figure 2.6, we utilize a 15 meV scattering rate and a 50 μm long device to evaluate ER and IL at various V_{pp}. The maximal ER rises with increasing V_{pp}, with maximum ER occurring at 4.5 V_{DC} bias. Under the same V_{pp} (1, 2, 3, and 4 V), the maximum ER of DLG devices (2.8, 4.7, 5.9, and 6.4 dB) is always two times larger than that of SLG devices (1.1, 1.9, 2.3, and 2.5 dB). At high

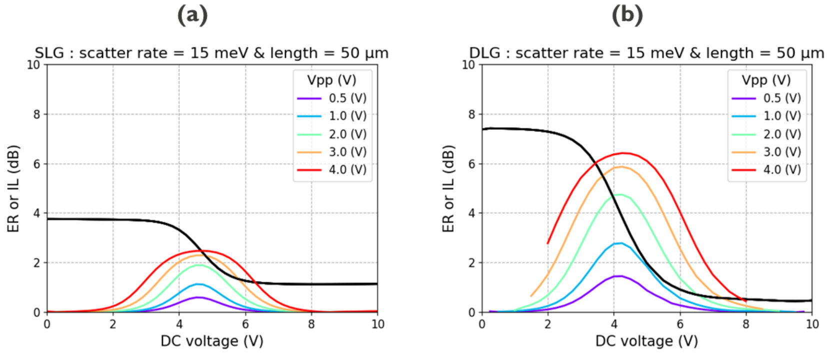

Figure 2.6: Calculated insertion loss (black curve) and extinction ratio (colored curves) of (a) SLG and (b) DLG as a function of DC bias at various V_{pp}, for graphene with Γ = 15 meV and active length (L_{active}) of 50 μm.

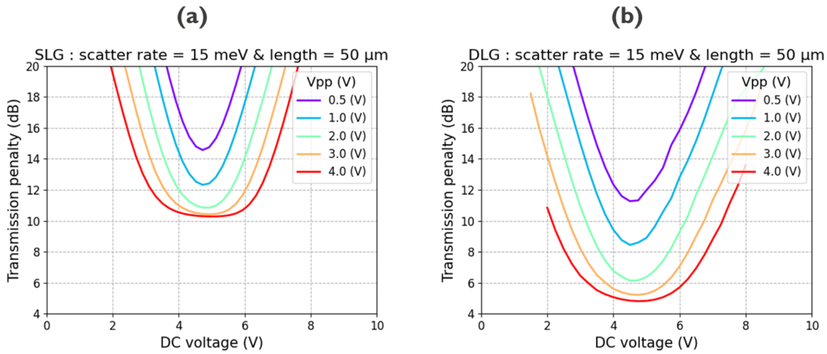

Figure 2.7: Calculated transmission penalty of (a) SLG and (b) DLG as a function of DC bias at various V_{pp}, for graphene with Γ = 15 meV and L_{active} = 50 μm.

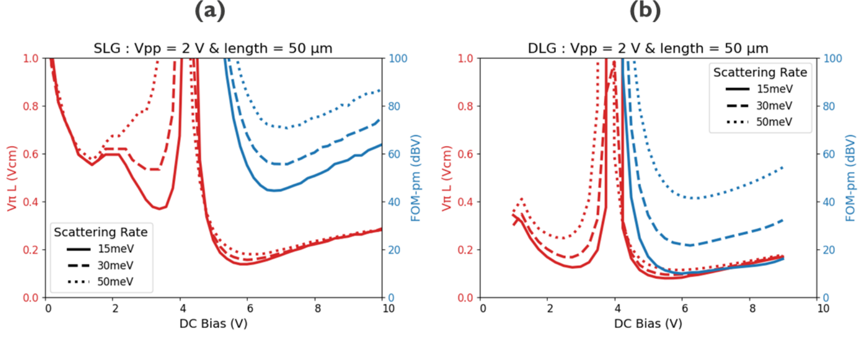

Figure 2.8: Calculated phase modulation efficiency (V_{π} $_L$) and figure of merit (FOM_{PM}) of (a) SLG and (b) DLG as a function of DC bias at TE mode and 1550 nm wavelength, for graphene with Γ = 15, 30, and 50 meV. L_{active} = 50 μm and V_{pp} = 2 V are considered here.

E_F, one may assume that the IL of the device would be better (lower) in SLG. Nonetheless, the loss from the doped silicon and ungated graphene region have to be taken into account. Since the gated region in the SLG is determined by the W_{wg}, the evanescent field near the waveguide edge still has a significant interaction with the ungated graphene, causing larger absorption in the devices. In contrast, the DLG is constructed with a 750-nm overlap region. It covers the evanescent electrical field at the border of the waveguide, resulting in a drop in IL as the E_F value increases. However, a larger device width results in a trade-off with bandwidth, which we will discuss in a later section. Next, we further calculate TP for both structures by using the Eq. 2.12. Figure 2.7 illustrates the outcome under the same settings as Figure 2.6. With a larger V_{pp}, the modulation efficiency and TP of both devices could be improved. For V_{pp} = 1, 2, 3, and 4 V, the best TP values for SLG are 11.2, 9.0, 8.1, and 7.8 dB, whereas the best TP values for DLG are 8.4, 6.1, 5.2, and 4.8 dB, respectively. The better performance in the DLG, compared to the SLG, can be attributed to a larger ER and lower IL at high E_F. In addition, the DLG demonstrates a TP = 6.1 dB @ $2V_{pp}$, which is superior to the lowest recorded Ge and III-V -based amplitude modulators. [68, 80]

The emphasis is then switched from amplitude modulator to phase modulator. First, we convert Δ n_{eff} in Figure 2.8 to a phase change using Eq. 2.8. To enable a driving voltage compatible with a conventional CMOS driver, we set V_{pp} = 2V and calculated the phase change efficiency (V_{π} L) for three graphene scattering rates, as represented by the red curves in Figure 2.8. With higher graphene quality (lower scattering rate), the performance of a device can be improved. For both architectures, a V_{DC} = 5 V shows the best V_{π} L. In DLG (SLG), V_{π} L = 0.080 (0.138) Vcm is obtained with graphene Γ = 15 meV, resulting in a device that

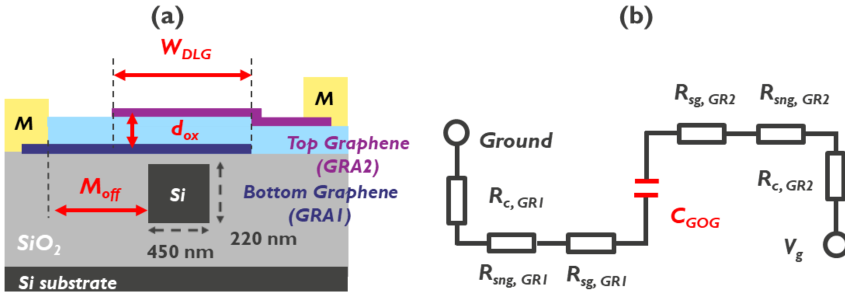

Figure 2.9: (a) A 2D schematic of DLG EAM integrated on a strip waveguide with 450 nm width and 220 nm height. Three key design parameters are defined. Metal offset (M_{off}) is the distance between metal and edge of waveguide. d_{ox} and W_{DLG} are the thickness of gate oxide and width of overlapped DLG, respectively. (b) The electrical circuit of DLG modulator, where V_g, R_c, R_{sng}, R_{sg}, and C_{GOG} represent the input voltage, contact resistance, resistance of non-gated graphene (access region), gated graphene (active region), and capacitance of graphene-oxide-graphene structure, respectively.

only needs 400 (690) μm in length to induce a π shift at $2V_{pp}$. These values are already superior to a silicon-based (0.25 Vcm) phase modulator with a similar capacitor-based construction and EOT. [7] The FOM_{pm} was then calculated using the Eq. 2.10 after accounting for loss. Since device loss is still significant when V_{DC} is below 4V, FOM_{PM} is significantly worse. FOM_{PM} is ineffective until device loss approaches the transparent zone. After V_{DC} >5V, FOM_{PM} can be drastically improved to be 45, 56, 71 dBV in the SLG and 10, 22, 41 dBV in the DLG for Γ = 15, 30, 50 meV. At high DC bias, the graphene quality dominates device loss and consequently FOM_{PM}. A graphene-based phase modulator can outperform a silicon-based device when a higher quality of graphene is introduced into the DLG.

2.1.4 Modelling of device's parameters

In the preceding sections, our exploration centered on the optical DC performance of graphene-based modulators featuring two distinct configurations. The results highlight the superior modulation efficiency and figure of merit exhibited by DLG devices. However, for applications in data communications, modulators must not only showcase efficient modulation but also deliver high-speed performance. In this section, we specifically consider DLG on a strip waveguide as an illustrative example and delve into the critical parameters that influence both optical and electrical performance. By examining these parameters in detail, we aim to gain insights into optimizing the overall functionality of graphene-based modulators for

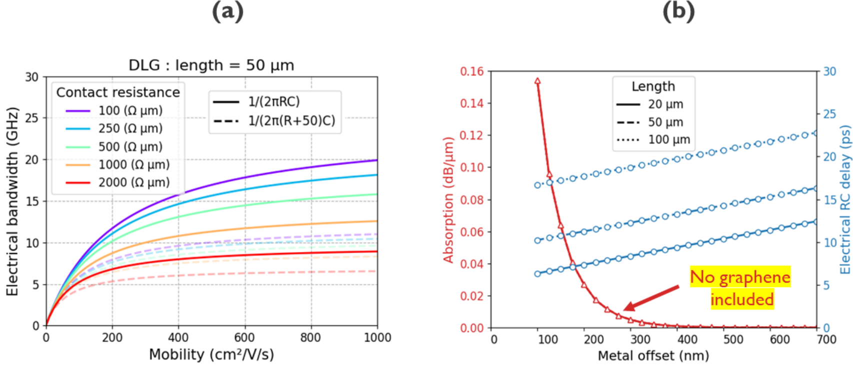

Figure 2.10: (a) Calculated intrinsic (solid curves) and 50-ohm (dashed curves) bandwidth as a function of graphene mobility for various contact resistance. The device active length is 50 μm. (b) Simulated absorption and electrical RC delay as a function of metal offset (M_{off}). No graphene layer is considered in simulated absorption results, indicating that the increase in absorption is due to metal itself. Calculated RC delay considers graphene with Γ = 15 meV, equally to mobility of 1130 $cm^2V^{-1}S^{-1}$ at 1e13 carrier concentration.

applications demanding not just efficiency but also high-speed capabilities.

Figure 2.9 depicts the cross-section of our DLG device and the definition of its most important parameters. We employ $450 \times 220nm$ for the strip waveguide and a 10 nm buffer oxide between the waveguide and graphene. W_{DLG} is the width of the overlap between the two graphene layers, also known as the active area of the device. d_{ox} represents the thickness of the gate oxide, whereas M_{off} represents the distance between the metal contacts and the waveguide's edge. In this context, we can also further define the access region of graphene, which is the region outside the active region and before entering into the metal. The E_F and R_s in the access region are considered to be voltage-independent and determined primarily by the background doping and impurities. To prevent an endless and unrealistic resistance, we simply assume an impurity concentration of $8 \times 10^{11}\ cm^{-2}$ [30] in the access zone. The equivalent circuit model is depicted in Figure 2.9(b) below. Basically, it is a more detailed version of C_{dv} and R_{dv} in Figure 2.2. C_{GOG} is the capacitance of the DLG device, which is determined by W_{DLG} and d_{ox}. R_c, R_{sng}, and R_{sg} represent graphene 1 and 2's contact resistance, non-gated sheet resistance, and gated sheet resistance, respectively. The sum of all resistances is referred to as the device's total resistance, or R_{dv} in Figure 2.2. As a reference, we select a device with W_{DLG}= 750 nm, d_{ox} = 20 nm (EOT = 10 nm), M_{off} = 500nm, R_c = 500 $\Omega\mu m$, and graphene Γ = 15meV, and we systematically vary each parameter.

First of all, we study the influence of graphene mobility and contact resistance on the electrical bandwidth. These are the only values that do not result in any trade-

off between EO performance and frequency responsiveness. In fact, as indicated previously, enhanced graphene mobility could even result in better modulation efficiency. Here, a capacitance (C_{GOG}) of 129 fF is computed using a reference device with a length of 50um. As for the resistance of the gated region, it is determined by the mobility at E_F = 0.45 eV, where modulation efficiency is at its highest. In Figure 2.10(a), we plotted the results using Eq. 2.14 and Eq. 2.13 for both intrinsic bandwidth (solid lines) and 50-ohm bandwidth (dashed lines). When mobility increases or R_c decreases, estimated electrical bandwidths expand. With mobility equal to 1000 $cm^2V^{-1}S^{-1}$, the total resistance of DLG is 62, 78, and 138 Ω, resulting in an intrinsic bandwidth of 20, 16, and 9 GHz and a 50-ohm bandwidth of 11, 10, and 7 GHz for R_c = 100, 500, and 2000 $\Omega\, \mu m$, respectively. The driver's 50 Ω impedance adds additional resistance to the circuit, preventing the device from achieving its intrinsic bandwidth during the actual measurement. To better compare with experimental results in later chapters, electrical bandwidth is referred to the 50-ohm bandwidth, unless otherwise specified.

In Figure 2.10(b), the influence of the metal offset (M_{off}) is simulated. The red curve in Figure 2.10(b) shows a simulation in which no graphene layers are present. This allowed us to clearly notice that the device's metal induced absorption is near to 0 dB/μm when M_{off} >500nm. By decreasing M_{off} from 500 nm to 200 nm, the optical loss from metal contacts increases, reaching maximum absorption = 0.027 dB/μm. It corresponds to additional loss of 1.35 dB for a 50 μm device. In contrast, when M_{off} decreases, the corresponding electrical RC delay decreases as the resistance of the unbiased region is reduced. The RC delay presented here is calculated by equation 2.14 and is inversely proportional to bandwidth. As seen by the blue lines in Figure 2.10(b), the same approaches were employed to determine the electrical RC delay as a function of M_{off} for L_{active} = 20, 50, and 100 um. When M_{off} is reduced from 700 to 100 nm, the RC delay decreases from 12.4 to 6.3 ps, equivalent to a bandwidth increase from 12.8 to 21.6 GHz. The improvement is diminished for longer devices since they are dominated by the 50 Ω impedance from the driver. A value of 500 nm appears to be the optimal compromise between optical loss and frequency response for a DLG strip waveguide.

Next, the effect of the gate oxide thickness is investigated. Here, we assume Al_2O_3 for the gate oxide with ϵ_{ox} = 7.8 and graphene layers with Γ = 15 meV in the simulation. Figure 2.11(a) depicts the absorption as a function of voltage for various gate oxide thicknesses. This figure contains two key pieces of information. First, the absorption at V_g = 0 (V) drops from 0.153 to 0.125 dB/μm as the thickness increases from 5 to 40 nm, which may be related to the mode profile and the increase in the vertical distance between the second layer of graphene and the waveguide. At high voltage, where loss is minimal, absorption is comparable (0.01 dB/μm), resulting in a greater modulation for devices with a thinner gate oxide. Secondly, the

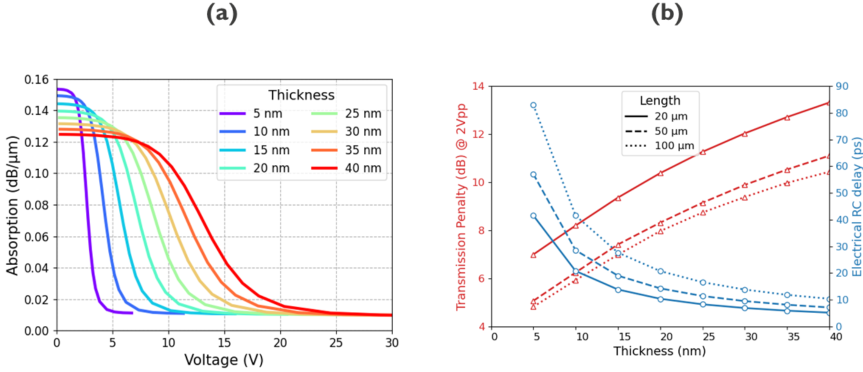

Figure 2.11: (a) Simulated absorption as a function of applied voltage at TE mode and 1550 nm wavelength, for gate oxide thickness ranging from 5 to 40 nm. Γ *= 15 meV and oxide permittivity (*ϵ_{ox}*) = 7.8 are considered. (b) Calculated TP (red curves) and electrical RC delay (blue curves) as a function of* d_{ox} *for device with* L_{active} *= 20, 50, and 100* μm

required voltage for graphene to enter the Pauli blocking area grows with increasing d_{ox}. For example, a device with d_{ox} = 40 nm requires nearly V_{pp} = 30 V, whereas a device with d_{ox} = 5 nm only needs V_{pp} = 5 V to swing between maximum and minimum absorption. Consequently, devices with thinner oxide can be driven directly by a CMOS-compatible driver (<2V). On the other hand devices with thicker oxide require a more sophisticated driver design. Here, we determined the modulation efficiency using 2 V_{pp} and obtained values of 0.063, 0.047, 0.028, and 0.014 $dBum^{-1}V^{-1}$ for device with d_{ox} = 5, 10, 20, 40 nm. Consequently, better modulation and efficiency occur when the gate oxide thickness is reduced. In terms of FOM_{EAM}, a smaller thickness device also provides a better TP value as shown by the red curves in Figure 2.11(b). TP = 4.82, 5.93, 7.97, and 10.4 dB are attained for 100um-long devices with d_{ox} = 5, 10, 20, and 40nm. With reduced thickness, modulation, modulation efficiency, and TP are all enhanced; but, electrical RC delay (bandwidth) is also anticipated to increase (decrease). The smaller the thickness, the larger the capacitance and the larger (smaller) the electrical RC delay (bandwidth). RC delay of 41.6, 20.8, 10.4, and 5.2 ps, corresponding to bandwidths of 3.8, 7.7, 15.3 and 30.6 GHz, are simulated for a 20um-long device with d_{ox} = 5, 10, 20, and 40 nm in Figure 2.11(b). Although devices with a greater thickness provide a superior frequency response, devices with a moderate thickness are the key to achieving an optimal balance between EO performance and bandwidth.

Finally, we manipulate the width of the DLG (W_{DLG}) to achieve a balance between optical performance and frequency response. By narrowing W_{DLG}, the capacitance of the device can be decreased, resulting in a wider 3dB bandwidth. However, it does not come without a cost. With a narrower DLG width, the optical mode interacts

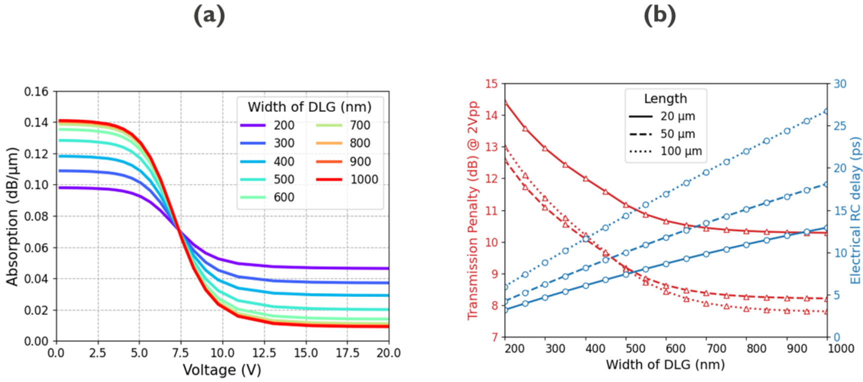

Figure 2.12: (a) Simulated absorption as a function of applied voltage at TE mode and 1550 nm wavelength, for width of DLG (W_{DLG}) ranging from 200 to 1000 nm. Γ = 15 meV and ϵ_{ox} = 7.8 are both considered. (b) Calculated TP (red curves) and electrical RC delay (blue curves) as a function of W_{DLG} for device with L_{active} = 20, 50, and 100 μm

less with the active region of the graphene layers and more with the unbiased region. When there is no background doping introduced, the unbiased region normally exhibits large optical loss and does not provide modulation. When W_{DLG} is decreased, ER drops, IL increases, and TP worsens. Figure 2.12(a) demonstrates that when the DLG width is reduced from 1000 to 200 nm, the minimum IL increases from 0.009 to 0.046 dB/μm and the maximum ER reduces from 0.132 to 0.052 dB/μm. Consequently, the modulation efficiency decreases from 0.029 to 0.011 dB/μm when 2 V_{pp} is applied. Figure 2.12(b) depicts a summary of the trade-off between optical (TP) and electrical (RC delay) performance. TP with $2V_{pp}$ worsens from 7.8 to 13.1 dB as W_{DLG} decreases, although the RC delay decreases from 26.7 to 6.0 ps, which equals to a 3dB bandwidth increase from 6.0 to 26.7 GHz for a 100um-long device.

L_{active}, M_{off}, d_{ox}, and W_{DLG} all generate trade-offs between optical performance and frequency responsiveness. Graphene quality and contact resistance are the only two factors that do not result in a trade-off. By enhancing graphene's mobility, the sheet resistance can be decreased and a greater modulation can be created. Besides, a lower contact resistance can improve the 3dB bandwidth and seems not to harm the optical performance. Therefore, a smart strategy is required for a device to simultaneously achieve high performance and speed.

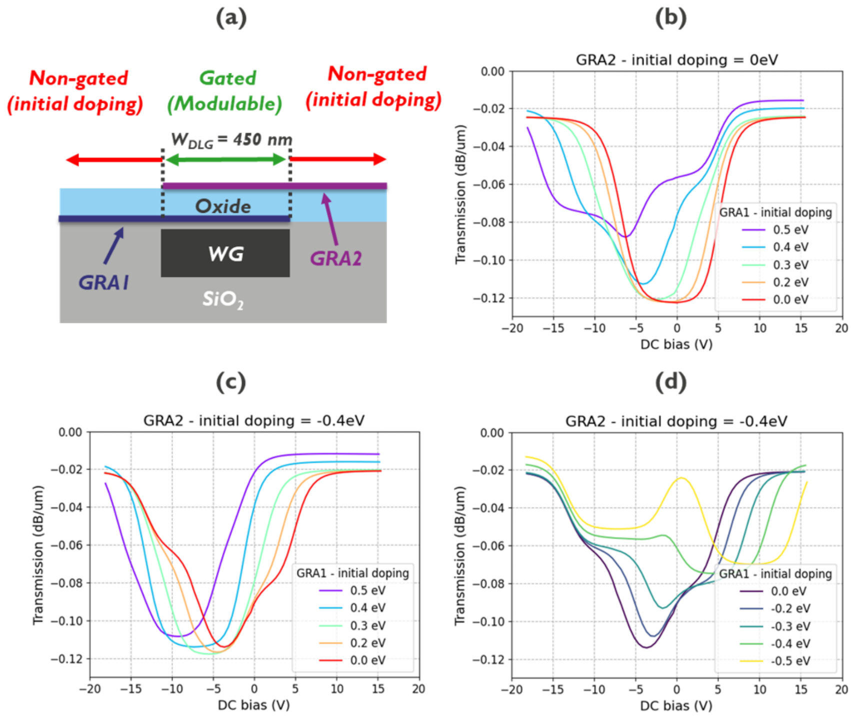

Figure 2.13: (a) A 2D schematic of DLG EAM integrated on a strip waveguide with 450 nm width and 220 nm height. The green (red) area is gated (non-gated) region, which graphene E_F can (cannot) be modulated. Simulated transmission as a function of DC bias for graphene 1 with initial doping values ranging from 0 to 0.5 eV and graphene 2 with background doping values of (a) 0 eV and (b) -0.4 eV. (c) Simulated transmission as a function of DC bias for graphene 2 with background doping value of -0.4 eV, and graphene 1 with background doping values ranging from 0 to -0.5 eV.

2.1.5 Modelling of background doping

Previous simulations assumed neutral graphene; backgroud doping was not taken into account. Due to its atomic thickness, graphene can adsorb molecules from the atmosphere and become doped during the integration process. [156] In order to comprehend the effect of background doping and get the simulation closer to the experimental case, we consider background doping of the graphene layers in this section. We investigate the impact on absorption modulation using DLG with strip waveguide and EOT=10nm as an example. The width of the gated region is 450 nm, and the metal offset is 750 nm to prevent loss from metal contacts. First, we swept the background doping of graphene 1 and kept graphene 2's doping constant. The Fermi-level will increase/decrease during modulation, starting from the level determined by the background doping. Please note that the Fermi-level of graphene is modulable in gated regions but not in the non-gated regions. In other words, the carrier concentration of graphene will remain the same as the background doping in non-gated regions. It is practical and simple to do the calculates based on the carrier concentration, therefore we converted the original chemical potential to carrier concentration and conduct a carrier sweep in the opposite direction on both sides of graphene. For instance, the top layer of graphene raises by $1 \times 10^{13} cm^{-2}$ carriers, while the bottom layer lowers by $1 \times 10^{13} cm^{-2}$ carriers. To avoid an impractical number, both layers are assumed to have an impurity carrier concentration of $8 \times 10^{11} cm^{-2}$. After summarizing all the carriers (background doping, sweeping carrier, and impurity carrier), we convert back to E_F and simulate the loss in Lumerical.

Figure 2.13(b) depicts the result, in which the initial Fermi level of graphene 2 is 0 eV and the initial Fermi level of graphene 1 ranges from 0 to 0.5 eV. The DC bias is calculated using a 20 nm Al_2O_3 with EOT = 10 nm as the gate oxide. When the background doping of graphene 1 changes from 0 to 0.5 eV, three phenomena can be observed: (1) The minimal transmission point is shifting to the left, allowing modulation to occur at DC bias = 0V. (2) The maximum modulation depth decreased from 0.098 to 0.072 dB/μm. The drop is more pronounced for graphene with a higher background doping because more carriers are required to return back to the neutrality point. At the same time, the other layer of graphene (graphene 2) is already less absorbing due to the same number of carriers moving in opposite directions. Consequently, the sum of minimum transmission is less, resulting in a lower modulation depth than in the case of neutral graphene. (3) The transmission maximum increases from 0.025 to 0.016 dB/μm. The enhancement is a result of early doping in the non-gated region of graphene. Since the width of the DLG is only 450nm, light still interacts strongly with the ungated graphene, particularly at the waveguide's edge. With increased background doping, non-gated graphene becomes more transparent, resulting in larger transmission in the complete device.

In addition, we simulate the situation in which graphene 2 has an background doping value of -0.4 eV, and the results are presented in Figure 2.13(c) with the same range of background doping for graphene 1. When the background doping value of graphene 1 and graphene 2 is 0.4 eV and -0.4 eV, respectively, the slope and modulation depth are identical to those of Figure 2.13(b) with both layers having 0 eV. Pre-doping of both graphene layers shifts the curve to the left, enabling greater transmission (lower loss) at graphene transparent region. This shift eliminates the need for higher voltage to access the low-loss region, potentially mitigating challenges associated with identifying an appropriate gate oxide for graphene-based modulators [146]. Consequently, a device with one layer of p-doped graphene and another layer of n-doped graphene appears to be efficient. On the other hand, the performance of a device containing identical doping types of graphene could be limited. Both graphene 1 and graphene 2 have a negative background doping level in Figure 2.13(d) (p-doped). The greatest modulation depth of the devices is 0.093, 0.087, 0.072, 0.058 and 0.057 dB/μm for background doping values of 0, -0.2, -0.3, -0.4, and -0.5 eV in graphene 1, respectively. The deterioration is caused by graphene 1 and graphene 2 moving in opposite directions, and is exacerbated by a higher background doping concentration. As an illustration, consider the background doping curve of -0.4 eV for both graphene 1 and graphene 2. After applying a positive bias (from 0 V to 5 V) on graphene 2 and ground on graphene 1, graphene 2 shifts downward and becomes more transparent, but graphene 1 shifts upward and increases absorption prior to reaching the neutrality point. When a voltage larger than 5V is applied, graphene 2 stays transparent; hence, transmission modulation is exclusively generated by graphene 1 (in conduction band). Therefore, modulation is ineffective for devices with the same type of doping.

2.2 Device characterization

This section we explain the experimental methods used in this thesis to characterize the performance of the devices.

2.2.1 Transmission measurement

The transmission measurement is a purely passive measurement (without electrical signal involved). The primary objective is to estimate device loss. Figure 2.14(a) depicts the setup in which the light from an external laser travels via the input fiber and couples to the waveguide through input grating couplers. The light within the waveguide then interacts with the device under test (DUT) and is coupled out by another grating coupler. By measuring the difference between input and output

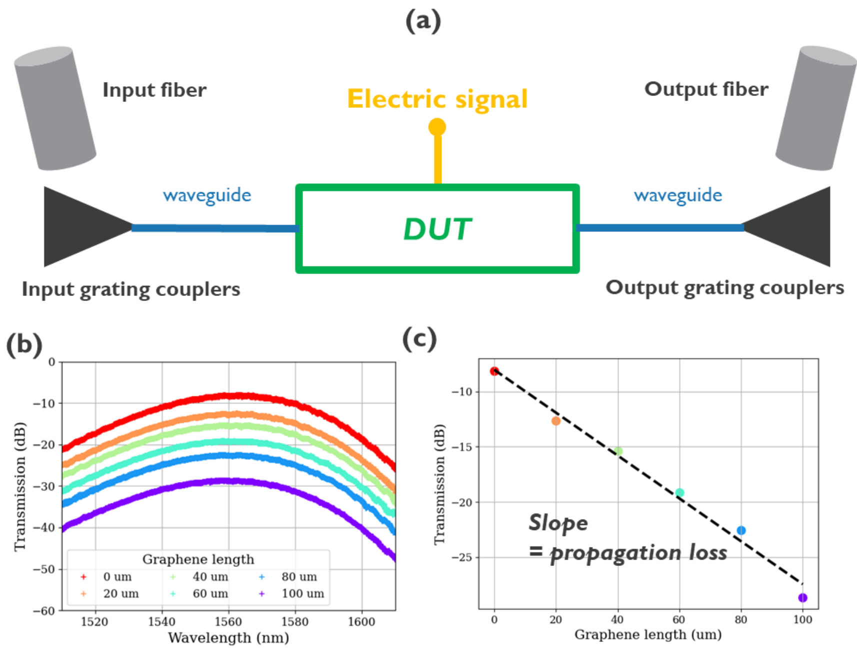

Figure 2.14: (a) A schematic setup used to measure loss and DC measurement. (b) Measured transmission as a function of incident wavelength for graphene length ranging from 0 to 100 μm (c) Extracted and fitted data of transmission as a function of graphene length. The slope represent the propagation loss of the material.

power, the DUT's loss can be determined. Standard and advanced forms of grating couplers are presented in this thesis. Standard grating couplers are directly etched and fabricated in the SOI wafer and typically result in 5 dB of insertion loss per coupler. The design of the advanced grating couplers is based on the published literature [157], which requires the deposition of polysilicon (or amorphous silicon) to locally thicken the silicon layer. Advanced grating couplers have an insertion loss of only about 2 dB. However, a topography of 160 nm is anticipated locally due to the deposition of an additional silicon layer. Larger surface topography may make it harder to transfer graphene uniformly and have a strain effect on material itself. To minimize problems, both grating couplers are located far from the active region (where the graphene layers are designed). This thesis does not observe any significant performance differences or issues for the modulators between wafers with standard and advanced grating couplers.

Figure 2.14(b) depicts a typical transmission measurement experiment outcome. Using a wavelength sweep from 1510 to 1610 nm, various length devices were measured. The shape of the curves is a result of the grating couplers' response. The device with 0 μm graphene length can be considered as the reference device and the additional loss due to graphene layers can be determined from the transmission difference between the curves. As illustrated in Figure 2.14(c), the peak transmission value of each device is then extracted and linearly fitted with the corresponding graphene length. The slope of the fitting line can be used to get the propagation loss (in dB/μm) of graphene layers.

2.2.2 DC measurement

While the transmission measurement does not involve an electrical signal, the DC measurement requires the probes to be landed and a bias to be applied to the devices. Essentially, a loss measurement is performed at each DC voltage applied, and then the device's modulation can be monitored. The only aspect that requires caution is the sweeping range. If the voltage is too low, it may be impossible to see modulation of absorption. However, if the voltage is too high, it will ruin the device by destroying the gate oxide. According to [146], a good gate oxide layer is the key to realizing a high-performance modulator with pristine graphene. This thesis discusses both SLG and DLG architectures. In SLG devices, a gate oxide of 5nm is defined through the planarization step during the waveguide's fabrication. To extract most of the modulation without causing damage to the electronics, the voltage was swept from -4 to 4V. In contrast, in DLG devices, the gate oxide is produced through the deposition of Al_2O_3 or HfO_2. Different sweeping ranges were utilized based on the thickness, dielectric constant, and dielectric strength of the material. Figure 2.15(a) and (b) depict the DC measurement results for EAM

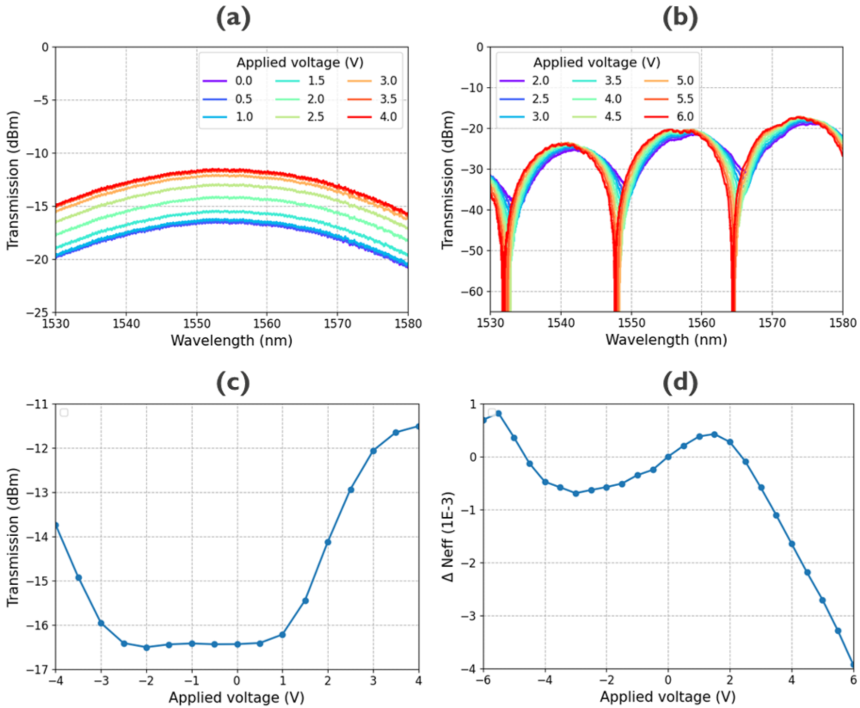

Figure 2.15: Measured transmission as a function of incident wavelength for (a) EAM at applied bias ranging between 0 to 4 V and (b) MZM at applied bias ranging between 2 to 6 V. Extracted data of (c) transmission from EAM and (d) ΔN_{eff} from MZM as a function of applied voltage.

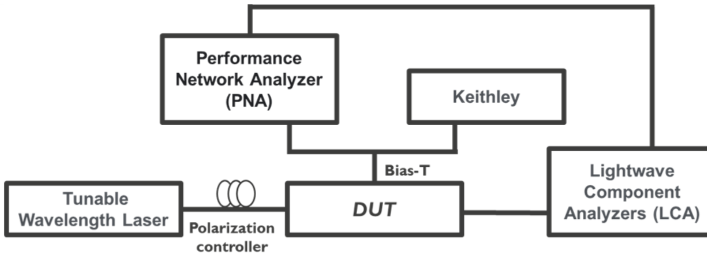

Figure 2.16: A schematic setup used to measure small-signal RF characterization.

and MZM architectures, respectively. By collecting the peak transmission value in Figure 2.15(a), transmission as a function of applied voltage can be obtained as indicated in Figure 2.15(c), allowing for further analysis including absorption modulation depth, modulation efficiency, and transmission penalty. In contrast, the MZM is typically used to monitor the change of index. A constant voltage is applied to one arm of the MZM in Figure 2.15(b), whereas the the voltage on the other arm is swept. After fitting a single valley, the shift in the position of the minimum wavelength can be tracked and converted to a change in n_{eff}. Figure 2.15(d) depicts the change of n_{eff} as a function of applied voltage, allowing the phase modulation efficiency to be calculated.

2.2.3 Small-signal RF measurement

The primary objective of measuring small signal S-parameters is to characterize a device's high-speed performance. The layout is depicted in Figure 2.16. First, input light travels through the polarization controller and interacts with the device. A bias-T is utilized to integrate and apply the high-speed electrical AC signal from the performance network analyzer (PNA) and the DC voltage from the Keithley 2400. After the modulator converts the electrical signal to an optical signal, the Lightwave Component Analyzer (LCA) converts the optical signal back into an electrical signal. The PNA is then used to generate the S11 and S21 responses. The bandwidth of the device can be calculated directly from S21, and the capacitance and resistance of the DUT can be estimated by fitting S11 with an equivalent circuit model, as depicted in Figure 2.2. These capacitance and resistance measurements are used to estimate the electrical bandwidth, which can then be compared to the bandwidth obtained from S21.

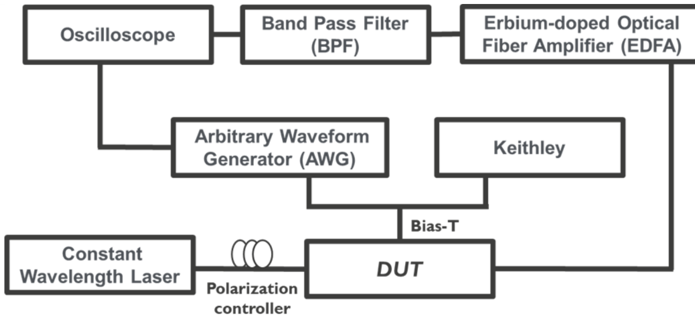

Figure 2.17: A schematic setup used to measure large-signal RF characterization.

2.2.4 Large-signal RF measurement

The final type of EO characterisation is large-signal high-speed measurement. The device is measured using a signal consisting of a pseudorandom binary sequence (PRBS) and DC bias. The output signal from the modulator is amplified with an erbium-doped fiber amplifier (EDFA) and filtered with a band pass filter (BPF) before being sent to the oscilloscope for eye diagram collection. The bitrate is increased from 5 Gbit/s to 25 Gbit/s, and the peak-to-peak voltage is set to be as low as possible in order to be compatible with the CMOS driving voltage (smaller than 2V).

2.3 Material characterization

This section we will explain the experimental methods used in this thesis to characterize the quality of 2D materials.

2.3.1 Optical characterization: Raman

In Raman spectroscopy, a monochromatic laser (with a wavelength of 532 nm in our case) is used to interact with molecular vibrational modes and phonons in a sample. This interaction can either increase (Stokes mode) or decrease (anti-Stokes mode) the frequency of the scattered light by emitting or absorbing the energy of a phonon [158]. Only the Stokes process is considered because it is more likely to occur and produces a higher intensity [159]. Since only laser excitation is used to identify vibrational modes, Raman spectroscopy has become a fast and non-destructive method to characterize graphene [159, 160]. It can reveal information

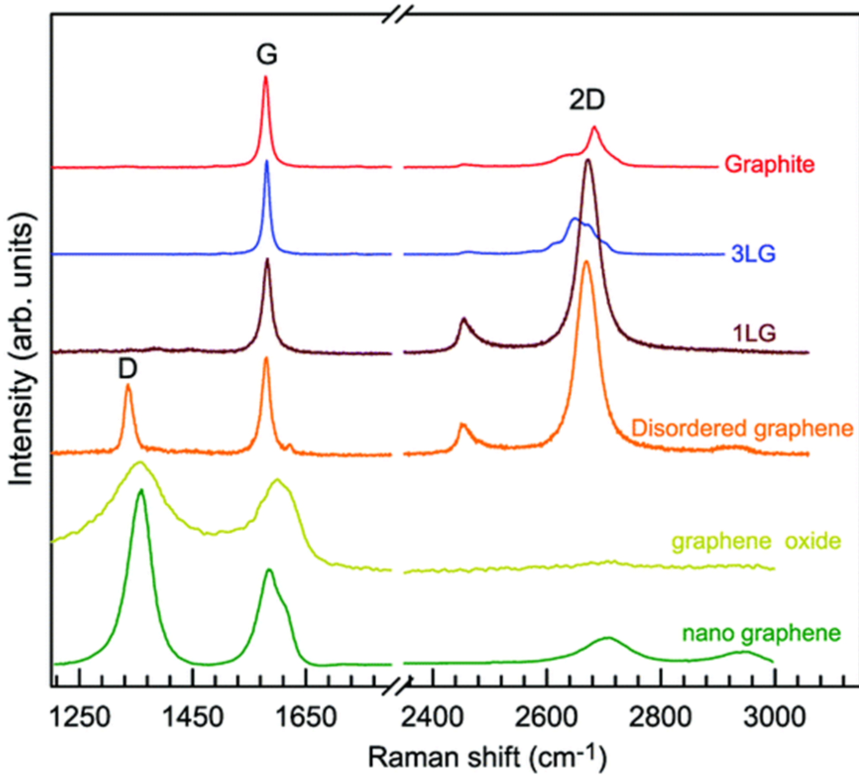

Figure 2.18: Raman spectrum of graphene-based materials, taken from reference [31]

on thickness, doping, strain and stress, and electrical mobility [159], providing a level of detail sufficient to allow comparison of graphene used by different research groups. Furthermore, it can be used not only in the laboratory but also in production lines [161], allowing for graphene quality control on wafer-scale.

A typical example of the Raman spectrum for graphene is shown in Figure 2.18. There are three key peaks: the G, D, and 2D peaks. The position of the G peak lies around 1580 cm^{-1}, corresponding to the in-plane E_{2g} vibrational mode [162]. As the excitation usually resonates with the π states, the sp^2 sites predominate in the Raman spectra of carbon films. Therefore, the G peak can easily be observed on graphene, graphite, and even highly sp^3-bonded amorphous carbon. [163] The D peak (1360 cm^{-1}) arises from A1' vibrational modes of the six-atom ring and appears when structural disorder happens in the graphene film [164, 165]. The intensity of the D peak increases with an increasing number of defects. On the other hand, intrinsic graphene with an ideal structure does not exhibit a D peak. The 2D peak is a secondary D peak, lying between 2500 to 2800 cm^{-1} in the Raman spectra. In single-layer graphene, it has the highest intensity, but in multi-layer graphene, it broadens and loses intensity. If there are more than five layers of graphene, there is typically not much difference from graphite. The D, G and 2D peaks constitute the Raman signature of graphene. By looking at the ratio of ID/IG and I2D/IG from Raman spectrum, the quality of a single layer of graphene can be estimated. [159, 162, 163, 166–169]

2.3.2 Electrical characterization: transfer length method

A transfer length measurement (TLM) is the most frequently used method for determining the metal/graphene (2D) contact resistance and graphene's (2D) sheet resistance. If the carrier concentration is known, it is possible to determine the graphene (2D) mobility. A TLM structure is composed of many field effect transistors (FETs) with varying metal spacing. Figure 2.19(a) depicts our TLM structure as an example. The channel length (metal spacing) of FETs spans from 500 nm to 10 μm, whereas the channel width is 100 μm. One of the metal pads in each FET (Figure 2.19(b)) serves as the source, allowing to apply a voltage (V), while the other serves as the drain, connected to ground. For a single FET, the output current (I) can be used to calculate the overall resistance ($R = V/I$). In TLM, it is assumed that each FET has the same material quality and contact resistance. As shown in Figure 2.19(c), the measured total resistance of each device is plotted as a function of channel length, and a linear fit is applied to each data point. In this instance, the sum of contact resistance on both sides may be calculated from the y-intercept, whereas the sheet resistance can be derived from the slope of the fitting line, as shown in the following equations:

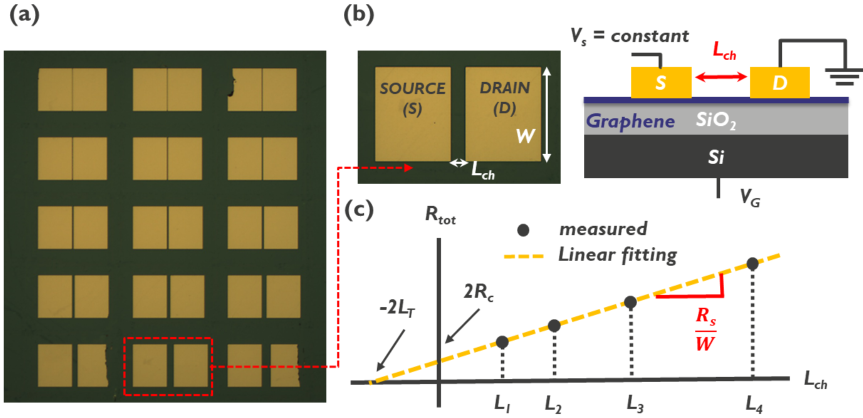

Figure 2.19: (a) Optical microscope image of TLM devices. (b) Top-down and cross-section of single field-effect transistor (FET) from TLM with definition of channel length (L_{ch}) and width (W). (c) Measured and fitted total resistance as a function of channel length. Sheet resistance (R_s), contact resistance (R_c) and transfer length (L_T) are defined.

$$R_{total} = 2R_m + 2R_c + R_{semi} \tag{2.15}$$

$$R_{semi} = R_s \frac{L}{W} \tag{2.16}$$

where R_m is associated with the resistance of metal, R_c is the contact resistance of material/contact metal and R semi is the resistance of material itself. R_m can be ignored as normally it is much smaller than the other two. R_{semi} can be expressed by the sheet resistance (R_s), channel length (L) and channel width (W).

Graphene (2D) TLM characterization is performed under different electrical field by applying a voltage sweep from the back of the sample (Figure 2.19(b)). A typical measured result of drain current against gate voltage is shown in Figure 2.20(a) for both graphene and MoS_2. The minimum point of the graphene's curve is the graphene neutrality point (V_{NP}) while the threshold voltage (V_{TH}) is used for MoS_2, defined as the extrapolation from the tangent line of inflection point to the x-axis. In practice, the position of the neutrality point (or the threshold voltage for MoS_2) varies from device to device due to slightly different levels of doping during fabrication. In order to compare and calculate an accurate result from TLM, all curves have to be normalized with V_{NP} (V_{TH}) before the linear fitting as shown in Figure 2.20(b). With such normalization for gate voltage, we could calculate the contact resistance and sheet resistance of graphene as a function

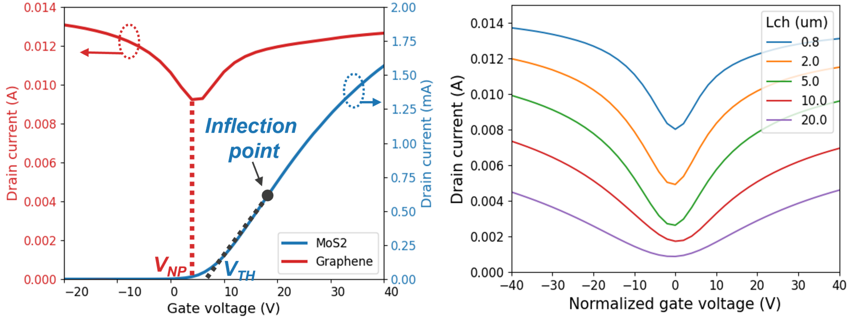

Figure 2.20: (a) Example of drain current as a function of gate voltage ($I_d - V_g$) for graphene (red curve) and MoS_2 (blue curve) -based FET. (b) Measured drain current as a function of normalized gate voltage for L_{ch} ranging from 0.8 to 20 μm.

of normalized gate voltage. Graphene's mobility can be estimated based on its conductivity (G_s). Graphene's conductivity is inversely proportional to the sheet resistance ($G_s = 1/R_s$), and can be related to the carrier concentration (n) and mobility(μ) [170] by,

$$G_s = nq\mu \tag{2.17}$$

For our back-gated device, the carrier concentration in graphene can the estimated [19] by,

$$n = \frac{C_{ox}}{e}(V_G - V_{Dirac}) = \frac{\epsilon_0 \epsilon_r}{ed_{ox}}(V_G - V_{Dirac}) \tag{2.18}$$

Where C_{ox} is the capacitance of the gate oxide, V_g is the gated voltage, V_{Dirac} is the voltage of the neutrality point or threshold. C_{ox} is calculated from the permittivity of free-space (ϵ_0), relative permittivity of the oxide (ϵ_r) and the dielectric thickness (d_{ox}).

Combining Eq. 2.17 and Eq. 2.18, the field-effect mobility, μ, can be calculated by dG_s/dV_g [19] as Eq. 2.19:

$$\mu = \frac{1}{C_{ox}} \frac{dG_s}{dV_g} \tag{2.19}$$

2.4 Conclusion

The chapter concludes by detailing the EO characterization methods employed to gather static and dynamic performance data for this thesis. Furthermore, it delves into optical and electrical material characterization techniques, providing insights into material quality. This chapter delves into investigating and modeling graphene-based modulators for achieving high-performance modulation within the 1550 nm wavelength range. Initially, we scrutinized the static Electro-Optic performance of SLG and DLG devices. Notably, DLG-based devices exhibited a figure-of-merit, defined as the transmission penalty and FOM_{PM}, roughly twice that of SLG devices under identical conditions of graphene quality and measurement methodology. However, for effective modulators, both good efficiency and high-speed performance are essential.

Addressing the frequency response necessitates a discussion of trade-offs among loss, Extinction Ratio, and bandwidth. To comprehensively understand and design a graphene-based modulator, a DLG device based on a strip waveguide served as a test platform. Key parameters influencing EO static and dynamic performance, such as graphene mobility, contact resistance, metal offset, DLG width, DLG length, and gate oxide thickness, were explored. This exploration revealed the need for strategic considerations to achieve the desired performance. Additionally, the chapter presents a model examining the effect of background doping, offering a potential path to further improve device performance. Furthermore, with the right doping design, achieving pure phase modulation with minimal loss at low DC bias becomes a possibility.

The chapter concludes by detailing the EO characterization methods employed to gather static and dynamic performance data for this thesis. It also explores optical and electrical material characterization techniques, providing insights into material quality.

3

FAB-LEVEL SINGLE-LAYER GRAPHENE ELECTRO-ABSORPTION MODULATORS

Graphene-based photonics devices have shown great promise for several applications. For graphene devices to be used in real-world systems, it is necessary to demonstrate competitive device performance, repeatability of results, reliability, and a path to large-scale manufacturing with high yield at low cost. However, the vast majority of these demonstrations employ small coupons or non-scalable CVD-grown graphene, preventing industrial adoption. Therefore, the development of new and robust modules, adhering to the strict contamination requirements of CMOS fabs, are required for the scalable integration of graphene devices. In this chapter, a single-layer graphene (SLG) electro-absorption modulator (EAM) is chosen as the test vehicle, and wafer-scale integration for graphene-based photonics devices is developed in a 300mm pilot CMOS foundry environment. The brief in-line integration flow is shown in Figure 3.1, starting with a silicon on insulator (SOI) wafer (Figure 3.1(a)), defining doped waveguides, including their planarization (Figure 3.1(b)), graphene transfer (Figure 3.1(c)), graphene encapsulation (Figure 3.1(d)), patterning of graphene (Figure 3.1(e)), back-end-of-line (BEOL)

planarization (Figure 3.1(f)), defining contacts to the doped silicon (Figure 3.1(g)), graphene contacts (Figure 3.1(h)) and a final copper damascene metal routing layer (Figure 3.1(i)).

This chapter performs and discusses two phases of research. In phase one, which is described in section 3.1, three crucial parameters are investigated and optimized: the planarization step prior to graphene transfer, encapsulation of the graphene layer, and contacts with the graphene layer via a damascene process. Hundreds of devices demonstrate performance comparable to that of lab-based devices with similar design and graphene quality, proving the robustness of wafer-scale integration. In the second phase, as detailed in section 3.2, we explore three avenues to enhance device performance, building upon the integration process established in phase one: (1) employing different gate oxides between the doped waveguide and the graphene layer, (2) enlarging the size of the transferred graphene layer, and (3) implementing precise graphene patterning modules. While the Electro-Optic (EO) performance may not consistently surpass that of the champion wafer discussed in section 3.1, we demonstrate improved control over the graphene patterning process. Moreover, the successful transfer and fabrication of devices with 8-inch graphene underscore the scalability of the integration flow.

The developed integration route, characterized by its reproducibility and robustness, serves as a foundation for scaling not only EAMs but also other graphene-based photonic devices. This progress paves the way for broader industrial adoption of graphene-based photonics technology.

Part of the text and results contained in this chapter have been published in Wu, Cheng Han, et al. ”Graphene electro-absorption modulators integrated at wafer-scale in a CMOS fab.” 2021 Symposium on VLSI Circuits. IEEE, 2021. [171] and Wu, Chenghan, et al. ”Wafer-Scale Integration of Single Layer Graphene Electro-Absorption Modulators in a 300 mm CMOS Pilot Line.” Laser & Photonics Reviews (2023): 2200789. [172]

3.1 Phase one study: development and optimization of fab-level integration

The lithography process, graphene encapsulation, and graphene contacts are the primary obstacles preventing the integration of graphene-based devices with CMOS technology. [173] Currently, electron-beam lithography (EBL) and lift-off-based contact metallization are the most prevalent techniques, but they are incompatible with high-volume industrial production. [173] Standard photolithography utilizing a mask is preferred to enable high throughput and keep the process cost effective,

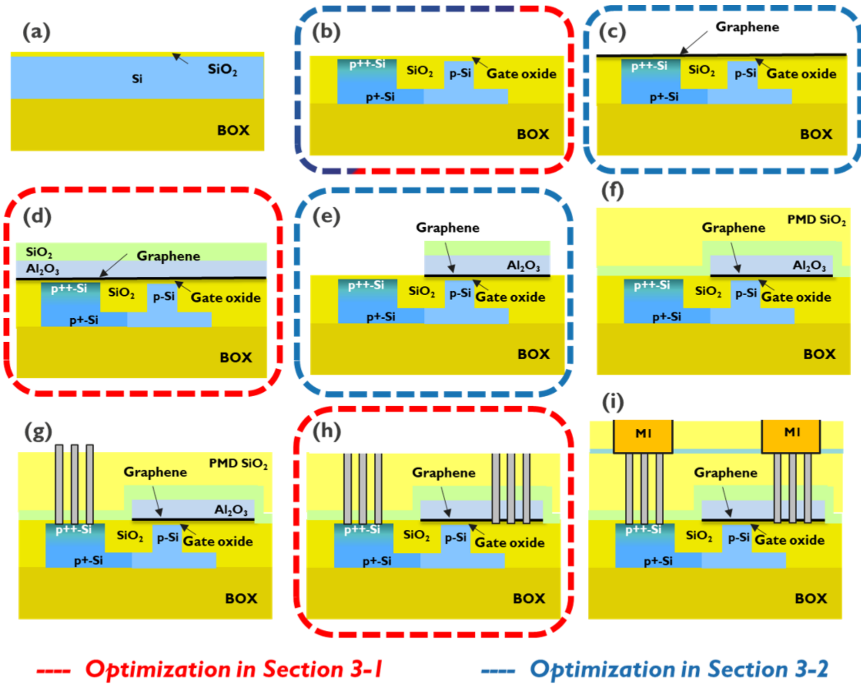

Figure 3.1: Proposed integration flow with red and blue rectangles indicating the optimization stpes implemented in later sections. (a) SOI wafer, (b) waveguide patterning, surface planarization, and Si implantation steps, (c) wafer-scale graphene transfer, (d) graphene encapsulation, (e) graphene patterning, (f) BEOL planarization, (g) damascene contacts to p++ Si, (h) graphene damascene contacts (i) final Cu metal lines.

whereas the damascene process, which includes via-etching, metal filling, and planarization, is typically used to realize contacts in CMOS fabrication facilities. An efficient capping layer is another crucial step that needs to be established using CMOS infrastructure in order to stabilize and protect graphene during further processing. In this section, we concentrate on these three issues and optimize each module to develop a standardized and robust integration flow.

3.1.1 Detailed integration flow

The integration flow started from 300 mm silicon-on-insulator (SOI) wafers with a 220 nm crystalline silicon layer and a 2 μm buried oxide (BOX). Standard 193 nm immersion lithography was used for pattering the silicon waveguides with a nominal width of 500 nm. One side of the waveguide was only partially etched to create a rib structure, allowing for electrical contacting through a 70 nm silicon slab layer. Afterwards, we utilized a standard chemical mechanical polishing (CMP) process, stopping on the SiN hardmask (Figure 3.2(a)), a process also typically used in CMOS fabrication for shallow trench isolation (STI). [174] Before removing the hardmask, we performed an oxide etch-back with diluted HF (Figure 3.2(b)) in an effort to lower the step height induced by the SiN mask removal. However, this approach typically results in a topography of a few nanometers locally at the edge of the waveguides (Figure 3.2(c)). As graphene is a monolayer material, it is highly susceptible to its environment, and a few nanometers of step-height can already affect its properties and eventually device uniformity and yield across a 300 mm wafer. Therefore, we examined the impact of an extra CMP step designed to minimize the topography of the wafer prior to wafer-scale graphene transfer. After the hardmask removal, an additional oxide layer was deposited using a PECVD process on some wafers (Figure 3.2(d)), followed by an extra CMP step stopping selectively on the Si waveguide (Figure 3.2(e)).

In Figure 3.2(f), step height measurements at the silicon-oxide transition area show median values of 3.06 nm and 0.41 nm for the standard STI process and the process with the extra CMP step, respectively, confirming an improvement of surface flatness. The improved flatness of the wafer surface can also be observed from the cross-sectional transmission electron microscope (XTEM) images shown in Figure 3.2(g) and (h). These images were taken after the full device fabrication. As indicated by the arrows in Figure 3.2(g) and (h), the wafer with the additional CMP module has a more uniform and smooth oxide surface, especially near the waveguide edge. In contrast, the wafer with the conventional CMP module exhibits a discernible step at the side of the waveguide and a greater variation in the gate oxide thickness, which could result in larger strain in the graphene layer and a non-uniform electric field. This will be elaborated further when discussing the results of

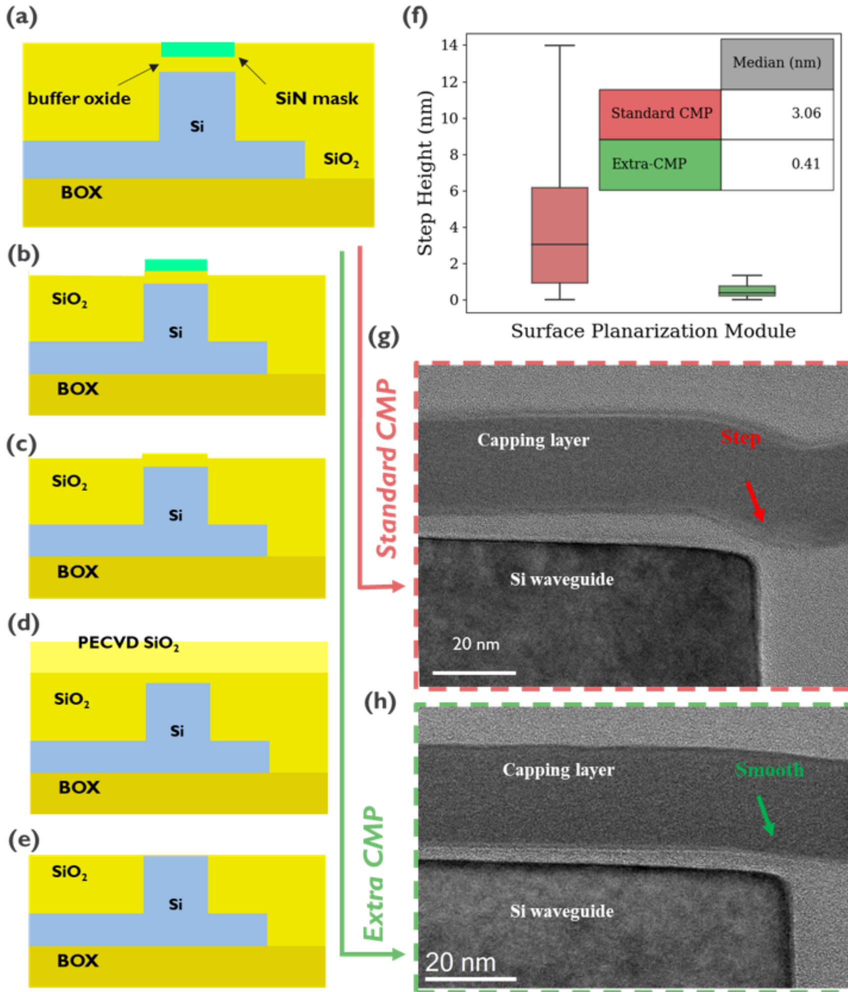

Figure 3.2: Detailed CMP processes. (a) Surface planarization by standard CMP, (b) oxide etch-back, (c) SiN mask removal, (d) thick PECVD SiO_2 deposition, (e) extra CMP stopping selectively on Si waveguide. (f) Comparison of the step height remaining after surface planarization. Within 170 measured devices, the mean and standard deviation values of the step height are 4.3 ± 4.1 and 0.5 ± 0.3 nm for the standard CMP process and the process with the extra CMP step, respectively. Cross-TEM images taken at the waveguide edge for wafer with (g) standard CMP and (h) extra-CMP module. The standard planarization process results in a considerably higher remaining step and non-uniform gate oxide thickness.

Raman measurements and the electro-optical performance in the following sections.

Next, a 5 nm gate oxide was thermally grown on top of the waveguides. Three

implantation steps were carried out, to minimize the contact and sheet resistance of the Si layers, without considerably increasing the optical loss in the waveguides. Then, a commercial company, Graphenea, grew a 6-inch graphene layer by chemical vapor deposition (CVD) and transferred it to the middle of a 300-mm wafer using a semi-dry technique as shown in Figure 3.3(a). In this process, the graphene layer on its copper catalyst is attached to a polymer substrate, which allows to etch the copper catalyst away using a standard $FeCl_3$ wet etching method. After the etching, several consecutive ultra-pure DI water and acidic rinses were used to minimize Fe contamination. Graphene interface was then dried with N_2 flow. When the graphene layer was dry, a dry lamination method was used to transfer the graphene onto the target wafers. The polymers/Graphene was laminated at a pressure above 1 bar and a temperature of 150°C for the transfer. Finally, the remaining protective polymer layer is removed by a wet solvent process.

Given graphene's self-passivated properties [175–177], it is difficult to directly deposit a dielectric on its surface. Commonly, a seeding layer is used to achieve homogeneous oxide deposition. Here we used a low-temperature surface physisorption based 'soak' method with tri-methylaluminium (TMA) as the precursor to carefully deposit a dielectric seeding layer. The actual Al_2O_3 capping layer was then deposited using an atomic layer deposition (ALD) process. To investigate the impact of the capping layer uniformity on the performance of the final devices, a second study was defined at this stage, whereby the soaking time was varied. Figure 3.3(c) shows a top-down scanning electron microscope (SEM) image after the plasma-enhanced atomic layer deposition (PEALD) deposition when a short soaking time was used. This image shows a large number of distinct voids in the Al_2O_3 layer. These voids could potentially lead to unintentional etching of the graphene layer during subsequent processing steps. Figure 3.3(d), where a longer soaking time was applied, exhibits superior Al_2O_3 coverage of graphene, and the number of voids is significantly reduced. Only a few wrinkles generated during graphene growth and transfer remain visible. Overall, by optimizing the coverage of the capping layer, we expect to reduce the impact of later integration steps on the graphene layer achieving better device yield.

After deposition of the Al_2O_3 layer, a SiO_2 layer is deposited, also using a PEALD process, which is then patterned using DUV lithography and dry etching. Following resist strip, the oxide layer is used as a hardmask to pattern the Al_2O_3 and graphene stack. Careful control of these steps is critical to avoid etching into the underlying silicon waveguides and is made possible through the use of high-end tools typical for a CMOS foundry. After graphene patterning, a pre-metal dielectric (PMD) is deposited and planarized by CMP, following a standard CMOS flow. Finally, the contacts to both the graphene and the doped silicon layers are defined. The

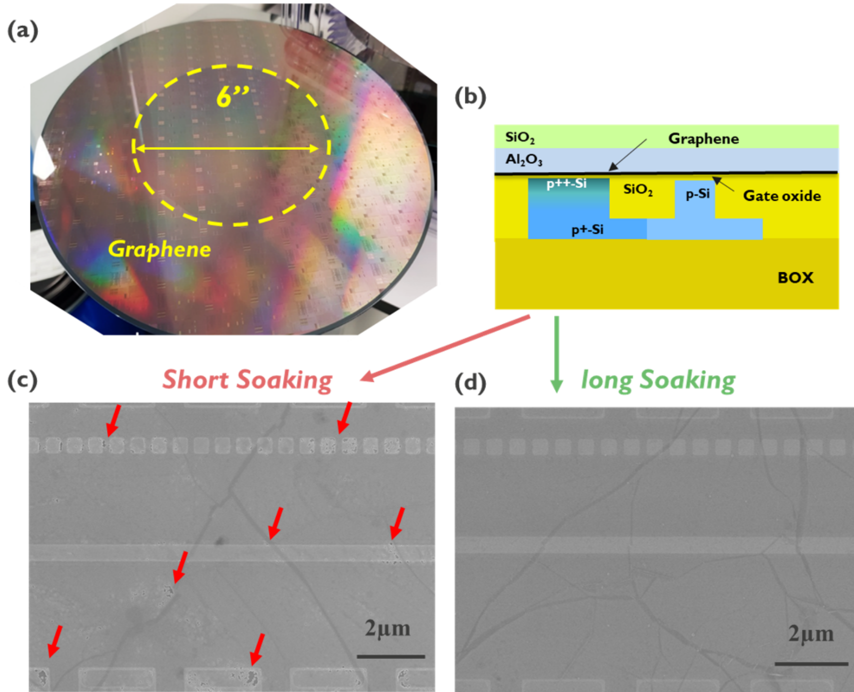

Figure 3.3: Impact of soaking time. (a) Top-down image of 300 mm wafer with 6-inch graphene transferred at the center. Representative top-down SEM image of wafer with (b) short and (c) long soaking time. Red arrows indicate the voids on top of the surface. The wrinkles in the graphene layer also visible in the pictures are induced during graphene growth and transfer.

latter are fabricated first, by etching contact holes using reactive ion etching (RIE), which are then filled using a CMOS Ti/TiN/W damascene metallization process. A similar damascene process was used for contacting the graphene layer. This is very different from most other work reported in literature, where typically a liftoff process is used to define top-contacts on graphene [24, 161]. Although this provides a low-cost and simple method for contact fabrication, it is not compatible with industrial CMOS process flows, where damascene processes are preferred as they offer higher yield and uniformity.

As selectively stopping the via etching process directly on top of the graphene layer would be very challenging, we choose to over-etch the oxide layer and create edge contacts. Recent reports indicate that such an edge contact could offer lower contact resistance [178, 179]. The contact holes of 250nm diameter were patterned using DUV lithography and transferred in the PMD oxide by dry etching, selectively stopping on the Al_2O_3 capping layer. This step was then followed by resist stripping, and etching of the Al_2O_3 and graphene layers, stopping in the underlying SiO_2 layer. Etching of graphene creates fresh dangling bonds, which can form strong covalent bonding with the metal [180, 181] that is subsequently deposited. However, with increasing the time elapse between the etching and metal deposition steps, these dangling bonds could bind with atmospheric water and oxygen and be passivated, hindering the formation of good contacts and increasing the resistance. The latter is detrimental for the high-speed response of the devices, as they are RC-limited. To study this effect in more detail, we kept this time-delay as short as possible for all wafers, except for one, for which we introduced an intentional gap of two days between the two steps, as illustrated in Figure 3.4(a) and (b). Finally, the integration flow was completed with a conventional Cu-oxide metal-1 module.

The final crosssection of the device is shown in Figure 3.4(c). In this TEM image, the graphene layer is located below the Al_2O_3 capping layer. Notably, despite the fact that 6-inch graphene currently limits the number of available dies, the CMOS-compatible modules developed in this work provide a 300 mm platform to scale up graphene-based photonics devices. Table 3.1 summarizes the complete design of experiment (DoE) defined to study the effect of planarization, soaking time and contact module optimization. The results from four wafers with this DoE, labelled wafers A, B, C, D, will be discussed in the following sections.

3.1.2 Raman Characterization

Before any electro-optical measurement, the graphene quality was checked by Raman Spectroscopy. Figure 3.5 summarizes the most relevant results, focusing

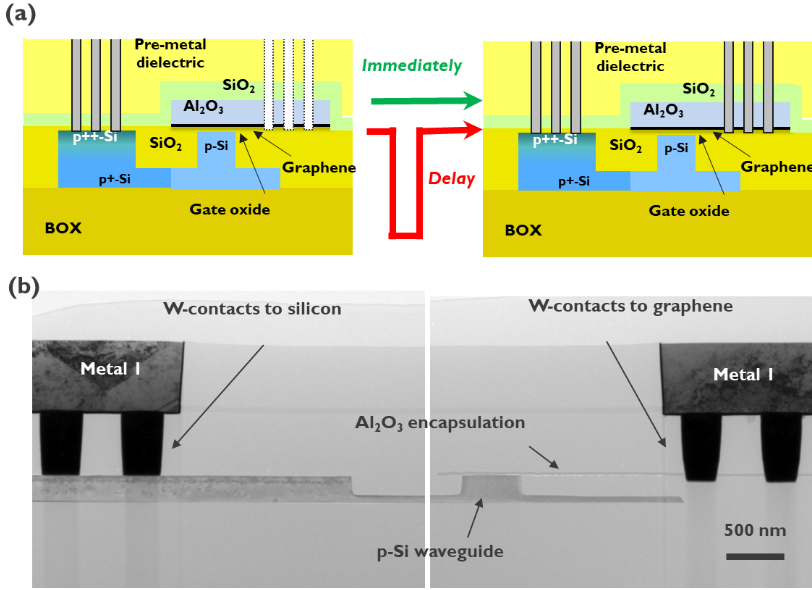

Figure 3.4: (a) Cross-section device scheme and description of the study on graphene contact. (b) Cross-section TEM of final device.

Table 3.1: DOE summary of four wafers reported in this section.

DOE	Wafer A	Wafer B	Wafer C	Wafer D
Surface planarization	Standard STI	Standard STI	Extra CMP	Extra CMP
Encapsulation soaking	Short	Long	Long	Long
Contact metal deposition	No delay	No delay	2 days delay	No delay

on the effect of the extra planarization step by comparing wafer B (standard CMP) and wafer D (extra CMP). The measurements were carried out after completion of the full process flow, through the dielectric stacks of the metal-1 and PMD modules as shown by Figure 3.5(a). From Figure 3.5(b), the defect peak (D) is negligible for both wafers, confirming the proposed integration process does not result in significant degradation of the graphene quality. After fitting the G and 2D peaks of spectra taken at different locations within the wafer with a single Lorentzian, their relative position is mapped in Figure 3.5(c) and (d). The black and red lines with slope of 2.745 [182], and 0.722 [183], represent the effect of biaxial strain and doping respectively. The results indicate that the doping level of graphene varies from 6 to 10 × 10^{12} cm^{-2} after the integration process. Wafer B suffers from more tensile strain effects (up to 0.14%) compared to Wafer D (up to 0.07%). Both wafers exhibit a similar amount of compressive strain, which could be explained by the deposition of the Al_2O_3 capping layer [184, 185]. Figure 3.5(d) shows the full width at half-maximum (FWHM) of the 2D peak, with median values of 40 and 35 cm^{-2} for Wafers B and D, respectively. These results verify that the smoother surface provided by introducing the extra CMP step is reducing strain effects and better preserves the quality of the graphene layer. [186]

3.1.3 EO Static performance of inline EAMs

The EAMs are designed for operation in the C-band with transverse electric (TE) polarization and coupled to an external laser source via grating couplers as shown in Figure 3.6. In order to highlight the broadband nature of graphene, the wavelength was swept from 1530 nm to 1580 nm, for devices with four distinct device lengths. This wavelength range is restricted by the response of the grating couplers. The inset of Figure 3.7(a) depicts a representative transmission spectrum for all device lengths considered. By comparing with a neighboring straight waveguide without modulator, the loss from the grating coupler can be excluded and the wavelength dependent insertion loss (IL) can be determined. Figure 3.7(a) summarizes the IL for the unbiased devices measured across 17 dies of wafer D. The solid line represents the median value, while the band reflects the 25th to 75th percentiles for each active length. Next, we defined the normalized IL by comparing the peak transmission values of each curve and dividing by device length to capture the wafer-to-wafer variation in performance. Figure 3.7(b) shows a histogram of the normalized insertion loss for all 4 wafers. The mean values for wafers A, B, C, and D are 89 ± 7, 85 ± 12, 87 ± 7, and 87 ± 8 dB/mm, respectively. The comparable distribution in all four wafers suggests that graphene is transferred and patterned uniformly in each wafer, despite local variations in CVD graphene quality. Table 2

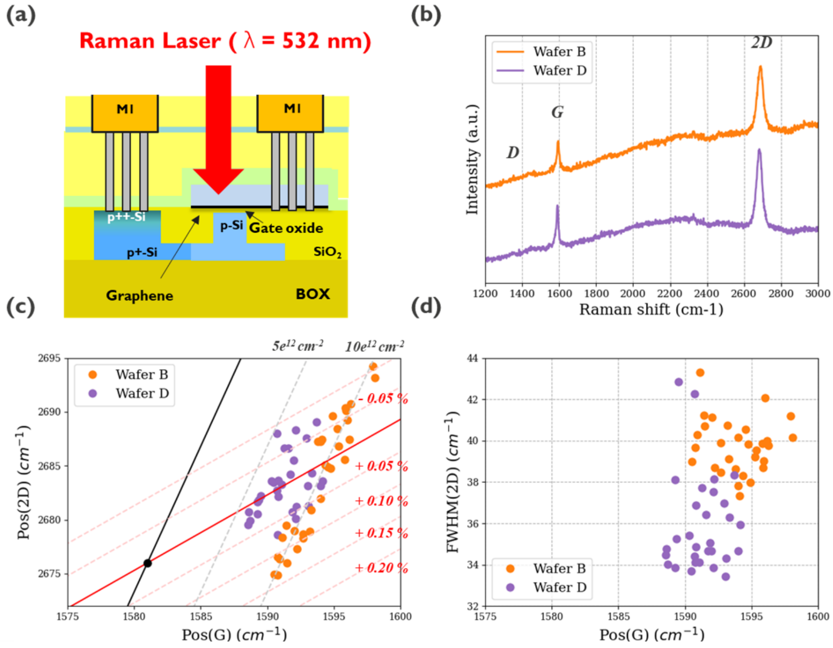

Figure 3.5: (a) Cross-section of the device and Raman measurement. (b) Representative Raman Spectra for Wafers B and D after the full integration process. (c) Position and (d) FWHM of 2D peak as a function of the position of G peak. The black and red lines in Figure 3b are the theoretical trajectories indicating the effect of doping and biaxial strain, respectively. The black dot represents un-strained and un-doped graphene.

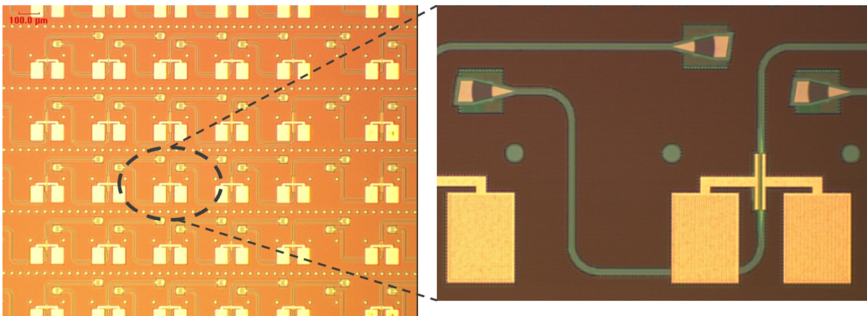

Figure 3.6: Top-down image of SLG EAM devices after in-line fabrication.

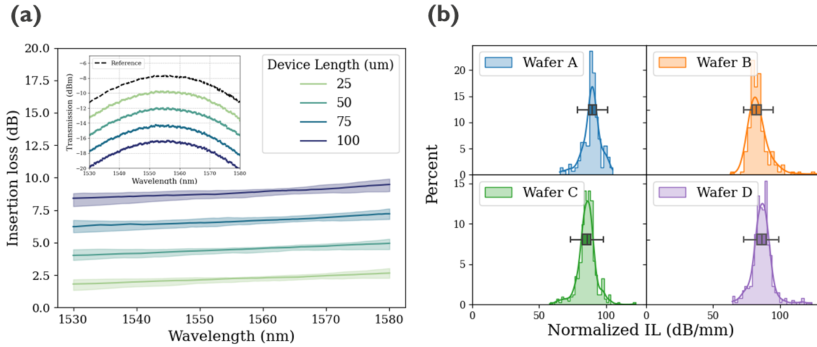

Figure 3.7: (a) Insertion loss of unbiased devices as a function of wavelength for 25, 50, 75, and 100µm-long devices in Wafer D. The solid lines indicate the median value while the shaded areas show the 25-75 percentile. The inset shows representative transmission spectra of unbiased devices with different length. (b) Histogram of normalized insertion loss in an unbiased condition for all four wafers.

provides a summary of the loss measurement data.

To evaluate the electro-optical (EO) response, a DC bias is then supplied to the devices. Figure 3.8(a) shows a typical transmission response curve, measured at 1550 nm wavelength and normalized with respect to a straight waveguide. The red line represents the median value obtained from four hundred 75 µm-long devices measured on wafer D, whereas the black lines are simulation results generated by a commercial solver ($Lumerical$) using three different graphene scattering rates. In the simulation, we set the doping level of the silicon waveguide and graphene layer at 1.5e18 cm^{-3} and 1e13 cm^{-2} , respectively. We noticed that the curves generated by the simulation need a 1 dB downward shift in transmission and a -1.5 V shift in voltage to match well with the experimental results. The voltage adjustment can be explained by fixed charges inside the gate oxide, while the additional loss could originate from residues remaining after graphene transfer. The minimum transmission occurs at a negative voltage, indicating p-type doping of graphene. Figure 3.8(b) shows the wavelength dependent extinction ratio (ER), for a 6V peak-to-peak drive voltage. The solid line and shaded range indicate the median and 5-95 percentile for each of Wafer D's four different active lengths. We clearly observe that the EO response is consistently broadband and that the ER scales uniformly with device length, resulting in median values of 1.3, 2.5, 3.8, and 5.0 dB for 25, 50, 75, and 100 µm-long devices, respectively, at 1550 nm wavelength.

To compare the DC performance between wafers, the modulation depth (MD), defined as the ER normalized by the active length, is calculated. The difference in

performance and uniformity between the wafers is visualized by the cumulative distribution function (CDF) shown in Figure 3.8(c). The mean and standard deviation values of the MD are 32 ± 13, 39 ± 4, 49 ± 2, and 50 ± 4 dB/mm for Wafers A, B, C, and D, respectively. The CDF curves in Figure 3.8(c) lead to three conclusions:
(1) Despite the fact that the maximum MD of Wafer A and Wafer B are comparable, Wafer B has substantially lower variability. We ascribe this enhancement to the improved coverage of the capping layer, which minimizes the impact of following graphene integration processes. Here, a functioning device is defined as one whose MD is greater than fifty percent of the maximum MD demonstrated on the same wafer. Overall, a longer soaking time and the resulting more uniform capping layer increased device yield by more than 20 percent and decreased the within-wafer standard deviation of MD.
(2) Comparing wafer B (standard CMP) and wafers C and D (extra CMP) shows that the improved planarization boosts the modulation depth by 25%. As indicated previously when discussing the Raman results, the smoother surface of wafers C and D reduces strain effects and better preserves graphene material quality, resulting in a larger ER within the same voltage range. In addition, the homogeneous gate oxide can provide a constant electric field and uniform tuning of the graphene fermi level resulting in a steeper modulation response.
(3) Finally, comparing wafers C and D, we can conclude that the DC performance is unaffected by the time delay introduced in the contact module, since both wafers exhibit a nearly identical CDF.

Figure 3.8(d) depicts a wafer mapping of the modulation depth MD, with black dashed circles indicating the area where graphene was transferred. We measured devices on dies within a circular area with 75mm radius from the center of the wafer. Both wafers C and D exhibit excellent uniformity across 17 dies and 400 tested devices. On average, a modulation depth MD = 50 dB/mm is recorded, which is comparable to lab-based champion devices employing similar CVD graphene [24]. Wafers A and B on the other hand clearly exhibit less good uniformity and performance, which we attribute to the lower quality of graphene capping and planarization as discussed before. Table 3.1 summarizes the results for extinction ratio and modulation response for all 4 wafers.

3.1.4 EO Dynamic performance of inline EAMs

We performed S-parameter measurements to assess the frequency response of the devices. An RF small-signal ranging from 100 MHz to 30 GHz was applied to the graphene modulators. A DC bias of 1 V is selected to ensure modulation at the slope of the transmission curve. Figure 3.9(a) shows a representative result for

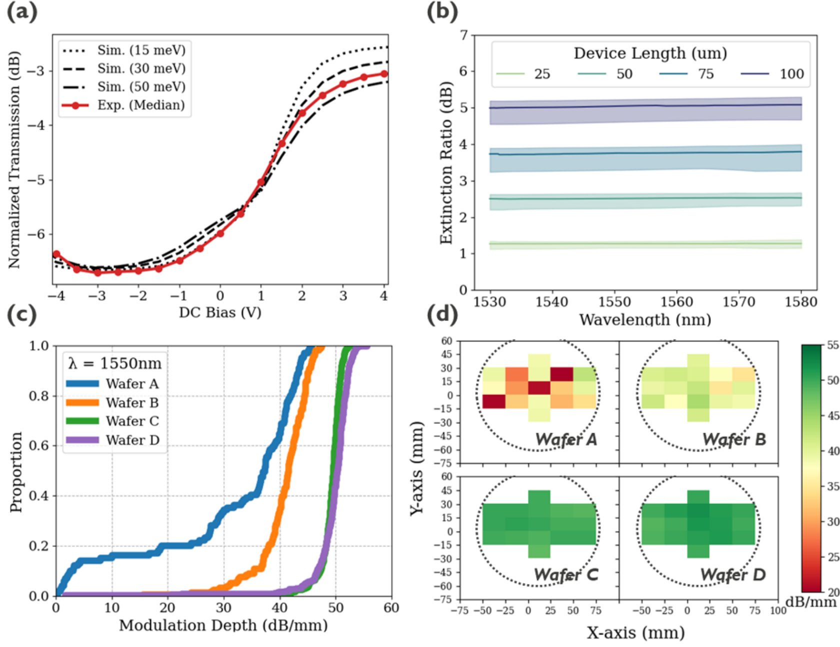

Figure 3.8: (a) Normalized transmission of 75 μm-long devices of wafer D as a function of applied bias. Red solid line shows the median value of experimental results for 400 devices, black dashed lines represent simulation results for 3 different scattering rates. (b) Extinction ratio as a function of wavelength for 25, 50, 75, and 100μm-long devices (Wafer D). The solid lines represent the median value while the shaded areas show the 5-95 percentile of the results. (c) Cumulative distribution function and (d) wafer mapping of modulation depth at 1550nm wavelength for all four wafers.

Table 3.2: Summary of the static performance for all four wafers with four different active lengths. The unit of IL(ER) and normalized IL (modulation depth) are dB and dB/mm respectively. IL is measured and calculated under an unbiased condition.

Wafer	IL-25μm	IL-50μm	IL-75μm	IL-100μm	Normalized IL	Observed devices
A	2.2 ± 0.2	4.4 ± 0.3	6.6 ± 0.3	8.8 ± 0.2	89 ± 7	144
B	2.4 ± 1.1	4.2 ± 0.5	6.3 ± 1.4	8.1 ± 0.5	85 ± 12	155
C	2.0 ± 0.7	4.1 ± 0.5	6.3 ± 0.5	8.5 ± 0.5	87 ± 7	408
D	2.1 ± 0.4	4.4 ± 0.7	6.8 ± 1.5	8.8 ± 1.7	87 ± 8	400
Wafer	ER-25μm	ER-50μm	ER-75μm	ER-100μm	MD	Observed devices
A	0.9 ± 0.3	1.6 ± 0.7	2.0 ± 1.1	2.9 ± 1.6	31 ± 14	100
B	1.0 ± 0.2	2.0 ± 0.2	3.1 ± 0.3	4.1 ± 0.4	41 ± 5	155
C	1.2 ± 0.1	2.5 ± 0.1	3.7 ± 0.2	4.9 ± 0.1	49 ± 2	408
D	1.2 ± 0.2	2.5 ± 0.1	3.7 ± 0.3	5.0 ± 0.2	50 ± 4	400

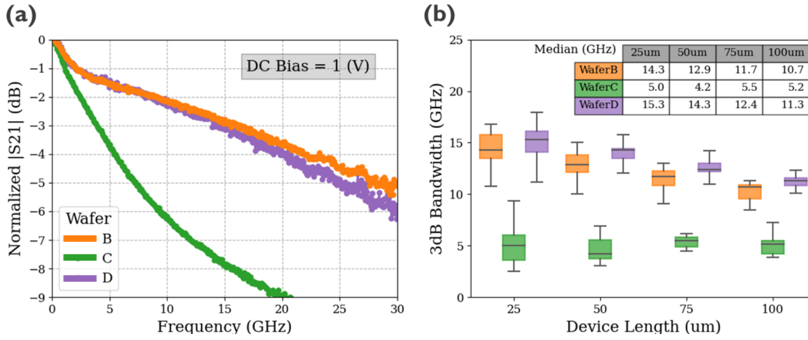

Figure 3.9: (a) Representative S21 response and (b) box plots of extracted EO bandwidth for wafers B, C and D at DC bias of 1V. Inserted table gives the median value for each device length and each wafer.

a 25-µm long device of wafers B, C and D. The 3dB-bandwidth for the wafer C device is 3.8 GHz, evidently much lower than for the other two devices (15.3 and 16.1 GHz for wafer B and D respectively). Figure 3.9(b) shows the statistics for all devices measured. These reveal that wafer C, for which a delay was introduced between the contact etch and metallization process, has consistently a lower EO bandwidth than the other two wafers, for all four device lengths. It suggests that the time-delay during fabrication hinders good bonding between metal and graphene resulting in a higher contact resistance. This will be discussed further in the next section. For wafer D, median values of 15.3, 14.3, 12.4, and 11.3 GHz are measured for 25, 50, 75, and 100-µm long devices respectively, comparable with lab-based hero devices with similar design and graphene quality. To understand this length dependence better and get more insight on these devices, we further analyzed the S11 response for wafer B and C devices.

Since the dynamic response of our graphene modulator is primarily limited by the electrical RC constant [24], we continue our analysis by fitting the S11 response to the equivalent circuit model shown in the inset of Figure 3.10(a). The graphene-oxide-silicon (GOS) structure can be considered as a lumped device with a capacitance C_{gos}. The total resistance R_{gos} of the device includes both contact and sheet resistance of silicon and graphene. R_{si}, C_{ox}, and C_m are parasitic components, representing resistance of the substrate, capacitance of the buried oxide layer and capacitance of the metal pad, respectively.

Figure 3.10(a) shows the S11 response for a 25-µm long device of wafer D, along with the result of the fitting process. From these, the total resistance R_{gos}, and capacitance C_{gos} can be determined. Figure 3.10(b) summarizes the extracted device capacitance for Wafer D, which served as the basis for this analysis. As

Table 3.3: Summary of the outcomes from S-parameter for Wafer D with four different active lengths.

S-parameter outcomes	Unit	$25\mu m$	$50\mu m$	$75\mu m$	$100\mu m$
Measured EO BW	GHz	15.1 ± 1.8	14.1 ± 1.4	12.6 ± 0.9	11.2 ± 0.7
Fitting result: C_{gos}	fF	26.7 ± 1.5	62.1 ± 3.7	102.8 ± 4.7	139.2 ± 7.9
Fitting result: R_{gos}	Ω	280 ± 61	86 ± 18	49 ± 6	38 ± 4
Intrinsic BW	GHz	22.0 ± 3.1	30.6 ± 4.0	32.2 ± 0.4	30.5 ± 2.6
Intrinsic + Driver	GHz	18.5 ± 2.2	19.0 ± 1.3	15.8 ± 0.3	13.1 ± 0.8
Final estimated BW	GHz	16.8 ± 2.0	17.2 ± 1.2	14.5 ± 0.4	12.2 ± 0.7
Observed devices		29	29	32	28

anticipated, C_{gos} scales linearly with device length, resulting in wafer median values of 27, 62, 104, and 140 fF for devices that are 25, 50, 75, and 100 µm long, respectively. When evaluating Wafer C, the range of the capacitance was given to match the results obtained from Wafer D. This allowed to have reasonable value and prevent unrealistic outcomes. Figure 3.10(c) shows a wafer median value for the resistance R_{GOS} of 711, 271, 146 Ω for Wafer C and 263, 84, 47 Ω for Wafer D, for 25, 50, 75-µm long devices, respectively. The smaller resistance in Wafer D confirms that the limited time between oxide etch and metal deposition better preserves the graphene contact quality, resulting in larger EO bandwidth.

Lastly, we recalculated the electrical bandwidth of the devices based on the fitting results. Wafer D's intrinsic RC bandwidth, considering only R_{gos} and C_{gos}, attains wafer median values of 22, 31, 32, and 30 GHz, respectively, for devices measuring 25, 50, 75, and 100 µm in length. However, when the 50 Ω load resistance from the vector network analyzer (VNA) is considered, the calculated values (BW) are reduced to 19, 19, 16 and 13 GHz. These values are close to the final calculation, which takes into account all other parasitic components (C_{ox} and R_{si}). Figure 3.10(d) summarizes the calculation for the 75-µm long device, showing the intrinsic 3dB-bandwidth (1/2π $R_{gos}C_{gos}$) extracted from S11-measurements, the effect of the 50 Ohm load resistance, the effect of the parasitics and finally the measured electro-optical 3dB bandwidth. Table 3.3 provides information for the other lengths. In general, the final electrical BW derived from the S11 data is close to our experimentally measured EO BW, demonstrating the accuracy of our equivalent circuit model.

Following the discussion above, the EO bandwidth of our SLG EAM devices is mainly limited by the RC constant. Reducing the capacitance and resistance of the devices is key towards realizing a high-speed EAM. In recent work, large-area single-crystal graphene with 7.3 × 10^3 $cm^{-2}V^{-1}s^{-1}$ mobility [93] and extraordinarily low contact resistance (23 Ω at room temperature) using a Ti-graphene edge contact configuration [178] has been demonstrated, which would allow for

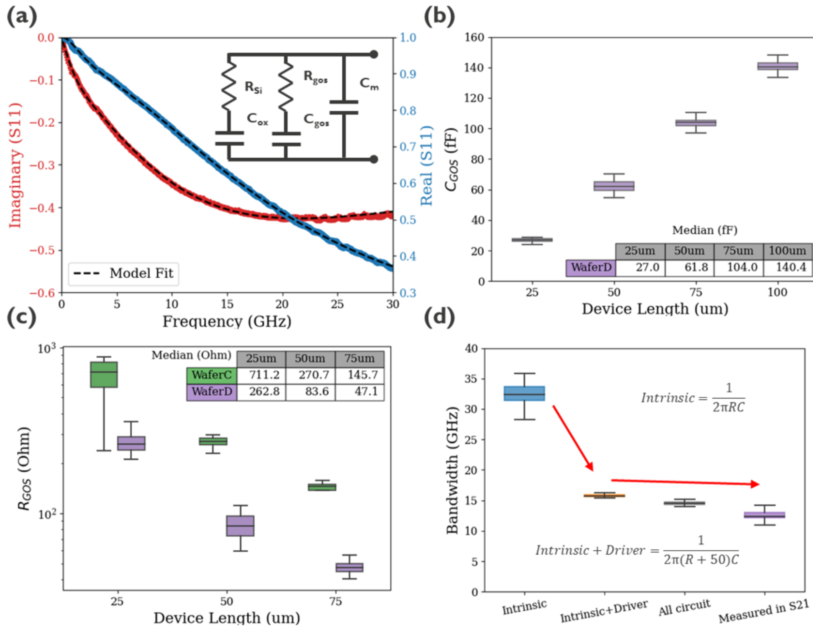

Figure 3.10: (a) Representative S11 response and fitting results. The inset shows the equivalent circuit model of our structure, where R_{Si}, C_{ox}, R_{gos}, C_{gos} and C_m represent silicon resistance, oxide capacitance, GOS resistance, GOS capacitance and metal capacitance, respectively. (b) Box plots of extracted GOS capacitance C_{gos} for wafer D. (c) Box plot of extracted GOS resistance R_{gos} for 25, 50, and 75-µm long devices in Wafer C and D. R^2 values for the fit were larger than 0.9 and 0.98, respectively. The table in the inset shows the median values. (d) Bandwidth estimated from the fitting results, and bandwidth measured from S21 for Wafer D. The equations used to calculate these values are shown inside the figure.

devices with lower sheet and contact resistance in the future. Capacitance reduction, on the other hand, is not as straightforward. As discussed in Chapter 2, reducing the capacitor surface or increasing the equivalent oxide thickness (EOT) of the gate oxide will both result in a lower capacitance but lead to a trade-off between bandwidth, modulation efficiency and drive voltage. Modulation efficiency and speed should be balanced for modulators driven at CMOS-compatible voltages (below 2 V for conventional CMOS circuitry).

A possible solution to this conundrum is to enhance the mode interaction with graphene. As modelled in Chapter 2, the efficiency of graphene-based modulators can be substantially improved, resulting in larger ER and IL. This enhancement is achieved through the strategic use of slot waveguides and/or a double-layer structure. Implementing the first solution is straightforward within our proposed integration approach. By designing and patterning a waveguide with dimensions tailored to support the mode, the interaction of light with graphene can be significantly enhanced. On the other hand, the second solution, involving a double-layer structure, demands more meticulous attention. It necessitates the application of a high-quality oxide with uniform thickness on top of the first layer of graphene before transferring the second layer. Additionally, the graphene patterning process must be optimized to ensure that the first layer remains intact during the patterning of the second layer.

Our high-yield wafer-scale integration method positions itself as an ideal platform for systematically addressing these challenges and exploring potential device architectures. Furthermore, CMOS-compatible processing enables co-integration of graphene-based devices with other photonics and electronics building blocks on the same chip, and for high-volume low-cost manufacturing.

3.1.5 Measurement-dependent behavior

In addition to the EO characterization described in the preceding section, we observe a measurement-dependent behavior (MDB) in our devices. It was initially discovered in DC measurements, specifically when various voltage sweeping directions are made, as shown in Figure 3.11. First, a “fresh” 100-μm device on Wafer D that had not been previously measured was chosen at random. In order to demonstrate the MDB effect, we then conduct three measurements with voltage sources at the graphene contact and the ground at the silicon contact. In measurement 1 (M1), the voltage is swept twice between 0 and -4 V, and the transmission vs. bias curves in both sweeps (S1 and S2) are found to be identical, as shown in Figure 3.11(a). It suggests that a good encapsulation layer was fabricated, thereby limiting the hysteresis effect typically observed in the literature [187–189].

However, MDB occurs during measurement 2 (M2), when the DC bias increases

from 0 V to 4 V and then returns to 0V. As demonstrated by M2-S1 in Figure 3.11(b), the forward and reverse voltage sweeps result in different transmission-bias curve slopes after the DC bias reaches 4 V. The entire curve appears to be shifted to the left, and the transmission at 0 V becomes less absorptive after the voltage sweep. In order to verify the repeatability, the second set of M2 is performed immediately, and the result of forward and backward is only identical to the backward curve in M2-S1 (Figure 3.11(c)). It suggests that the entire device has been altered following the M2-S1 measurement and cannot be restored to its original state.

Last, measurement 3 (M3) was performed with the same voltage sweep as M1 to compare the transmission-bias curve before and after M2. As shown in Figure 3.11(d), the result of M3 is completely different from that of M1, despite the fact that their respective M3-S1 and M3-S2 are identical. The uniform encapsulation layer provides excellent graphene passivation, thereby preventing the hysteresis effect in SLG EAMs. Nevertheless, when a large positive DC bias (>3.5 V in our case) is applied, the EO behavior changes. The applied voltage can be regarded as the position of graphene Fermi level. When a positive voltage is applied, the Fermi level moves along the valence band. In other words, the MDB only occurs when the graphene fermi-level has shifted to a lower level in the valence band. It indicates that charge traps may exist at this energy level, altering device performance after being charged/discharged. Thanks to the high device yield and uniformity, we could confirm that this effect is repeatable, for devices measured across the whole wafer.

Changes in the device's behavior can also be detected with a capacitance-voltage (CV) measurement, a purely electrical measurement. Typically, we employ it to determine the capacitance of our device. As our capacitor is composed of a graphene-oxide-Si stack, the quantum capacitance (C_q) of graphene must be taken into account [24, 30]. C_q typically has a lower value near the graphene neutrality point and increases symmetrically on both valence and conduction bands [30, 190–192]. A representative CV measurement of our device as function of DC bias is shown in Figure 3.12(a). There are two states (Fresh & After light DC) as well as four measurements.

First, a fresh device is selected and measured twice from -4V to 4 V, as shown in Figure 3.12(a) by the blue and orange curves. As opposed to the smooth transition typically observed in conventional MOS structures, we observe here a distinct dip in the curves, which can be explained by the effect of the graphene quantum capacitance. This is an intriguing discovery since the position of the dip can roughly approximate the neutrality point and doping state of the graphene layer. An additional intriguing observation is that there is no change between the first and second sweeps, even when the DC bias reaches 4V. Since the working environment is dark during the CV measurement, this indicates that no device change has

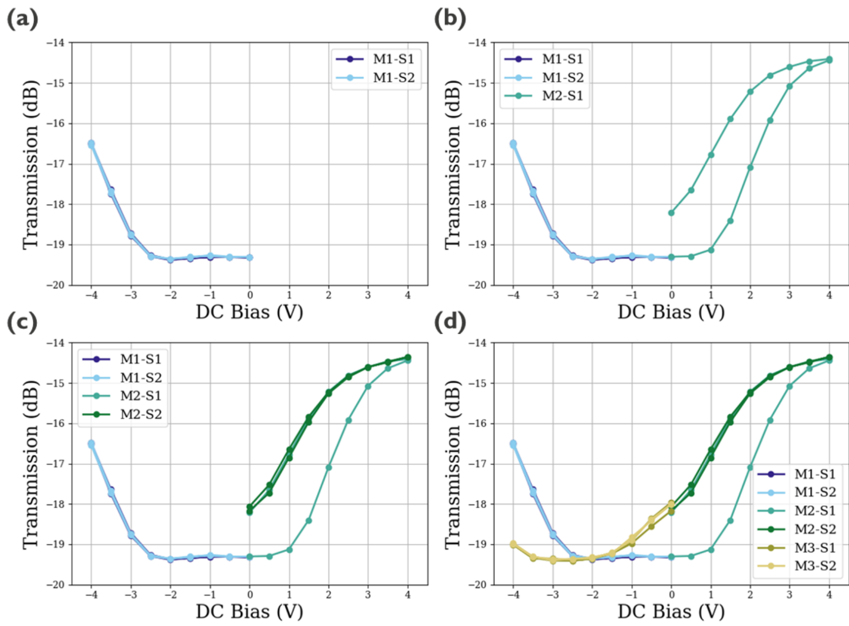

Figure 3.11: EO DC measurement on a fresh device with step-by-step voltage sweeps. (a) Measurement 1 with voltage sweeps from 0V to -4V and back to 0V in two sets. (b) First and (c) second set of measurement 2 with voltage sweep from 0V to 4V and back to 0V. (d) Measurement 3 with voltage sweeps from 0V to -4V and back to 0V in two sets.

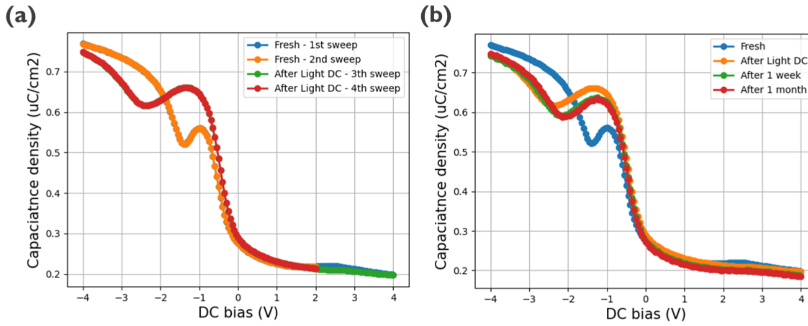

Figure 3.12: Capacitance-voltage measurements on a fresh SLG EAM. (a) Comparison of CV result between fresh and after light DC device. (b) Comparison of CV result between fresh, after light DC, after 1 week and after 1 month storing in the atmosphere. Voltage always sweeps from -4 to 4 V.

occurred after the purely electrical sweep. That is to say, the MDB found in Figure 3.11 can only occur with the assistance of photons, as demonstrated by this new evidence.

Next, we perform the standard EO measurement on the device (as marked by After Light DC) and remeasure the CV value, as depicted in Figure 3.12(a) by the red and green curves. By observing the location of the dip, we can detect a clear shift to the left of the curves, which is similar as what we have observed in Figure 3.11. The absence of a variation between the third and fourth sweeps reaffirms the minimal effect of the pure electrical measurement. To evaluate the relaxation time of those traps, we remeasured the same device and recorded the results in Figure 3.12(a) after 1 week and 1 month. After one week, we can observe that the position of the dip is migrating slightly to the right. However, the improvement is limited after waiting one month. Figure 3.11's CV measurements expand our understanding of the MDB. This impact is photon-induced, and not self-recovering under atmospheric conditions.

We also put these devices through an annealing test at 400 degrees Celsius, and the resulting transmission-bias curves are depicted in Figure 3.13. The MDB is observable after the initial forward sweep. As soon as the DC bias reaches 4 V, all of the measurements remain consistent with the same curve. In annealing tests, only pure Ar is applied in the furnace. Clearly, the device possesses characteristics of a fresh device after the annealing. It suggests that thermal annealing can assist in de-charging and restoring the SLGEAM to its original state, which cannot be accomplished by exposing the sample to the atmosphere for one month. In conclusion, the MDB is an intriguing discovery that only occurs at a particular energy level and with the aid of light. The origin of this effect can be better

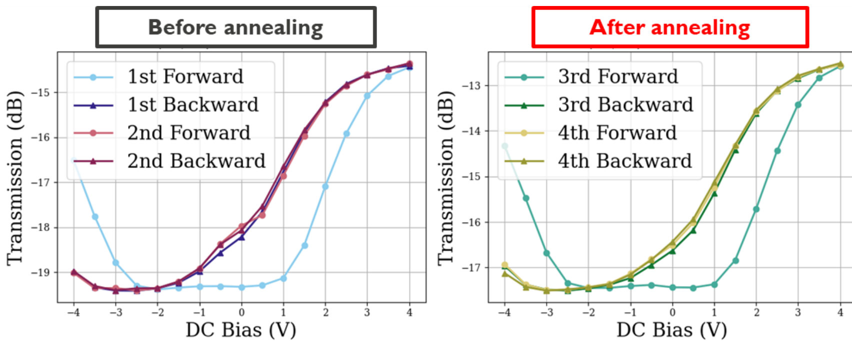

Figure 3.13: Comparison of transmission curves, measured with double voltage sweep from -4 V to 4 V (forward) and immediately sweep from 4 V back to -4 V (backward), between before and after Ar annealing at 400 degrees Celsius.

understood by experimenting with various wavelengths, intensities of power, and temperatures. Ultimately, it may serve as a photon-activated defect monitor for graphene-based devices.

3.2 Phase two study: device improvement based on developed integration

Based on the CMOS integration process introduced in section 3.1, this section explores three approaches for further enhancing device performance. First, we observe an over-etching issue on waveguides after graphene layer patterning. To decrease the loss produced by these broken waveguides, we have optimized these modules with an endpoint detection system based on optical emission spectroscopy. Second, we investigate a different environment around the graphene layer to protect the CVD-grown graphene quality since better graphene quality could enhance both modulation depth and speed. As the soaked encapsulating layer is an essential step, we focus exclusively on the gate oxide beneath. Lastly, 8-inch graphene was manufactured and transferred by the external partner $Graphenea$, followed by the full CMOS integration in imec's pilot fab, as described in section 3.1. With a larger graphene layer, there are more dies and devices available. Moreover, it could extend the confirmation regarding the scalability of the SLG EAM across the entire wafer.

3.2.1 Detailed integration flow for three improvements

In the graphene patterning modules, two etching stages are implemented to prevent graphene layer delamination and the depth of both steps is controlled by etching time. First, the SiO_2 layer deposited by PEALD is etched at a rate of 0.7 nm/s utilizing a chemistry based on CF4:CH2F2. Following the removal of the resist, the residual oxide is utilized as a hardmask to pattern the Al_2O_3 and graphene stack using BCl_3 with, an etching rate of more than 1 nm/s. Ideally, we want to halt etching immediately after graphene etching is complete. This is difficult to accomplish with a conventional time-controlled etching process for an atomic-thick material, which typically results in an over-etch and a depression on the underlying material. In Figure 3.14(a), a recess on the silicon waveguide can be clearly observed. This occurrence is observed in regions without graphene coverage, particularly along the routing waveguides, potentially leading to additional device losses. To address this concern, an optimized etching process is essential. This process should have the precision to halt just before reaching the silicon waveguide consistently across entire wafers.

To make this possible, we implemented an endpoint detection (EPD) system based on optical emission spectroscopy (OES) to stop etching with optimal accuracy and precisely control layer damage at the wafer scale. The plasma generated by the inductively coupled plasma (ICP) source contains molecules, free radicals, and gaseous etching byproducts that are excited and reacted with the material being etched, with the removal of material beginning from the exposed parts of the substrate. By monitoring the change in carbon intensity in the plasma with OES, we are able to identify a transitional point between layers and stop the etching process to limit over-etching. More importantly, as the technique monitors across the plasma above the wafer, it effectively monitors the etching process over the entire wafer. The optimized result is displayed by the TEM picture in Figure 3.14(b). With the help of this new technique, we minimize the over-etch issue and barely observe a recess on the silicon waveguide. It is expected that the improvement is reflected in the loss of the devices, which will be discussed in detail in a later subsection.

The second direction explored in this section is the improvement (or preservation) of the graphene quality. A higher quality graphene can alleviate the trade-off caused by our capacitive structure, while simultaneously improving the modulation efficiency and frequency response of the final devices (see Chapter 2). There are primarily two directions to have a better quality of graphene. The first direction is the optimization of the graphene growth and transfer processes. The synthesis of single-crystal, wafer-scale CVD-grown graphene has reached maturity, resulting in graphene with ultra-high intrinsic mobility [93, 193, 194]. In this direction,

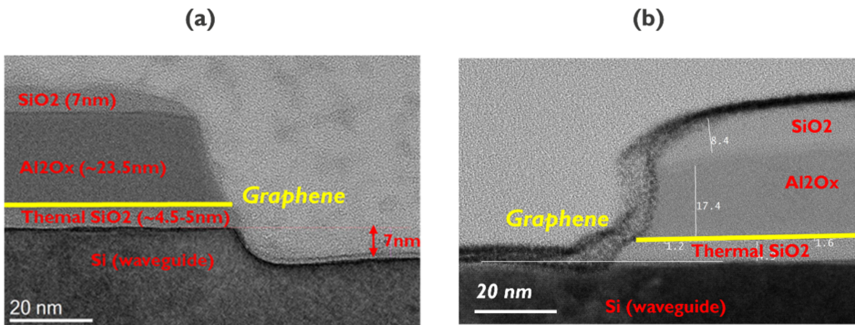

Figure 3.14: Cross-TEM images taken at the waveguide edge for (a) Wafer D with time-controlled etching process and (b) Wafer 3 with EPD implemented. The time-controlled etching process results in a considerably larger recess on silicon waveguide below while EPD-implemented etching process stop etching with better accuracy, limiting the damage on the waveguide.

the challenge is in transferring graphene in a CMOS-compatible environment for wafer-scale devices. Typically, this can be accomplished in either numerous steps using smaller patches to cover the entire wafer [161], or in a single step utilizing wafer-sized graphene layers, as we described in section 3.1 [172]. However, the first method has the potential to leave behind a significant amount of residue throughout multiple transfers, which raises the issue of contamination, while the second way may require a different substrate to grow ultra-high-quality graphene, necessitating a new growing and transferring process. As both transfer methods requires a more comprehensive and efficient strategy, it is outside the scope of this thesis.

In this thesis, we focus on the second direction that is improving the environment around the graphene layer so that its inherent qualities can be better preserved. In suspended single-layer graphene, an electron mobility of 200,000 has been demonstrated at ambient temperature. [195] However, in the majority of graphene-based heterostructures, the SLG is supported on an insulating dielectric substrate, typically SiO_2, which introduces additional scattering sources such as surface roughness, charged impurities [196–198], and remote phonons [199–201], hence reducing mobility. Among these, charged impurities are the most influential [202]. A typical strategy for reducing charged-impurity scattering in thin-film electronics is to use substrates and/or passivation layers with high dielectric constants (k) to screen the Coulomb potential and maintain a low charged-impurity density [203–205]. As a result, we compare the new gate oxide, SiO_2 + Al_2O_3, which embeds graphene in Al_2O_3, to SiO_2 alone as illustrated in Figure 3.15(a). With this sort of gate oxide, we may utilize the same wafer-scale CVD-grown graphene with improved preservation on its quality. More importantly, the change can simply

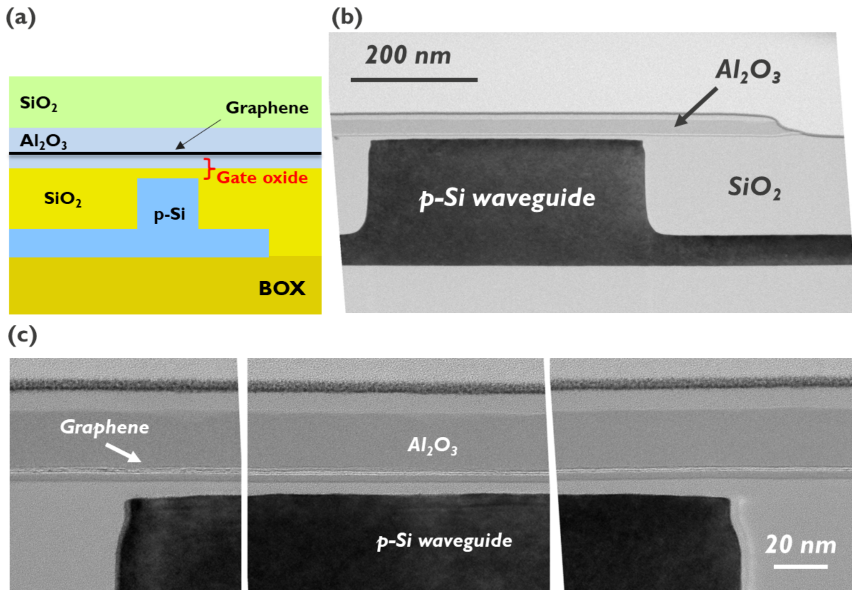

Figure 3.15: Cross-sectional (a) scheme and (b)(c) TEMs of proposed new gate oxide stack.

be implemented during the integration by CMOS infrastructures, reducing the manufacturing complexity. In the experiment, Al_2O_3 with a nominal thickness of 3 nm is grown by ALD following an extra CMP for surface planarization and the growth of 5 nm thermal SiO_2. The TEM images in Figure 3.15 (b) and (c) demonstrate that graphene has been successfully integrated on top of this complex gate oxide stack. In the following part, the EO performance of the devices will be described in depth.

The size of the graphene layer is the final improvement made in this section. In prior research, we were only able to demonstrate working devices in a 6-inch area, which was mostly limited by the transferred size of graphene. Nevertheless, we believe it can be expanded and applied over the entire 12-inch substrate wafer once graphene is synthesized and transferred with a larger wafer scale. This increases the number of dies and devices available. In this part, Graphenea has increased the size of the graphene layer from 6 inches to 8 inches using the same growth and transfer processes described in section 3.1. The graphene growth was performed in a Black Magic Pro 2x8" CVD furnace. An untreated copper foil of 20-25μm thickness with high purity was used as a catalyst. Prior to the actual graphene growth, a 900°C H_2 pre-annealing was carried out. The temperature was subsequently increased to 1,000 degrees Celsius, and methane was injected as a carbon source through a vertically arranged showerhead until the pressure reached 25 millibars. Graphene

Table 3.4: DOE summary of three wafers reported in this section, along with champion wafer (Wafer D) discussed in section 3-2.

DOE	Wafer 1	Wafer 2	Wafer 3	Wafer D
Graphene Size	8 inch	8 inch	6 inch	6 inch
Silicon doping	higher	higher	higher	lower
Graphene patterning	EPD-controlled	EPD-controlled	EPD-controlled	time-controlled
Gate oxide	Al_2O_3 + SiO_2	SiO_2	SiO_2	SiO_2

grown on the foils was taken from the reaction chamber after 30 minutes of growth by removing the methane, purging the chamber, and bringing it to room temperature in Ar.

The malleable Graphene/Cu foil catalyst was covered with a PMMA coating and then laminated with an adhesive carrier polymer to give a more rigid support. For the graphene delamination from the Cu foil catalyst a wet method was used. The catalyst was etched in a wet etching process performed in borosilicate glass tanks using $FeCl_3$ solution as an etchant. Several consecutive ultra-pure DI H_2O and acidic rinses of diluted solutions of Hydrochloric Acid 37%, ULSI grade were used to wash the $FeCl_3$ etchant and minimize the metal traces concentration on the resulting supported graphene monolayer. The graphene interface was then dried with an N_2 flow. When the graphene layer was dry, a dry lamination method was used to transfer the graphene onto the target wafers. The adhesive carrier/P-MMA/Graphene was roll-laminated at a pressure above 1 bar and a temperature of 150°C for the actual transfer. Then, the carrier polymer was removed leaving PMMA/graphene layers behind on the wafer. The PMMA coating was then cleaned from the graphene surface using a wet solvent method in a cleaning tank at room temperature. Figure 3.16 depicts the 8-inch graphene transferred to the photonics substrate before the PMMA removal.

In the following part, we will explore device yield and wafer mapping in further detail. Table 3.4 summarizes the complete DOE defined to study the optimization on graphene patterning, gate oxide and size of graphene layer. Please note that all three wafers in Lot 2 have been treated with extra CMP modules, a long soaking for encapsulation, and no time delay on contact metal deposition, a used for the best wafer (Wafer D) in Lot 1. The results from three wafers in Lot 2, labelled wafers 1, 2, 3, will be discussed in the following sections.

3.2.2 Passive, EO static and EO dynamic performance

First, we perform transmission measurements on optical test structures under unbiased conditions, as illustrated in Figure 3.17(a). These optical test devices are

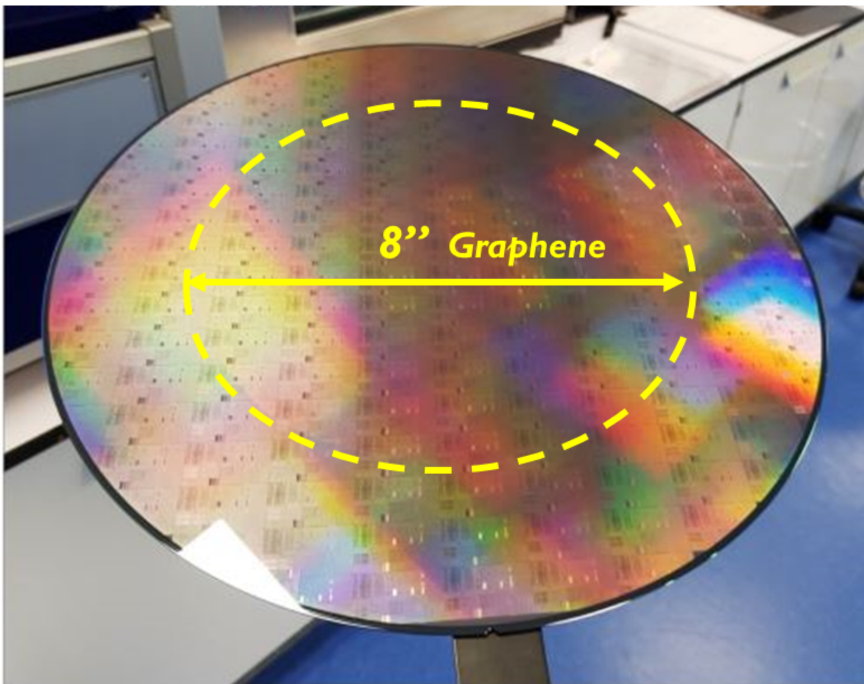

Figure 3.16: Top-down image of 300 mm wafer with 8-inch graphene/PMMA transferred at the center.

Table 3.5: Summary of the propagation loss for SPIRAL structures in all three wafers (Lot 2), along with Wafer D (Lot 1), under three different stages during the integration. The unit of propagation loss is dB/cm.

Strip waveguide	Wafer 1	Wafer 2	Wafer 3	Wafer D
Before graphene transfer and patterning	1.7 ± 1.1	1.4 ± 0.8	1.3 ± 0.4	-
After graphene transfer and patterning	3.4 ± 1.8	4.1 ± 1.2	4.5 ± 1.2	-
After full device integration	4.0 ± 0.8	4.3 ± 0.9	4.0 ± 0.5	7.4 ± 4.4
Socket waveguide	Wafer 1	Wafer 2	Wafer 3	Wafer D
Before graphene transfer and patterning	2.8 ± 0.5	1.5 ± 0.1	1.6 ± 0.1	-
After graphene transfer and patterning	3.4 ± 1.1	3.8 ± 0.9	3.9 ± 1.1	-
After full device integration	3.1 ± 0.4	3.8 ± 0.2	3.8 ± 0.5	9.9 ± 5.7

referred to as ”SPIRAL structures,” and the loss in two types of waveguides (strip and socket) has been studied. The socket waveguide discussed in this paper comprises a strip-like waveguide core with shallow etchings on both sides, serving to confine and guide the optical mode within the core. Frequently utilized in photonic integrated circuits, socket waveguides enable the efficient guidance and manipulation of optical signals with minimal loss. Moreover, they serve as a pivotal waveguide in single-layer graphene EAM structures by providing a rib for silicon contacts. Please note that no graphene layer is designed for this region; hence, the calculated loss is based only on the loss of the waveguides, making SPIRAL structures ideal devices for estimating the impact of the optimization in graphene patterning modules. The details of transmission measurement and characterization can be found in Chapter 2. A representative result is depicted in Figure 3.17 (b), where the length-dependent scaling of loss is clearly observed. As illustrated in Figure 3.17 (c), the propagation loss of the waveguides can be derived by linearly fitting the data points. Identical measurements and characterizations are performed on 14 dies across all wafers, and the statistical loss results of the strip and socket waveguides are depicted in Figure 3.17(d) and (e), respectively, along with the champion wafer (Wafer D) demonstrated in Section 3.1. Before the graphene transfer and patterning in lot 2, the propagation loss of wafers 1, 2, and 3 for strip waveguides is calculated to be 1.7±1.1, 1.4±0.8, and 1.3±0.4 dB/cm, respectively. After optimizing the graphene patterning process, the propagation loss increases to 3.4±1.8, 4.1±1.2, and 4.5±1.2 dB/cm, respectively. Compared to 7.4±4.4 dB/cm in Wafer D, we confirm that wafers with improved graphene patterning modules allow for a superior loss performance. It is attributed to superior control over stopping the etching process, which reduces waveguide damage and, consequently, the sidewall effect [206,207]. The same conclusion holds for the socket waveguides, as depicted in Figure 3.17 (e). The results of Figure 3.17 (d) and (e) are summarized in Table 3.5.

Next, the standard EO DC characterization is carried out. A representative result is

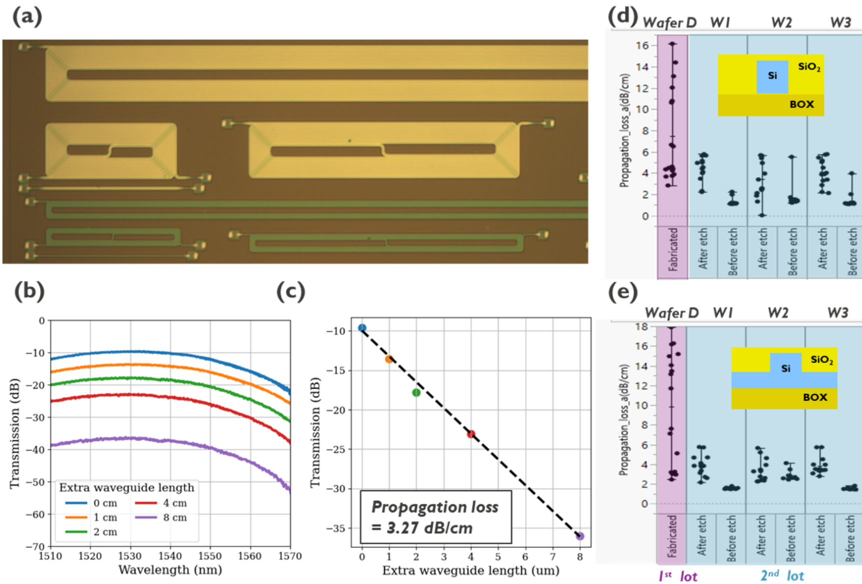

Figure 3.17: (a) Top-down image of strip-based and socket-based SPIRAL structures. (b)Representative transmission spectra of strip-based SPIRAL structures with different lengths. (c) At 1530 nm, extracted and fitted data of transmission as a function of graphene length. The slope represent the propagation loss of the strip-based SPIRAL structures. Box plot of calculated propagation loss for (d) strip-based and (e) socket-based SPIRAL structures. Two lots and total four wafers are discussed an compared here. Please note that there is no graphene designed and fabricated on SPIRAL structures.

shown in Figure 3.18 (a). Initially, the same voltage range (-4 to 4 V) is applied to all the devices in Lot 2, and it is observed that devices of Wafers 2 and 3 fail to reach the graphene transparent region. Instead, they are at the maximum transition slope when a DC bias of 4V is applied, suggesting that a higher positive voltage is required to achieve full Pauli Blocking of the graphene layer. As for Lot 2 - Wafer 1, devices act differently from the other two wafers, which begins the transition at 0 V. These findings may have been caused by a number of variables, including the neutrality point (NP) of graphene layer, oxide thickness, and fixed oxide carrier concentration. Additional research is required to adequately explain the observation. In order to validate the optimization implemented in Lot 2, we increase the voltage applied to extract the majority of modulation for all three wafers and compare the performance with the champion wafer (Lot 1 -Wafer D).

Figure 3.18 (a) and (b) reveal that Wafer 1 exhibits an enormous insertion loss (IL), which is not observed in SPIRAL structures on the same wafer. This finding was unexpected and is currently being investigated. However, given that we can still modulate graphene's absorption and that the ER (and modulation depth) are comparable to those of the other two wafers as shown in Figure 3.18 (c) and (d), we believe the loss likely originates from the structure itself rather than the graphene layer. Possible reason for the high insertion loss is that the graphene layer is not fully etched, leaving a portion of the layer on the routing waveguide and/or grating couplers, causing the additional and unintended loss in Wafer 1. On the other hand, the median value for the insertion loss of Wafers 2 and 3 is comparable, even though both of them are slightly larger than the IL obtained in Wafer D as shown in Figure 3.18 (b). The disparity could be explained by the greater number of residues remaining in this lot after graphene transfer and the higher doping level of the silicon waveguide.

Figure 3.18 (c) and (d) show the maximum ER and MD. The median MD values for Wafer 1, 2, and 3 are 39.1, 40.6, and 46.6 dB/mm, respectively. Three conclusions can be drawn about the DC performance from the outcome in Figure 3.18 (d):
(1) Despite the fact that Wafer 2 and Wafer 3 have identical gate oxides (5 nm SiO_2) designed, Wafer 3 has a higher maximum MD. We ascribe this difference to the graphene layer's quality on the wafers. Compared to Wafer 3's 6-inch graphene, Wafer 2's 8-inch graphene may be of inferior quality, resulting in a smaller modulation under the same measurement conditions. A TLM structure could provide evidence for this claim, but we do not have any suitable electrical test structures included on this mask. Nevertheless, we believe that future Raman Spectroscopy could provide relevant details and confirm our hypothesis.
(2) Comparing Wafer 1 and Wafer 2, we can conclude that the DC performance is comparable for different types of gate oxides in our study, as both wafers show a nearly identical MD with 8-inch graphene layer. In other words, using high-k

dielectrics as a supporting layer to better preserve graphene quality does not work. It can be explained and understood when phonon scattering is taken into account [197, 208, 209]. Recent research has demonstrated that high-k dielectrics in close vicinity to a conducting channel in a semiconductor result in an increase in surface-optical phonon scattering due to remote optical phonon coupling between electrons in the channel and polar vibrations in the dielectric. This property manifests itself not only in graphene [197, 208, 210], but also in carbon nanotubes [199] and silicon Metal-Oxide Field-Effect Transistors (MOSFETs) [211]. Therefore, despite the fact that a high-k dielectric can drastically reduce the scattering of defects and consequently enhance the quality of graphene, this benefit is nullified by the surface phonon scattering.
(3) Lastly, when comparing wafers with the same gate oxide and 6-inch graphene layer (Wafer 3 vs. Wafer D), it is observed that both the median value and variation of MD are relatively lesser in Wafer 3. It may have been caused by the measurement method due to the various graphene NP, oxide thickness, and fixed oxide carrier concentration. An even higher voltage (>6V) is required for some of the devices in Wafer 3 to extract the full modulation. The similar maximum MD of Wafer 3 and Wafer D, however, indicates that the device's potential in these two wafers is identical. We believe that the performance of Wafer 3 can be made comparable to that of Wafer D by utilizing an appropriate measurement scheme.

The FOM of the devices is expressed in terms of transmission penalty (TP), and the outcome is depicted in Figure 3.18 (d). Wafers 2 and 3 exhibit comparable performance, whereas Wafer 1 demonstrates a considerably poorer TP due to its high insertion loss. Figure 3.18 (e) shows the wafer mapping of TP, and the graphene transfer site is indicated by the black dashed lines in the figure. Although Wafers 2 and 3 do not outperform Wafer D (due to the aforementioned potential cause), Wafer 2 demonstrates outstanding uniformity across 23 dies in an 8-inch area. It experimentally validates the robustness of our device integration. Now, the 300mm CMOS platform is ready for graphene-based photonics devices. Based on this integration, scientists and engineers can concentrate on ways to improve graphene quality at the wafer scale and build a more efficient architecture for large-scale next-generation devices. Table 3.6 provides a summary of the IL, ER, MD, and TP results for all four wafers shown in Figure 3.18.

All the wafers in Lot 2 are subjected to the same small-signal dynamic test. In Figure 3.19 (a), the 3dB bandwidth is calculated from S21 and the median value of 4.0, 13.6, and 18.1 GHz is collected for 25-μm devices on Wafer 1, Wafer 2, and Wafer 3, respectively. Note that during the graphene contact fabrication process, there is no time delay applied on any of the wafers in Lot 2, as for Wafer D in Lot 1. To better comprehend the devices, the S11 fitting is used with the

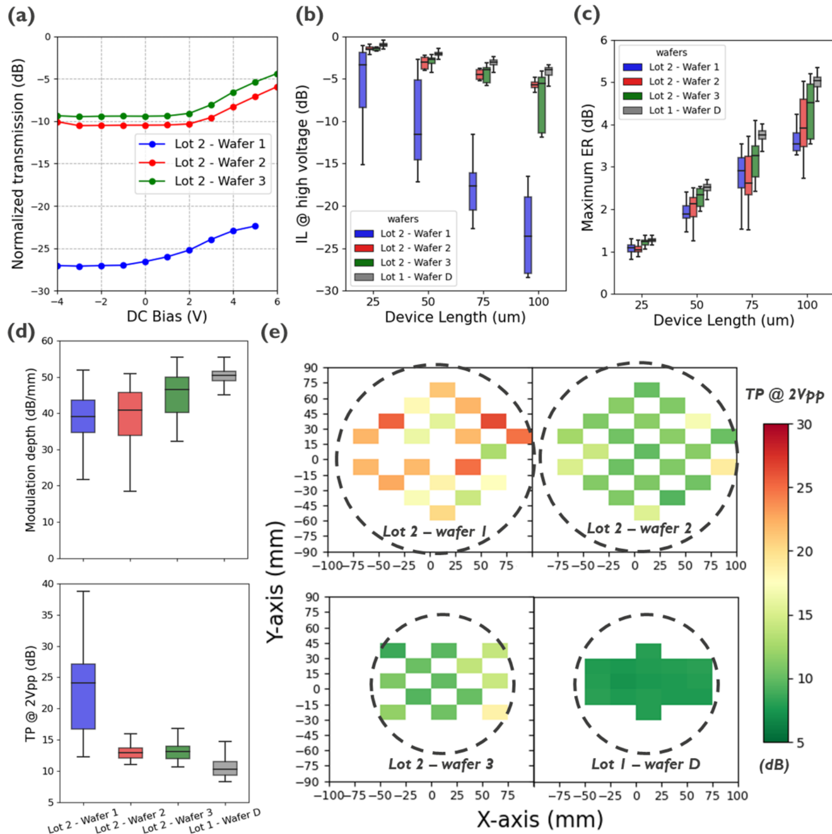

Figure 3.18: (a) Normalized transmission of 100 µm-long devices of Wafer 1, 2, and 3 as a function of applied bias. Box plot of (b) IL at high voltage, (c) maximum ER, (d) modulation depth and TP for the comparison between Wafer D, Wafer 1, Wafer 2, and Wafer 3. (e) Wafer mapping of TP for all four wafers with black dash line indicating the area of transferred graphene.

Table 3.6: Summary of the static performance for SLG EAMs in all three wafers (Lot 2), along with Wafer D (Lot 1), with four different active lengths. The unit of IL, ER, modulation depth, and TP are dB, dB, dB/mm and dB respectively. IL is calculated under the condition with high voltage applied.

Insertion loss at high voltage	Wafer 1	Wafer 2	Wafer 3	Wafer D
25 μm	5.5 ± 4.4	2.1 ± 2.3	1.7 ± 0.8	1.0 ± 0.3
50 μm	10.2 ± 5.4	4.6 ± 3.7	3.3 ± 1.5	2.2 ± 0.7
75 μm	18.7 ± 4.3	6.3 ± 4.6	6.6 ± 5.6	3.7 ± 2.7
100 μm	23.3 ± 4.7	6.4 ± 3.1	8.8 ± 6.4	4.6 ± 2.3
Extinction ratio (-4 V to 6 V)	Wafer 1	Wafer 2	Wafer 3	Wafer D
25 μm	1.0 ± 0.2	1.0 ± 0.2	1.2 ± 0.1	1.2 ± 0.2
50 μm	1.9 ± 0.2	2.0 ± 0.4	2.3 ± 0.2	2.5 ± 0.1
75 μm	2.8 ± 0.6	2.7 ± 0.6	3.2 ± 0.5	3.7 ± 0.3
100 μm	3.6 ± 0.6	4.0 ± 0.7	4.1 ± 1.3	5.0 ± 0.2
Modulation depth	Wafer 1	Wafer 2	Wafer 3	Wafer D
All four different device lengths	39 ± 7	39 ± 8	44 ± 8	50 ± 4
Transmission penalty	Wafer 1	Wafer 2	Wafer 3	Wafer D
All four different device lengths	22.9 ± 6.9	14.1 ± 3.6	14.2 ± 4.6	10.8 ± 2.4

same equivalent circuit model. We observe that the capacitance of all four wafers is comparable, but there is a variation in the total resistance. In Figure 3.19 (b), the median number for 25-μm devices on Wafer 1, Wafer 2, and Wafer 3 is 362, 237, and 183 Ohm, respectively. Compared to Wafer D's resistance of 262 Ohm, Wafers 2 and 3 have a reduced resistance, which may be due to the increased silicon doping and/or improved graphene contacts. The quality of the graphene, which we stated in the DC analysis, can also account for the resistance difference between Wafers 2 and 3. The quality of Wafer 2's 8-inch graphene is marginally inferior, resulting in a smaller MD and bandwidth. Finally, Wafer 1 exhibits a high total resistance, causing its frequency to be consistently less than 10 GHz. We think that Wafer 1 and Wafer 2 have comparable graphene mobility based on the results of the DC analysis. Therefore, we believe that the larger total resistance is due to the contact resistances. Unfortunately, the hypothesis cannot be verified due to a lack of appropriate electrical test structures; we strongly suggest including TLM structures, which can provide in-depth device detail, in future designs.

3.3 Outlook

We showed wafer-scale integration for graphene electro-absorption modulators using the imec 300mm CMOS fab. This framework clears the way for investigating cutting-edge EAM devices and their adoption for use in industrial applications.

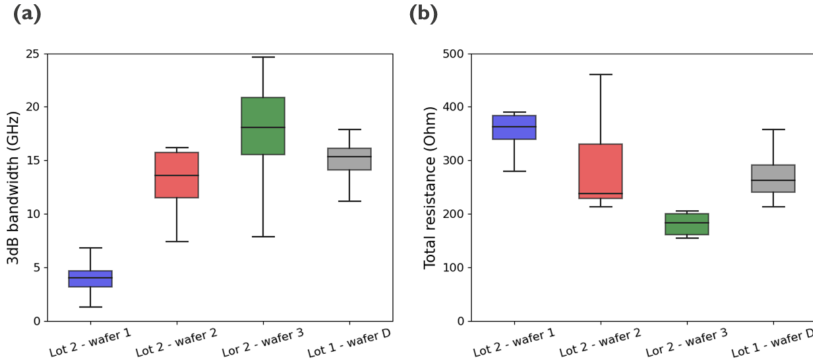

Figure 3.19: Box plots of (a) extracted EO bandwidth and (b) calculated GOS resistance for three wafer in Lot 2 at DC bias of 1V, along with champion wafer in Lot 1 (Wafer D).

Here, we highlight three possible structural upgrades based on the same socket waveguide design and integration process used in this chapter. Although graphene itself has a strong interaction with light, the total performance of the device is still poor. The primary issue is the weak optical field interaction with the atomically thick graphene layer. It leads to low modulation efficiency, which necessitates relatively long devices to achieve a desired ER, increasing the device capacitance and slowing down the speed. To achieve high-performance graphene modulators, it is essential to increase the mode confinement in the graphene sheet.

3.3.1 Mode shifter

The first technique we suggested is the addition of a mode shifter, which enables greater mode interaction with the graphene layer. In this thesis, we focused on a polycrystalline silicon (Poly-Si) mode shifter, which is easily made using conventional CMOS manufacturing. The module to integrate such Poly-Si is already available in imec's isipp50G platform for grating couplers. Figure 3.20 (a) depicts the cross-section, where the width of the waveguide (W_{wg}) is 500 nm and the thickness of the gate oxide (d_{ox}) is 5 nm. Graphene's width is specified to be the same as W_{wg} because only this portion of E_f can be changed. Figure 3.20 (b) provides an illustration of normalized absorption as a function of graphene chemical potential. By calculating the difference between maximum and minimum absorption, we can determine the modulation depth (MD), which is used to evaluate the improvement after placing the Poly-Si. The effects of Poly-Si width ($W_{Poly-Si}$) and Poly-Si thickness ($d_{Poly-Si}$) on MD are examined in Figure 3.20 (c). As $W_{Poly-Si}$ increases, MD rises as well, peaking at 500 nm. With d_{polySi}

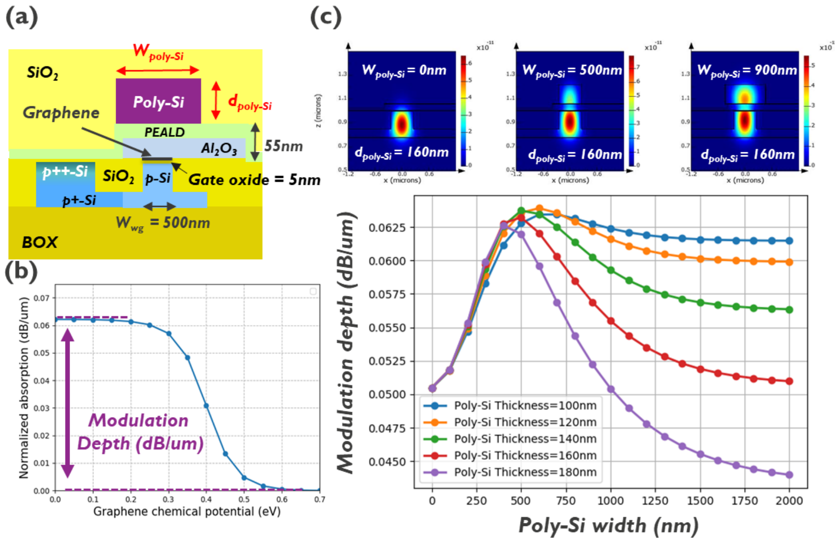

Figure 3.20: (a) Schematic of Poly-Si layer integrated on the SLG EAM device. (b) Representative normalized absorption in a function of graphene chemical potential. Modulation is defined by the difference between maximum and minimum of the absorption and will be used to evaluate the improvement after adding Poly-Si layer. (c) Mode profiles of SLG EAM without Poly-Si layer (left), with $W_{Poly-Si}$ = 500nm of Poly-Si layer (middle), and with $W_{Poly-Si}$ = 900nm of Poly-Si layer (right). The bottom shows the MD in a function of $W_{Poly-Si}$ for five different $d_{Poly-Si}$.

= 160 nm, MD increases by 23% from 51 to 63 dB/mm. The upward shifting of modes is depicted by the mode profiles in Figure 3.20 (c).

Tapers are necessary when designing a new cross-section in order to communicate with the basic strip waveguide. To check whether the light can successfully propagate through the tapers, we now conduct EigenMode Expansion (EME). Two tapers are clearly visible in the cross-sections of the simulation structure, which are described in Figure 3.21 (a). One is the 30-μm standard taper that is used to change strip waveguide into socket waveguide. The other is a Poly-Si taper, which raises the waveguide's mode and improves interaction with the graphene layer. The Poly-Si taper's width begins at 150 nm and finishes at 500 nm. To convert the mode back to the standard strip/socket waveguide, the opposite side of the active area has a second Poly-Si taper with the same design but in the opposite direction. Here, the 1, 3, and 5 μm lengths of the Poly-Si taper are examined. It is evident in Figure 3.21 (b) and (c) that Poly-Si taper with lengths of 3 and 5 μm has a high coupling effectiveness (>99%) between 1.5 and 1.6 μm of wavelength. The simulation demonstrates that the mode shifter technique is theoretically feasible

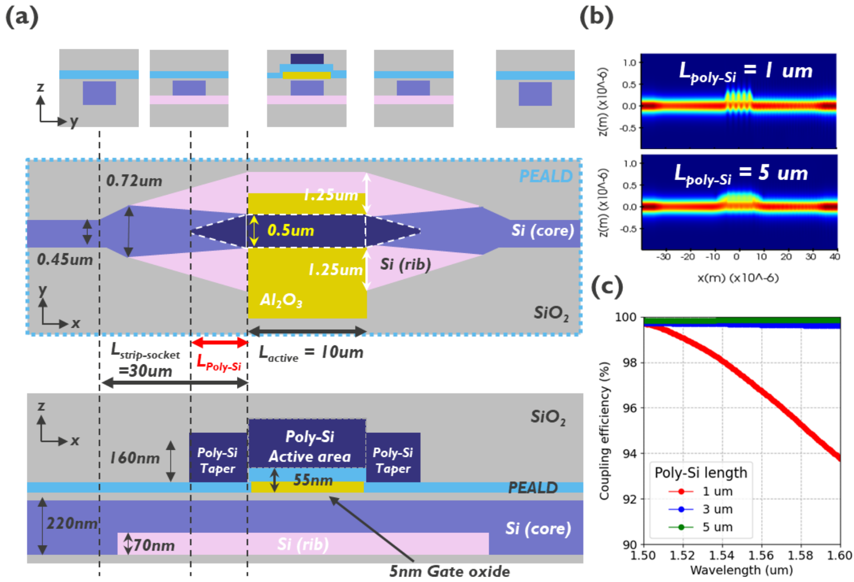

Figure 3.21: (a) Schematic of simulated structure in EME solver. The structure contains strip waveguide, socket waveguide, strip-to-socket tapers, Poly-Si tapers, and Poly-Si layer in 10-µm active area. (b) Simulated propagation profiles for $L_{Poly-Si}$ = 1 and 5 µm. (c)Simulated coupling efficiency in a function of wavelength for $L_{Poly-Si}$ = 1, 3 and 5 µm.

and that the taper is well designed.

We continue to research the Poly-Si distance, as shown in Figure 3.22 (a). In a prior simulation, a 55 nm Poly-Si distance was created using 30 nm Al_2O_3 and 25 nm SiO_2. We now reduce this number to increase the impact of Poly-Si. It is evident in Figure 3.22(b) that a smaller Poly-Si distance yields a larger modulation. MD can be further enhanced from 63 to 86 dB/mum with $W_{Poly-Si}$ = 500 nm, which is a 70% increase over the device without a Poly-Si layer. However, there will be some challenges in controlling the capping layer's thickness. To allow small Poly-Si distance, a better CMP module needs to be developed.

3.3.2 TM mode

The second method involves using the TM mode rather than the TE mode to enhance the mode overlap on the graphene layer. According to the mode profiles in Figure 3.23, the TM mode has less light confinement in waveguide and it could interact with graphene more intensely, allowing for a larger modulation using the same measurement technique. A device with TE mode, TE mode + Poly-Si (as

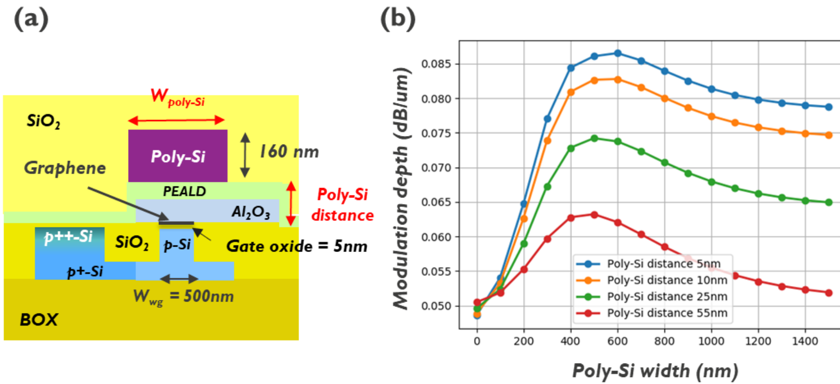

Figure 3.22: (a) Schematic of Poly-Si layer integrated on the SLG EAM device with various $W_{Poly-Si}$ and Poly-Si distance. (b) MD in a function of $W_{Poly-Si}$ for four different Poly-Si distances.

stated in the first approach), and TM mode are three different cases that are compared in the Figure 3.23. It is evident that devices using TM mode and devices with poly have greater modulation than devices using TE mode (standard). For three distinct scenarios where the Fermi level is sweept from 0 to 0.7 eV, we measured the modulation depth at 51, 86, and 85 dB/μm. Here, the simulated graphene layer consists of two regions: gated and non-gated regions. The gated area, which determines the width of the capacitor, is approximately equivalent to the width of the waveguide, whereas the non-gated area refers to the graphene layer outside the gated area. By employing Poly-Si and TM mode, light has a greater interaction with both regions of graphene, resulting in a greater IL at high Fermi levels. Consequently, we further calculate transmission penalty (TP) with EOT=10 nm and compare between the three cases as shown in Figure 3.23(c). For the device with TE mode, Poly-Si mode, and TM mode, respectively, we measured 10.4, 8.8, and 8.7 dB. It demonstrates that the interaction between mode and graphene can be increased to further improve the device. Importantly, the method of employing TM mode can be easily implemented by modifying the waveguide design without changing anything in the overall integration flow.

3.3.3 Dual-single-layer graphene structure

The final approach is to create a graphene-oxide-graphene (GOG) capacitor on top of a passive waveguide by integrating a second layer of graphene. This allows to prevent the loss of doped-Si while having two layers of graphene contributing

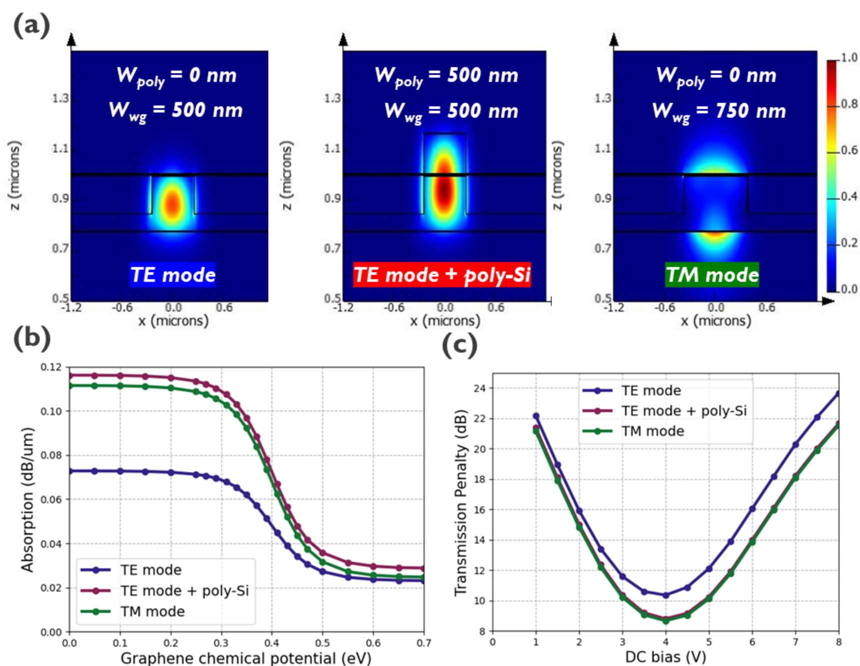

Figure 3.23: Simulated (a) mode profiles, (b) absorption in a function of graphene chemical potential, and (c) TP in a function of DC bias for three SLG EAM cases: without Poly-Si layer using TE mode, with $W_{Poly-Si}$ = 500nm of Poly-Si layer using TE mode, and without Poly-Si layer using TM mode. EOT = 5 nm is considered here.

to the modulation process. Figure 3.24 (a) depicts the cross-sectional appearance of the proposed dual-single-layer (DLG) graphene EAM, which was constructed using the platform and modules developed in this chapter. To see how the device can be improved further, we analyze the results with and without Poly-Si. Al_2O_3's dielectric constant of 7.8 and three different gate oxide thicknesses (4, 10, and 20 nm) are taken into account. Figure 3.24 (b) depicts an example of simulated absorption as a function of DC bias for a DLG with a width of 750 nm. First, when comparing the performance of SLG and DLG devices (both without polySi), the modulation depth in the DLG structure has been approximately doubled, resulting in 0.13 dB/μm in Figure 3.24 (b). It can be enhanced further to 0.21 dB/μm by putting a Poly-Si layer on top. Modulation becomes more efficient as modulation depth increases, and a reduced device length is sufficient to generate the desired ER. It allows for a lesser influence of 50 Ohm from the driver, which may result in a large bandwidth. To increase the performance of the devices further, the width of the DLG (W_{DLG}) can be decreased to reduce the capacitance. Consequently, the RC delay can be decreased and potentially a greater bandwidth can be obtained. However, a smaller W_{DLG} causes light to interact more with non-gated regions (typically absorptive) and less with gated regions (where Fermi-level modulation is possible), resulting in smaller ER and larger IL. Figure 3.24 (c) summarizes TP and BW results for DLG devices with 3 different EOT (2, 5, 10 nm) and 9 W_{DLG} values (200 to 1000 nm with 100 nm as span) in order to better evaluate the trade-off and determine the optimal parameters for the devices.

Three conclusions can be derived regarding the effect of parameters based on the outcome presented in Figure 3.24 (c):
(1) Comparing devices without polySi (left) to devices with polySi (right), we find that devices with mode shifter have a larger chance of reaching the golden corner (bottom right), where high efficiency and bandwidth are achieved. That a mode shifter improves light interaction with graphene layers is a result of the same effect as explained in previous subsection.
(2) The thinner the gate oxide thickness, the better the TP value owing to a larger extracted modulation at V_{pp} = 2V. However, it has a smaller bandwidth due to larger capacitance.
(3) Lastly, devices with a narrower W_{DLG} width have superior bandwidth performance but inferior TP values.

Although the method of the GOG structure seems to provide the best performance and compromise among all three methods, it is expected that it will take more effort experimentally to fabricate the structure. In order to transfer the second layer of graphene, a high-quality oxide with a uniform thickness must be placed on top of the first layer. Additionally, the graphene patterning procedure must be carried out carefully so that the first graphene layer is not etched during the patterning of the

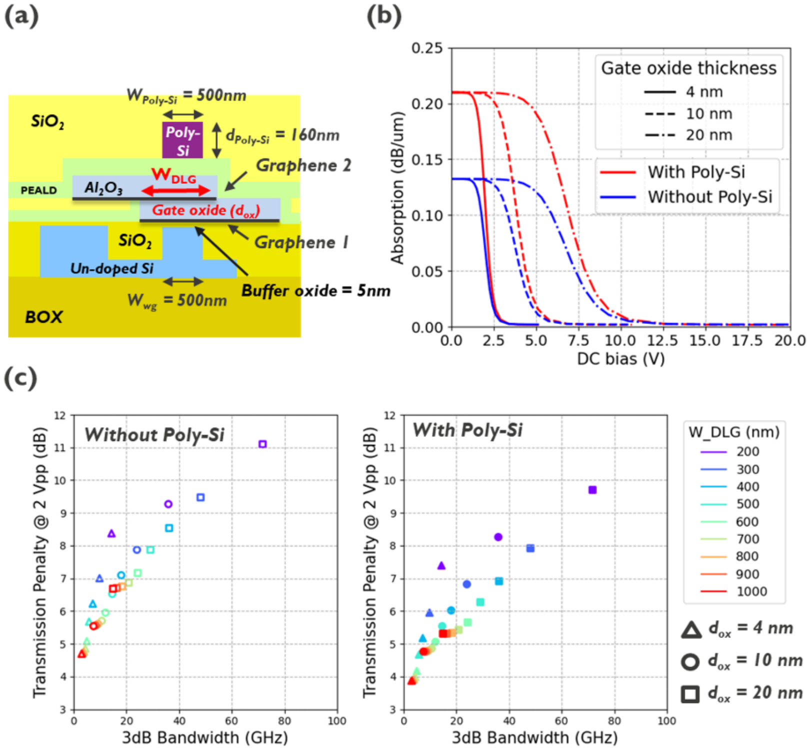

Figure 3.24: (a) Schematic of dual-single-layer structure integrated on the undoped socket waveguide based on the modules developed in this chapter. With and without Poly-Si layer have both been simulated here. (b) Absorption in a function of DC bias for three different gate oxide thickness (4, 10, 20 nm) with and without Poly-Si layer. W_{DLG} = 750 nm is considered here. (c) TP-Bandwidth relationship for DLG devices with (left) and without (right) Poly-Si layer. W_{DLG} ranges from 200 to 1000 nm. We considered a 40 μm long device and calculated the bandwidth with a carrier concentration of 1.6×10^{13} cm^{-2} (equivalent to E_F 0.44 eV) for the gated graphene and 8×11^{11} cm^{-2} (equivalent to E_F 0.1 eV) [30] for the graphene in the un-gated regions to avoid an infinite resistance. A contact resistance of 500 Ω μm is considered for both layers of graphene.

second layer. We believe our high-yield wafer scale integration method is ideal for methodically investigating these challenges and achieving those potential device architectures.

3.4 Conclusion

In this chapter, first we have demonstrated the integration of single layer graphene electro-absorption modulators in a CMOS fabrication environment. Damascene contacts and standard photo-lithography were used to build the wafer-scale devices in accordance with industry standards. Three critical processing steps were studied in this work to determine their effect on device performance. We discovered that the surface flatness has a significant impact on the graphene quality and electric field homogeneity, both of which affect the modulation depth of the final device. Following that, the uniform capping layer reduces the impact of later integration steps on the graphene layer, resulting in increased device yield. Finally the time delay involved in constructing the damascene contacts affects the contact resistance and the 3dB bandwidth of the EAMs. After optimizing these three critical processing steps and implementing a CMOS-compatible dedicated integration approach, the device yield exceeds 95% with loss, extinction ratio, and 3dB bandwidth values comparable to CVD graphene devices previously demonstrated in the lab.

Secondly, we have investigated three directions to optimize device performance based on the CMOS integration developed in the first section. (1) The graphene patterning module has been optimized through the use of an endpoint detection system based on optical emission spectroscopy. With the aid of new technique, we are able to stop etching with optimal accuracy and precisely control layer damage at the wafer scale. (2) Implementing a new stack of gate oxide which can embed graphene in a high-k dielectric. Although we anticipated that this type of structure will screen impurity scattering and improve device performance, the phonon scattering cancels out the benefit, resulting in no improvement in device performance. (3) Ultimately, we can now transfer graphene in larger sizes. The number of available dies and devices can be doubled by extending the size from 6 inches to 8 inches. It also confirms again the robustness of our high-yield 300 mm CMOS integration platform. Now, scientists can focus on how to improve graphene quality and contact resistance on wafer-scale to further improve the performance of SLG EAMs .

We anticipate that the knowledge presented in this study can be extended and applied to a sophisticated building block library of graphene-based optoelectronic devices, that includes modulators, photodetectors, and sensors. This work will underpin the industrial adoption of graphene-based photonics devices, paving the way for the next-generation datacom and telecommunications applications.

4

DUAL-SINGLE-LAYER GRAPHENE MODULATORS INTEGRATED ON STRIP AND SLOT WAVEGUIDES

In Chapter 3, we showcased a significant milestone—the successful integration of single-layer graphene electro-absorption modulators into a 300mm CMOS pilot line, marking a crucial step towards the widespread industrial adoption of graphene-based modulator devices. However, we also observed that the primary limitation of the SLG EAM is the low modulation efficiency and the requirement of sophisticated implantations in the silicon layers. To address these challenges, we transition from fab-level to lab-level devices and investigate the potential of graphene-based modulators using a dual single-layer graphene (DLG) structure. The DLG EAM, boasting two layers of graphene, showcases promising attributes, including a larger extinction ratio (ER) and an expanded electro-optical (EO) bandwidth [25, 26, 146]. Notably, the DLG EAM introduces increased flexibility by eliminating the need for implantation and enabling integration on various types of waveguides. To further elevate device performance, we propose a novel approach utilizing slot waveguides for constructing graphene-based modulators.

In the initial sections of this chapter, we present simulation results for slot waveguides and mode converter, laying the foundation for the inline fabrication process. Next, we demonstrate the lab-based integration flow for DLG modulator fabrication.

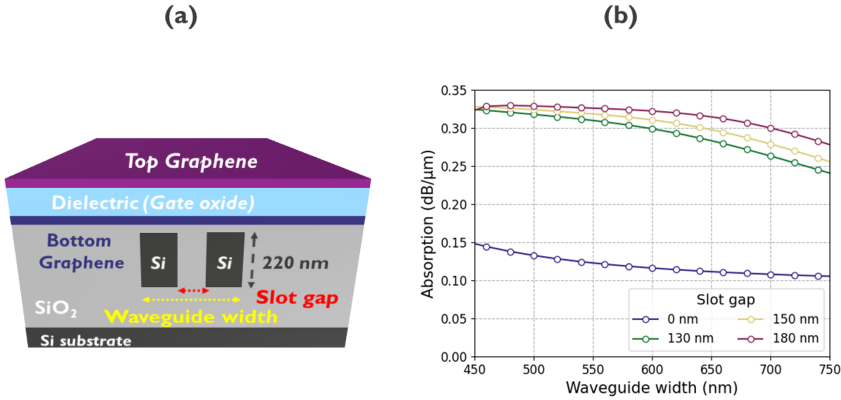

Figure 4.1: (a) A 3D schematic of DLG EAM integrated on a silicon waveguide. The W_{wg} and slot gap (W_{slot}) are defined by the width of $Si - SiO_2 - Si$ and sandwiched SiO_2, respectively. (b)Simulated absorption as a function of waveguide width for W_{slot} = 0, 130, 150, and 180 nm. Graphene has a chemical potential of 0 eV and a scattering rate value of 15 meV.

Optical and electrical characterizations are conducted using EAM and transfer length measurement (TLM) structures, respectively, providing essential insights into graphene and device quality. Subsequently, we perform a comprehensive analysis and comparison of DLG performance in three different types of modulators: EAM, Mach-Zehnder modulator (MZM), and ring modulator (RM). In the final sections, we draw conclusions and offer an outlook on optimizing performance to achieve high speed and efficiency in a CMOS-compatible environment. This forward-looking perspective sets the stage for the next generation of high-capacity optical communication systems, emphasizing the role of DLG-based modulators in advancing optical communication technologies.

Part of the text and results contained in this chapter have been published in Wu, Chenghan, et al. ”Large>0.2 dB/μm Modulation Depth Double-Layer Graphene Electro-Absorption Modulator on Slot waveguide.” CLEO: Science and Innovations. Optica Publishing Group, 2022. [212] and Wu, Chenghan, et al. ”High-efficiency dual single layer graphene modulator integrated on slot waveguides.” Optics Express 31.22 (2023): 36872-36882. [213]

4.1 Slot waveguide and mode converter

Given that graphene consists of only a single atomic layer, its modulation capability is exceptionally strong. However, the overall modulation efficiency of the

device remains insufficient due to the weak overlap of the optical field with the graphene layers. To enhance the modulation efficiency and bandwidth of high-performance graphene modulators, increasing the mode confinement within the graphene layer is imperative. We investigate the slot waveguide to enhance the light-matter interaction. Slot waveguides, depicted in Figure 4.1(a), consist of a narrow gap between two silicon rails. This design facilitates a robust electric field enhancement in the slot gap, resulting in superior mode confinement on the graphene layers. The schematic representation of DLG on a slot waveguide is also presented in Figure 4.1(a). This configuration involves stacking a bottom graphene layer (GRA1) and a top graphene layer (GRA2), separated by a dielectric oxide, on an embedded silicon waveguide.

For the purpose of investigating the mode interaction between waveguides and DLG, the simulation simplifies the scenario by evenly distributing both layers across the entire substrate (over 5μm). It's crucial to acknowledge that these dimensions are not practically applicable in a real device due to the significantly large capacitance, which hinders high-speed performance. The simulation, in this case, serves the purpose of providing a conceptual understanding of dimensions for slot waveguides fabrication.

We use Lumerical to simulate the structure's absorption. We sweep the W_{wg} and W_{slot} values to optimize the dimensions. Here, "strip waveguide" refers to devices having a slot gap of 0 nm, whereas "slot waveguide" refers to devices with a slot gap greater than 0 nm. For the fundamental TE mode, Figure 4.1(b) demonstrates that the absorption of slot waveguide based DLG EAM is always over two times that of a strip waveguide based device with neutral graphene layers. The increased interaction between the graphene layers and the mode profile contributes to the increase in absorption. To enable CMOS-compatible fabrication, the waveguide width and slot gap for the slot waveguide in this thesis were chosen to be 680 nm and 180 nm, respectively. In that case, oxide can be uniformly filled in after silicon waveguide patterning and the surface can be uniformly planarized over a 200 mm wafer. As stated in the previous sections, W_{wg} = 450 nm is selected for strip waveguide.

Given that the majority of PIC building blocks, such as grating couplers and routing waveguides, are typically built using strip waveguides, a mode converter is required to connect the slot waveguide used in the slot modulators with other structures on the chip and reduce the loss. It can be defined in the integration flow mentioned above during silicon patterning. Our converter design is based on [214]. As shown in Figure 4.2, the width of the strip waveguide decreases from 450 to 250 nm, while the width of a second waveguide coming near increases from 150 to 250 nm. The coupling efficiency simulated by $Lumerical$ FDTD exceeds 99.5% for quasi-TE

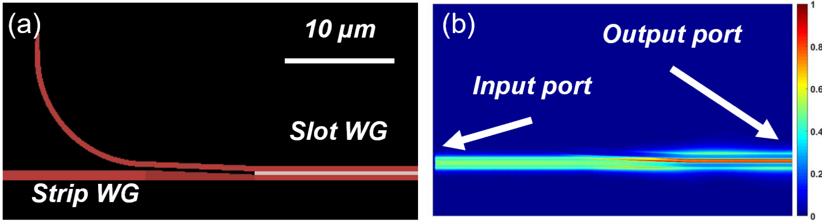

Figure 4.2: (a)Top-down view of constructed simulation structure for strip-slot mode converter. (b) side view of simulated power distribution.

fundamental modes, which corresponds to around 0.02 dB of insertion loss for a single mode converter. Two mode converters are positioned at both ends of the slot waveguide so that the same grating couplers and access waveguides can be used as for the devices based on strip waveguides, thereby minimizing their difference.

4.2 Fabrication of DLG devices

The fabrication of the modulator started from a 200-mm silicon-on insulator (SOI) wafer with a 220 nm crystalline silicon layer and a 2 μm buried oxide, as illustrated in Figure 4.3(a). After waveguide patterning and $\approx 2\mu m$ oxide deposition, the wafer is planarized with chemical mechanical polishing (CMP) until a 10 nm-thick buffer oxide is left on top of the waveguides (see Figure 4.3(b)). Next, the wafer was diced, and the first CVD-grown graphene layer (GRA1) was transferred using a wet-transfer technique, followed by an acetone cleaning process (Figure 4.3(c)). After that, we utilized electron beam lithography (EBL) to define the graphene layer. Note that the required patterning accuracy could be readily reached also by a deep UV lithography system as we demonstrated in Chapter 3 [171]. We used a double layer resist process, with poly-methyl methacrylate (PMMA) at the bottom for protecting the graphene layer and hydrogen silsesquioxane (HSQ) on top being exposed by EBL. After exposure and development, an oxygen plasma was used to pattern the graphene layer together with the PMMA layer (Figure 4.3(d)). Then, the metal contacts were fabricated through EBL and a lift-off process. Figure 4.3(e) schematically shows the structures after the lift-off process. A top + edge contact scheme was used, combining two typical contact geometries to graphene [215,216], targeting low contact resistance. Next, the gate oxide was grown using atomic layer deposition (ALD). In this thesis, two types of gate oxide (Al_2O_3 and HfO_2) were used to fabricate the devices. To generate a uniform gate oxide on the self-passivated graphene layer, first we deposited 1 nm of Al (Si) by thermal evaporation and

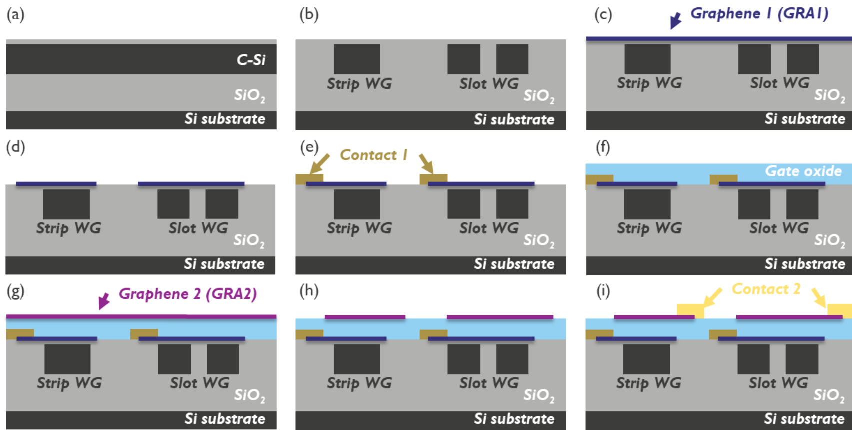

Figure 4.3: Process flow for DLG EAM fabrication. (a) SOI wafer, (b) waveguide patterning and surface planarization, (c) wet transfer of first graphene layer, (d) patterning by EBL, (e) contact with Pd, (f) Al_2O_3 or HfO_2 deposition, (g) wet transfer of second graphene layer, (h) patterning by EBL, and (i) top + edge contact with Pd.

subsequently 10 nm Al_2O_3 (HfO_2) was deposited by ALD (Figure 4.3(f)). Then the second layer of graphene (GRA2) was transferred (Figure 4.3(g)), patterned (Figure 4.3(h)) and contacted (Figure 4.3(i)) using the same methods.

4.3 Characterization of graphene optical and electrical properties

Before conducting a characterization and comparison of various types of modulators, we performed pure optical and electrical characterizations. Figure 4.4 (a) and (b) illustrate the structures used for the pure optical and electrical characterization, respectively. For the optical transmission measurement, a light power of 0 dBm was applied to all devices before the light entered the input grating couplers. The transmission measurements for both Al_2O_3- and HfO_2-based devices are presented in Figure 4.5. When comparing devices with the same graphene length, it is evident that the insertion loss of the Al_2O_3-based devices is higher than that of the HfO_2-based devices across the entire measured wavelength range. This higher loss in Al_2O_3-based devices may be attributed to oxygen-deficient defects introduced during deposition [217, 218], which can be potentially mitigated by thermal annealing [219]. Figure 4.5 (c) shows the maximal transmission for Al_2O_3-based (blue) and HfO_2-based (red) devices as a function of graphene length. Al_2O_3-based devices exhibit insertion losses of 22 dB and propagation losses of 0.113 dB/μm,

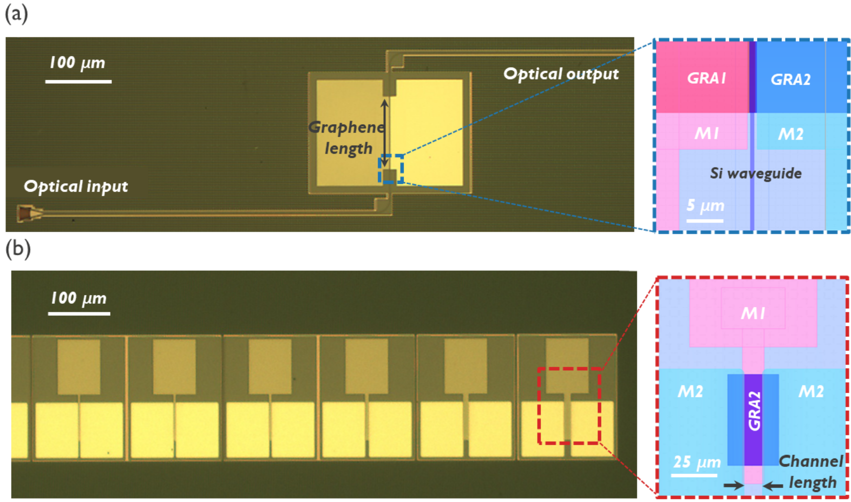

Figure 4.4: Top-down microscope images of (a) EAM structure and (b) TLM structure. The right side of each microscope image includes a zoomed-in view of the associated mask design.

while HfO_2-based devices show insertion losses of 10 dB and propagation losses of 0.174 dB/µm. Accounting for approximately 5 dB insertion loss from each grating coupler, Al_2O_3-based devices still have roughly 12 dB additional losses from the routing waveguides, whereas HfO_2-based devices experience minimal additional loss. These results indicate that HfO_2-based devices may have stronger mode interaction with the graphene layers and, owing to their lower insertion loss, are more suitable for characterizing long and large devices, such as the MZM.

In the electrical measurement, we employ the TLM method to extract graphene's contact and sheet resistance. To assess the quality of graphene in both layers within their respective environments, the mask used for fabricating graphene photonics devices includes a design area with TLM structures. Figure 4.4 (b) provides a top-down view of TLM structures fabricated on SOI substrates alongside other graphene photonics devices. The transistors used in this study have channel lengths ranging from 0.5 to 10 μm and channel widths of 50 μm. To accommodate the TLM fabrication in the integration flow of DLG photonics devices, the transistors for graphene 2 are measured in a back-gated configuration, while the transistors for graphene 1 are measured in a top-gated configuration. The cross-sectional views of the transistors for graphene 1 and graphene 2 are depicted in the insets of Figure 4.6 (b) and (c), respectively. In Figure 4.6 (a), an example of the TLM results is presented, with the drain voltage held constant at 0.5 V while the gate voltage is swept from -5 to 5 V. The clear dip in each drain-current-gate-voltage

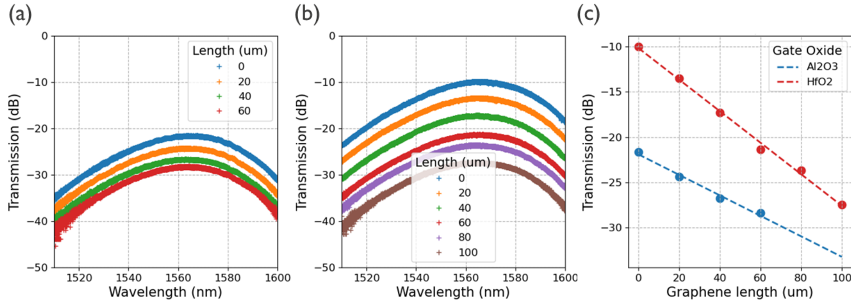

Figure 4.5: EAM transmission as a function of wavelength for various graphene lengths of (a) Al_2O_3-based devices and (b) HfO_2-based devices. (c) Extracted maximum transmission as a function of graphene length. The slope of fitted results (dash lines) are 0.113 and 0.174 $dB\mu m^{-1}$ for Al_2O_3- and HfO_2-based devices, respectively.

curve originates from graphene's neutrality point. After normalizing the voltage, the total resistance as a function of channel length is plotted and fitted for graphene 1 and graphene 2 in both Al_2O_3- and HfO_2-based devices, as shown in Figure 4.6 (b) and (c). Since the contact resistance dominates when the channel length is short [220], here we only fit the dots with channel length smaller than 6 μm as shown by Figure 4.6 (b) and (c).

For graphene 2, the data points fit well, and the Al_2O_3-based (blue) and HfO_2-based (red) devices exhibit contact resistances of 504 and 598 Ω μm and mobilities of 632 and 598 $cm^2V^{-1}s^{-1}$, respectively, at 1.5×10^{13} carrier concentrations. However, the TLM characterization for graphene 1 faced challenges due to difficult probe-landing (probes needing to scratch through the oxide to make good contact with embedded metal), resulting in considerable device variation. Despite these challenges, we managed to extract contact resistances of 1777 and 1178 Ω μm and mobilities of 327 and 496 $cm^2V^{-1}s^{-1}$ in Al_2O_3- and HfO_2-based devices, respectively, for graphene 1. It is essential to note that these values provide a limited view since only one set of TLM structures was characterized for each case, and the calculated values could be influenced by material and process variations over the wafer. We highly recommend conducting electrical tests with a larger number of TLM sets to perform statistical electrical analysis in the future. Moreover, using a via-opening step on metal 1 can prove beneficial in resolving probe landing issues and ensuring effective contacts during the measurement on embedded graphene. In the subsequent sections, Al_2O_3-based devices were used to characterize EAMs, while HfO_2-based devices were used to characterize RMs and MZMs.

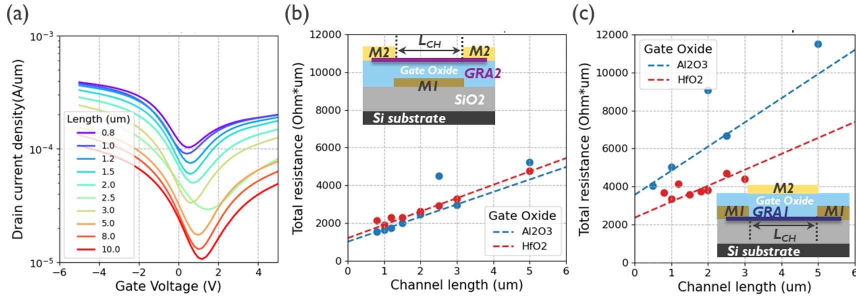

Figure 4.6: (a) Measured drain current density as a function of gate voltage for L_{ch} ranging from 0.8 to 10 μm in Al_2O_3-based TLM. Extracted and fitted total resistance of (b) graphene 2 and (c) graphene 1 as a function of channel length at 1.5×10^{13} carrier concentrations. The insets in (b) and (c) show the schematic cross-section of the TLM devices.

4.4 DLG electro-absorption modulators

Electro-Absorption Modulators (EAMs) are simple and compact devices that utilize an active component placed on waveguides to modulate the absorption of propagating light. In this context, we refer to the DLG EAM with strip waveguide as ”STRIP-DLG EAM” and the DLG EAM with a slot waveguide as ”SLOT-DLG EAM”. For the discussion and comparison between STRIP-DLG and SLOT-DLG EAMs in this section, we have chosen the sample with an Al_2O_3 gate oxide. Figure 4.7 presents optical and scanning electron microscope (SEM) images of both STRIP-DLG EAM and SLOT-DLG EAM. The inset of Figure 4.7(b) showcases the mode converter, which facilitates the seamless transition between the strip and slot waveguides.

4.4.1 EO static performance of DLG EAMs

We initiated the study by performing unbiased fiber-to-fiber transmission measurements to verify the mode converter design. The test devices, depicted in the inset of Figure 4.8(a), are simple stand-alone waveguides that underwent the complete processing modules with DLG devices but lacked graphene coverage. The wavelength was swept from 1540 to 1600 nm. Notably, there was no significant difference observed between the strip waveguide (blue curve) and the strip + slot waveguide (red curve), confirming the minimal loss of the mode converters.

To characterize the DC performance of the DLG EAMs, we applied a bias voltage with the source placed at contact 2 and the ground at contact 1. Figure 4.8(a)

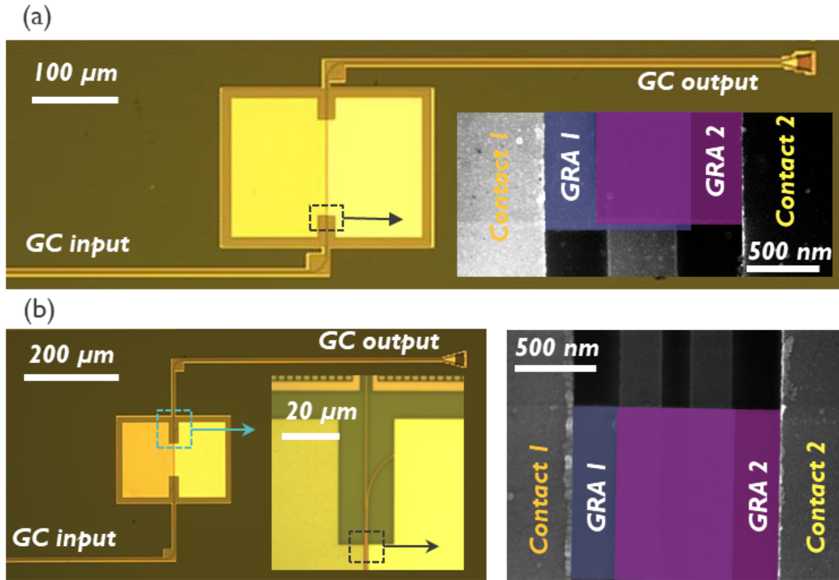

Figure 4.7: Top-down microscope images of (a) STRIP-DLG and (b) SLOT-DLG. The right side of each microscope image includes a top-down scanning electron microcope (SEM) image.

displays the transmission as a function of the applied voltage for strip waveguide-based DLG EAMs with three different active lengths (20, 40, and 60 µm), alongside the transmission of an identical structure without DLG. With a peak-to-peak voltage of 6 V, the majority of the modulation was achieved. At 5 V, the insertion losses for devices with lengths of 20, 40, and 60 µm were 0.68, 0.88, and 1.84 dB, respectively. To highlight the capability of being driven with low drive voltage, the extinction ratio (ER) is calculated using a peak-to-peak voltage of 2 V. The ERs scale linearly with device length, reaching 1.0, 2.2, and 3.2 dB for 20, 40, and 60 µm long devices, respectively. For a high-performance modulator, it is necessary to exhibit a sufficiently large extinction ratio, a low insertion loss, and a wide bandwidth at a CMOS-compatible drive voltage. To evaluate different modulator designs more effectively, the transmission penalty (TP) is introduced [221]. It is defined as $TP = (P_1 - P_2)/(2P_{in})$, where P_1 and P_2 are the high and low output power levels, respectively, and P_{in} represents the input power. TP was calculated and presented in Figure 4.8 (c). The TP values are 11.1, 8.9, and 9.4 dB. This FOM outperforms previous graphene-based modulators that have been reported in the scientific literature [26, 146]. Moreover, with identical driving voltage settings (2V), it is comparable to a state-of-art Ge-based FK modulator. [68]

Next, we performed the same DC measurement on SLOT-DLG EAMs. Figure 4.9(a)

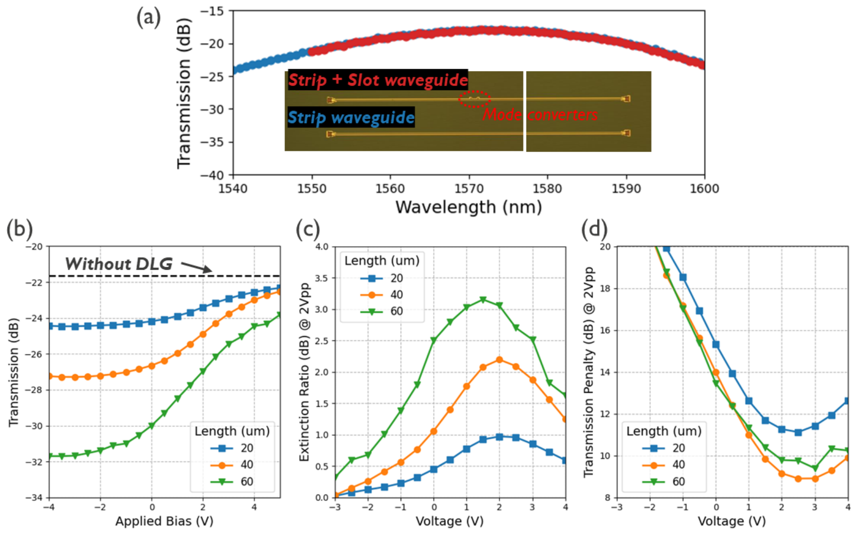

Figure 4.8: (a) Transmission of the passive strip and strip + slot waveguides. The insertion loss and wavelength dependency originate from the grating couplers. Insets show the top-down microscope images of the passive structures. (b) Transmission curves of strip waveguide based DLG devices as a function of gate bias for device lengths of 20, 40, and 60 μm at a peak wavelength of 1570 nm. The black-dashed line indicates the transmission of an identical structure without DLG at the same peak wavelength. Calculated (c) ER and (d) TP with V_{pp} = 2 V for all three device lengths.

and (b) present the measured transmission response of the two types of DLG EAMs, which are normalized by the transmission of an identical structure without DLG, at a wavelength of 1550 nm. The STRIP-DLG EAM shows the expected behavior, with a transmission which is modulated from -2.8dB to -0.6dB when varying the normalised voltage from 0 to 9 Volt. At first sight, the SLOT-DLG EAM shows a similar behaviour, with a somewhat larger extinction ratio as expected. However, we consistently observed that the SLOT-DLG EAM exhibits significantly higher insertion loss. As both devices were fabricated on the same chip, the observed difference can not be explained solely by device-to-device variations. To understand the origin of these losses, we carried out simulations using a commercial mode solver (Lumerical). All device dimensions, including DLG width and metal distance, were taken from the actually fabricated devices shown in Figure 4.7(h) and (i). Four different scattering rates for the graphene layers were considered, where lower scattering rates indicate higher quality [23]. Considering initial doping values of 0.2 eV and -0.3 eV for the GRA1 and GRA2 layers respectively and an equivalent oxide thickness of 9.5 nm, we found excellent agreement between the experimental and simulated results, as is clear from both Figure 4.9(a) and (b). Through these simulations, one significant factor contributing to the higher insertion loss in the SLOT-DLG EAM became evident: the short distance between the fabricated metal contacts and the slot waveguides. The slot waveguides exhibit larger evanescent wave tails outside the waveguide itself [222], necessitating a design with contacts placed further away from the slot waveguides to minimize the additional loss caused by the metal contacts. This adjustment in the layout could potentially mitigate the insertion loss and improve the overall performance of the SLOT-DLG EAMs, as will be discussed further in the outlook sections.

Given this loss issue, the performance of the STRIP-DLG EAMs and SLOT-DLG EAMs was compared by normalizing their minimum transmission and extracting the modulation depth (MD). The MD excludes the effect of IL and can be used to compare the pure DC performance of the devices. Figure 4.9(c) presents the MD as a function of normalized DC bias for both STRIP-DLG EAMs and SLOT-DLG EAMs with varying active lengths. Both device types exhibited comparable DC performance, with maximal MD values of 0.122 dB/μm for STRIP-DLG EAMs and 0.183 dB/μm for SLOT-DLG EAMs. Within a 2V span, modulation efficiencies of 0.026 $dB\mu m^{-1}V^{-1}$ and 0.038 $dB\mu m^{-1}V^{-1}$ were measured for STRIP-DLG EAMs and SLOT-DLG EAMs, respectively. While the latter value is comparable to state-of-the-art devices [146], the high insertion loss resulting from contact metal losses make our current SLOT-DLG EAMs unacceptable for practical applications. Therefore, in the outlook sections, we will delve into greater detail on potential improvement strategies and any necessary compromises.

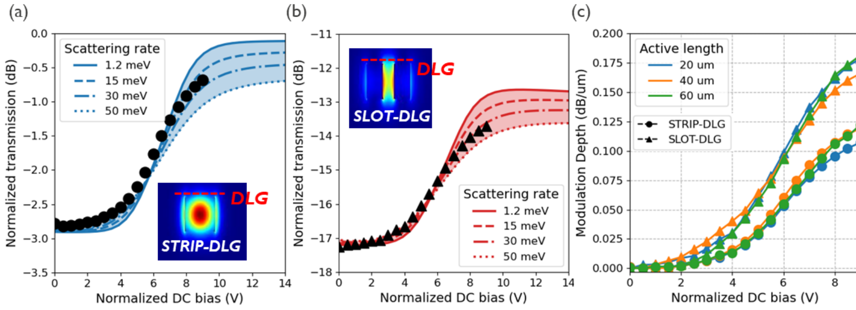

Figure 4.9: Normalized transmission as function of normalized DC bias for 20 µm (a) STRIP-DLG EAM and (b) SLOT-DLG EAM with simulated results in blue and red, respectively. (c) Modulation depth (MD) as a function of normalized DC bias for both STRIP-DLG EAMs and SLOT-DLG EAMs with 20, 40, and 60 µm active length.

4.4.2 EO dynamic performance of DLG EAMs

The electro-optical (EO) bandwidth of the DLG EAMs was evaluated by sweeping the frequency from 100 MHz to 25 GHz using a network analyser to retrieve the S-parameters. Figure 4.10(a) shows the normalized S21 values for STRIP-DLG EAMs of various lengths (20 µm, 40 µm, and 60 µm) and a SLOT-DLG EAM (20 µm). The extracted 3 dB bandwidth was determined to be 15.9 GHz for the 20 µm-long SLOT-DLG EAM and 15.9 GHz, 12.5 GHz, and 9.2 GHz for the 20 µm, 40 µm, and 60 µm long STRIP-DLG EAMs, respectively. The length-dependence in the results for the STRIP-DLG EAMs can be attributed to the influence of the 50 Ω impedance of the vector network analyzer (VNA) [161, 172]. To gain a deeper understanding of our devices, the measured S11 response was fitted using the equivalent circuit model depicted in Figure 4.10(a). In the model, C_{gog} represents the capacitance of the DLG structures, while R_{tot} represents the total resistance, combining the contact and sheet resistance of both graphene layers. C_{air}, C_s, and R_s denote the capacitance between the metal pads, the capacitance of the silicon substrate, and the resistance of the silicon substrate, respectively. As shown in Figure 4.10(b) and (c), the real and imaginary parts of the S11 response were successfully fitted using this model. The capacitance (C_{gog}) values were found to be 53 fF, 45 fF, 92 fF, and 139 fF for the 20 µm (SLOT-DLG EAM), 20 µm (STRIP-DLG EAM), 40 µm (STRIP-DLG EAM), and 60 µm (STRIP-DLG EAM) long devices, respectively. The corresponding R_{tot} values were found to be 101 Ω, 116 Ω, 47 Ω, and 43 Ω. Considering all the other parasitic components, the resulting electrical 3 dB bandwidths were calculated to be 16.9 GHz, 17.8 GHz, 15.2 GHz, and 10.7 GHz, respectively, which closely align with the values observed in our experiments.

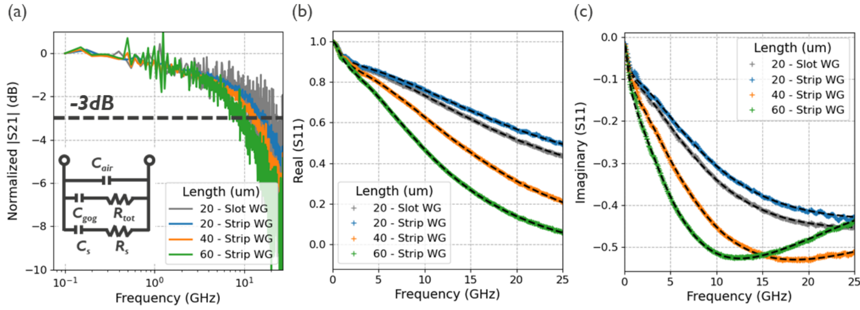

Figure 4.10: (a) Normalized S21 response and the model (b) Real and (c) imaginary part of S11 response and fitted results.

Non-return-to-zero eye diagram measurements using a pseudo-random binary sequence (PRBS) of length $2^{15} - 1$ further demonstrate the high speed of our DLG devices. Figure 4.11(a) shows the open eye diagrams at 10, 20 and 25 Gbps for the 40-μm-long STRIP-DLG with a drive voltage of 3.4 V and a DC bias of 4V at the wavelength of 1563 nm. The corresponding Q factors are 5.56, 4.54, and 3.84 and the bit error rate, $-log(BER)$, of 7.87, 5.32, and 4.19 are calculated. To further demonstrate the low driving voltage of our device, we show the eye opening at 25 Gbit/s when V_{pp} = 3 and 2.6 V, realizing a promising dynamic power consumption (E_{bit} = $CV^2/4$) of 155 fJ/bit. The value is comparable to state-of-art graphene-based modulators [24]. However, we are unable to collect any open eyes for slot-based DLG devices, which we blame to the massive insertion loss caused by the metal losses. We anticipate that by positioning the metal at a safer distance, slot-based DLG devices may be able to achieve comparable or even better eye diagrams than strip-based DLG devices.

4.5 DLG Mach-Zehnder modulators

Graphene strongly modulates not only its absorption but also its refractive index, making it a promising candidate for realizing phase modulators (PMs) as well. This section explores DLG-based MZM devices and compares the efficiency of devices using strip and slot waveguides. Figure 4.12 (a) and (b) depict a top-down perspective of a 2x2 MZM device with DLG integrated on strip and slot waveguides, respectively. Here, "MZM-STRIP-DLG" refers to the DLG MZM integrated on the strip waveguide, while "MZM-SLOT-DLG" refers to the DLG MZM integrated on the slot waveguide. In the MZM-STRIP-DLG, the input light is coupled by grating couplers and then divided by a multi-mode interferometer (MMI) into two

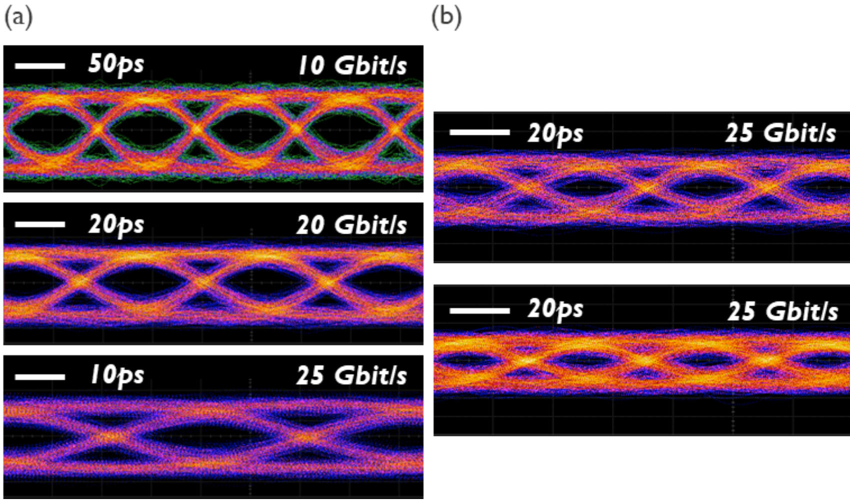

Figure 4.11: Optical eye diagram measured at 1563 nm for the strip-based device with 40 μm length. (a) Modulation speed of 10, 20, and 25 Gbit/s with a driving voltage of 3.4 V. (b) Modulation speed of 25 Gbit/s, using V_{pp} = 3 V (top) and 2.6 V (bottom).

paths. After passing through the DLG active area, the separated light beams are recombined at the output to interfere constructively or destructively. The MZM-SLOT-DLG comprises the same components as the MZM-STRIP-DLG, with the addition of two mode converters in each arm to convert strip waveguides to slot waveguides. Both types of devices are unbalanced with 40 μm of strip waveguide arm length difference. Compared to EAMs and RMs, MZMs generally require a larger area and lengthier waveguides for routing. Due to the high insertion loss in Al_2O_3, HfO_2-based devices are used to characterize the DLG MZM devices in this section.

Figure 4.12 (c) (top and bottom) presents the cross-sectional architecture of the designed MZMs. Similar to the EAMs, the silicon waveguide width utilized in the MZMs is 450 nm for strip waveguides and 680 nm (with 180 nm SiO_2 gap) for slot waveguides, intended for TE-polarized C-band operation. MZM-STRIP-DLG's metal offset and DLG width are designed with nominal values of 500 nm and 750 nm, respectively, while MZM-SLOT-DLG's metal offset and DLG width are designed with nominal values of 500 nm and 980 nm. The active lengths of 100, 200, and 400 μm are designed in MZM-STRIP-DLG, whereas shorter lengths (50, 100, and 200 μm) are designed in MZM-SLOT-DLG taking into account the anticipated improvement in modulation efficiency.

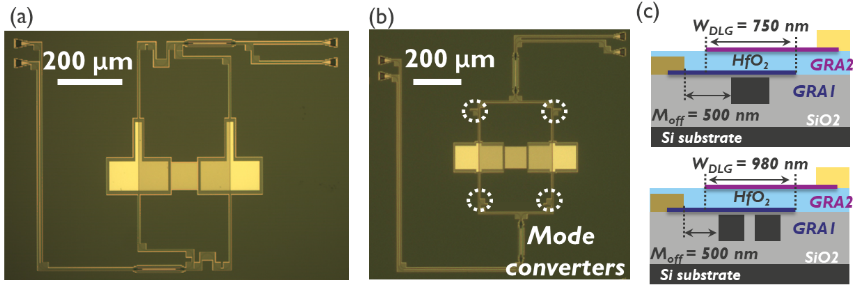

Figure 4.12: Top-down microscope images of (a) MZM-STRIP-DLG and (b) MZM-SLOT-DLG. (c) Schematic cross-section of MZM-STRIP-DLG (top) and MZM-SLOT-DLG (bottom).

4.5.1 EO static performance of DLG MZMs

First, we performed unbiased fiber-to-fiber transmission measurements on strip and slot based MZM before the DLG integration. In Figure 4.13 (a), interference fringes can be observed in the transmission spectra due to the length difference between the MZMs' arms. Both types of MZMs showed low insertion loss and a subtantial difference between the maximum and minimum transmission levels, indicating well-designed MZMs and accurately fabricated waveguides. After integrating the DLG, we repeated the measurements for the MZM-STRIP-DLG and the MZM-SLOT-DLG, as shown in Figure 4.13 (b) and (c), respectively. The MZM-STRIP-DLG, with an active length of 400 µm, and the MZM-SLOT-DLG, with an active length of 200 µm, were too lossy to be measured accurately. We collected a free spectral range (FSR) of 13.7 nm in both types of devices as expected. The ratio between the maximum and minimum transmission levels in the MZM-STRIP-DLGs (>20 dB) are consistently higher than in the MZM-SLOT-DLGs (<10 dB), indicating that the loss difference between the two MZM's arms are smaller in the MZM-STRIP-DLGs. This suggests that the left and right arms of the MZM-STRIP-DLGs provided a larger tolerance over DLG fabrication. On the other hand, greater DLG variation between arms was expected in MZM-SLOT-DLGs, most likely due to the slot waveguide's high sensitivity and e-beam exposure misalignment. The propagation loss of the DLG was calculated using the same method shown in Figure 2.14. The MZM-STRIP-DLG shows a propagation loss of 0.173 dB/μm, which is comparable to that in EAMs (Figure 4.5) while the MZM-SLOT-DLGs shows a propagation loss of 0.359 $dB\mu m^{-1}$. The reason for the reduced value compared to that collected in SLOT- DLG EAMs (0.7 $dB\mu m^{-1}$) was the safer design of the metal offset.

Next, the MZMs underwent biased fiber-to-fiber transmission measurements. In

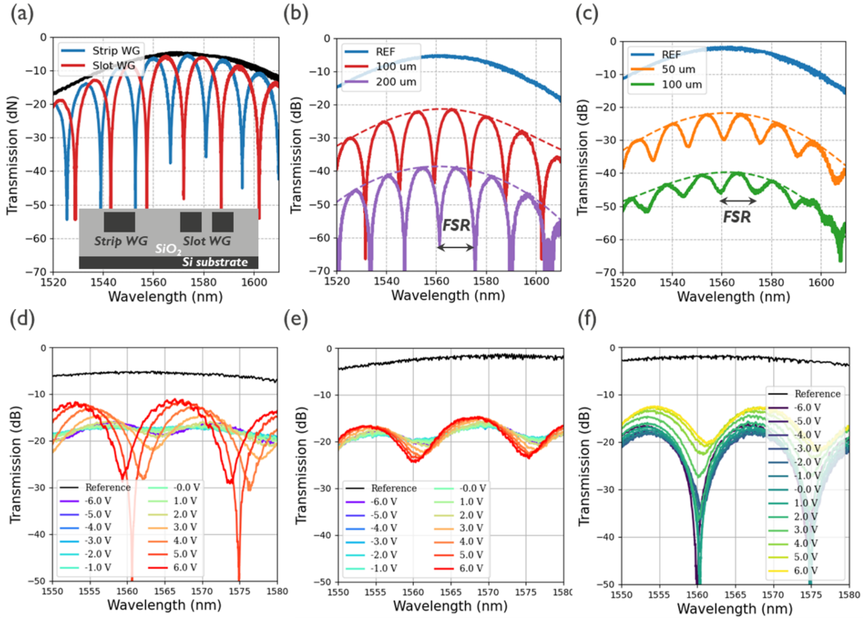

Figure 4.13: (a) Transmission of the passive strip and slot waveguides based MZM along with reference waveguides prior to DLG integration. The wavelength dependency and insertion loss originate from the grating couplers. Insets show the schematic cross-section of the passive structures. Transmission as a function of wavelength for (b) MZM-STRIP-DLG and (c) MZM-SLOT-DLG, with FSR both showing 13.7 nm. Fiber-to-fiber transmission spectra of (d) MZM-STRIP-DLG with 200 μm active length and (e) MZM-SLOT-DLG with 50 μm active length at different DC voltages. The voltage on the left arm is swept while a constant 6 V bias is applied on the right arm. (f) Fiber-to-fiber transmission spectra of the same MZM-SLOT-DLG shown in Figure 4.13 (e) with sweeping the bias on the right arm and a constant voltage on the left arm. Please note that the input power were not the same when measuring MZM-STRIP-DLG and MZM-SLOT-DLG, resulting in slightly different transmission in the reference waveguides.

order to maximize the transmitted power, one arm's DLG (right) was constantly biased at 6 V while the other arm's DLG (left) was subjected to a sweeping bias voltage. Figure 4.13 (d) and (e) show the wavelength-dependent transmission of a MZM-STRIP-DLG (200μm length) and a MZM-SLOT-DLG (50μm length) for a -6 V to 6 V voltage sweep. Clearly, when the applied bias is less than 2 V, the interference fringe visibility considerably decreases or even disappears. This is predominantly due to the loss difference between the left and right DLG, with the right arm being transparent and the left arm remaining absorptive. Due to the decreased absorption in the left DLG, the fringe depth for the MZM-STRIP-DLG increases with increasing bias and reaches its maximal value when V = 5V. At this voltage, the loss difference between the two arms is minimal, resulting in the greatest ratio. When V equals 6 V, the depth of the fringes decreases, which can be attributed to the lower loss in the left arm relative to the right arm. In an ideal situation, the maximum depth is achieved when the same voltage is applied to both arms. However, this condition can be affected by local graphene doping concentrations in the experimental devices. As shown in Figure 4.13 (e), the MZM-SLOT-DLG demonstrates a similar trend. Throughout the sweep, the fringe depth is always less than 10 dB. This leads us to the conclusion that, when the same voltage is applied to both arms of the MZM-SLOT-DLG, the left arm is more absorptive than the right arm. This can be confirmed by switching the way we apply voltage on both arms. In Figure 4.13 (f), the same MZM-SLOT-DLG is measured again, but this time with constant voltage applied to the left arm and sweeping the voltage applied to the right arm. We can find out that the highest ratio occurs when V = -6 V and 1 V, showing that the loss of the DLG in the right arm is comparable to that of the left arm. Above 1V, the right arm of the DLG becomes more transparent, resulting in a decrease of the visibility again. Here, a SEM inspection would be needed in order to confirm device's dimension on both arms but was not available at the time of writing.

To characterize and compare the efficiency of both types of MZMs, the wavelength shift of the fringes was measured and converted to a phase change using the following equation.

$$\Delta\phi = \frac{wavelengthshift}{FSR} 2\pi \tag{4.1}$$

Then by using Equation 2.8, we can further convert the change in phase to a change in effective index. Since the change in effective index is independent of length, it allows for a direct comparison of the efficiency between strip and slot-based MZMs as shown in Figure 4.14 (a). Both types of MZMs exhibit the typical up-and-down index modulation observed in simulations for biased DLG devices. As the voltage is swept from -2 to 2 V, effective index changes of 1.11×10^{-3} and 1.78×10^{-3} are

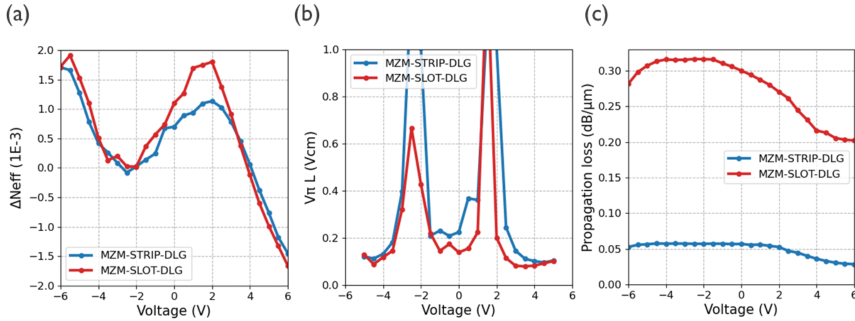

Figure 4.14: Calculated (a) effective index change, (b) $V_\pi L$, and (c) propagation loss as a function of DC bias for MZM-STRIP-DLG and MZM-SLOT-DLG shown in Figure 4.13 (d) and (e).

measured for strip and slot-based MZMs, respectively. Similar enhancements for the slot waveguide are observed in the voltage range of 2 to 6 V. This improvement is attributed to the enhanced mode interaction in the slot waveguides, which leads to increased performance. The efficiency of phase modulation ($V_\pi L$) can be calculated using Equation 2.9. Figure 4.14 (b) shows $V_\pi L$ as a function of voltage, and the best $V_\pi L$ values found for the MZM-STRIP-DLG and the MZM-SLOT-DLG are 0.0954 and 0.0789 V, cm, respectively. With a driving voltage of 2 V, this means that the MZM-STRIP-DLG and the MZM-SLOT-DLG require only 477 and 395 μm of DLG length to achieve a π-phase shift. These $V_\pi L$ values outperform the lowest reported values for lithium niobate (LN $\approx$ 1.8 V, cm) [223] and silicon-insulator-silicon (SIS $\approx$ 0.2-0.7 V, cm) [7, 224, 225] MZMs, and are comparable to III-V MZMs (0.047V, cm) [226].

Finally, to calculate the phase modulator's final figure of merit (FOM_{pm}), we extracted the insertion loss data from Figure 4.13 (d) and (f) for MZM-STRIP-DLG and MZM-SLOT-DLG, respectively. While an identical MZM structure without graphene would have been ideal as a reference to distinguish losses from passive waveguides and the DLG device, we lacked the space for such a design. Consequently, we assumed that all calculated insertion losses originated from the DLG itself. By normalizing the losses with the corresponding active length, the propagation loss of the DLG device as a function of DC bias was calculated, as shown in Figure 4.14 (c). Combining this information with that in Figure 4.14 (b), we obtained the best FOM_{PM} of 27.6 dBV for our MZM-STRIP-DLG at V_{DC} = 4.5 V, outperforming other graphene-based MZMs ($\approx$ 66-223 dBV) [27, 227], and comparable to SIS MZMs ($\approx$ 15-35 dBV) [7]. However, MZM-SLOT-DLG only shows FOM_{PM} of 168 dBV at V_{DC} = 3.5V due to the high propagation loss. This inspires us to further investigate the full parameter space in detail. Similar to what

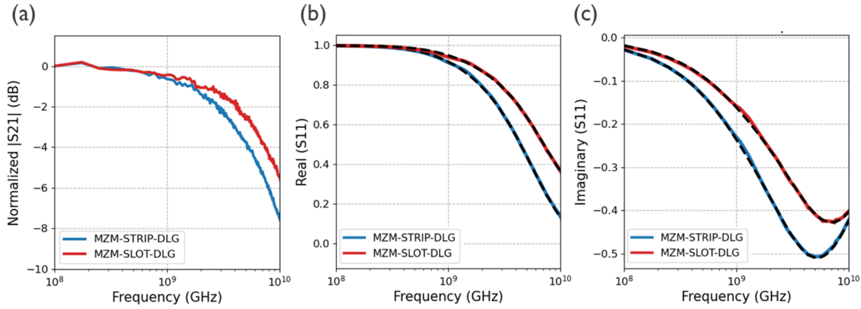

Figure 4.15: (a) Normalized S21 response, (b) real and (c) imaginary part of S11 response for MZM-STRIP-DLG and MZM-SLOT-DLG with 100 and 50 μm active length, respectively.

we learned in EAMs, we might benefit from an increased modulation efficiency due to enhanced light interaction in slot waveguides, but the current design also increases device losses. Therefore, a better strategy to balance modulation efficiency and loss will be discussed in the outlook section.

4.5.2 EO dynamic performance of DLG MZMs

To characterize the bandwidth of our DLG MZMs, S-parameter measurements were carried out by sweeping the frequency between 100 MHz and 10 GHz. In order to effectively measure the frequency response, one arm of the MZM was biased at a constant voltage (6V) by landing a DC probe from the north side, while the other arm was loaded with an RF probe from the south side. Via a bias tee, the RF probe's voltage signal is a composite of a sinusoidal voltage with an amplitude of -8 dBm and a DC voltage with a sweeping range between -6 and 6 V. In such a scenario, we can maximize transmitted power and capture EO frequency data with a high gain. In order to mitigate the effect of the 50 Ω impedance of the vector network analyzer (VNA) [161, 171], we measured only the MZM devices with the shortest length, namely MZM-STRIP-DLG with 100 μm and MZM-SLOT-DLG with 50 μm.

Figure 4.15 (a) depicts the normalized S21 results, and the extracted 3 dB bandwidth was determined to be 4.2 and 5.5 GHz, respectively. The greater bandwidth of the MZM-SLOT-DLG can be attributed to multiple factors, including the length of the DLG, the width of the DLG, and the metal offset. To gain a deeper comprehension of our devices, we fitted the measured S11 response using the equivalent circuit model depicted in Figure 4.10 (a). As demonstrated in Figure 4.15 (b) and (c), the model was able to effectively fit the real and imaginary components of the S11

response. C_{gog} was determined to be 287 fF for 100 μm MZM-STRIP-DLG and 175 fF for 50 μm MZM-STRIP-DLG, while R_{tot} was determined to be 44 and 81 Ω, respectively. The greater capacitance of the MZM-STRIP-DLG is primarily due to the device's extended length. After normalizing with the nominal DLG width and length, similar capacitance density values are collected, which is to be expected since they are fabricated on the same sample with the same gate oxide.

Regarding total resistance, since the access length (edge of metal to edge of DLG) in both types of MZMs is the same (350 nm), it is presumed that they have the same value of normalized resistance ($\Omega\, \mu m$), just like the contact resistance. Consequently, the total resistance is determined primarily by the length of the devices, and normalized total resistance values of 4400 and 4050 $\Omega\, \mu m$ were obtained in the experiment. The value is sufficiently close to prove our hypothesis, with a small deviation possibly resulting from regional graphene quality. With S11-fitted capacitance and resistance and equation 2.13 and equation 2.14, we calculate the intrinsic bandwidth to be 12.6 and 11.2 GHz, which decreases to 5.9 and 6.8 GHz when the 50Ω load resistance from the driver is taken into account. If we use capacitance density and normalized resistance to calculate the electrical bandwidth for a 10-μm-long DLG, we will obtain the same intrinsic bandwidth values, but the 3dB bandwidth will increase to be 12.0 and 10.6 GHz, which is much closer to the intrinsic bandwidth. Therefore, shorter devices are preferred for demonstrating the limit of electrical bandwidth, despite the fact that it can result in a trade-off with DC performance.

4.6 DLG ring modulators

In the previous sections, we explored the potential of EAMs and MZMs for amplitude and phase modulation, respectively. However, implementing these devices into practical optical communication systems poses design difficulties. EAMs require large extinction ratios (ER), typically 4 dB and 8 dB for 2 km and tens of km transmission links, respectively, to ensure a high signal-to-noise ratio and maintain a low bit error rate [228–232]. To meet these requirements, our strip-based DLG EAM requires DLG lengths of 33 and 67 µm, and even longer lengths are needed when considering CMOS-compatible driving voltages (lesser than 2V). However, such extended active lengths cause the 50-ohm impedance from the driver to dominate the frequency response, hindering the demonstration of the DLG's intrinsic bandwidth. Changing the width of the DLG and the thickness of the gate oxide can improve the situation, but it leads to trade-offs between speed, efficiency, and loss. Similarly, although our DLG MZMs outperform state-of-the-art graphene-based MZMs [27, 227], active lengths of hundreds of micrometers are still required to

achieve a pi-phase shift, resulting in a large capacitance and high power consumption. Moreover, the larger physical dimensions of MZMs also limit their integration in high-density photonic circuits. Therefore, exploring DLG-based ring resonator modulators (RMs) becomes an intriguing research direction to overcome or mitigate these restrictions.

Unlike EAMs, the transmission of an RM is dependent on the incident wavelength; thus, both the real and imaginary components of the index change modulate the RM's transmission spectrum [44]. The light travels through thousands of cycles in the ring waveguide, making even a small change in the refractive index result in a significant shift in the resonant wavelength, effectively modulating the light's intensity. Additionally, RM devices are extremely compact, with a radius of only tens of micrometers [6, 28], making them well-suited for compact applications like short-reach interconnects with high device density.

Figure 4.16 (a) illustrates a top-down view of RM devices with DLG established on strip (top) and slot (bottom) waveguides, following the same processing flow as used for EAMs and MZMs. "RM-STRIP-DLG" refers to the DLG RM with a strip waveguide (Figure 4.16 (b)), whereas "RM-SLOT-DLG" refers to the DLG RM with a slot waveguide (Figure 4.16 (c)). Both waveguides have the same dimensions as those used in EAMs. The nominal width of the DLG (750 nm) and the metal offset (500 nm) are the same for the RM-STRIP-DLG and the RM-SLOT-DLG. The ring radius is set at 50 μm for both types of RMs, while the active length is 10 μm for RM-STRIP-DLG and 4 μm for RM-SLOT-DLG. Additionally, one converter is incorporated in the bus waveguide to seamlessly convert strip mode to slot mode, enabling slot waveguides based ring resonator. In the subsequent subsections, HfO_2-gated devices are chosen for characterization and further discussion.

4.6.1 EO static performance of DLG RMs

The static performance of the devices was characterized through biased fiber-to-fiber transmission measurements after DLG integration. Similar to EAMs, the bias voltage was swept from -6 to 6 V, with the source connected to contact 2 and the ground connected to contact 1. To ensure reliable measurements, the wavelength was swept from 1530 nm to 1600 nm with a 10 dBm attenuation to counteract self-heating in the ring resonators [233–235]. RM-STRIP-DLG and RM-SLOT-DLG devices with gap distances of 150 nm and 345 nm, respectively, were identified as the devices closest to critical coupling when DC bias = 0V, as depicted in Figure 4.17 (a) and (d). Measured insertion losses were 0.1 dB and 0.46 dB for RM-STRIP-DLG and RM-SLOT-DLG, with corresponding free spectral ranges (FSRs) of 1.76 nm and 2.77 nm. RM-SLOT-DLG exhibited higher insertion

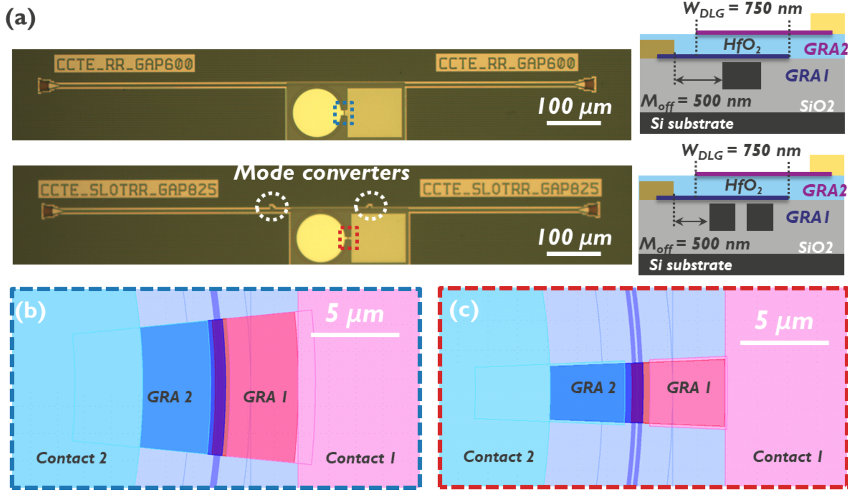

Figure 4.16: (a) Top-down microscope images of RM-STRIP-DLG (top) and RM-SLOT-DLG (bottom). Layout of (b) RM-STRIP-DLG and (c) RM-SLOT-DLG.

loss due to additional losses in the coupling region and higher propagation loss in the slot waveguides, while the larger FSR was a result of the lower index in the slot waveguide. Figure 4.17 (b) and (e) show the transmission of RMs with the entire voltage sweeping range. As the voltage (V) increases from 0 to 6 V, the depth of the dips in RM-STRIP-DLG and RM-SLOT-DLG decreases by approximately 25 dB and 5 dB, respectively. Assuming that the self-coupling coefficient (t) does not vary with voltage, this decrease in depth can be attributed to the modulators' changing absorption. The reduction in depth also indicates that the coupling of these ring modulators shifted from critical coupling to over-coupling or under-coupling, resulting in an increase in transmission through the bus waveguide. This effect has been exploited to create optical switches with high sensitivity [236, 237].

With a V_{pp} of 2V, RM-STRIP-DLG and RM-SLOT-DLG demonstrated maximum extinction ratios of 7.9 dB and 2.6 dB, and insertion losses of 8.1 dB and 10.2 dB, respectively. Then, a TP of 9.44 dB and 14.3 dB is calculated for RM-STRIP-DLG and RM-SLOT-DLG, respectively, at 1549.444 nm and 1549.706 nm, as shown in Figure 4.17 (c) and (f). The optimum TP of the RM-STRIP-DLG is similar to the value observed in EAMs (STRIP-DLG EAM's TP = 8.9 dB) at the same 2V peak-to-peak voltage. Regarding RM-SLOT-DLG, it demonstrates an improved TP value compared to that of SLOT-DLG EAM (>20 dB), which can be attributed to the reduced insertion loss brought about by the safer design in the metal offset. However, the improved metal offset may still not be enough to suppress the additional loss coming from the metal contacts in the RM-SLOT-DLG,

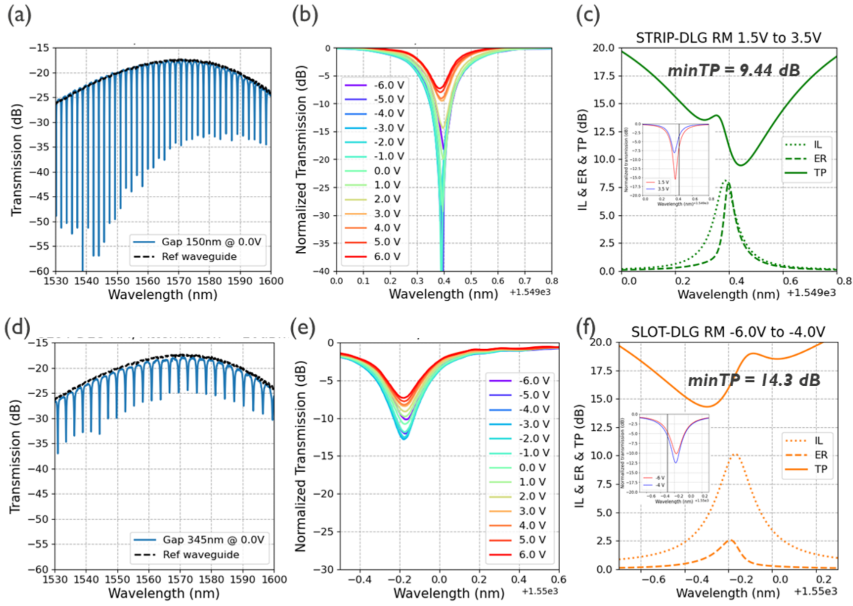

Figure 4.17: RM-STRIP-DLG's (a) transmitted optical power spectrum at bias = 0 V, (b) transmitted power versus wavelength for the entire voltage sweep, and (c) ER, IL TP spectra calculated from the DC data of Figure 4.17 (b) for voltage swing from 1.5 V to 3.5 V. RM-SLOT-DLG's (d) transmitted optical power spectrum at bias = 0 V, (e) transmitted power versus wavelength for the entire voltage sweep, and (f) ER, IL TP spectra calculated from the DC data of Figure 4.17 (e) for voltage swing from -6 V to -4 V.

which results in a higher TP value compared to RM-STRIP-DLG. The minimum TP for RM-STRIP-DLG and RM-SLOT-DLG with V_{pp} = 1V was 11.75 dB and 15.39 dB, respectively, comparable to Si-based ring modulators [238]. Enhancements in graphene quality and optimized DLG dimensions could further improve the TP. Details on simulated improvements will be discussed in the outlook section.

Next, the phase modulation of the RM was characterized by fitting the transmission results with equation 1.11 for each applied bias. Figure 4.18 (a) compares the corresponding ring losses for the two types of RMs. The absorption of the DLG played a significant role in the change of the ring's loss. As the voltage increased from -3 V to 6 V, the absorption in RM-STRIP-DLG decreased from 160 $dBmm^{-1}$ to 66 $dBmm^{-1}$, resulting in a modulation depth of 94 $dBmm^{-1}$. Conversely, the absorption in RM-SLOT-DLG remained consistently higher, ranging from 384 dB/mm to 235 dB/mm due to the increased mode interaction in the slot waveguides. The modulation depth of 149 $dBmm^{-1}$ in the RM-SLOT-DLG represents an enhancement of approximately 60%, which is comparable to what we

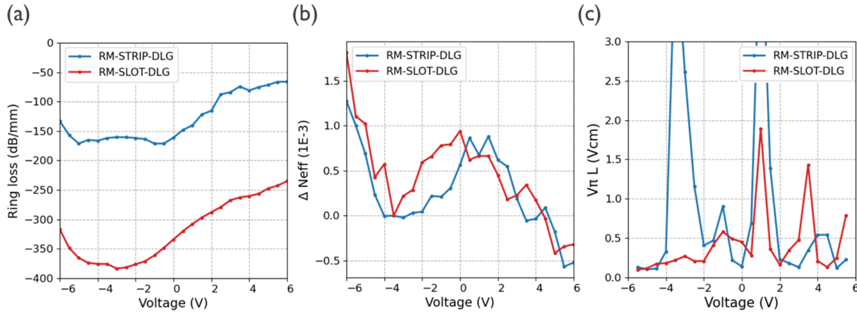

Figure 4.18: Calculated (a) effective index change, (b) $V_\pi L$, and (c) propagation loss as a function of DC bias for RM-STRIP-DLG and RM-SLOT-DLG shown in Figure 4.17 (b) and (e).

have found in EAMs.

The corresponding effective index, denoted as Δn, was determined by measuring the change in effective index relative to the Dirac point (when V = -3.5 V). In Figure 4.18 (b), we observe that Δn is positive when the applied voltage sweeps from -3.5 V to 0 V but becomes negative as the voltage increases. This behavior is consistent with the simulation performed in Chapter 2, where Δn >0 when E_F <0.4 eV and Δn <0 when E_F >0.4 eV. Surprisingly, mode-enhanced slot waveguides did not provide a significant enhancement in Δn, which could be attributed to the variation in graphene quality and the relatively small wavelength shift effect. Longer devices and/or a larger FSR may facilitate better detection of the resonance wavelength shift, offering an opportunity for future improvements.

However, despite the lack of significant enhancement in Δn, the efficiency of phase modulation can still be calculated using equation 2.9 at V_{pp} = 2V. Figure 4.18 (c) shows the $V_\pi L$ as a function of voltage. The best $V_\pi L$ values for RM-STRIP-DLG and RM-SLOT-DLG are 0.101 Vcm and 0.097 Vcm, respectively, when V <0 V, and 0.118 Vcm and 0.132 Vcm when V >0 V. After considering the propagation loss shown in Figure 4.18 (a), this leads to FOM_{PM} = 78 dBV in RM-STRIP-DLG when DC bias = 5 V. On the other hand, the RM-SLOT-DLG demonstrates a poor FOM_{PM} value of 308 dBV at a DC bias voltage of -5.5 V. The main limiting factor in the performance of the slot waveguide-based RM is the increased optical loss. We believe that the RM-SLOT-DLG can be further improved through design and fabrication optimization, offering a new platform with greater design trade-off flexibility, as discussed in the outlook section.

4.6.2 EO dynamic performance of DLG RMs

Due to damage to the sample (Sample 1) used to discuss the static performance, we were unable to characterise the EO bandwith on the identical device depicted in Figure 4.17. Instead, we present the bandwidth results for a similar sample (Sample 2) with identical design of waveguide and DLG dimensions. The gate oxide is also HfO_2 with a nominal thickness of 10 nm. The only difference is that after the gate oxide deposition, we conducted an annealing step to remove the polymer residue from the top of the first layer graphene. The annealing process is anticipated to reduce graphene carrier mobility while simultaneously enhancing contact resistance, which may compensate for the bandwidth reduction. Figure 4.19 (a) and (b) illustrate the DC response of Sample 2's RM-STRIP-DLG and RM-SLOT-DLG, respectively. As no attenuation was applied, the high-power laser is responsible for the asymmetric resonance valleys. However, except for the asymmetry, the DC performances is comparable with those of Sample 1 devices (Figure 4.17).

Upon increasing the bias voltage from 2 to 6 V, we observed that the full width half maximum (FWHM) of the RM-STRIP-DLG decreased from 0.196 to 0.159 nm, which corresponds to an increase in Q-factor from 7942 to 9785 when using equation 1.13. With the same bias range, the FWHM of the RM-SLOT-DLG decreases from 0.317 to 0.265 nm, equivalent to a Q-factor increase from 4924 to 5887. Due to the shorter carrier lifetime (equation 1.14), a smaller Q-factor results in a greater f_{cav}. At 6V, f_{cav} of 19.6 and 32.6 GHz are calculated for RM-STRIP-DLG and RM-SLOT-DLG, respectively, using equation 1.15.

The S-parameters were measured by scanning the frequency from 100 MHz to 30 GHz with -8 dB of RF power and a DC bias voltage swept from -2 to 6 V. In order to comprehend the effect of wavelength, we also conducted a wavelength survey that encompassed the entire wavelength of the resonance valley. The real and imaginary components of the S11 response in RM-STRIP-DLG (RM-SLOT-DLG) are depicted in Figure 4.19 (c) and (d) (Figure 4.19 (e) and (f)), respectively, along with the fitting result using the equivalent circuit model depicted in Figure 4.10's insert. The values of C_{GOG} and R_{tot} that resulted in optimal fitting for RM-STRIP-DLG and RM-SLOT-DLG are plotted in Figure 4.20 (a) and (b) for RM-STRIP-DLG and (c) and (d) for RM-SLOT-DLG, respectively. When the bias is decreased, a small reduction in capacitance is observed in both kinds of RMs, which can be attributed to the graphene quantum capacitance [30]. Around the graphene neutrality point, the graphene quantum capacitance has a small value, which will dominate and reduce the overall capacitance. Similarly, the increase in R_{tot} is largely caused by the decrease in graphene mobility as E_F approaches the graphene neutrality

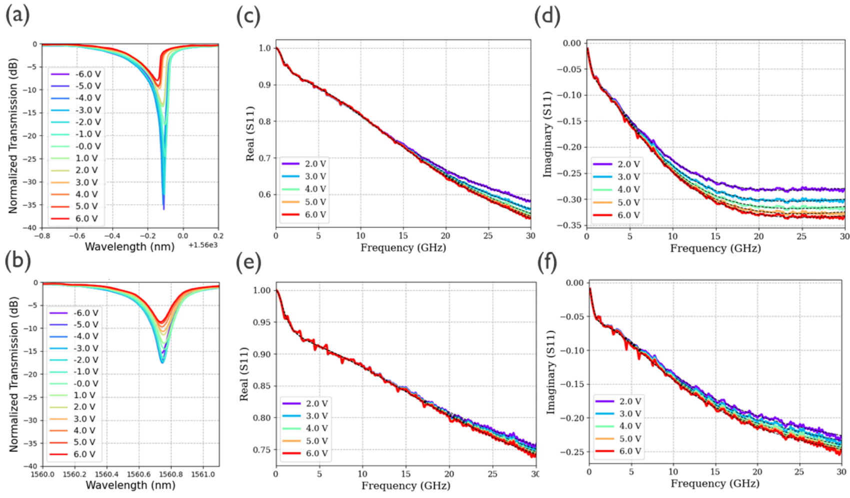

Figure 4.19: Normalized transmission as a function of wavelength with bias voltage swept from -6 to 6 V in (a) RM-STRIP-DLG and (b) RM-SLOT-DLG. (c) The real and (d) imaginary part of S11 response for the voltage swept from 2 to 6 V in RM-STRIP-DLG. (e) The real and (f) imaginary part of S11 response for the voltage swept from 2 to 6 V in RM-SLOT-DLG (all results from sample 2).

point [239–241].

At 6 V, the median capacitance values for RM-STRIP-DLG and RM-SLOT-DLG are 43 and 18 fF, while the median total resistance values are 132 and 331 Ω. On the basis of these values, intrinsic electrical bandwidths of 28.0 and 26.9 GHz and 3-dB bandwidths of 20.3 and 23.3 GHz are calculated. Since the RM-SLOT-DLG has a reduced length and consequently a higher resistance, the 50 Ω impedance from the driver has less of an effect on the 3dB bandwidth. Figure 4.20 (e) depicts the RC electrical bandwidth derived from the S11 fitting using the entire equivalent circuit (including C_s and R_s). Similar to what was just discussed, the RC electrical bandwidth is greater in RM-SLOT-DLG (median value = 21.3 GHz at 6V) than in RM-STRIP-DLG (median value = 18.6 GHz at 6V) due to the reduced impact of the driver. As shown in Figure 4.20 (f), we can use the equation 1.16 to calculate the overall bandwidth, which takes into account both RC delay and carrier lifetime. The median estimated bandwidth at 6V DC bias for RM-STRIP-DLG and RM-SLOT-DLG is 13.5 and 17.8 GHz, respectively. The larger value of RM-SLOT-DLG can be attributed to the shortened carrier lifetime and reduced impact of the driver, which are the two primary benefits of slot waveguides. Table 4.1 provides a summary of all values presented in Figure 4.20.

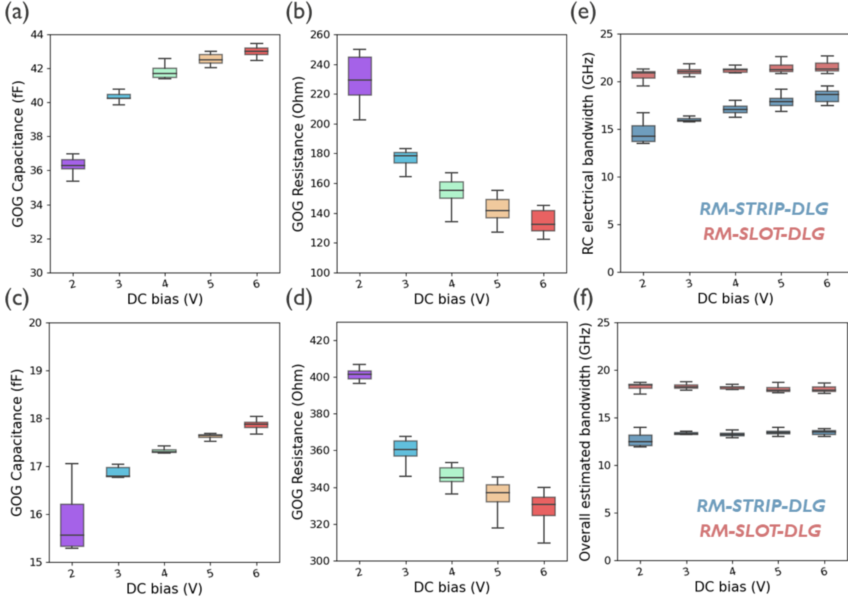

Figure 4.20: (a) DLG Capacitance and (b) DLG total resistance resulting in optimal fit for RM-STRIP-DLG as a function of DC bias. (c) DLG Capacitance and (d) DLG total resistance resulting in optimal fit for RM-SLOT-DLG as a function of DC bias. (e) Calculated RC electrical bandwidth and (f) overall estimated bandwidth as a function of DC bias for both types of DLG RMs.

Table 4.1: Summary of the S11 fitting results and calculated bandwidth for RM-STRIP-DLG and RM-SLOT-DLG at various bias.

Devices	Bias	C_{GOG}	R_{tot}	f_{RC}	f_{cav}	$f_{overall}$
-	[V]	$[fF]$	[Ω]	$[GHz]$	$[GHz]$	$[GHz]$
RM-STRIP-DLG	2	36.5 ± 1.1	228 ± 20	14.5 ± 0.9	25.5	12.6 ± 0.6
RM-STRIP-DLG	3	40.4 ± 0.5	175 ± 9	16.1 ± 0.5	24.2	13.4 ± 0.3
RM-STRIP-DLG	4	41.8 ± 0.3	154 ± 9	17.1 ± 0.6	21.0	13.2 ± 0.3
RM-STRIP-DLG	5	42.5 ± 0.3	143 ± 8	17.8 ± 0.7	20.4	13.4 ± 0.3
RM-STRIP-DLG	6	43.0 ± 0.3	134 ± 7	18.4 ± 0.6	19.6	13.4 ± 0.3
RM-SLOT-DLG	2	15.8 ± 0.5	398 ± 11	20.6 ± 0.6	39.0	18.2 ± 0.4
RM-SLOT-DLG	3	16.9 ± 0.2	358 ± 9	21.1 ± 0.4	36.7	18.3 ± 0.3
RM-SLOT-DLG	4	17.3 ± 0.1	343 ± 10	21.3 ± 0.5	35.2	18.2 ± 0.3
RM-SLOT-DLG	5	17.6 ± 0.1	334 ± 11	21.4 ± 0.6	33.2	18.0 ± 0.3
RM-SLOT-DLG	6	17.8 ± 0.1	328 ± 10	21.6 ± 0.6	32.6	18.0 ± 0.3

Figure 4.21 (a) and (b) depict the normalized S21 response in a RM-STRIP-DLG and a RM-SLOT-DLG, with the laser wavelength = 1559.8 nm and 1560.8 nm, respectively. Here, a 'peaking' effect is evidently observed, resulting in a bandwidth that far exceeds the anticipated values. Several experimental studies [234, 242–245] have demonstrated that peaking is a transient modulator response resulting from more complex time dynamics in the optical domain. When peaking occurs, it indicates that the system has a greater gain or sensitivity at specific frequencies, which can cause a temporary increase in signal intensity or distortion. Peaking in the transient modulator response can be caused by a number of factors, including nonlinearity, optical dispersion, and the ring's resonant behavior [41, 245, 246]. For the RMs to be practically applicable in high-density optical communication systems, it is necessary to strike a balance between optical modulation efficiency and modulation bandwidth [245]. Commonly, RMs are operated at the wavelength with the lowest TP. Due to the fact that a distinct sample is used for S-parameter measurement and the actual optical power used in the RF measurement is significantly higher than that used in the DC measurement, the optimized wavelength calculated in the DC measurement may not be suitable for the RF measurement. Consequently, we attempt to determine the optimal operational wavelength by monitoring the S21 magnitude. A greater S21 magnitude indicates a larger signal transmitted through the device under test (DUT) relative to the input signal.

Figure 4.21 (c) and (d) depict the S21 magnitude at 100MHz for RM-STRIP-DLG and RM-SLOT-DLG, respectively, using a voltage sweep and a wavelength sweep. S21 has a larger magnitude across the entire wavelength sweep when bias = 4 V because it is at the slope of the modulation with a relatively modest insertion loss. Maximum S21 magnitude appears when wavelength is 1559.6 nm and 1560.4 nm in RM-STRIP-DLG and RM-SLOT-DLG, respectively; the S21 magnitude then decreases, increases, and decreases once more, resulting in a second peak wavelength of 1559.8 nm and 1560.7 nm. The overall behavior resembles the TP trend depicted in Figure 4.17. For optimal optical modulation efficiency in RM-STRIP-DLG (RM-SLOT-DLG), EO bandwidth of 10.7 GHz (15.1 GHz) is achieved when the first peak wavelength is 1559.6 nm (1560.4 nm) and bias is 4 V (4 V). These values obtained from S21 are comparable to those estimated from S11 and Q-factor (13.5 and 17.8 GHz, respectively). In the ring modulator, the EO bandwidth is wavelength-dependent and will be significantly affected by the wavelength detuning of the resonance peak [245]. The same pattern can be seen in our DLG RMs, as shown in Figure 4.21 (e) and (f). If the operating wavelength shifts from the position of maximal S21 magnitude away from the resonance, the EO bandwidth will increase. In contrast, the EO bandwidth decreases when the operation wavelength shifts from the position of maximal S21 magnitude towards resonance. Experimentally, it is possible to obtain EO bandwidths in excess of 30 GHz. However, the modulation efficiency suffers significantly as a result. In order

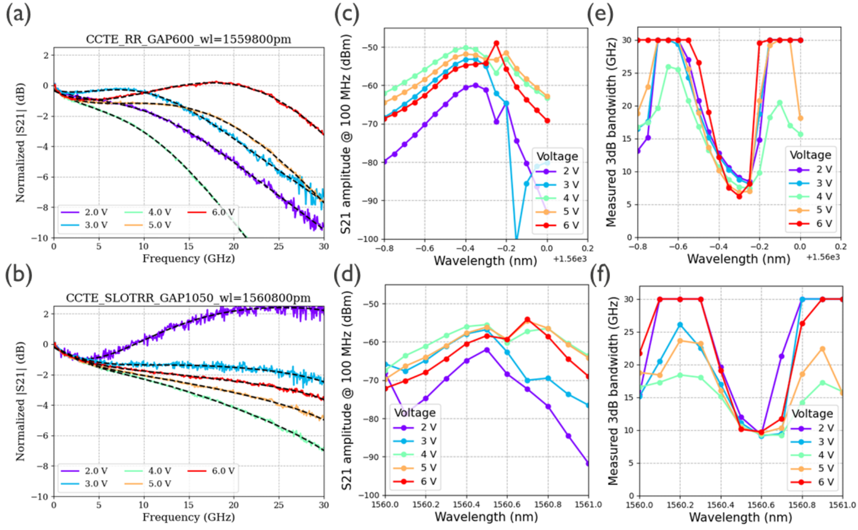

Figure 4.21: Normalized S21 response of (a) RM-STRIP-DLG with wavelength = 1559.8 nm, and (b) RM-SLOT-DLG with wavelength = 1560.8nm. S21 amplitude at 100 MHz as a function of wavelength for (c) RM-STRIP-DLG and (d) RM-SLOT-DLG. Corresponding 3dB bandwidth as a function of wavelength for (e) RM-STRIP-DLG and (f) RM-SLOT-DLG. Kindly be aware that the maximum 3dB bandwidth is restricted to 30 GHz, as determined by the setup.

to optimize the optical modulation efficiency and modulation bandwidth in a ring modulator for the intended applications, a solid strategy is required.

4.7 Outlook

To achieve a high-performance modulator, it is crucial to exhibit a sufficiently large extinction ratio (ER), a low insertion loss (IL), and a wide bandwidth at a CMOS-compatible drive voltage [22]. It is desirable to keep the peak-to-peak drive voltage (V_{pp}) as low as possible, preferably below 2 V. By doing so, one can effectively minimize system-level power consumption. By employing a slot waveguide, the modulation efficiency of a DLG EAM can be significantly improved. To explore the true potential of a SLOT-DLG EAM, substantial simulations were conducted to investigate the impact of three device parameters: the metal offset (M_{off}), the gate oxide thickness (d_{ox}), and the width of the DLG (W_{DLG}), as defined in Figure 4.22(a). In the simulations, we utilized a conservative value for the graphene scattering rate (15 meV) and normalized contact resistance (500 $\Omega\,\mu m$). It is important to note that the optical simulation was simplified by not

considering initial doping. The gate oxide between graphene 1 and graphene 2 is Al_2O_3 with a dielectric constant of 7.8 [247, 248]. The electrical bandwidth was calculated using the formula $f[Hz] = 1/(2\pi(R_{tot}[\Omega] + 50[\Omega])C_{gog}[F])$, where 50Ω represents the impedance from the driver. Although the product $R_{tot}C_{gog}$ is in principle length independent, this constant impedance introduces a length dependence in the electrical bandwidth. Devices with a shorter active length (larger resistance) are less influenced by the 50 Ω impedance compared to devices with a longer active length (smaller resistance). Therefore, determining the appropriate active length is crucial for a fair comparison. In our subsequent simulations, we choose the condition "ER = 4 dB at V_{pp} = 2 V" and "π phase shift at V_{pp} = 2 V" as the criterion for all simulated EAMs and PMs, respectively. Please note that we assume all the simulated devices as lumped capacitive devices, which simplifies the bandwidth calculation. However, in reality, a traveling-wave design is typically used for MZMs owing to its long active length. Therefore, the bandwidth calculation of PMs here may not be realistic and can only provide a basic idea.

4.7.1 Metal offset

The first parameter we investigated is the metal offset M_{off}, ranging from 200 nm to 1000 nm, with d_{ox} = 20 nm and W_{DLG} = 650 nm and 740 nm for STRIP-DLG EAMs and SLOT-DLG EAMs, respectively. When the metal contacts are sufficiently far from the waveguides, the devices only exhibit the (desired) loss of the DLG EAMs, as indicated by the shaded bands in Figure 4.22(b). However, as the metal contacts are placed closer together, the loss increases exponentially. Figure 4.22(b) shows that SLOT-DLG EAMs require roughly twice the M_{off} compared to STRIP-DLG EAMs to mitigate the loss. Next, we present the absorption as a function of DC bias using a safe metal offset value (M_{off} = 1000 nm for both). Figure 4.22(c) shows that SLOT-DLG EAMs exhibits a higher modulation depth than STRIP-DLG EAMs but also a higher overall loss. This figure also shows that, due to the stronger modulation in SLOT-DLG EAMs, the required device length to satisfy the condition imposed on the extinction ratio is approximately half that of STRIP-DLG EAMs. After determining the length of both devices for a given DC bias, we calculate the associated TP and bandwidth, as shown in Figure 4.22(d). With a DC voltage V_{DC} = 7V, SLOT-DLG EAMs achieve the minimum length (around 42 μm) and the largest bandwidth (8.3 GHz). However, due to the higher loss at this point (4.9 dB), the TP value of 10.11 dB is not the best. We notice the minimal TP value (8.98 dB) occurs when V_{DC} = 8V. More importantly, it comes with only a slight reduction in bandwidth (8.0 GHz). Therefore, this point can be considered as the best compromise between TP and bandwidth. In Figure 4.22(e), this analysis has been repeated for EAMs with varying M_{off} values. Although

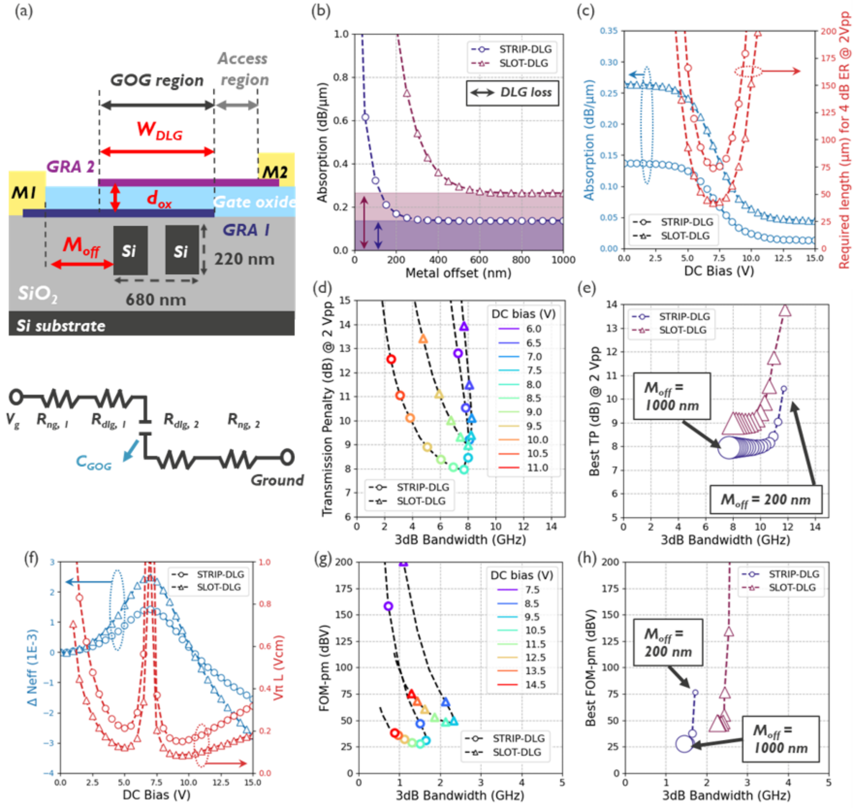

Figure 4.22: (a)A 2D schematic of DLG EAM integrated on a slot waveguide. Three key design parameters are defined: M_{off}, d_{ox} and W_{DLG}. The equivalent electrical circuit of the DLG EAM is shown below, where V_g, R_{ng}, R_{dlg}, and C_{GOG} represent the input voltage, the resistance of the non-gated graphene section (including the contact resistance), the resistance of the gated graphene, and the capacitance of the device, respectively. Bandwidth is calculated with 8×11^{11} cm^{-2} (equivalent to $E_F \approx 0.1$ eV) [30] for the graphene in the access regions to avoid an infinite resistance. A contact resistance of 500 $\Omega\,\mu m$ is considered for both graphene layers. (b) Simulated absorption as a function of M_{off} for STRIP-DLG EAMs and SLOT-DLG EAMs with wavelength = 1550 nm at the neutrality point (graphene chemical potential at 0 eV). The shaded bands indicate the (desired) loss of the DLG EAMs. The additional loss for smaller M_{off} stems from metal absorption. (c) Simulated absorption (blue curves) and required length for ER=4V at 2 V_{pp} (red curves) as a function of DC bias for both STRIP-DLG EAMs and SLOT-DLG EAMs with M_{off} = 1000 nm. (d) Simulated TP and the corresponding calculated bandwidth based on the results in Figure 4.22(c). (e) Best TP-bandwidth compromise for both device types with M_{off} ranging from 200 nm to 1000 nm (step = 50 nm), as illustrated by the size of the markers. (f) Simulated change of effective index (blue curves) and required length for π phase shift at 2 V_{pp} (red curves) as a function of DC bias for both STRIP-DLG PMs and SLOT-DLG PMs with M_{off} = 1000 nm. (g) Simulated FOM_{pm} and the corresponding calculated bandwidth based on the results in Figure 4.22(f). (h) Best FOM_{pm}-bandwidth compromise for both device types with M_{off} ranging from 200 nm to 1000 nm (step = 50 nm), as illustrated by the size of the markers.

there is a small increase in bandwidth (from 8 to 12 GHz) when M_{off} is decreased, the insertion loss (IL) and TP rise significantly if the metal contacts are placed too closely together. We found M_{off} = 450 nm and 750 nm to strike a good balance between TP and bandwidth for DLG-STRIP EAMs and DLG-SLOT EAMs, respectively. For this choice of parameters, the metal loss is less than 1e-3 dB/μm in both cases, resulting in a required length of approximately 47 μm (83 μm), IL of 3.8 dB (2.8 dB), ER of 4 dB (4 dB), TP of 9.01 dB (8.00 dB), and bandwidth of 9.2 GHz (10.0 GHz) for the SLOT-DLG EAM (STRIP-DLG EAM).

In the context of phase modulators, we investigated the variation of effective index with DC bias at M_{off} = 1000 nm, as illustrated in Figure 4.22(f). Due to the enhanced mode interaction in slot waveguides, SLOT-DLG PMs show a constantly larger index modulation. At V_{DC} = 9.25 V, SLOT-DLG and STRIP-DLG PMs achieved the best $V_{\pi}L$ values of 0.085 and 0.151, respectively, enabling devices with lengths of 427 μm and 755 μm to achieve a π shift at V_{pp} = 2 V. Considering the absorption at the same voltage point, we calculated corresponding FOM_{pm} values of 51.8 and 33.4 dBV, respectively. However, we notice the minimal FOM_{pm} value of 47.8 dBV (27.9 dBV) occurs when V_{DC} = 10 V (10.75 V) for SLOT-DLG PM (STRIP-DLG PM) with only a slight reduction in bandwidth. Consequently, this datapoint was considered as the optimal compromise between optical and electrical performance for DLG phase modulators. The better FOM_{pm} value in STRIP-DLG PMs can be explained by the lower absorption in STRIP-DLG modulator (221 dB/cm) compared to that in SLOT-DLG modulator (607 dB/cm). Notably, the main contributor to device loss in both waveguides was the DLG region itself rather than the metal contacts, which were strategically placed far away. The higher loss in SLOT-DLG modulators stemmed from the skin-depth expansion of evanescent waves [222], resulting in larger tails outside the waveguide. Due to the current W_{DLG} value (740 nm in SLOT-DLG modulator), the DLG region was not long enough to cover the mode tail expansion in the slot waveguide, leading to a strong mode interaction on absorptive and un-modulable graphene in the access region. Finally, Figure 4.22(h) shows the analysis for PMs with varying M_{off} values. We can clearly observe that the bandwidths do not improve by reducing the M_{off} and are consistently smaller than what were simulated for EAMs. The main reason is that the active length is approximately one order longer in PMs compared to EAMs, which makes 50 Ω impedance from driver dominate the RC delay. However, one similar trend is observed in Figure 4.22(h): the insertion loss (IL) and FOM_{pm} rise significantly when the metal contacts are placed too closely together. Therefore, in conclusion, we select M_{off} = 450 nm and 750 nm to strike a good balance between FOM_{pm} and bandwidth for DLG-STRIP PMs and DLG-SLOT PMs, respectively.

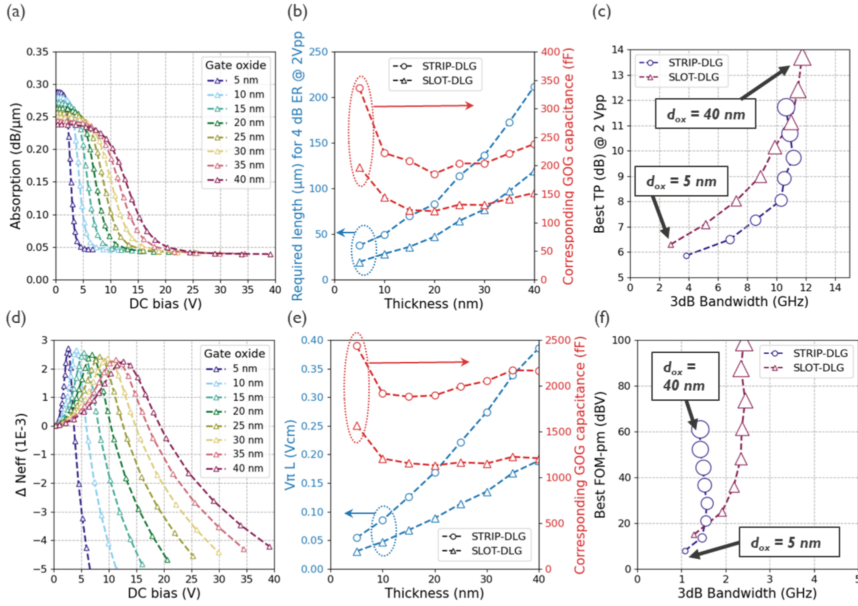

Figure 4.23: Simulated (a) absorption and (d)Δn of SLOT-DLG EAMs as a function of DC bias at 1550 nm wavelength, for gate oxide thickness ranging from 5 to 40 nm. Required length (blue curves) and corresponding DLG capacitance as a function of d_{ox} for both STRIP-DLG and SLOT-DLG (b) EAMs and (e) PMs. (c) Best TP-bandwidth (f) FOM_{pm}-bandwidth compromise for both device types with d_{ox} ranging from 5 nm to 40 nm (step = 5 nm), as illustrated by the size of the markers.

4.7.2 Thickness

Next, the effect of the gate oxide thickness is explored for STRIP-DLG modulators and SLOT-DLG modulators with M_{off} = 450 nm and 750 nm and W_{DLG} = 650 nm and 740 nm, respectively. Figure 4.23(a) and (d) illustrates the absorption and (d)Δn, respectively, for the SLOT-DLG modulators as a function of voltage for gate oxide thicknesses ranging from 5 nm to 40 nm. Two notable observations can be made from Figure 4.23(a). First, at V_{DC} = 0 V, the absorption decreases from 0.29 dB/μm to 0.23 dB/μm as the thickness increases. This can be attributed to the mode profile and the increasing vertical distance between graphene 2 and the waveguide. At high voltages, where loss is minimal, the absorption becomes comparable (around 0.04 dB/μm), resulting in a greater modulation depth for devices with thinner gate oxide. Second, as the oxide thickness increases, the voltage required for graphene to enter the Pauli blocking region also increases [96]. For instance, a device with d_{ox} = 40 nm requires approximately V_{pp} = 30 V to modulate between maximum and minimum absorption, whereas a device with d_{ox} = 5 nm only needs

V_{pp} = 5 V. Consequently, devices with thinner oxide can satisfy the criterion of a 4 dB extinction ratio (ER) at V_{pp} = 2 V with a shorter active length compared to devices with thicker oxide. Both trends can also be observed in Figure 4.23(d). The maximum peak of Δn decreases from 2.72 to 2.26 with transition voltage shifting from 2.6 V to 12.6 V when d_{ox} increase from 5 nm to 40 nm.

Figure 4.23 (b) shows the required length for both devices at the point of achieving the best TP while Figure 4.23 (e) shows the $V_{\pi}L$ for both devices at the point of achieving the best FOM_{pm}. The corresponding capacitance is determined by considering the required length at V_{pp} = 2 V and capacitance density for different gate oxide thicknesses. As the thickness increases, both figures show that the capacitance initially decreases sharply and then gradually increase. The larger capacitance in Figure 4.23 (e) is attributed to the long required length to satisfy the condition imposed on the π phase shift. Figure 4.23(c) and (f) presents the TP-bandwidth and FOM_{pm}-bandwidth trade-off, respectively. Although the device with d_{ox} = 5 nm exhibits the best TP value of 6.30 dB and FOM_{pm} value of 15.0 dBV for SLOT-DLG EAMs, it also has the lowest bandwidth in both cases. Increasing the oxide thickness can enhance the bandwidth but worsens TP and FOM_{pm}, which exhibits a steep increase when d_{ox} exceeds 20 nm. Therefore, a thickness of 20 nm is considered ideal for achieving a good balance between TP, FOM_{pm} and bandwidth.

4.7.3 Width of DLG

Lastly, we investigate the influence of the width of the DLG capacitive stack. Reducing W_{DLG} can decrease the capacitance of the device, leading to a larger 3 dB bandwidth. However, this improvement comes with a trade-off. With a narrower DLG width, the optical mode interacts less with the GOG region and more with the access region (graphene layer between contacts and GOG stack). Since no initial doping is applied, the access region often exhibits high optical loss and does not contribute to modulation. Figure 4.24(a) shows that, as W_{DLG} decreases from 1000 nm to 200 nm, the modulation depth decreases (from 0.29 dB/µm to 0.22 dB/µm) and the minimum loss increases (from 0.03 dB/µm to 0.08 dB/µm), resulting in a deteriorated TP value. Similarly, the trend can also be observed in Figure 4.24(d). The maximum Δn decreases from 2.95 to 1.62 at $V_{DC} = 6.9V$ when W_{DLG} decreases from 1000 nm to 200 nm. At the transparent region (e.g. V_{DC} = 17.9 V), Δn also shows a smaller value for device with narrower W_{DLG}, resulting in a deteriorated FOM_{pm} value. Figure 4.24(b) and (e) shows how the optimal TP-bandwidth and FOM_{pm}-bandwidth compromise changes, respectively, when decreasing W_{DLG} decreasing from 1000 nm to 200 nm. For completeness,

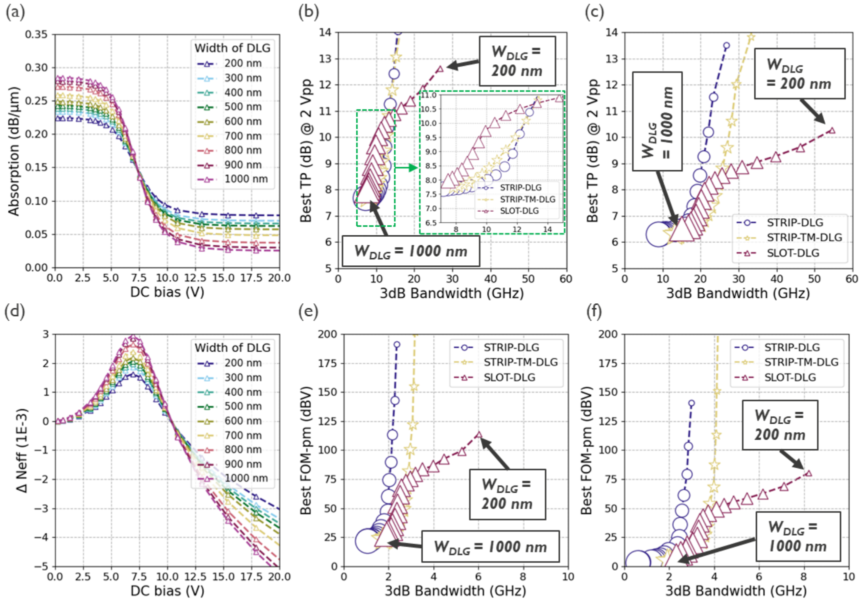

Figure 4.24: Simulated (a) absorption and (d) Δn of SLOT-DLG EAMs as a function of DC bias at 1550 nm wavelength, for DLG EAMs width ranging from 200 to 1000 nm. (b,c) Best TP-bandwidth compromise and (e,f) FOM_{pm}-bandwidth compromise for three device types, with graphene scattering rate of (b, e) 15meV and (c, f) 1.2meV. W_{DLG} ranges from 200 nm to 1000 nm (step = 50 nm), as illustrated by the size of the markers.

we included a third device type (STRIP-TM-DLG modulator), which uses the quasi TM-polarised waveguide mode (with M_{off} = 600 nm and d_{ox} =20 nm). In absorption modulators, Figure 4.24(b) shows that narrowing the GOG stack of a SLOT-DLG EAM can improve the bandwidth from 7.5 GHz to 26.7 GHz, at the cost of increasing the TP value from 7.97 dB to 12.63 dB. Comparing the different device types, it can be seen that they exhibit similar optical and electrical performance when W_{DLG} is large, e.g. 1000 nm. When reducing W_{DLG}, initially the TP for the SLOT-DLG EAM deteriorates significantly, making it less efficient compared to the other devices. However, when W_{DLG} becomes less than 400 nm, the SLOT-DLG EAM starts to outperform the other two. For W_{DLG}= 200 nm a bandwidth of 26.7 GHz and TP = 12.63 dB is obtained. Regarding PMs, SLOT-DLG PM can improve the bandwidth from 1.9 GHz to 6.0 GHz, at the cost of increasing the FOM_{pm} value from 28 dBV to 114 dBV. It can also be observed that FOM_{pm} degrades faster in SLOT-DLG PMs compared to the other two devices when W_{DLG} decreases from 1000 nm to 500 nm. However, when W_{DLG} becomes less than 500 nm, the degradation becomes slower in SLOT-DLG PMs and shows a better FOM_{pm}-bandwidth compromise than the other two. Finally, we repeated these simulations, assuming a higher quality graphene (scattering rate = 1.2 meV). Such quality can currently be obtained using exfoliated graphene and might in the future also be attainable for graphene grown using waferscale methods [137, 249]. The results in Figure 4.24(c) and (f) clearly indicate improvements in both TP-bandwidth and FOM_{pm}-bandwidth for each data point. Notably, compared to STRIP-DLG modulators and STRIP-TM-DLG modulators, the SLOT-DLG modulators demonstrates a higher potential for achieving a good compromise between high speed and low transmission penalty while generating the desired extinction ratio and π phase shift at a practical drive voltage.

4.8 Conclusion

In this chapter, we have conducted an experimental investigation of strip and slot waveguide-based DLG modulators, including EAMs, MZMs, and RMs. Each modulator type was extensively characterized both statically and dynamically. Leveraging the advantages of slot waveguides, which offer a narrow mode profile and strong mode confinement on the graphene layers, the slot waveguide-based modulators demonstrated superior efficiency in both amplitude and phase modulation.

However, despite the improved modulation efficiency, the figure of merit (FOM) in our current amplitude and phase devices did not outperform strip-based devices. The primary reason behind this discrepancy lies in the intrinsic property of slot

waveguides. While they provide enhanced confinement in the small gap, this comes at the expense of an expansion of the evanescent field [222]. Consequently, there is a stronger interaction with the lossy graphene in the access region next to the waveguides, which results in higher optical loss and does not effectively contribute to modulation. Additionally, the placement of metal contacts too close to the waveguide in the current SLOT-DLG modulators resulted in significant loss and, subsequently, poor FOM in these devices. However, the simulation results provide valuable insights, and excellent agreement was achieved between the measured and simulated results for both device types.

Building upon these findings, we conducted an extensive design study in the outlook section, varying the main dimensional parameters of both device types to find an optimal trade-off between extinction ratio, insertion losses, and modulation bandwidth. This study revealed that SLOT-DLG modulators indeed have the potential to outperform STRIP-DLG modulators, offering lower transmission penalties and better FOM_{pm} at higher bandwidths. To achieve these benefits, the width of the capacitive GOG stack needs to be reduced below 400 nm, and the metal contacts should be placed sufficiently far from the waveguide.

In conclusion, our work highlights the promising potential of slot waveguide-based devices as a superior platform for realizing high-performance EAMs, and their potential application in next-generation data communication and telecommunications systems. By addressing the challenges associated with loss and device design, we believe that slot waveguide-based modulators hold great promise for advancing the field of integrated photonics and enabling advanced communication technologies.

5

LOW-LOSS INTEGRATED PHASE MODULATOR BASED ON TRANSITION METAL DICHALCOGENIDE

In Chapter 4, we demonstrated remarkable modulation efficiency in both absorption and phase when utilizing a graphene layer as the active material. However, when considering (insertion) loss, our current device's performance is merely on par with state-of-the-art devices, rather than surpassing them. The primary culprit for this discrepancy is the quality of the graphene layer we currently employ, which falls short of the high-quality graphene reported in the literature.

Our low-quality graphene suffers from heightened intra-band scattering, resulting in elevated loss levels at higher Fermi levels, which are typically associated with the transparent region. This increased loss adversely impacts the final figure of merit and places our device in a comparable league with existing state-of-the-art devices. Altering the device's dimensions and design won't offer a straightforward solution since these adjustments generally introduce their own trade-offs among speed, loss, and efficiency.

The most effective means to address this challenge without compromising other

aspects of device performance is to enhance the quality of the graphene layer. However, this endeavor is far from straightforward. It involves the growth of high-quality graphene, typically attainable on substrates like Pt and Cu. Subsequently, a robust transfer method is required to relocate the grown graphene to the target substrate, often SiO2, without compromising its quality. Hexagonal boron nitride (h-BN) becomes essential due to lattice mismatch between graphene and the target substrate. Encapsulation by h-BN minimizes the formation of defects or disruptions at the interface, preserving the integrity of the graphene lattice, which is paramount for maintaining its electronic properties. Lastly, all these processes must be compatible with complementary metal-oxide-semiconductor (CMOS) technology to enable the cost-effective, large-scale production of high-quality graphene-based devices.

Our research doesn't directly address the enhancement of graphene quality, as it lies beyond the scope of our work. Instead, we shift our focus to another prominent member of the 2D materials family: transition metal dichalcogenides (TMDCs). TMDCs have garnered significant attention in logic devices due to their bandgap properties [16], high on-off ratios [250], and potential for large-scale integration [251]. Additionally, these materials are known for their strong light-matter interaction, especially at their excitonic peaks [17, 252]. Moreover, they have demonstrated substantial index modulation with low loss, particularly within the C-band wavelength range [29].

Efficient phase modulators with high Δn/Δk and low propagation losses are instrumental for enabling large-scale photonic systems, encompassing applications like light detection and ranging (LIDAR), phased arrays, optical switching, coherent optical communication, and quantum and optical neural networks [253–255]. Therefore, our research venture embarks on an initial exploration of TMDC-based photonics devices, with a particular emphasis on low-loss MZMs. Our objective is to establish a robust integration process for TMDC-based devices and subsequently investigate whether we can replicate the strong effects observed in the existing literature. This chapter presents our preliminary investigations, encompassing three distinct device structures utilizing molybdenum disulfide (MoS_2).

5.1 Single layer MoS2 (SL-MoS2)

The single-layer MoS_2 (SL-MoS_2) structure involves sandwiching a gate oxide between a doped silicon layer and a single MoS_2 layer. This configuration offers efficient fabrication with the integration of just one MoS_2 layer. Leveraging the existing MZMs designed by collaborators from CNIT ($Consorzio\ Nazionale\ Interuniversitario\ per\ le\ Telecomunicazioni$), we carried out initial experiments with this novel material, targetting phase modulation. Figure 5.1 (a) shows

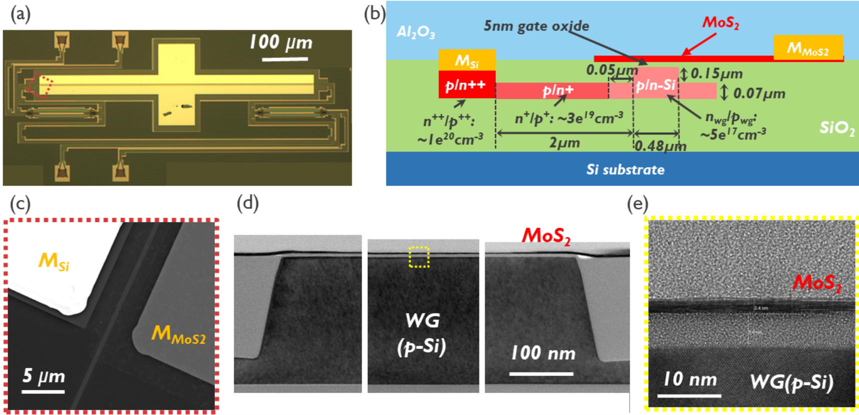

Figure 5.1: (a) Top-down microscope image, (b)schematic cross-section, (c) SEM (d) and (e) TEM of the SL-MoS_2.

the device, a 2x2 MZM with one arm featuring SL-MoS_2 and the other with a strip waveguide only. In Figure 5.1 (b), we provide a closer examination of the structure. In our approach, we employed three implantation steps on the silicon layers to minimize contact and sheet resistance without significantly increasing optical loss in the waveguides. However, we realized later that the 50 nm spacing between the waveguide and the highly doped BODY region might be too small and may contribute to increased loss in the device. Thus, there is room for potential improvement through design modifications. Figure 5.1 (c), (d), and (e) showcase SEM and TEM images of the fabricated devices, revealing well-defined MoS_2 layers, gate oxide, and metal contacts. In the following subsections, we elaborate on the laboratory-based integration flow for SL-MoS_2. Each processing step, including MoS_2 transferring, patterning, and contacting, is defined. Subsequently, we highlight the significance of MoS_2 doping by Al_2O_3 in enhancing AC performance. The last subsection presents the characterization of static and dynamic EO responses, acknowledging design limitations with only one MZM device for each silicon doping type.

5.1.1 Integration flow

The SL-MoS_2 structure is based on a 220 nm thick silicon (Si) waveguide, defined on a silicon-on-insulator (SOI) wafer featuring a 2 µm buried oxide layer within imec's 200 mm Si photonics platform [256]. The Si waveguide is partially etched on one side, creating a rib structure that allows to contact the waveguide through the 70 nm-thick Si slab layer. To optimize the Si contact and sheet resistance while

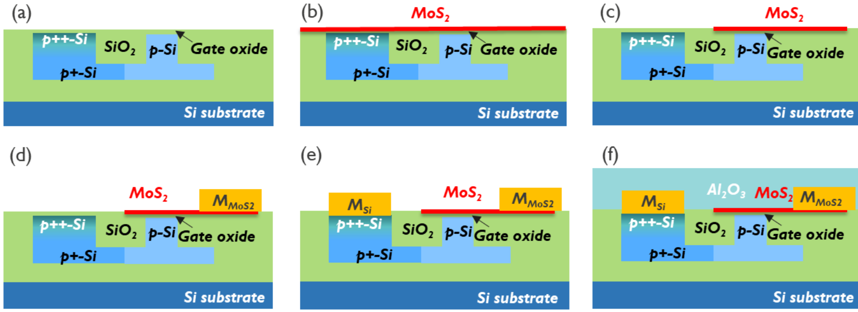

Figure 5.2: Process flow for the SL-MoS_2 fabrication. (a) Waveguide patterning, implantations and surface planarization, (b) semi-dry transfer of MoS_2 layer, (c) patterning by EBL, (d) contact to MoS_2 with Ni + Pd, (e) contact to Si with Ti + Pd + Au (f) Al_2O_3 deposition.

keeping waveguide loss in check, we executed three implantation phases involving phosphorus or boron. This strategy led to three distinct regions with varying doping concentrations, as illustrated in Figure 5.1(b): p++ (or n++) for the contact region, p+ (or n+) for the slab region, and p-Si (or n-Si) for the waveguide region. Following Si waveguide patterning, a chemical mechanical polishing procedure was conducted to ensure the waveguides were perfectly planarized. To isolate the MoS_2 layer from the waveguide, a 5 nm-thick thermal oxide layer was grown on top. As the final step before MoS_2 transfer, the wafer underwent mechanical dicing, as the MoS_2 layer will be transferred in smaller coupons.

For our experiments, we utilized MoS_2 synthesized via chemical vapor deposition (CVD) on a wafer scale, typically grown on a sapphire substrate [257–259]. The growth of synthetic MoS_2 has been comprehensively discussed in Chapter 1. However, it's important to note that the detailed development of these techniques was not part of this work and won't be elaborated on extensively. In our experiments, the MoS_2 was then transferred in-house using a semi-dry method [260]. Initially, the MoS_2 was delaminated from the growth substrate with the aid of thermal release tape while immersed in water. After the layer was dried, it was manually affixed to the designated area on the target substrate. Subsequently, the thermal release tape was eliminated through a heating process and the remaining polymer layers were removed through a wet solvent procedure. The schematic look after this stage is shown in Figure 5.2 (b).

Subsequently, we employed electron beam lithography (EBL) to precisely define the MoS_2 layer. Instead of relying solely on a pure poly-methyl methacrylate (PMMA) resist stack for EBL, we adopted a double-layer resist process, akin to the technique introduced in Chapter 4 for patterning the DLG. This choice was

primarily driven by the fact that PMMA functions as a positive resist, demanding extended exposure times for our samples. Given the significantly smaller area of the designed region within the sample, the use of a negative resist was essential to ensure efficient exposure. Hydrogen silsesquioxane (HSQ) is a well-established negative resist; however, its development process involves a water-based solution, which can potentially lead to MoS_2 delamination and degradation. To mitigate this concern, we opted for a double-layer resist process. In this approach, PMMA served as the bottom layer to shield the MoS_2 layer, while HSQ was applied on top for exposure through EBL. Following the exposure and development of HSQ, we employed an oxygen plasma to pattern the PMMA resist. Next, using the same mask, the MoS_2 layer was patterned using chlorine + oxygen (Cl_2 + O_2) based dry etching. Lastly, we removed the residual resist stack through a wet solvent process, resulting in the schematic cross-section of the device depicted in Figure 5.2 (c).

The procedure for fabricating the metal contacts to the MoS_2 layer employs a lift-off method. In this process, another round of electron beam lithography (EBL) is employed, utilizing pure PMMA resist to cover the entire sample. Subsequent to exposure and development, metal layers of 10 nm-thick nickel (Ni) followed by 20 nm-thick palladium (Pd) are evaporated across the entire sample. The critical lift-off process is executed by immersing the sample in acetone at 50°C. During lift-off, the photoresist dissolves, removing the deposited metal layer, leaving behind only the desired metal shapes in contact with MoS_2 resulting in the schematic cross-section of the device depicted in Figure 5.2 (d).

The fabrication process for the Si contacts closely resembles that of the MoS_2 contacts, with one notable distinction. After exposure and development, and before the metal layer is evaporated, the sample undergoes a wet etching process in buffered hydrofluoric acid (BHF) to eliminate the thermal oxide layer from the contact region. To prevent excessive oxide re-growth, it is crucial to carry out the metal evaporation for the contacts immediately after completing the etching step. For the Si contacts, we utilize a metal stack consisting of titanium (Ti), platinum (Pt), and gold (Au). Initially, we deposit 20 nm of Ti via thermal evaporation. Without removing the sample from the chamber, we add 20 nm of Pt to serve as a protective layer against Ti oxidation. Finally, we transfer the sample to another tool and apply a 30 nm layer of Au via e-gun evaporation. This Au layer facilitates robust contact with the probes used for measurements (Figure 5.2 (e)).

At this point, we were ready to measure the device; however, we anticipate that the resistance at the access region of MoS_2 would be excessively high, leading to poor and unreliable AC performance. To address this challenge, we devised a solution: the deposition of an Al_2O_3 capping layer. This layer serves a dual purpose, acting as both an encapsulation layer for MoS_2 and a doping layer aimed at reducing

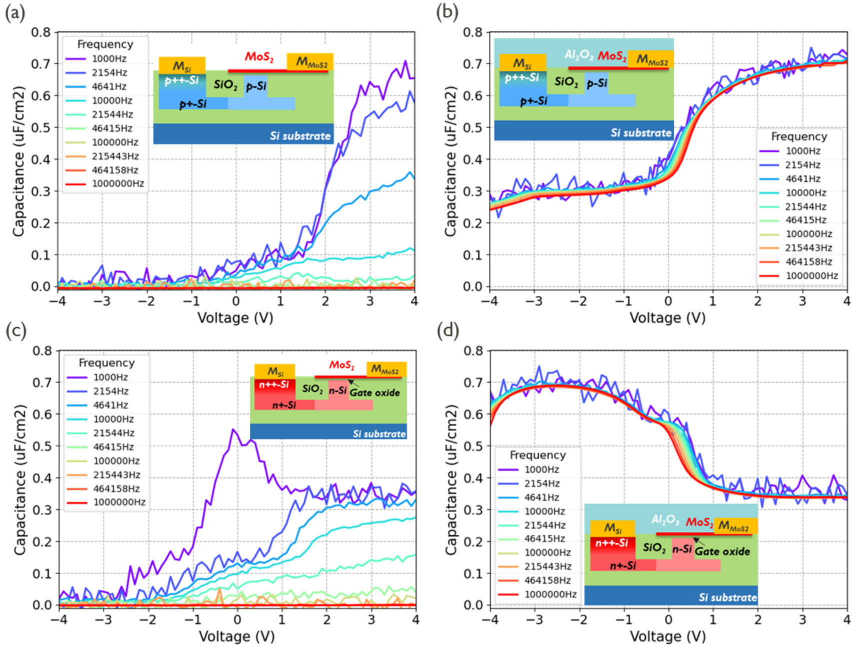

Figure 5.3: Capacitance-voltage measurements on p-type silicon-doped $SLMoS_2$ (a) before and (b) after Al_2O_3 deposition.The capacitance-voltage measurements on n-type silicon-doped $SLMoS_2$ (c) before and (d) after Al_2O_3 deposition.

resistance, a topic we will delve into further in a subsequent section. To ensure a uniform capping layer on MoS_2, we initially deposited 1 nm of Al via thermal evaporation, followed by the deposition of 10 nm of Al_2O_3 through ALD. The final schematic representation of the device is depicted in Figure 5.2 (f).

5.1.2 Effect of Al2O3 doping

Within our structure, the MoS_2 layer can be divided into two distinct regions: the gated area and the ungated area. In the gated region, the carrier concentration is controllable via electrical gating, allowing us to transition MoS_2 from an off state (characterized by high resistance) to an on state (with lower resistance). This region is also where we anticipate a notable change in the refractive index. Conversely, in the ungated region, the carrier concentration of MoS_2 remains unmodifiable. It retains its background carrier concentration, which is introduced mostly during the growth and fabrication process before the deposition of the Al_2O_3 layer. In other words, the ungated MoS_2 area primarily remains in an off state with high

resistance, potentially compromising its AC performance.

An illustrative example of CV measurements on an uncapped SL-MoS_2 on a p-doped silicon waveguide is presented in Figure 5.3 (a), with the frequency ranging from 1000 to 1000,000 Hz. At lower frequencies, we observe an approximate capacitance density of 0.7 $\mu F/cm^2$ when a high voltage is applied. However, when the applied voltage drops below 3V, the curve begins to decline, reaching nearly zero after the voltage falls below -1 V. This significant drop cannot be simply attributed to the depletion of the p-doped silicon layer, as we obtain minimal response at low applied voltage. Instead, we attribute it to the strong depletion and exhaustion of free carriers within the MoS_2 layer. When the applied voltage falls below the MoS_2 threshold voltage (V_{th}), there are hardly any detectable free carriers within MoS_2, resulting in nearly zero capacitance in the CV measurement.

Furthermore, we've noticed that the capacitance is dependent on frequency. As the frequency increases, the maximum capacitance decreases. This phenomenon primarily arises from the high resistance and slower response of the access region in MoS_2 to higher frequencies. Similar trends are observed in n-doped silicon SL-MoS_2 devices, as demonstrated in Figure 5.3 (c).

To overcome these challenges and enhance AC performance, doping the MoS_2 layer has been considered a viable solution. In existing literature, it has been reported that depositing an AlO_x layer on MoS_2 can effectively introduce selective doping [217]. Given its dual functionality as an encapsulation layer, this process is ideal for enhancing device performance. Figure 5.3 (b) displays CV measurements of the same device after Al_2O_3 deposition. Thanks to the doping effect on MoS_2, which results in a left-shift of MoS_2's V_{th}, the measured results exhibit reliable and consistent CV curves across the entire voltage range. The accumulation and depletion of the silicon layer within the device are clearly observable and align closely with the intended gate oxide thickness of 5nm. Notably, when the voltage dips below -3V, the CV curves commence a downward trend. This observation suggests that the available free carriers are nearly depleted, providing insights into the threshold voltage of MoS_2 after Al_2O_3 doping.

Furthermore, the deposition of AlO_x resolves the high-resistance issue in the access region of MoS_2. As a result, CV curves now respond stably to varying frequencies. A similar enhancement is observed in n-doped silicon-based devices, as depicted in Figure 5.3 (d), albeit with the opposite stages for accumulation and depletion.

This CV analysis underscores the significance of AlO_x doping on MoS_2 and demonstrates how this step can significantly enhance the stability of AC results. We highly recommend incorporating doping into MoS_2-based devices, especially when high-frequency response is essential.

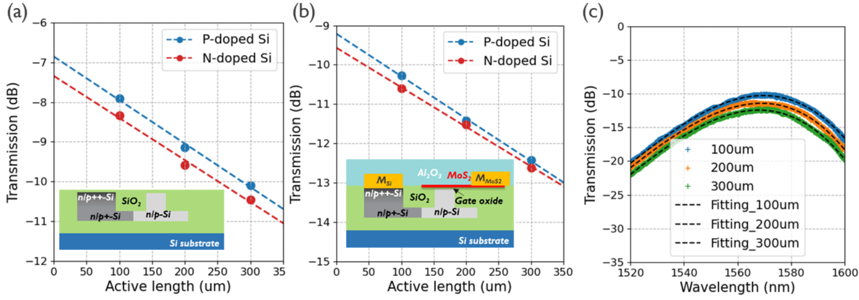

Figure 5.4: Extracted maximum transmission as a function of active length (a) before and (b) after MoS_2 integration. The dashed lines represent fitted slopes of 109 dB/cm (p-type) and 106 dB/cm (n-type) before MoS_2 integration, and 108 dB/cm (p-type) and 100 dB/cm (n-type) after MoS_2 integration. (c) EAMs transmission as a function of wavelength for encapsulated devices with three different active lengths.

5.1.3 Static and dynamic EO characterization

To ascertain the low loss characteristics of MoS_2, we conducted loss measurements before and after MoS_2 integration. We employed EAM structures with identical cross-sections but varying lengths to calculate the propagation loss of the devices. In Figure 5.4, we obtained propagation loss values of 109 dB/cm (106 dB/cm) and 108 dB/cm (100 dB/cm) for p-type (n-type) silicon-doped devices before and after MoS_2 integration, respectively. These figures exhibit minimal variation, indicating that the integration of MoS_2 introduces negligible additional loss[1]. The predominant sources of loss are attributed to doped silicon and the device design. Specifically, when referring to doped silicon, we primarily highlight the n+ (p+) regions. Since the carrier concentration is low in the n-Si (p-Si) region, it does not significantly contribute to the high propagation loss. Instead, we attribute it to the (too) short distance (50nm) between the n+(p+) regions and the waveguides. We anticipate achieving lower propagation loss values after appropriate adjustments to this distance.

Subsequently, we applied a DC bias to both devices, with the source connected to silicon and the ground to MoS_2. In Figure 5.5 (a), we present the results for the p-type silicon-doped device with an applied bias ranging from -4V to 4V. The interference fringes are clearly visible, and the voltage-dependent shift is easily discernible, with only a minor change in depth. By measuring the shift of the peak, we calculated the change in effective refractive index (Δn), as illustrated in Figure 5.5. Comparing with the CV measurements, we can distinctly separate the

[1]This will be confirmed later in this chapter, through more accurate measurements employing undoped silicon waveguides.

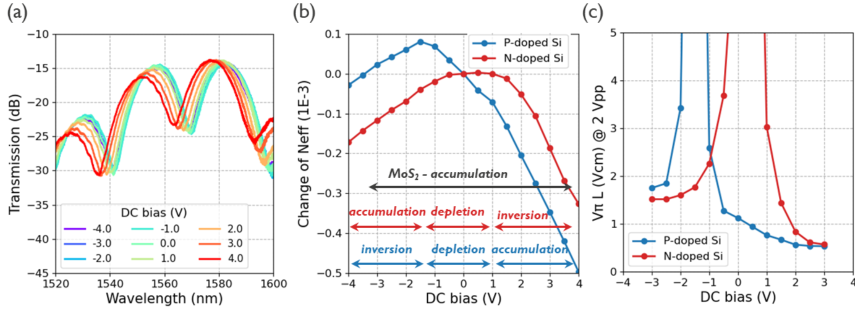

Figure 5.5: (a) Biased transmission spectrum of p-type silicon-doped SL-MoS_2 as a function of wavelength with an active length of 600 µm. Calculated (b) effective index change and (c) $V_\pi L$ as a function of DC bias for both types of SL-MoS_2.

electro-optic (EO) response of p-doped silicon in three regions: (1) an accumulation region, where the applied voltage spans roughly from 4 V to 1 V, (2) a depletion region, where the voltage ranges from approximately 1V to -1V, and (3) an inversion region, where the voltage ranges from approximately -1V to -4V. The EO response of n-doped silicon also exhibits three regions but with a different order, as indicated in Figure 5.5 (b). In contrast, MoS_2 primarily demonstrates an accumulation region across almost the entire range of applied voltage due to the shift of threshold voltage by AlO_x doping.

We later employed V_{pp} = 2V to calculate the phase modulation efficiency ($V_\pi L$) and present the results in Figure 5.5 (c). The optimal $V_\pi L$ values are measured at 0.53 Vcm and 0.57 Vcm for p-type silicon-doped and n-type silicon-doped SL-MoS_2, respectively. When combined with the propagation loss, which we simplified by assuming voltage-independent loss in our devices, we calculated a figure of merit of 57 dBV for both types of devices by using the Equation 2.10. This value surpasses the state-of-the-art TMDC-based phase modulators (approximately 108 dBV) [29] and is comparable to single-layer graphene MZMs (66.1 dBV) [27]. We anticipate further enhancements in device performance by optimizing the MZM design, particularly by increasing the separation between the n+(p+) region and the waveguide.

The frequency response characteristics of our devices were assessed through S-parameter measurements. A DC voltage ranging from -3V to 4V and an AC signal of -8 dBm were applied to the devices using a bias-tee. In Figure 5.6 (a), we present the S21 results for the n-type silicon-doped device as the frequency sweeps from 0.3 to 5 GHz. We extracted the 3dB bandwidth as a function of DC bias, depicted in Figure 5.6 (b). Maximum bandwidths of 0.68 and 0.91 GHz were measured for n-type and p-type silicon-doped SL-MoS_2 devices, respectively.

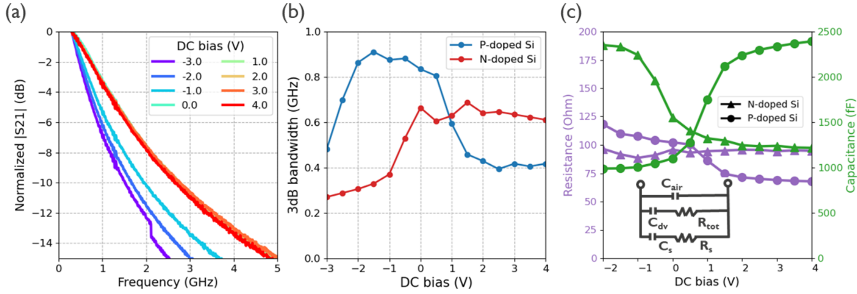

Figure 5.6: (a) Normalized S21 response, (b) EO bandwidth extracted from S21 and (c) capacitance and resistance values calculated from S11 fitting for both p-type and n-type silicon-doped SL-MoS_2 at various DC bias conditions.

To gain deeper insight into our devices, we conducted S11 fitting, considering the equivalent circuit model shown in the inset of Figure 5.6 (c). In this model, C_{dv} represents the capacitance of the SL-MoS_2 structures, while R_{tot} represents the total resistance, comprising the contact and sheet resistance of both the MoS_2 and silicon layers. Additionally, C_{air}, C_s, and R_s denote the capacitance between the metal pads, the capacitance of the silicon substrate, and the resistance of the silicon substrate, respectively.

From the S11 fitting procedure, we were able to extract the capacitance and resistance of the device as a function of DC bias, illustrated in Figure 5.6 (c). While R_{tot} remained relatively constant across the applied voltages, the capacitance of the device exhibited varying values, akin to those observed in the CV results shown in Figure 5.3. In the depletion (and inversion) region, the device displayed smaller capacitance, resulting in reduced RC delay and consequently a wider bandwidth. Accordingly, we noted that the optimal bandwidth was achieved when the silicon was in a depleted (or inverted) state, aligning with findings in previous literature [24, 261]. At -1V (2V) DC voltage, we measured C_{dv} values of 1004 (1246) fF and 108 (96) Ohms for p-type (n-type) silicon-doped SL-MoS_2. Accounting for electrical RC delay, the resulting electrical 3 dB bandwidth was calculated to be 1 (0.87) GHz, closely aligning the values observed in our experiments.

5.2 Graphene-oxide-MoS2 (G-O-MoS2)

Building upon our successful implementation of the first TMDC-based phase modulator using a SL-MoS_2 stack, we sought to extend our knowledge to a dual-layer structure. Compared to the SL-MoS_2, the dual-layer configuration eliminates the

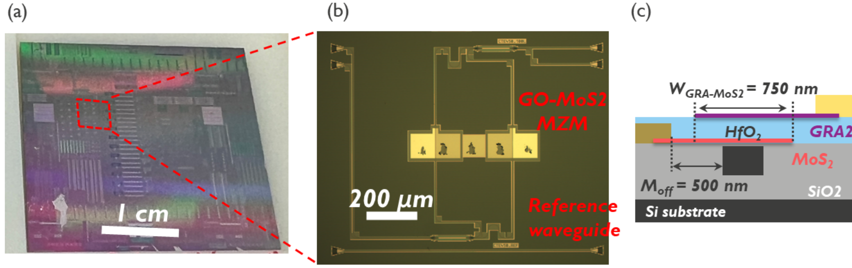

Figure 5.7: (a) The look of diced sample. (b) Top-down microscope image, (b) schematic cross-look of the G-O-MoS_2.

need for complex silicon implantation, making it adaptable to a variety of substrates, including SiN waveguides and silicon slot waveguides, thereby enhancing the device's versatility. In this section, we leverage the DLG platform introduced in Chapter 4, specifically focusing on MZM structures with strip waveguides to investigate phase modulators based on dual 2D layers.

Figure 5.7 (a) shows the diced sample. The 2x2 MZMs used in this study maintain the same dimensions as those employed in for the DLG, featuring a waveguide width of 450nm and a 40µm delay line (Figure 5.7 (b)). However, we deviate from the previous configuration by substituting the bottom graphene layer with MoS_2, resulting in the construction of a Graphene-oxide-MoS_2 (G-O-MoS_2) structure. We anticipate that this novel configuration offers advantages, including a reduction in the high loss typically associated with the DLG and improved phase modulation efficiency, thanks to the substantial index change reported in MoS_2 [29]. A schematic cross-sectional view of the device is depicted in Figure 5.7 (c), featuring a nominal overlap width ($W_{GRA-MoS_2}$) of 750 nm and M_{off}= 500 nm.

5.2.1 Integration flow

The process of fabricating the G-O-MoS_2 structure closely resembles that used for DLG modulators. It starts with a 200-mm silicon-on-insulator (SOI) wafer, featuring a 220 nm-thick crystalline silicon (c-Si) layer and a 2 µm buried oxide (BOX) layer. To begin, standard 193 nm immersion lithography is employed to pattern the c-Si layer, defining waveguides with a width of 450 nm. Following waveguide patterning and the deposition of a 2 µm oxide layer, the wafer undergoes planarization through chemical mechanical polishing (CMP), ultimately leaving a 10 nm-thick buffer oxide atop the waveguides, as depicted in Figure 5.8 (a).

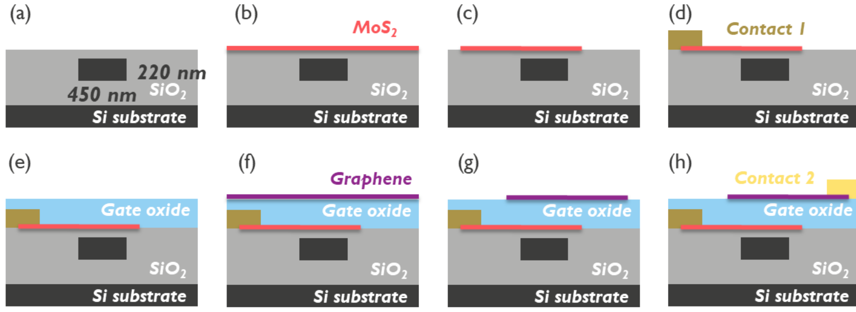

Figure 5.8: Process flow for G-O-MoS_2 MZMs fabrication. (a) Waveguide patterning and surface planarization, (b) semi-dry transfer of MoS_2 layer, (c) patterning by EBL, (d) contact with Ni + Pd, (e) HfO_2 deposition, (f) wet transfer of graphene layer, (g) patterning by EBL, and (h) top + edge contact with Pd.

Subsequently, the wafer underwent a dicing process, to prepare it for the integration of 2D materials within the laboratory setting. The growth and transfer of the MoS_2 layer followed the procedures detailed in the prior section, resulting in the device's schematic representation displayed in Figure 5.8 (b).

Following this, electron beam lithography (EBL) was used to define the shape of the MoS_2 layer, using the same double-layer resist process previously outlined. After the exposure and development steps, an oxygen plasma was employed to etch the PMMA layer, followed by a Cl_2 + O_2 based dry etching to transfer the pattern into the MoS_2 layer. Subsequently, the resist was eliminated using acetone, yielding a well-defined MoS_2 layer, as depicted in Figure 5.8 (c).

To contact the MoS_2 layer, a set of metal contacts comprising 10 nm Ni and 20 nm Pd were fabricated using another round of EBL and a subsequent lift-off process, see Figure 5.8 (d).

Next, before the second transfer of the 2D layer, graphene in this case, it was essential to deposit a dielectric layer to serve as the gate oxide. Originally, the plan was to create one device using Al_2O_3 as the dielectric layer and another device using HfO_2 for comparison. However, the fabrication of the Al_2O_3-based device encountered issues, leaving only the HfO_2-based device available for the study of the G-O-MoS_2 modulator. To ensure the uniformity of the gate oxide, our process began with the deposition of a 1 nm Si seeding layer via thermal evaporation, followed by a 6 nm HfO_2 layer using ALD, as depicted in Figure 5.8 (e). Afterward, the graphene layer was transferred, patterned, and contacting using the same procedures as those employed for the DLG devices in Chapter 4.

5.2.2 Static and dynamic EO characterization

In the electro-optic (EO) characterization, we landed the probe on G-O-MoS_2, connecting the source to the graphene layer and grounding the MoS_2 layer. To maximize the transmission through the MZM, we applied a constant bias of 4V to the shorter arm while sweeping the voltage on the longer arm from -4V to 4V. We expected to observe maximum transmission with the deepest interference fringe depth when both arms were biased at 4V. Interestingly, the deepest fringe depth occurred at V_{DC} = 1V, as shown in Figure 5.9 (a). The fringe depth decreased as the voltage exceeded 1V, although the transmission continued to increase. This discrepancy between our expectation and measurement can be attributed to variations in G-O-MoS_2 properties between arms, resulting from differences in doping levels and material quality.

By analyzing the peak shifts, we calculated the change in effective index (Δn). Figure 5.9 (b) illustrates that G-O-MoS_2 with three different lengths exhibited similar performance, with Δn exceeding 1E-3 as V_{DC} was swept from 1V to 4V. With V_{pp} = 2V, we calculated $V_\pi L$, revealing the best values to be 0.17, 0.15, and 0.19 for G-O-MoS_2 devices with lengths of 100 µm, 200 µm, and 400 µm, respectively. These values surpassed those of SL-MoS_2 (approximately 0.5 Vcm) demonstrated in the previous section and even outperformed state-of-the-art 2D-based phase modulators (approximately 0.28-0.8 Vcm) [27, 29, 262].

We also re-evaluated these devices using a different measurement scheme, where both arms were sourced with the same voltage simultaneously, effectively using the MZM as an electro-absorption modulator (EAM). Ideally, in this configuration, there should be no shift in the interference fringes, only an increase in transmission. However, a slight shift was still observed in Figure 5.9 (d), which, once again, can be attributed to the variation in G-O-MoS_2 properties mentioned earlier. Nevertheless, we tracked the maximum point of the curve and normalized it to calculate the modulation depth as a function of DC bias (Figure 5.9 (e)). All three devices exhibited similar performance, with a maximum modulation depth of 0.060, 0.061, and 0.057 for devices with active lengths of 100 µm, 200 µm, and 400 µm.

To distinguish the individual contributions of graphene and MoS_2, we compared our experimental results with simulations. In the simulations, we considered a structure with only one layer of graphene, as depicted in Figure 5.9 (g). We explored three different qualities (scattering rates) of graphene and an equivalent oxide thickness (EOT) of 3.3 nm for the gate oxide (calculated from the CV measurements in Figure 5.9 (h)). After normalizing the DC bias in the experimental results, Figure 5.9 (f) demonstrates that both delta Neff and delta absorption can be matched well when the scattering rate is approximately 30 meV. It was challenging to isolate

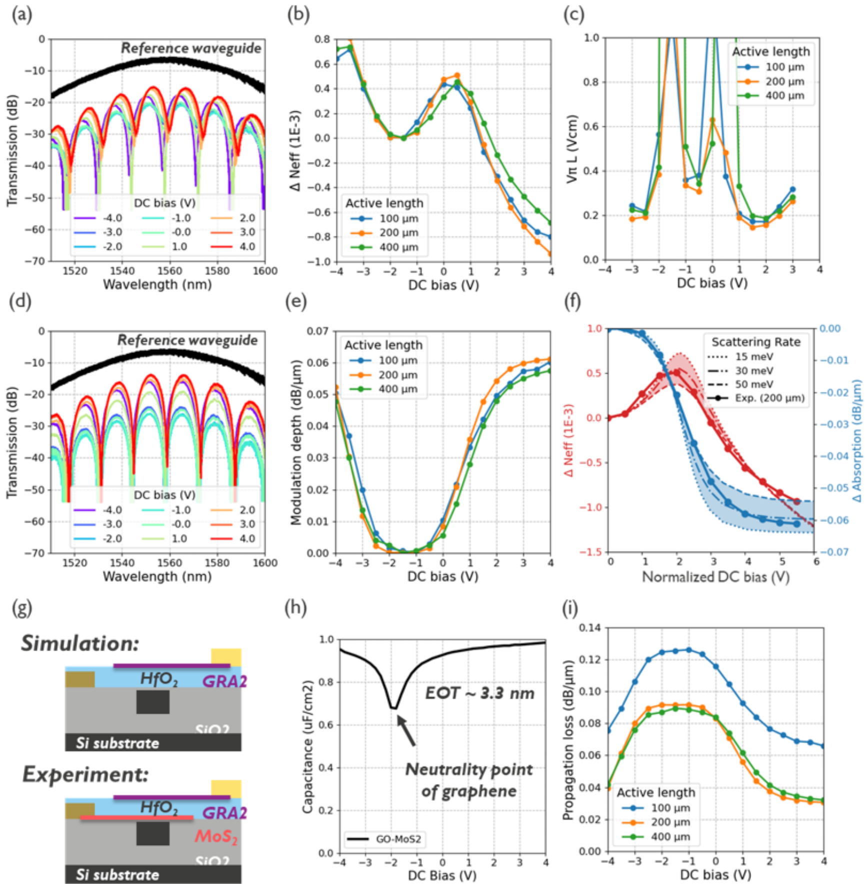

Figure 5.9: (a) Transmission spectrum of 200 µm-long G-O-MoS_2 with varying bias applied on the left (long) arm while a constant voltage of -4 V is applied on the right (short) arm. Calculated (b) effective index change and (c) $V_\pi L$ as a function of DC bias for G-O-MoS_2 devices. (d) Biased transmission spectrum of 200 µm-long G-O-MoS_2 with varying bias applied on both arms. (e) Calculated modulation depth as a function of DC bias for G-O-MoS_2 devices. (f) Simulated change of effective index (red) and absorption (blue) as a function of bias normalized by the neutrality point of the graphene layer (approximately 1.5 V). The solid curves represent experimental results obtained from G-O-MoS_2 devices with a length of 200 µm. (g) Schematic cross-section of the devices used for simulation and experiment. (h) Capacitance-voltage measurement of 200 µm-long G-O-MoS_2. The dip around 1.5 V is due to the neutrality point of the graphene layer. To determine the EOT of the gate oxide, the capacitance density at high voltage is selected for the calculation since the effect of graphene quantum capacitance is negligible. The EOT is calculated to be approximately 3.3 nm. (i) Calculated propagation loss as a function of DC bias for G-O-MoS_2 devices.

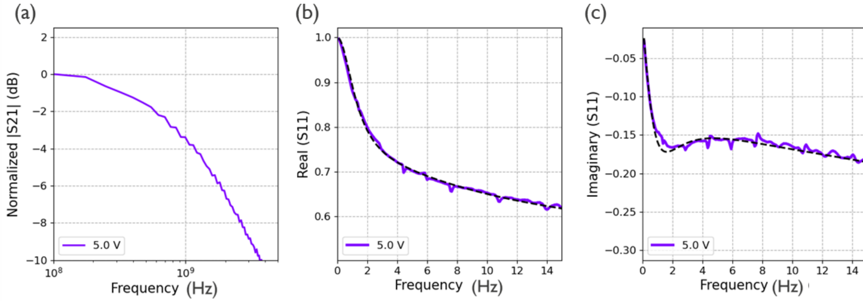

Figure 5.10: (a) Normalized S21 response, (b) real and (c) imaginary part of S11 response for G-O-MoS_2 with 100 active length.

the effect of MoS_2, likely because its impact is relatively smaller compared to the graphene layer.

Next, we attempted to calculate the propagation loss of the device, which would enable us to determine the figure of merit (FOM_{PM}) of the devices. The difference in transmission between the MZM and the reference waveguide served as the insertion loss of the device, which encompasses the propagation loss of G-O-MoS_2 and the routing waveguides. Although it would have been ideal to use an identical MZM structure without G-O-MoS_2 as a reference to determine these losses, practical constraints led us to employ the straight strip waveguide as the reference (Figure 5.7 (b)). To simplify the calculation, we assumed that all the observed insertion losses originated from G-O-MoS_2's propagation loss. By normalizing these losses with the corresponding active length, we computed the propagation loss of the G-O-MoS_2 device as a function of DC bias (Figure 5.9 (i)). Combining this information with that in Figure 5.9 (c), we derived the best figure of merit for phase modulation to be 48.8 dBV for our G-O-MoS_2 device. This value is comparable to SL-MoS_2 (57 dBV) and surpasses other 2D-based MZMs reported in the literature (66-223 dBV) [27, 29, 262].

The frequency response of the G-O-MoS_2 device was characterized through S-parameter measurements conducted with a frequency sweep ranging from 0.1 GHz to 15 GHz. For the device with a length of 100µm, a bandwidth of 0.85 GHz was observed as shown by Figure 5.10 (a). To analyze these results, we employed the equivalent circuit model presented in Figure 5.6 (c), with C_{dv} now representing the capacitance of the G-O-MoS_2 structure and R_{tot} representing the total resistance, encompassing the contact and sheet resistance of both the MoS_2 and graphene layers. The fitted curves for the real and imaginary parts of S11 are shown in Figure 5.10 (b), yielding a calculated capacitance of 400 fF and resistance of 337 Ohms. Using these values in the relevant equations, we estimated an electrical

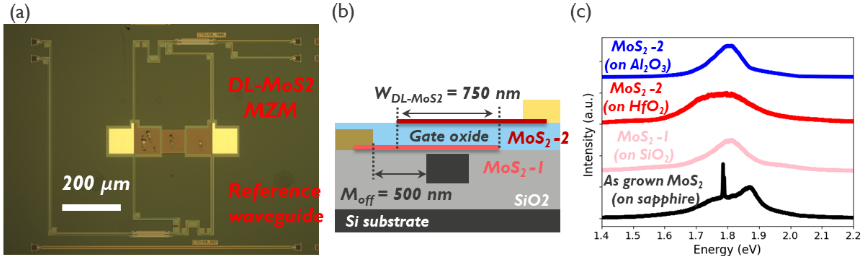

Figure 5.11: (a) Top-down microscope image, (b) schematic cross-look of the DL-MoS_2. (c) Measured photoluminescence of as-grown MoS_2, first transferred MoS_2 (on SiO2), and second transferred MoS_2 on Al_2O_3 (blue) and HfO_2 (red).

bandwidth of 1.03 GHz, close to our experimental findings.

Presently, the device's performance is constrained by its capacitance. To enhance its performance, we can consider depositing a thicker oxide layer with a larger equivalent oxide thickness (EOT). This adjustment would reduce the capacitance without significantly altering the resistance. For example, with an EOT of 20 nm, the capacitance can be roughly reduced to 47 fF. Assuming the resistance remains unchanged, this modification would result in a 3dB bandwidth of 8.75 GHz. However, it is important to note that such a modification could impact the DC performance by potentially reducing efficiency (increasing $V_\pi L$) and necessitating larger V_{pp} to drive the devices effectively.

5.3 Dual single layer MoS2 (DL-MoS2)

In response to the loss still observed in G-O-MoS_2, we have chosen to fabricate a pure MoS_2 phase modulator with low loss in this section, referred to as the dual single layer MoS_2 MZM (DL-MoS_2). In this configuration, we replace the graphene layer with a second layer of MoS_2. Given that MoS_2 is a more transparent material than graphene, we anticipate lower propagation losses in the DL-MoS_2. The MZM design replicates that of the G-O-MoS_2, shown in Figure 5.11 (a). The cross-section of the device is presented in Figure 5.11 (b). In this study, we considere two different gate oxides, Al_2O_3 and HfO_2, for the DL-MoS_2 and compare their respective performances. The quality of the MoS_2 layers is monitored through photoluminescence (PL) measurements before and after transfer, as shown in Figure 5.11 (c).

The as-grown MoS_2 exhibits a PL peak at 1.87 eV, accompanied by the signal from the sapphire substrate at 1.78 eV. Subsequently, we conducted PL measurements af-

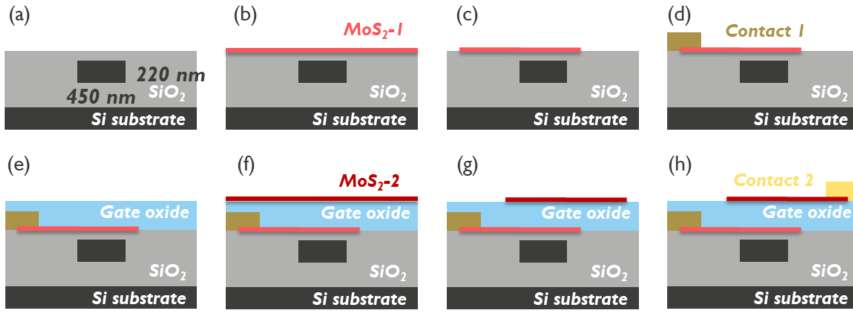

Figure 5.12: Process flow for DL-MoS_2 MZMs fabrication. (a) Waveguide patterning and surface planarization, (b) semi-dry transfer of the first MoS_2 layer (MoS_2-1), (c) patterning by EBL, (d) contact with Ni + Pd, (e) HfO_2 or Al_2O_3 deposition, (f) semi-dry transfer of the second MoS_2 layer (MoS_2-2), (g) patterning by EBL, and (h) contact with Ni + Pd.

ter transferring MoS_2 onto three different target substrates, yielding peak positions of 1.81 eV, 1.80 eV, and 1.81 eV for SiO2, Al_2O_3, and HfO_2, respectively. This redshift in the peak suggests a slight reduction in the bandgap of MoS_2 following the transfer. These variations can be attributed to multiple factors, including strain effects, dielectric environment, and surface quality [18,105,263–266]. Additionally, we observe that the peak broadens for MoS_2 transferred onto HfO_2, indicative of a higher concentration of defects. However, it is important to note that providing an extensive explanation of MoS_2 quality falls beyond the scope of this work and will not be elaborated upon extensively. What we can confirm is that the integration of MoS_2 layers onto photonic substrates was successful. In the following sections, we will demonstrate and compare the electro-optic results of these two types of devices.

5.3.1 Integration flow

The processing flow for DL-MoS_2 closely resembles that of G-O-MoS_2. The entire process, from waveguide patterning (Figure 5.12 (a)) to transfer (Figure 5.12 (b)), patterning (Figure 5.12 (c)), and contacting (Figure 5.12 (d)) of the first layer of MoS_2 (MoS_2-1), remains the same. The deposition of the gate oxide follows the same seeding method employed in our other 2D devices. Initially, 1 nm of Si (or Al) is thermally evaporated to serve as the seeding layer atop the MoS_2. Subsequently, 10 nm of HfO_2 (or Al_2O_3) is deposited using atomic layer deposition (ALD) to complete the gate oxide layer.

The second layer of MoS_2 (MoS_2-2) is transferred using the same semi-dry transfer

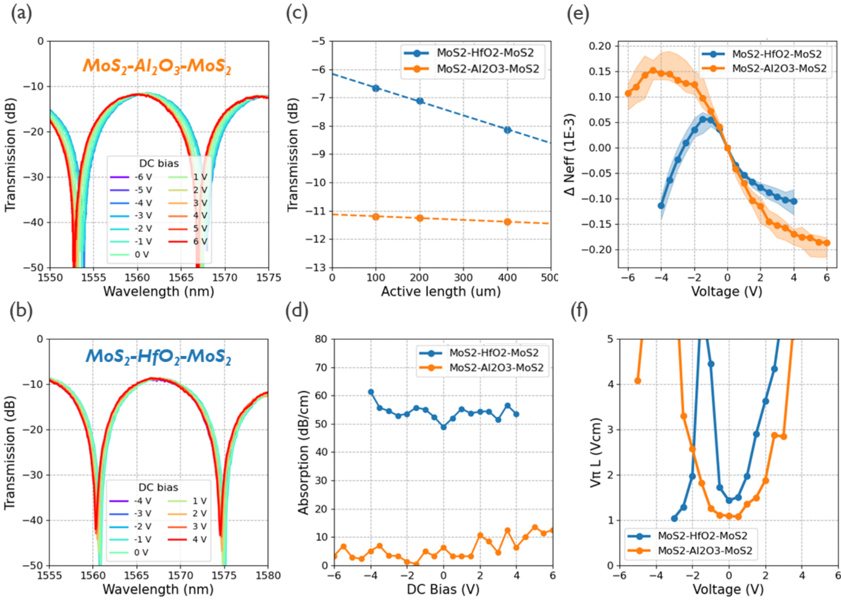

Figure 5.13: Biased transmission spectrum of 400 µm-long (a) Al_2O_3- and (b) HfO_2-based DL-MoS_2 as a function of wavelength with varying bias applied on the left (long) arm while a voltage of 0 V is applied constantly on the right (short) arm. (c) Extracted maximum transmission as a function of active length at V_{DC} = 0V. The dashed lines represent fitted slopes of 6.4 dB/cm and 49 dB/cm for Al_2O_3- and HfO_2-based DL-MoS_2, respectively. Calculated (d) propagation loss (e) effective index change and (f) $V_\pi L$ as a function of DC bias for DL-MoS_2 devices. The orange and blue bands in (e) represents the 10th to 90th percentiles for the devices.

method as applied to the first layer, preventing the delamination of the first layer during transfer. Following this, we employ the same electron beam lithography (EBL) process and resist stack to define the shape of the second layer of MoS_2. The subsequent etching sequence consists of an oxygen plasma and a chlorine (Cl_2) based plasma to patterning PMMA and MoS_2. After removing the resist stack with acetone, the second layer of MoS_2 is precisely defined, as depicted in Figure 5.12 (g). Finally, we employ another EBL step, utilizing pure PMMA as the resist, followed by the fabrication of 10 nm Ni + 20 nm Pd using a lift-off process. The final appearance of the device is illustrated in Figure 5.12 (h).

5.3.2 Static and dynamic EO characterization

To assess the electro-optic (EO) performance of DL-MoS_2, we swept the bias applied to the devices. The voltage applied to the long arm of the device was swept, while both electrodes of the short arm remained grounded. Figure 5.13 (a) and (b) shows examples for Al_2O_3-based and HfO_2-based DL-MoS_2, respectively. To prevent breakdown, we swept the voltage from -6 (-4) to 6 (4) V for AlO_x (HfO_2)-based DL-MoS_2. In both cases, we observed a noticeable left-shift of the interference fringes with minimal changes in depth. This suggests that the effective index is changing without impacting the device's loss. Based on the DC results, we examined DL-MoS_2 devices with varying lengths (100, 200, 400 µm) at V_{DC} = 0 V to calculate their propagation losses, as shown in Figure 5.13 (c). This yielded propagation loss values of 6.4 dB/cm and 49 dB/cm for AlO_x-based and HfO_2-based DL-MoS_2, respectively.

We then extended our calculations to evaluate the propagation losses under different applied bias voltages, as presented in Figure 5.13 (d). Across each sweeping range, the propagation losses exhibited minimal variation, indicating that biasing MoS_2 introduced negligible additional loss.

Continuing our analysis, we tracked the shift of the interference fringes to extract the Δn as a function of DC bias for both types of devices. This data is based on statistical results from 10 devices with varying lengths for each device type. In Figure 5.13 (e), the solid line represents the median value, while the upper and lower boundaries represent the 90% and 10% confidence intervals, respectively. Al_2O_3-based DL-MoS_2 exhibited a Δn >0.35e-3 when the bias is swept between -2 V and 2 V, resulting in 1 Vcm $V_\pi L$ when V_{pp} = 2 V was used for the calculation. Similarly, the HfO_2-based DL-MoS_2 showed its largest slope when V_{DC} = -3 V, yielding a $V_\pi L$ of ≈1 Vcm when V_{pp} = 2 V was employed for the calculation. The $V_\pi L$ as a function of DC bias is illustrated in Figure 5.13 (f).

Drawing from the insights derived from the data presented in Figure 5.13 (d) and (f), we have computed the figure of merit for phase modulation (FOM_{PM}) for AlO_x-based and HfO_2-based DL-MoS_2 devices. Our calculations yield values of 6.2 dBV and 56 dBV, respectively. Notably, both of these FOM_{PM} values surpass those reported for other 2D-based MZMs in existing literature (ranging from 66 dBV to 223 dBV) [27, 29, 262]. Furthermore, the FOM_{PM} value of 6.2 dBV for AlO_x-based DL-MoS_2 even outperforms silicon-based MZMs, which typically exhibit values in the range of 15 dBV to 22 dBV [7]. These results underscore the considerable potential of DL-MoS_2 as a highly efficient and low-loss phase modulator in the realm of optical devices.

We acknowledge that the second layer of MoS_2 remains uncapped and undoped,

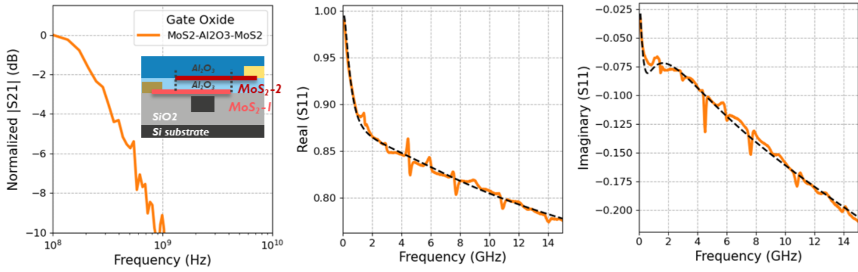

Figure 5.14: (a) Normalized S21 response, (b) real and (c) imaginary part of S11 response for Al_2O_3-based DL-MoS_2 with 100 active length.

leading to a significant resistance issue in the access region of MoS_2-2. This elevated resistance can impede reliable AC measurements. To assess the frequency response of DL-MoS_2, we opted to deposit AlO_x on top of the AlO_x-based DL-MoS_2. The deposition process mirrors the one used for the gate oxide, and this additional layer is expected to serve the dual purpose of encapsulating (protecting) and doping MoS_2-2. The schematic representation of this device can be seen in the inset of Figure 5.14 (a). It is worth noting that, due to time constraints, we were unable to complete the same process for HfO_2-based DL-MoS_2. Therefore, in this report, we solely present the AC results for the AlO_x-based device.

The frequency response analysis of the AlO_x-based DL-MoS_2 device was conducted using S-parameter measurements across a frequency range spanning from 0.1 GHz to 10 GHz. For the 200 µm-long device, we observed a bandwidth of approximately 0.3 GHz as shown in Figure 5.14 (a). To interpret these findings, we employed the equivalent circuit model depicted in Figure 5.6 (c). Here, C_{dv} now signifies the capacitance of the DL-MoS_2 structure, while R_{tot} represents the overall resistance, which encompasses the contact and sheet resistance of both MoS_2 layers. The fitting results for the real and imaginary parts of S11 are graphically depicted in Figure 5.14 (b) and (c), leading to calculated values of 436 fF for capacitance and 677 Ohms for resistance. Utilizing these parameters in the relevant equations, we estimated an electrical bandwidth of 0.5 GHz, a result that closely aligns with our experimental observations.

5.4 Conclusion

In this chapter, we have delved into the fascinating realm of two-dimensional materials-based photonics, with a primary focus on MoS_2 integration for efficient

phase modulation in photonic devices. Three distinct configurations have been explored, each offering unique insights and contributions to the field:

1.SL-MoS_2: The SL-MoS_2 structure was fabricated by sandwiching a gate oxide layer between a doped silicon waveguide and a single MoS_2 layer. This configuration offers a promising avenue for compact and efficient photonic device integration. The integration flow was comprehensively described, from silicon waveguide preparation to MoS_2 layer transfer, precise patterning, and metal contact fabrication. A significant breakthrough was the introduction of Al_2O_3 doping, which not only acted as an encapsulation layer for MoS_2 but also significantly improved the AC performance by modulating carrier concentration in the gated region. Static and dynamic electro-optic characterization revealed the low-loss characteristics of MoS_2, with minimal additional loss introduced upon integration. The electro-optic performance achieved with both p-type and n-type silicon-doped SL-MoS_2 devices was remarkable and competitive with state-of-the-art phase modulators. The study also provided insights into the importance of optimizing the separation between the doping region and the waveguide to further enhance device performance. In summary, this research has laid a solid foundation for the integration of MoS_2 into photonic devices, showcasing its potential as a versatile and efficient material for high-performance phase modulation.

2.G-O-MoS_2: This research aimed to extend the capabilities of traditional SL-MoS_2 phase modulators by introducing a novel configuration that leverages the unique properties of 2D materials. The dual-layer design eliminates the need for complex silicon implantation, enhancing the versatility of these devices by enabling integration on various substrates, including SiN and silicon slot waveguides. Static and dynamic electro-optic characterization revealed exciting outcomes for G-O-MoS_2 devices. The change in effective index (Δn) and phase modulation efficiency (VπL) surpassed those of SL-MoS_2 and even outperformed state-of-the-art 2D-based phase modulators, showcasing the potential of this configuration for medium-speed photonic applications. The frequency response analysis demonstrated a bandwidth of 0.85 GHz for a 100 µm device length, and potential improvements were identified by optimizing the gate oxide thickness to enhance the device's bandwidth. In summary, the integration of dual-layer G-O-MoS_2 structures has opened new avenues for advanced phase modulation in photonic devices.

3.DL-MoS_2: This study introduced the concept of Dual Single Layer MoS_2 (DL-MoS_2) as a promising low-loss phase modulator in the field of optical devices. This novel approach was developed in response to the relatively high loss observed in the Graphene-MoS_2 (G-O-MoS_2) configuration. Two different gate oxides, Al_2O_3 and HfO_2, were utilized, and the quality of the MoS_2 layers was monitored through photoluminescence measurements, which indicated a slight reduction

in bandgap following transfer. Static and dynamic electro-optic characterization experiments were conducted to assess the performance of DL-MoS_2. Bias voltage sweeping experiments showed a noticeable left-shift in interference fringes without a change of depth, suggesting a strong change in the effective index without impacting device loss. Propagation loss values of 6.4 dB/cm and 49 dB/cm were calculated for Al_2O_3-based and HfO_2-based DL-MoS_2, respectively. Furthermore, the study examined the shift of interference fringes to extract the phase modulation efficiency as a function of DC bias, yielding values of roughly VπL = 1 Vcm for both types of DL-MoS_2. The figure of merit for phase modulation (FOM_{PM}) was calculated as 6.2 dBV for Al_2O_3-based DL-MoS_2 and 56 dBV for HfO_2-based DL-MoS_2, surpassing values reported for other 2D-based modulators. In summary, the results underscore the considerable promise of DL-MoS_2 as a low-loss and good efficienct phase modulator in the realm of optical devices. Its superior electro-optic performance, particularly the great FOMPM values, positions it as a competitive candidate in the field, outperforming other 2D-based modulators and even silicon-based counterparts.

In conclusion, this chapter demonstrates the significant advancements made in the integration of MoS_2 within photonic devices, highlighting the versatility and potential of two-dimensional materials. Whether through SL-MoS_2, G-O-MoS_2, or DL-MoS_2 configurations, these studies open doors to exciting possibilities in optical communication and signal processing technologies. Further optimization and refinement in device design and fabrication processes promise even greater potential for two-dimensional materials-enabled photonics. Collectively, these findings contribute to the expanding field of two-dimensional materials-based photonics and hold promise for shaping the future of optical devices and applications.

Table 5.1 provides a summary of all the key results for three types of devices shown in this chapter.

Table 5.1: Overview of MoS_2-based modulators as discussed in this thesis, in comparison to state-of-the-art devices operating at the same wavelength (c-Band).

MZMs [reference]	EOT $[nm]$	Loss $[dB/cm]$	$V_\pi L$ $[Vcm]$	FOM_{PM} $[dBV]$	Bandwidth $[GHz]$
Si-oxide-Si [7]	5	60	0.25	15	5.6
Si-oxide-Si [7]	10	54	0.4	21.6	11.2
Si-oxide-Graphene [27]	10	≈236	0.28	66.1	5
Graphene-oxide-Graphene [227]	10	746	0.3	223	24
WS_2-oxide-ITO [29]	-	135	0.8	108	0.33
SL-MoS_2 (p-doped Si)	5	108	0.53	≈57.2	0.68
SL-MoS_2 (n-doped Si)	5	100	0.57	≈57.0	0.91
G-O-MoS_2 (HfO_2)	3.3	287	0.17	48.8	0.85
DL-MoS_2 (HfO_2)	5.8	49	1.14	56	-
DL-MoS_2 (Al_2O_3)	9.5	6.4	0.97	6	≈0.3

6 CONCLUSION and OUTLOOK

6.1 Conclusions

In this thesis, our primary focus was to address the core question embedded in our research objective: ”Can 2D material-based photonic devices be adopted by the industry for the next generation of data communication and telecommunications applications?”. To achieve competitiveness with state-of-the-art Si or Ge-based modulators, 2D material-based modulators must exhibit critical performance aspects. Starting from Chapter 2, we delved into the investigation and modeling of graphene-based modulators utilizing both SLG and DLG configurations operating at 1550 nm wavelength. The modulation of amplitude and phase has been studied, providing insights into the calculation of ER, IL, $V\pi L$, and different figure-of-merits. The outcomes underscored the superior modulation efficiency and figure of merit exhibited by DLG devices. However, for applications in data communications, modulators must not only showcase efficient modulation but also deliver high-speed performance. For instance, a device with a smaller EOT gate oxide can efficiently modulate (with smaller applied bias to transition between absorption and transparent regions), but it comes at the cost of significantly larger capacitance, resulting in slower speed. To provide a comprehensive understanding of the design intricacies of graphene-based modulators, we thoroughly modeled and discussed the trade-offs associated with key design parameters.

After the modeling, we shifted our focus to the first aim in addressing our core question. Moving away from laboratory-based processing for fabricating 2D-based photonic devices, a shift toward CMOS-compatible integration is imperative to achieve high yield, large volume, and low-cost production. This transition ensures that devices exhibit the crucial attributes of reproducibility and reliability, prerequisites for industry consideration in adopting 2D material-based modulators. Moreover, CMOS-compatible processing allows the seamless integration of graphene-based devices with other photonics and electronics components on the same chip. In Chapter 3, we showcased the integration of single-layer graphene electro-absorption modulators within a CMOS fabrication environment. Employing damascene contacts and standard lithography, we constructed wafer-scale devices adhering to industry standards. Through the optimization of three critical processing steps and the implementation of a CMOS-compatible dedicated integration approach, the device yield surpassed 95%, exhibiting loss, extinction ratio, and 3dB bandwidth values comparable to those of CVD graphene devices previously demonstrated in the lab. The insights gained from this integration are further leveraged to explore additional optimizations. We envision that the insights presented in this chapter can be extended and applied to a sophisticated library of building blocks for graphene-based optoelectronic devices, encompassing modulators, photodetectors, and sensors. The work presented in this chapter is poised to play a foundational role in driving the industrial adoption of graphene-based photonics devices.

In addressing our second aim, we shift our focus to demonstrating a competitive device performance. An ideal EO modulator must exhibit key characteristics, including a large extinction ratio, low insertion loss, high speed, and low power consumption. It is preferable for the device to have a compact footprint and a low driving voltage, making it compatible with CMOS circuitry. The exceptional physical properties of graphene, such as high mobility, broadband capability, flexibility to the substrate, temperature tolerance, and the ability to modulate both amplitude and phase, position graphene-based modulators as promising candidates for meeting these criteria. The numerous advantages inherent in graphene make it an intriguing material for potential transformation in the realm of silicon-based modulators. In Chapter 4, we conducted an experimental investigation focusing on strip and slot waveguide-based DLG modulators, encompassing EAMs, MZMs, and RMs. Both static and dynamic characterizations were performed for each modulator type. Notably, slot waveguide-based devices exhibited an enhanced modulation efficiency (0.038 $dB/\mu m/V$ and 0.079 Vcm), surpassing existing benchmarks in the literature. Furthermore, these devices demonstrated a commendable frequency response, boasting an approximately 16 GHz bandwidth. Despite these advancements, the figure of merit (TP over 20 dB and FOM_{pm} = 168 dBV) in our current amplitude and phase devices did not outperform our own strip-based devices (TP=8.9 dB and FOM_{pm} = 27.6 dBV). This discrepancy can be attributed to the

expanded evanescent field when using slot waveguides, necessitating the relocation of metal further away than in strip-based devices to mitigate additional losses from contacts. To gain a more profound understanding of the impact of key design parameters, we conducted a comprehensive simulation, elucidating the trade-offs associated with using slot waveguides. Our findings underscore the potential of slot waveguide-based devices as a superior platform for realizing high-performance modulators.

Finally, while graphene stands out as a significant member of the extensive 2D material family, numerous atomic-thick materials remain unexplored. In the current context, achieving pure phase modulation with minimal loss plays a pivotal role not only for high speed applications, optimizing data transmission rates, preserving signal integrity, and enabling advanced modulation formats, but also for low to medium-speed applications such as tuning and switching. Additionally, a low-loss and low-power phase modulator can potentially replace thermal heaters to compensate for fabrication errors. The challenge of demonstrating a low-loss pure phase modulator for graphene-based devices stems from the complexities introduced by the Kramers-Kronig relations. Alterations in carrier concentration impact both absorption and phase, necessitating the prevention of both interband and intraband transitions. Although the potential solution lies in gating with high carrier concentration on ultra-high-quality graphene, accomplishing this task proves challenging, especially in the context of large-scale manufacturing. Consequently, redirecting attention to other promising materials within the 2D family emerges as an intriguing approach. Utilizing alternative 2D materials with a bandgap larger than the incident light energy is expected to significantly reduce the device's loss. This exploration opens up new avenues for advancing pure phase modulation in 2D material-based devices

In Chapter 5, our exploration delves into MoS_2-based modulators designed for achieving low-loss phase modulation. Leveraging our prior experiences with graphene structures, we scrutinized three distinct configurations. Initially, SL-MoS_2 was employed to establish a robust foundation for the integration of MoS_2 into photonic devices. Tracking loss after each processing step highlighted the remarkable low-loss characteristics of MoS_2 at the C-band, with minimal additional loss upon integration. Subsequently, we combined this integration with a graphene layer to construct a GO-MOS_2 structure. The achieved phase modulation efficiency (0.17 Vcm) surpassed that of SL-MoS_2 (approximately 0.53 Vcm) and even exceeded state-of-the-art TMDC-based phase modulators (0.8 Vcm). Despite a relatively high loss (287 dB/cm, primarily from the graphene layer), the FOM_{pm} remained comparable with SL-MoS_2. To address this loss issue, we replaced the top graphene layer with a second layer of MoS_2 to form a DL-MoS_2. Benefiting from the low-loss characteristic of MoS_2, our device exhibited signif-

icantly reduced propagation loss (6.4 dB/cm). Coupled with an approximate 1 Vcm modulation efficiency, we achieved an impressive FOM_{pm} of 6 dBV. The superior electro-optic performance of MoS_2-based modulators positions them as competitive candidates in the field, outperforming other 2D-based modulators and even silicon-based counterparts.

To conclude, the cumulative efforts in this thesis contribute to advancing our understanding and application of 2D materials in photonic devices, paving the way for their industrial adoption in next-generation communication technologies.

6.2 Outlook

Over the past decade, graphene-based modulators have undergone significant development, commencing with the initial demonstration in 2011, followed by iterative device optimizations, and culminating in their integration into a CMOS pilot line as showcased in this thesis. Each stride in this trajectory not only represents progress in the field but also contributes to bridging the gap toward the commercialization of graphene photonics devices. These advancements have not only enhanced the technological landscape but have also laid the groundwork for the emergence of startups dedicated to furthering the application of graphene in photonics. However, for graphene-based modulators to dominate high-speed optical communication applications, several improvements are imperative. Foremost among these is the need to transfer high-quality graphene in a wafer-level scale. Despite promising potential demonstrated in simulations based on the assumption of using high-quality graphene, this is often not the case, especially in wafer-scale manufacturing. When graphene quality falls short, the graphene layer introduces additional loss (due to intra-band scattering), even in the transparent region. Furthermore, the carrier mobility does not reach the expected levels, leading to reduced speed results. The crux of this challenge lies not in graphene growth but in its transfer. Therefore, the development of a wafer-scale, CMOS-compatible transfer of high-quality graphene emerges as a critical path for graphene-based devices, bridging the gap between experimental and simulated results.

Another parameter with the potential to directly enhance device performance at no additional cost is the improvement of contact resistance. Lower contact resistance in graphene translates to a reduced RC delay, facilitating higher-speed performance. While various research groups have showcased contact resistances of around 100 $\Omega\mu m$ for graphene layers in laboratory settings, the challenge lies in seamlessly transferring this knowledge to a CMOS pilot line. Bridging the gap between laboratory-based results and integration into CMOS processes remains a formidable task. However, having good graphene quality and contact is not sufficient for a

real device. As highlighted in the thesis, graphene, being an atomic layer material, is susceptible to environmental influences. Consequently, it typically requires a suitable dielectric layer to enable the realization of high device performance. Currently, 2D hexagonal boron nitride is the preferred solution due to its clean van der Waals interface, but it is only suitable for encapsulation, not as a proper gate oxide, owing to its low dielectric constant. As a result, the quest for an ideal dielectric, whether a single material or a stack of various dielectrics, with an approach to scaling up in a CMOS pilot line, becomes an intriguing and crucial area of exploration.

After meticulously selecting suitable contacts and dielectric layers for high-quality graphene, the practical challenge of realizing high-performance modulators hinges on the intricacies of device design. As emphasized throughout this thesis, trade-offs are inevitable when striving for both high speed and efficiency in modulator performance. These trade-offs necessitate a delicate balance achieved by manipulating design parameters, as exemplified in Chapter 4 of this thesis. This underscores the critical importance of robust processing control to prevent misalignments, particularly in fine-designed dimensions. With precise processing control, devices with the correct dimensions can be fabricated, potentially exhibiting the expected performance. Exploring alternative structures, such as transitioning from SLG to DLG, and/or different mode profiles, such as moving from strip to slot waveguide-based devices, opens up new avenues for achieving optimal design configurations. Each modification introduces a level of freedom to pinpoint the most favorable design spots. Several potential solutions to enhance current devices are proposed in each chapter, yet each enhancement comes with its own set of costs. For instance, the introduction of a mode shifter in Chapter 3, while holding the potential to improve certain aspects, may increase the insertion loss of devices due to the incorporation of amorphous silicon with high loss. Similarly, our slot waveguide, designed to enhance mode interaction within a thin, low-refractive index region, also expands the evanescent field, leading to interaction with the absorptive access region graphene. Therefore, thorough simulation and practical considerations are inseparable components of the design process.

In the author's perspective, current graphene-based modulators have two primary challenges: (1) high loss and resistance in the un-gatable (access) region and (2) the complexity of gating graphene into the transparent (pure phase modulation) region. Both obstacles can potentially be overcome by significantly doping graphene layers. Doping graphene not only diminishes resistance in the un-gatable region but also mitigates absorptive tendencies, reducing the RC delay and device losses, respectively. Furthermore, our exploration of background doping in Chapter 2 reveals that, with a well-considered doping strategy, the transition curve shifts to approximately 0 bias. This observation indicates the feasibility of gating graphene

into the transparent region, facilitating pure phase modulation with a minimal bias applied. Ultimately, selective doping could be tailored to meet specific application requirements. The suggested avenues for enhancement outlined above are not limited to graphene; they can also be potentially implemented for MoS_2. Furthermore, the vast landscape of 2D materials offers numerous opportunities for diverse applications, including saturable absorption, photodetectors, and light sources. The exploration of various 2D materials holds great promise for advancing photonics applications. As we delve into the distinctive properties and capabilities of different 2D materials, the realm of photonics is poised for an exciting and transformative journey. The future holds the potential for a thrilling convergence of 2D materials and photonics, unlocking new possibilities and paving the way for innovative breakthroughs in technology and applications.

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