FACULTY OF ENGINEERING
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Co-Design of High-Speed Integrated SiGe BiCMOS Drivers and Silicon Mach-Zehnder Modulators for Optical Links

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Laurens José Breyne

Table of Contents

Glossary

A

AI	artificial intelligence
AM	amplitude modulator
AR	augmented reality
AWG	arbitrary waveform generator

B

BER	bit-error rate
BiCMOS	bipolar CMOS

C

CML	current mode logic
CMOS	complementary metal oxide semiconductor
CTLE	continuous time linear equalizer

D

DAC	digital-to-analog converter
DCD	duty-cycle distortion
DFF	dispersion flattened fiber
DML	directly modulated laser
DSF	dispersion shifted fiber
DSO	digital sampling oscilloscope

DSP	digital signal processing

E

EAM	electro-absorption modulator
EDFA	erbium doped fiber amplifier
EF	emitter follower
EIC	electronic integrated circuit
EML	externally modulated laser
ER	extinction ratio

F

FEC	feedforward error correction
FFE	feedforward equalizer
FGC	fiber grating coupler
FIR	finite impulse response
FSR	free spectral range
FWHM	full width at half maximum

H

HBT	heterojunction bipolar transistor

I

IC	integrated circuit
IL	insertion loss
IM/DD	intensity modulation and direct detection
IoT	Internet of Things
IQ-MZM	IQ Mach-Zehnder modulator
ISI	intersymbol interference

L

LSB	least significant bit

M

MMI	multimode interferometer
MOS	metal-oxide-semiconductor
MOSFET	metal-oxide-semiconductor field-effect transistor
MQW	multiple quantum well
MRM	micro-ring modulator
MSB	most significant bit
MZM	Mach-Zehnder modulator

N

NLC	nonlinearity compensation
NRZ	non-return-to-zero

O

OMA	optical modulation amplitude
OSNR	optical signal to noise ratio

P

PAM	pulse-amplitude modulation
PCB	printed circuit board
PD	photodiode
PDK	process development kit
PIC	photonic integrated circuit
PIN-PD	PIN-photodiode
PM	phase modulator
PRBS	pseudo-random bitstream

Q

QAM	quadrature-amplitude-modulation

R

RLM	level separation mismatch ratio
RTO	real-time oscilloscope
RX	receiver

S

SPI	serial peripheral interface
SPP	series push-pull
SRF	self resonance frequency
SSMF	standard single-mode fiber

T

TDECQ	transmitter and dispersion eye closure quatenary
TIA	transimpedance amplifier
TRX	transceiver
TW	traveling-wave
TW MZM	traveling wave Mach-Zehnder modulator
TX	transmitter

U

UHD	ultra high-definition

V

VCSEL	vertical-cavity surface-emitting laser
VGA	variable gain amplifier
VNA	vector network analyzer
VOA	variable optical attenuator
VR	virtual reality

W

WDM	wavelength division multiplexing

Nederlandstalige Samenvatting –Dutch Summary–

Het internet is geëvolueerd tot een hoeksteen van onze maatschappij. We gebruiken het om contact te houden met vrienden en familie, om video's te kijken, om te gamen, om online aankopen te doen .. Maar ook voor ons bankwezen, overheidsdiensten, gezondheidszorg, industrie en vele andere takken is het internet van vitaal belang. Een pandemie heeft het belang van zo'n globaal netwerk enkel maar verder onderstreept. De toename van het internetverkeer is dan ook heel sterk. De telecomgigant Cisco verwacht dat het globaal volume tussen 2017 en 2022 toeneemt van 120 miljard naar bijna 400 miljard gigabyte per maand.

Mochten we de weg volgen die onze data aflegt, dan leidt deze ons door een complex netwerk over verschillende landen en continenten tot bij een datacenter. Zo'n datacenter bestaat uit servers die een specifieke applicatie ondersteunen. Grotere centra bevatten vaak enkele tienduizenden servers die instaan voor het verwerken en opslaan van onze data. Aangezien deze servers samenwerken, zijn de verbindingen tussen servers van cruciaal belang. Het toenemend internetverkeer zet deze verbindingen onder druk: van het globaal internetverkeer moeten zij immers 70 % verwerken. Er is dus nood aan connecties met een hoge bandbreedte, laag energieverbruik en een lage kost.

Voor de meeste verbindingen tussen servers wordt glasvezel gebruikt omwille van de hoge bandbreedte en lage verliezen. Enkel om een afstand van enkele meter te overbruggen zijn elektrische verbindingen nog steeds goedkoper. Om een optisch signaal te genereren, wordt een elektrisch datasignaal op een optische draaggolf gemoduleerd door middel van een elektro-optische modulator. Het licht reist door de glasvezel en valt in op een fotodiode aan de ontvanger. Deze diode genereert een elektrische stroom die door middel van een transimpedantieversterker wordt omgezet naar een spanning en verder wordt verwerkt.

Om de capaciteit van een optische vezelverbinding te verhogen zijn er drie mogelijke vrijheidsgraden: een verhoging van het aantal verzonden datasymbolen per seconde, meerdere bits in een datasymbool verpakken of gebruik

maken van meerdere parallelle kanalen: verschillende golflengtes, vezels of beide polarizaties. De meest recente standaard voor intradatacenterverbindingen, IEEE802.3bs 400GBASE DR4, maakt gebruikt van vier parallelle kanalen (golflengtes), die elke een 53 Gbaud PAM-4 signaal versturen. Ieder datasymbool bevat dus 2 bits. Voor de volgende generaties wordt verwacht dat het aantal parallelle kanalen zal verdubbelen, om zo in totaal 800 Gb/s te versturen. Deze evoluties vergen een nauwe integratie en vereisen ook een laag vermogenverbruik aan zowel de zend- als ontvangstkant. Nieuwere generaties zullen waarschijnlijk ook een hogere datasnelheid en spectrale efficiëntie vereisen. Coherente optische communicatie, typisch gebruikt voor transcontinentale verbindingen, wordt op dit moment ook ontwikkeld voor verbindingen tussen datacenters (circa 80 km), zoals beschreven in de OIF 400G ZR standaard die gebruik maakt van 60 Gbaud DP-16QAM signalen. Dit werk spitst zich toe op het co-ontwerp van Mach-Zehndermodulatoren (MZMs) en de bijhorende hogesnelheidsschakeling om zo energie-efficiënte optische zenders te realizeren die aan hoge snelheden werken.

In het eerste deel van dit werk behandelen we het ontwerp van silicium Mach-Zehndermodulatoren. Silicium fotonica biedt compacte structuren met lage verliezen dankzij het hoge verschil in brekingsindex tussen de silicium kern en de siliciumdioxide mantel die samen de golfgeleider vormen. Verder kan het silicium platform gebruikmaken van gevestigde CMOS productielijnen, waardoor hoge volumes aan een lage kost geproduceerd kunnen worden. Dit werk focust op het gebruik van Mach-Zehndermodulatoren in optische zenders. De twee belangrijkste andere modulatortypes, ringmodulatoren (MRMs) of elektro-absorptie modulatoren (EAMs) mogen dan compacter zijn en minder energie verbruiken, ze zijn niet geschikt voor coherente communicatie. Daarnaast zijn MRMs erg gevoelig aan de golflengte en introduceren ze chirp. EAMs in een CMOS-compatibel platform functioneren enkel in de optische C-band. MZMs vertonen geen sterke golflengte afhankelijkheid, werken in zowel O- als C-band, zijn gemakkelijk in te stellen, introduceren erg weinig chirp en zijn geschikt voor coherente communicatie. Dit maakt hen uitermate geschikt voor de volgende generaties optische zenders.

Uit de analytische oplossing van het elektro-optisch frequentieantwoord van de MZM, kunnen we de meest belangrijke ontwerpparameters identificeren. Deze vormen het startpunt voor het ontwerp van een lopendegolf-modulator op imec's iSiPP50G platform die een 53 Gbaud PAM-4 signaal kan moduleren. Gegeven de PN-junctie voor de fasemodulatoren werd een elektrodestructuur met hoge bandbreedte ontworpen die tegelijk ook een naadloze integratie met onze aanstuurschakelingen toelaat. Om hoge bandbreedtes te waarborgen,

wordt de modulator gesplitst in twee lopendegolfsegmenten. Dit laat tevens ook toe om de modulator te gebruiken als 2-bit elektro-optische digitaal-naar-analoog omzetter (DAC). Dit stelt ons in staat om een aanstuurschakeling voor binaire signalen te gebruiken om de segmenten aan te sturen en kunnen zo de lineaire PAM-4 schakelingen met een hoger energieverbruik worden vermeden. De gefabriceerde modulatoren hebben echter een lagere bandbreedte dan verwacht. De metingen stelden ons wel in staat om onze simulatiemodellen te verbeteren voor toekomstige ontwerpen.

Een tweede ontwerp focust op het verhogen van de elektro-optische bandbreedte van onze MZMs. Een nieuwe techniek laat toe om egalisatie te integreren in het optische gedeelte van de modulator. Dit laat toe de bandbreedte van de modulator te verhogen, maar ook om de elektronische egalisatie (deels) te verschuiven naar het optisch domein. Zo verkrijgen we energie- en plaatsefficiënte egalisatie. De techniek werd gedemonstreerd in imec's iSiPP50G platform, maar kan ook toegepast worden in andere platformen.

Het tweede deel van dit werk behandelt het ontwerp van de geïntegreerde aanstuurschakelingen voor MZMs. Een vierkanaals > 50 Gb/s aanstuurschakeling werd ontworpen in een 55 nm SiGe BiCMOS platform. Ieder kanaal bevat een niet-lineaire uitgangstrap die tot 2 V_{pp} zwaai kan leveren door middel van twee parallelle differentiaalparen. Één paar heeft een gepiekt frequentieantwoord. Door de staartstromen van beide paren te variëren kan de relatieve contributie van het gepiekte antwoord ingesteld worden. Verder bevat ieder kanaal ook nog een egalisatietrap om eventueele bandbreedtebeperkingen van de voorgaande connecties of trappen op te heffen. Deze chip werd samen met de eerder ontworpen gesegmenteerde MZM geïntegreerd in een prototype optische zender om 50 Gbaud PAM-4 signalen op te wekken. De resulterende silicium zender verbruikt 3.6 pJ/bit, waardoor deze oplossing uitstekend kan concurreren met andere silicium zenders voor intradatacenterverbindingen.

Een 2-bit elektro-optische DAC is niet in alle situaties even toepasbaar door de vrij grote oppervlakte. Daarom werd er een tweede generatie chip ontwikkeld waarbij de vier kanalen elk 64 Gbaud PAM-4 signalen ondersteunen. Deze aanstuurschakeling is ontworpen in een 130 nm SiGe BiCMOS proces en bevat een lineaire uitgangstrap die een spanningszwaai van 2 V_{pp} kan genereren en een niet-lineaire uitgangszwaai van 3 V_{pp}. Om zo'n hoge spanningszwaai mogelijk te maken, werd een doorslagverdubbelaar gebruikt in de uitgangstrap. Deze werd geoptimalizeerd voor hoge snelheden, een hoge linearitеit en een laag energieverbruik. Verder bevat ieder kanaal terug een egalisatietrap die het frequentieantwoord kan laten pieken. Een instelbare versterker helpt om de totale versterking van een kanaal te regelen. Een niet-lineaire com-

pensatieschakeling werd geïntegreerd om de binnenste niveaus van het PAM-4 signaal te comprimeren als compensatie voor compressie van de buitenste niveaus door de uitgangstrap of de modulator. Een kanaal verbruikt ongeveer 2.7 pJ/bit.
Op het einde van dit werk wordt een kort overzicht gegeven de volgende stappen in dit onderzoek. We gaan dieper in op de volgende stappen in het modulatorontwerp en lichten ook toe welke volgende stappen genomen kunnen worden om het vermogenverbruik van de aanstuurschakelingen verder te verlagen. Deze worden gemotiveerd door middel van technologische vooruitzichten.

English Summary

The internet has become a cornerstone of our modern society. Applications are virtually endless: keeping in touch with friends and family, streaming video, gaming, e-commerce, but also banking and government affairs, healthcare, industries and many others. A pandemic emphasizes the importance of such an ubiquitous network, both from a social as well as an economic point of view. In the last four decades, the global traffic has been ever increasing, a prediction by Cisco shows an increase in internet traffic from 120 billion GB per month in 2017 to 400 billion GB per month in 2022.

Tracing back the origin of data leads us from the end-user through a complex network over various hierarchical levels and geographical areas that span the internet. Ultimately, we arrive at the datacenter that hosts a specific application. The datacenter houses many interconnected servers that perform the computations and store data, in larger datacenters tens of thousand of servers can be present. With the increasing traffic, significant challenges are imposed on the design of datacenters. Especially interconnections between servers are under tremendous strain, around 70 % of all internet traffic flows inside the datacenter. High-bandwidth, low-power and low-cost interconnects are required to keep up with the ever-expanding internet.

Many of the connections between servers are implemented using fiber-optic links. Only for the shortest links spanning a few meter, copper connections are currently more cost-efficient. Longer links, reaching a span of up to 2 km, are implemented using fiber-optics due to their superior bandwidth and loss characteristics. At the transmitter side, the electrical data is encoded onto the optical carrier through a modulator. The light is sent through the fiber and is detected by a photodiode at the receiving side. The light is converted to an electrical current and converted to a voltage with sufficient swing using a transimpedance amplifier before further processing.

In order to scale the link capacity, three degrees of freedom can be exploited: increasing the number of datasymbols sent per second, increase the number of bits contained in a datasymbol or make use of more parallel channels (wavelengths, fibers or both polarizations). These are reflected in the most recently

approved standard, IEEE802.3bs 400GBASE DR4, where four parallel lanes (wavelengths) are used, each carrying a 53 Gbaud PAM-4 signal. So each symbol contains 2 bits. For the next generation links, likely carrying 800 Gb/s, the number of lanes is expected to double. This puts quite some additional constraints on integration and power consumption at the transmitter and receiver. Future generations will probably further scale further in baudrate and spectral efficiency. Furthermore, coherent fiber optic links, typically employed in transcontinental interconnects, are being developed for datacenter-datacenter interconnects (approx 80 km), as e.g. described by the OIF 400G ZR standard which makes use of 60 Gbaud DP-16QAM signaling. This dissertation focuses on co-designing Mach-Zehnder modulators (MZMs) and integrated driver circuits enabling high-speed low-power optical transmitters.

In the first part of this dissertation, the design of silicon MZMs is covered. Silicon photonics provide compact, low-loss structures thanks to the high effective index difference between the silicon core and silica cladding. Furthermore, low-cost, high-yield, high-volume integrated circuits are possible due to the CMOS-compatibility. This work focuses on the use of MZMs in optical transmitters. While competing modulators like micro-ring modulators (MRMs) and electro-absorption modulators (EAMs) have a smaller footprint and potentially provide a lower power consumption, both are not suited for coherent optical communication. Furthermore, MRMs have a very high wavelength sensitivity and introduce significant chirp. EAMs embedded in a CMOS-compatible platform only function in the C-band. MZMs are easy to bias, show optical broadband behavior, provide O- and C-band operation, can be chirp free and are suited for next generation interconnects due to their coherent capabilities.

The electro-optic frequency response of the MZM is analyzed and the most important performance tradeoffs are identified. These were used as starting point for the design of a traveling-wave (TW) modulator on imec's iSiPP50G platform for a 53 Gbaud PAM-4 optical link. Given the PN-junction based phase modulator, an electrode structure was developed with optimized high-speed characteristics while allowing seamless integration with the driver integrated circuit (IC). To enable high bandwidths, the modulator is split into two traveling wave segments. At the same time, this enables a 2-bit electro-optic digital-to-analog converter (DAC) functionality. Since two low-power binary drivers can be used to drive the segments, a power hungry, linear PAM-4 driver is avoided. The measured bandwidth of the fabricated devices was lower than expected, however the device characterization led to improved simulation models for future design iterations.

A subsequent design focused on increasing the electro-optic bandwidth of the

devices. A novel technique is developed to embed finite impulse response (FIR) filters in the optical domain. The FIR filter can be used to boost the device bandwidth, or (partially) take over equalization from the electrical equalizers. The technique allows very power and area efficient equalization. While the technique is demonstrated on imec's iSiPP50G platform, it is not limited to silicon photonics.

The second part of the dissertation covers the design of driver ICs for the MZMs. A four channel > 50 Gb/s limiting driver is designed on a 55 nm SiGe BiCMOS platform. Each channel contains a limiting outputstage capable of 2 V_{pp} swing using two parallel differential pairs. One pair introduces peaking in the response, thus by changing the tail currents it is possible to tune the peaking while keeping the output swing constant. Furthermore, each channel also contains a continuous time linear equalizer (CTLE) at the input to compensate for bandwidth limitations preceding the driver. This driver was paired with the previously designed segmented traveling-wave modulator to demonstrate 50 Gbaud PAM-4 generation. The resulting silicon optical transmitter has a power efficiency of 3.6 pJ/bit, best-in-class for silicon optical modulators using MZM as these rates for intra-datacenter interconnects.

As such 2-bit electro-optic DAC solution might not be beneficial in all cases, due to the required footprint, a second generation driver IC was developed, containing four channels each capable of 64 Gbaud PAM-4. The driver was designed in a 130 nm SiGe BiCMOS technology and is able to reach a linear output swing of 2 V_{pp} and a full swing of 3 V_{pp}. To enable these high swings, a breakdown voltage doubler architecture was adopted. The stage was optimized for high bandwidth and linearity. Furthermore, a CTLE is available to introduce peaking. A variable gain amplifier (VGA) helps to finetune the gain and a nonlinearity compensation (NLC) circuit is present to precompensate for symmetric compression by the driver or the subsequent modulator. When transmitting 64 Gbaud PAM-4, the power efficiency of a channel is 2.7 pJ/bit.

At the end of this dissertation, a brief description of the next possible steps in the research is provided. These are motivated using some future prospects.

List of Publications

Publications in International Journals

1. **L. Breyne**, G. Torfs, X. Yin, P. Demeester, and J. Bauwelinck, "Comparison Between Analog Radio-Over-Fiber and Sigma Delta Modulated Radio-Over-Fiber," *IEEE Photonics Technology Letters*, vol. 29, no. 21, pp. 1808–1811, 2017.

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1 Introduction

1.1 The ever-expanding internet

The internet has become a cornerstone of our modern society. Applications are virtually endless: keeping in touch with friends and family, streaming video, gaming, e-commerce, but also banking and government affairs, healthcare, industries and many others [1]. A pandemic emphasizes the importance of such an ubiquitous network, both from a social as well as an economic point of view. In the last four decades, the global traffic has been ever increasing [1], a prediction by Cisco for the period between 2017 and 2022 is shown in Fig. 1.1(a). Various emerging applications, each more popular than the others, drive traffic each time to more astonishing rates [2]. New applications and technologies, like Internet of Things (IoT), ultra high-definition (UHD) video, virtual reality (VR) and augmented reality (AR), 5G, artificial intelligence (AI) and cloud computing are presenting themselves to continue this cycle leading to an ever-expanding internet.

Tracing back the origin of data leads us from the end-user through a complex network over various hierarchical levels and geographical areas that span the internet. Ultimately, we arrive at the datacenter that hosts a specific application or parts thereof. The datacenter houses many interconnected servers that perform the computations and store data, in larger datacenters tens of thousand of servers can be present [2]. Consequently, significant challenges are imposed on the design of datacenters with the increasing traffic. Espe-

cially interconnections between servers are under tremendous strain, as shown in Fig. 1.1(b). Around 70 % of all internet traffic flows inside the datacenter. Fig. 1.1(a) concerns the datacenter-to-user traffic, so the actual traffic rates inside the datacenter are a fivefold of Fig. 1.1(a). High-bandwidth, low-power and low-cost interconnects are required to keep up with the ever-expanding internet.

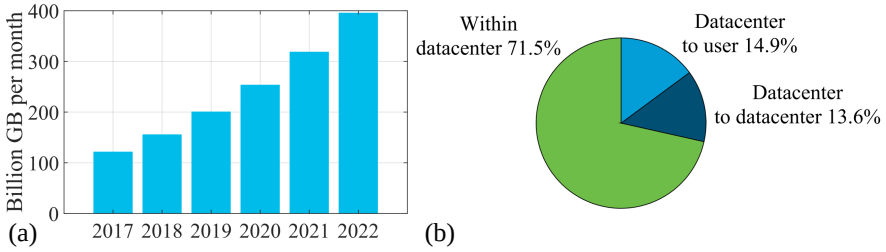

Figure 1.1: (a) Global Internet Traffic as predicted by Cisco. (b) Traffic breakdown as predicted by Cisco for 2021 [3].

1.2 Datacenter interconnects

1.2.1 Fiber-optic link

Many of the connections between servers are implemented using fiber-optic links. Only for the shortest links spanning a few meter, copper connections are currently more cost-efficient [4]. Longer links are implemented using optics, reaching spans of up to 2 km. A basic block diagram of a fiber-optic link for intensity modulation and direct detection (IM/DD) is given in Fig. 1.2. At the transmitter side, the intensity of the light is modulated, either using direct or external intensity modulation. Driving electronics are typically required to boost the weaker data signals. The modulated light is then transmitted over the fiber-optic channel to the receiver. A photodetector converts the light intensity to an electrical current, while a transimpedance amplifier converts this weak current to a voltage and amplifies it before further processing.

Two cases should be distinguished at the transmitter side: direct or external intensity modulation [5]. In the first case, the driving electronics directly modulate the intensity of the optical source, e.g. by changing the current through a laser diode. Hence the optical modulator is omitted. In an externally intensity modulated system, the optical source is kept at a fixed intensity while data is coded on the optical carrier using the modulator. While direct intensity modulation provides advantages in system complexity and size, direct inten-

sity modulation in semiconductor lasers causes an accompanying frequency modulation which limits the fiber reach and bandwidth [6]. External intensity modulators can exhibit much less residual frequency modulation, thus they are often preferred for high-speed systems [5].

Moreover, certain externally modulated systems allow control over the optical phase, resulting in an extra degree of freedom to improve the bit rate. Note that an adapted optical receiver is required to also extract the phase. Such systems are referred to as coherent systems. These systems are typically used for very long (100's or 1000's of km) distance optical links since the fiber optic channel induces dispersion and significant losses over long distances. Controlling and measuring the phase is key in such a system not only to improve the bit rate but also to counteract e.g. the dispersion. Recent trends shows however that coherent fiber-optic communication will also become a important enabler for optical interconnects between datacenters in relative close proximity, from 10's to 100's of km [7, 8].

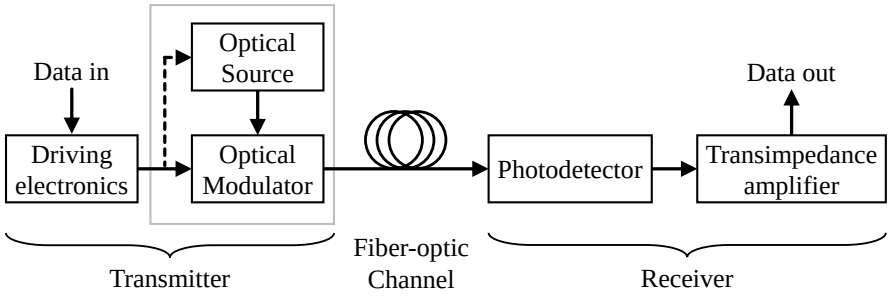

Figure 1.2: General block diagram of an IM/DD optical link.

For datacenter interconnects, a transmitter (TX) and receiver (RX) are present at both sides of the fiber optic channel, they are grouped together in a transceiver (TRX) to allow full duplex communication. Additional electronics for equalization, (de)muxing, clock-and-data recovery, (de)coding and control functions are added in the same package to form a pluggable optical module [9]. Two modules can be connected using a fiber-optic channel and can be plugged directly in the datacenter's switches. Both the package, electrical & electro-optic interface and functionality are standardized by several consortia and standarization bodies [10–12].

1.2.2 Scaling the link capacity

There are several ways to improve the capacity of datacenter interconnects: increase the number of datasymbols sent per second, increase the number of

bits contained in a datasymbol or make use of several parallel channels. These three options are also reflected in the available industry standards and shown in Fig. 1.3. We'll first discuss how these three degrees of freedom resulted in today's bit rates. Thereafter, we'll discuss how future systems can exploit these dimensions to answer increasing demands.

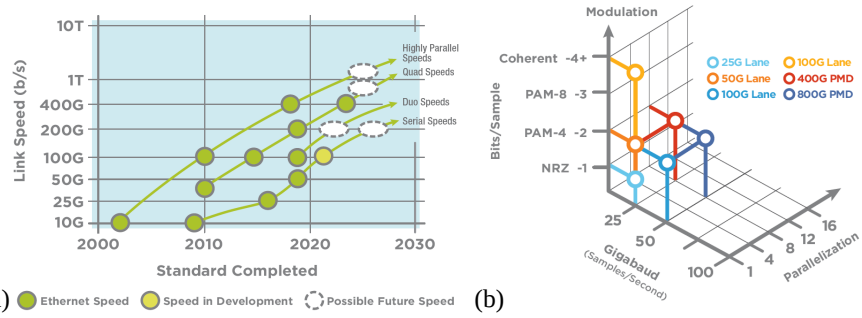

Figure 1.3: (a) Evolution of the link capacity over the years. (b) The degrees of freedom used to scale the link capacity in most recent standards. [9]

An obvious way to increase the link capacity is by adding additional parallel lanes, either by using separate fibers or multiple wavelengths inside one fiber [13]. However, the scalability in current systems is limited as more channels require more transceivers, and more lasers in the case of wavelength division multiplexing (WDM), inside one module. As a result, the packaging cost and complexity increase tremendously. Furthermore, the actual module size is limited and stringent thermal constraints exists to avoid overheating. At the time of writing, rarely more than 8 parallel channels are used per module. Note that also other physical dimension can be used to increase the number of lanes: e.g. both polarization of the light can be used, or the more exotic multicore fiber containing several fiber cores in relative close proximity [13]. A second scaling vector is the number of symbols sent per second. Latest standards currently require at 53.125 Gbaud signaling [14]. Further scaling will require even faster electronics and optical components and clever designs to keep pushing the symbol rate while avoiding overly complex and power hungry transceivers. Technology limits both on the optical and electronic side will cap the maximal symbol rate, together with the increasing importance of interface parasitics, both at the electrical input interface as well as the driver-modulator interface. The last dimension that can be exploited is the spectral efficiency, i.e. packing more bits inside a single symbol. In the latest 400GBASE standards [14], the spectrally less efficient 2 level NRZ signals have been replaced by 4 level pulse-amplitude modulation (PAM) signals. As the latter can contain 2 bits per symbol compared to 1 for NRZ, the net bit rate doubles.

Higher spectral efficiencies require more linear electronics and optics, which costs power, and are more prone to channel impairments.

Most recent standards, like 400GBASE-DR4 use 4 parallel fibers each operating at 53.125 Gbaud PAM-4 over 500 m single mode fiber [14]. For longer reaches, the 400GBASE standards use 8 wavelengths inside one fiber while each lane supports 26.5625 Gbaud PAM-4 [15]. Due to fiber impairments, like chromatic dispersion and loss, a lower data rate is required for longer fiber reaches. The next step is towards 800GBASE systems, which will most likely reuse part of the 400GBASE system: 8 lanes operating at 53.125 Gbaud PAM-4 for $<$2 km operation are being developed [16]. Closer integration of the optics and driving electronics with the server and switch will alleviate the area limitations, lower the integration cost and improve the interfacing between server/switch and module [17]. This demands low-power, high-yield and high-performance electro-optic transceivers that allow flawless integration.

Last paragraphs mainly discussed IM/DD systems. These can offer excellent performance over relative short distance and very high speeds. As explained earlier, the inter-datacenter link are quickly rising to the attention. Such links could offer intra-datacenter capacity over inter-datacenter reaches. Recently, the 400GBASE-ZR and ZR+ standards were approved [18]. These describe 60 Gbaud 16-quadrature-amplitude-modulation (QAM) (4 bits per symbol) over up to 80 km without any optical amplification. Larger distances are included but require optical amplification

1.3 Overview of this work

Previous sections emphasized the importance of high-speed, low-power, low-cost optical interconnects to keep up with the ever-expanding internet. This work focuses on the development of optical transmitters for such intra-datacenter applications. By approaching the problem from both the electronic as well as the photonic side, new insights can be achieved on how both sides can be designed for optimal integration.

Various silicon photonic traveling-wave Mach-Zehnder modulators (MZMs) were designed to operate with our drivers. The use of silicon photonics allows very compact, low-cost, high-yield optical circuits thanks to the compatibility with the CMOS process flow. In order to optimize the bandwidth of the MZMs, the electrode structure was optimized. Improvements of the phase-shifter are beyond the scope of this dissertation. Furthermore, in most commercial processes, optimization of doping levels is not possible. In a first design, a segmented traveling-wave (TW) MZM was designed and characterized. Two shorter segments have a higher bandwidth than one single long modulator while also allowing the modulator to be used as a 2-bit electro-optic digital-

to-analog converter (DAC). As both segments can be driven by nonlinear NRZ drivers, the use of power-hungry linear PAM-4 drivers can be avoided. A driver IC hosting four channels each capable of supporting up to 60 Gb/s NRZ signals is designed in a 55 nm SiGe BiCMOS technology. Specific care has been taken to optimize and simplify the interconnections with the modulators and to allow simple equalization to mitigate possible bandwidth limitations due to the driver-modulator interconnection or the modulator itself. By combining the driver IC and segmented traveling wave Mach-Zehnder modulator (TW MZM), a 50 Gbaud PAM-4 transmitter is obtained without having to use a linear driver IC. The power efficiency of the optical transmitter goes beyond state of the art compared to other silicon optical transmitters operating at the same rates. This work has been published in [19].

Further research on Mach-Zehnder modulators focused on how the bandwidth of silicon photonic MZMs could be improved, without having to adjust the optical phase shifters themselves. This path led to a new technique which allows adjusting the electro-optic frequency-response of the modulator to the designer's needs with only some minor changes to the optical waveguide routing. Due to the earlier constraints, the proposed technique is technology independent. The technique not only allows to boost the modulator bandwidth, but can take over part of the equalization in the link. Since the equalization is embedded in the modulator, it is very power- and area efficient. Using experiments, the advantage of such equalization has been shown with respect to conventional MZMs This work has been published in [20, 21].

For a second generation driver IC, the design focus was shifted towards generating linear signals while keeping power consumption under control. The IC hosting 4 channels each capable of 64 Gbaud PAM-4 signaling was designed in a 130 nm SiGe BiCMOS technology. Particular attention was paid to the output stage to optimize for large-swing linear signals while avoiding breakdown. The driver also features a variable gain amplifier (VGA) and nonlinearity compensation (NLC) was added to precompensate for symmetric compression of the PAM-4 eyes due to the driver itself or the subsequent modulator.

The author is involved in the EU H2020 PICTURE project [22]. PICTURE aims at developing a high-performance III-V on Silicon platform to enable 400 Gb/s transceivers. The four channel 64 Gbaud PAM-4 driver is designed within the scope of this project. Furthermore, the PAM-4 driver is currently being used for initial testing in the EU H2020 CALADAN project [23]. CALADAN focuses on wafer-scale assembly of terabit optical engines using micro transfer printing. Next to the experiments conducted within the scope of this PhD, the NRZ driver was used to demonstrate the possibilities in the photonic packaging pilot line set up by the EU H2020 PIXAPP project [24].

1.4 Outline of this dissertation

This dissertation is divided into two parts. The first part covers the analysis, modeling, design and measurements of the Mach-Zehnder modulators designed on imec's iSiPP50G silicon photonic platform. Chapter 2 covers the fundamentals of high-speed optical modulation. The most important performance metrics are outlined, followed by a brief introduction on the most common integrated optical modulators. We describe an in-depth analysis of the high-speed electro-optic response of MZMs in chapter 3. The most important design tradeoffs are synthesized and the design procedure for the segmented TW MZM is covered. The simulation is verified and optimized using measurements on fabricated devices. To conclude this first part, the electro-optic frequency response shaped MZMs are covered in chapter 4. A framework for the modeling of the modulator response is derived and used to develop a proof-of-concept device. Through experiments, the advantages of such a shaped design are demonstrated.

The second part of this dissertation shifts the focus to the driver integrated circuits (ICs). Chapter 5 covers the design of the four channel > 50 Gb/s NRZ driver in a 55 nm SiGe BiCMOS technology. Various topologies for the output stage are compared. The design of the input stage, continuous time linear equalizer (CTLE), predriver and output stage are covered. The finished driver is integrated with the earlier developed 2-bit segmented modulator to demonstrate the 50 Gbaud PAM-4 capabilities. The second generation driver, consisting of four 64 Gbaud PAM-4 channels is outlined in chapter 6. The IC is designed in a 130 nm SiGe BiCMOS technology. A more advanced output stage design is developed, while keeping the requirements on linearity and power consumption in mind. The operation of the driver is verified through post-layout simulations.

Chapter 7 concludes this work. Possible improvements for future designs are discussed, as well as prospects on silicon optical transmitters for datacenter interconnects.

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Part I

High Speed Mach-Zehnder Modulators

2 High-Speed Optical Modulation

This chapter discusses the advantages of most common modulation techniques with the focus on high-speed, integrated transmitters. We first dive into why the more complex external (intensity) modulation is advantageous over direct modulation in fiber optic systems. Next, we briefly review some typical techniques to perform modulation and discuss the operation, advantages and disadvantages of Mach-Zehnder modulators (MZMs), micro-ring modulators (MRMs) and electro-absorption modulators (EAMs). Furthermore, we will discuss how they can be integrated on various material platforms. The most important performance metrics will be listed.

2.1 Performance Metrics

As a basis for the remainder of this work, we go through some of the most important performance metrics in optical modulation. The optical eye diagrams of an NRZ and PAM-4 waveform are shown in Fig. 2.1 and serve as a visual aid.

The average launch power $\mathrm{P_{avg}}$ is defined as the average power of the signal launched into the fiber and is often standardized. For example, the most recent 400GBASE-DR4 standard [1] requires $\mathrm{P_{avg}}$ to be between -3.3 and 3.5 dBm to ensure compliance between components from different vendors. In our symmetric eye-diagrams of Fig. 2.1, the average power is in the middle of the eye. However, this can shift due to asymmetry in the transmitter.

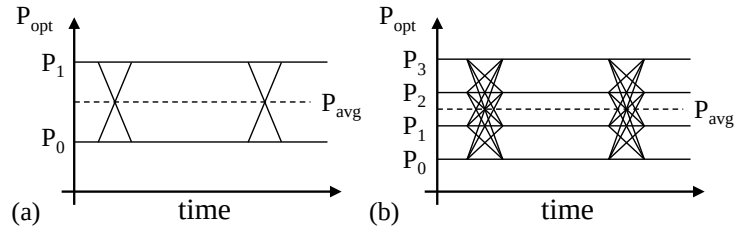

Figure 2.1: Simplified eye diagrams of a NRZ waveform (a) and a PAM-4 waveform (b).

The insertion loss (IL) is the loss of the complete modulator device, calculated as the difference between the input power to the device and the maximal launch power. This typically includes the losses from the device itself, but also from the input-output coupling, combiners and splitters. Note that in certain modulators, loss due to biasing is listed as modulation loss. For example, MZMs used for intensity modulation have 3 dB additional loss due to the quadrature biasing.

The extinction ratio (ER) is the ratio between the outermost levels, thus:

$$\mathrm{ER_{NRZ}} = 10\log_{10}\left(\frac{\mathrm{P_1}}{\mathrm{P_0}}\right), \qquad \mathrm{ER_{PAM-4}} = 10\log_{10}\left(\frac{\mathrm{P_3}}{\mathrm{P_0}}\right) \tag{2.1}$$

The ER is a measure on how well a '0' can be generated in the optical domain. If $\mathrm{P_0}$ is actually zero, then the ER becomes infinite. In practical modulators, $\mathrm{P_0}$ will never be zero, so the ER will be finite. For a given average launch power, it is also a measure on the eye-height. A lower ER means that the outermost levels are closer, which complicates detection. Note that the ER is independent of the optical power incident on the modulator. Changing the incident power results in the same change in outermost levels, which cancels due to the division. For a given modulator, a higher driving voltage can increase the ER. The 400GBASE-DR4 standard [1] requires a minimum ER of 3.5 dB.

The optical modulation amplitude (OMA) is the actual eyeheight, i.e. the difference between the outermost levels, defined as:

$$\mathrm{OMA_{NRZ}} = 10\log_{10}(\mathrm{P_1} - \mathrm{P_0}), \qquad \mathrm{OMA_{PAM-4}} = 10\log_{10}(\mathrm{P_3} - \mathrm{P_0}) \tag{2.2}$$

A high OMA indicates a large eye, the levels are further apart, thus the receiver will have an easier job distinguishing between the levels in a noisy environment. A higher OMA can be achieved by a higher driving voltage or optical launch power. Due to the optical power dependency, modulators with higher insertion loss may have a worse OMA.

The **electro-optical bandwidth** is defined as the frequency at which the OMA has dropped by 3 dB with respect to its low-frequency value. As such, it limits the symbol rate of the signal being processed by the modulator. The bandwidth limitation can be caused due to electrical limitations (e.g. interconnection parasitics), electro-optical effects (e.g. carrier lifetimes) or optical effects (e.g. velocity mismatch). In reality, a combination of several effects will be present.

The **chirp parameter**, also sometimes referred to as linewidth enhancement factor (as a similar effect is present in directly modulated lasers), is a measure of the frequency modulation accompanying the desired amplitude modulation in modulators. For external modulators, it can be defined as [2]:

$$\alpha = 2\frac{\frac{d\phi}{dt}}{\frac{1}{S}\frac{dS}{dt}} \tag{2.3}$$

With $\phi(t)$ the instantaneous phase and $S(t)$ the intensity. Due to the interplay between the phase modulation and chromatic dispersion in an optical fiber, the link bandwidth can be severely affected. This is a key point of the following section.

2.2 Direct versus external modulation

The most simple way to encode information on an optical carrier is using direct intensity modulation. This only requires modulation of the current through the laser diode, resulting in a directly modulated laser (DML), shown in Fig. 2.2. As only a laser diode is required, the final assembly can be very simple, compact and cheap [3]. However, directly modulated systems produce low-quality optical signals compared to external modulation for several reasons. As these lasers have a certain threshold current that needs to be exceeded to start the lasing, operation below this current causes significant delay, jitter and distortion [3]. This is typically resolved by avoiding operation below the threshold current, at the cost of a decreased optical signal swing. Next, certain DMLs like vertical-cavity surface-emitting lasers (VCSELs) show limited linearity. DMLs are temperature dependent, complicating integration with the heat-dissipating electronics. While these problems can be solved by clever tricks, laser diodes face a more fundamental issue: the intensity modulation is accompanied by a residual frequency modulation, thus there is a significant amount of chirp. This is an inherent effect present in any laserdiode [4]. The chirp, typically manifest itself as pulse broadening of the symbols over time when transmitted over an optical fiber. As such transmission at high baudrates

over longer fiber reaches will be severely impaired due to the interplay of chirp and chromatic dispersion in the single-mode fiber.

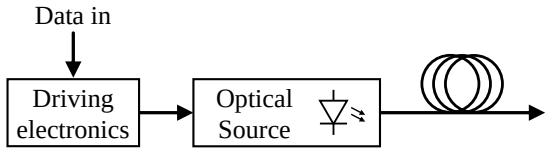

Figure 2.2: Block diagram of a direct intensity modulated transmitter using a laser diode.

Chromatic dispersion quantifies the frequency dependence of the fiber mode effective index. Assuming the optical output field of a pure laserline consisting of a single frequency, e.g. 193.5 THz or 1550 nm in vacuum. Sinusoidal modulation with frequency f_{RF} results in two additional tones at f_{RF} below and above the carrier tone. We assume there is no additional phase difference between these tones, i.e. there is no chirp. Due to the effective index difference between the various tones, they travel at different speeds through the fiber and reach the detector with a certain delay or phase difference. In an intensity modulation and direct detection (IM/DD) system, the receiver uses a photodiode to convert the optical field to an electrical current. However, the photodiode senses the power of the optical field, which is proportional to magnitude of the optical field squared. This operation causes mixing of the various tones. Combined with the phase difference due to chromatic dispersion, tones at certain frequencies will destructively interfere. For broadband signals, certain frequency components will destructively interfere. In [5], an analytical solution is derived for the response of such dispersive channels. In Fig. 2.3, the normalized transmission in an IM/DD system with chromatic dispersion operating at 1550 nm is shown over 1, 2 and 5 km without chirp. A typical number for chromatic dispersion at this wavelength is 16 ps/(nm.km). When 1 km standard single-mode fiber (SSMF) is present, the first notch occurs at 62.5 GHz, however, the 3 dB bandwidth of the system is 44.1 GHz, excluding additional bandwidth limitations from the transmitter and receiver. When extending the reach to 2 and 5 km, the notches occur at 44.2 & 27.9 GHz respectively and the 3 dB bandwidth drops to 32.2 & and 19.7 GHz. Given the Nyquist frequency of 53 Gbaud PAM-4 is at 26 GHz, 2 km of fiber transmission will already experience some impairments, while 5 km fiber will significantly impair the signal.

When generating a signal with chirp at the transmitter, the residual phase modulation causes an additional phase shift between the tones below and above the carrier tone. This additional phase shift, together with the phase difference

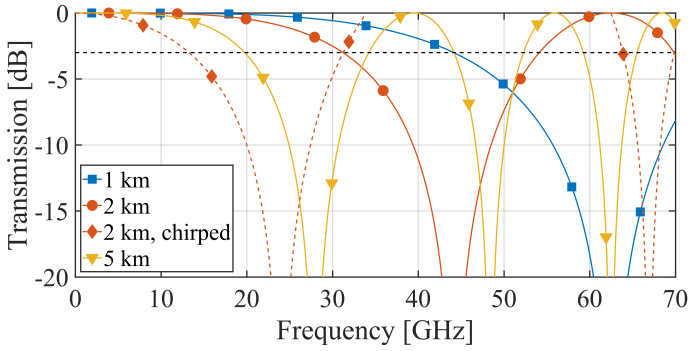

Figure 2.3: Normalized response from the electrical input to the electrical output of an IM/DD system operating at 1550 nm with 16 ps/(nm.km) dispersion over various fiber reaches without chirp and with a chirp parameter of 2 for a fiber reach of 2 km.

induced by dispersion, shifts the destructive interference to other frequencies. Depending on the sign of the fiber dispersion and the chirp, the destructive interference shifts to higher frequencies or to lower frequencies. Again the model of [5] can be used. When the fiber dispersion and chirp have opposite sign, the bandwidth of our IM/DD system drops. The response over 2 km fiber with a chirp parameter of 2 is given in Fig. 2.3 , all other parameters remain unchanged. This causes the first notch to occur at 23 GHz instead of 44.1 GHz while the 3 dB bandwidth drops from 32.2 GHz to 13.3 GHz. Note that this is a very reasonable value for DMLs, e.g. [6] and [7] report chirp parameters up to 6.5 and 5.5 respectively.

Because of this reason, intra-datacenter interconnects are often operated in the O-band (1260-1360 nm) rather than the C-band (1530-1565 nm) because the O-band has virtually no dispersion compared to the C-band. The dispersion of various wavelengths is given in Fig. 2.4(a). Between 1300 and 1324 nm [8], dispersion in the O-band even crosses zero, while a typical value at 1550 nm is 16 ps/nm.km. Note that while dispersion in the O-band is close to zero, a sufficient amount of chirp can still cause the notch to shift sufficiently far down over longer fiber reaches to limit the system bandwidth [7]. A disadvantage of O-band systems is the higher fiber attenuation, see Fig. 2.4(b): typically 0.5 dB/km instead of 0.2 dB/km. Since datacenter interconnects are typically only a few kilometer long, this excess attenuation is a fair cost to pay. More exotic fiber types, like dispersion shifted fiber (DSF) and dispersion flattened fiber (DFF) have less dispersion in the C-band, but they come at a higher attenuation and a higher cost. Therefore, they are typically not used in datacenters.

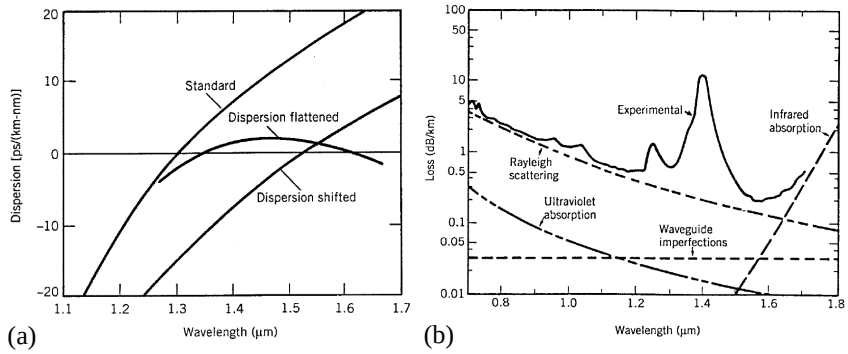

Figure 2.4: (a) Chromatic dispersion for SSMF, DSF and DFF. (b) Attenuation in SSMF. Both figures are from [4].

In most high-speed and long-reach systems, external modulation is preferred because of the higher-quality optical signal generation. Remark that for very short reach links up to a few 100 meters, 25 Gbaud PAM-4 links employ VCSELs. At these short reaches, VCSEL-based links still reign due to their very low cost [9]. A basic block diagram of an externally modulated optical transmitter is shown in Fig. 2.5. The optical source can be a DML biased at a constant current. While this a more complex and more expensive solution, the split between the laser and the modulator allow independent technology and operating optimizations. So the modulator can be integrated on a separate die or on the same die with the laser, resulting in an externally modulated laser (EML) [10, 11]. Monolithic integration of the modulator and the driver allows significant simplifications in the electrical interfacing between both [12, 13]. Or the driver and laser can be flipchipped onto a modulator IC to form one highly integrated assembly [14, 15].

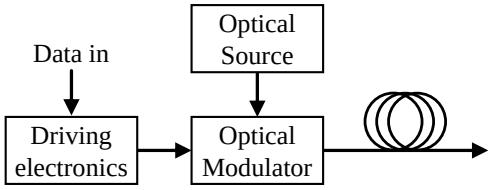

Figure 2.5: Block diagram of a external modulator and an optical source.

Compared to direct modulation, external modulators can have low-chirp or even zero-chirp properties [16–19]. Theoretically, a MZM introduces no chirp, but as proven in [17, 18], parasitic effects can cause some chirp. However, the MZM can be designed such that the chirp and dispersion have the same sign so

that the chirp improves the link performance at longer fiber reaches. In [16], the authors measure the chirp parameter of a germanium EAM, which has a magnitude less than 1. Due to the wavelength dependency, a zero-chirp or negative chirp can be chosen to improve the link performance at longer fiber reaches. The authors of [19] show how an MRM, which fundamentally introduces quite some chirp, can be engineered to improve the chirp and therefore improve the link performance.

While up until now we have focused on intensity modulation, certain external modulators or modulator architectures also allow control over the optical phase. This can be used, for example, to introduce phase modulation to counteract fiber dispersion [20]. But more importantly, it introduces an additional degree of freedom to increase the spectral efficiency of the optical link. As information can be coded on both the intensity as well as the phase of the optical carrier. This is clarified using Fig. 2.6. As can be seen, the non-return-to-zero (NRZ) format only contains 2 symbols corresponding to 2 different intensities, while PAM-4 contains four intensity levels. When also using the optical phase, the full complex plane becomes available. Here, only the 16QAM constellation is shown as an example. Since 16QAM contains 16 symbols, it packs 4 bits per symbol, double the amount of PAM-4. Depending on the link performance, more complex constellations are possible [21]. Such coherent constellations are typically used for long-reach links ($>$ 80 km) due to the higher implementation cost and more complex signal processing.

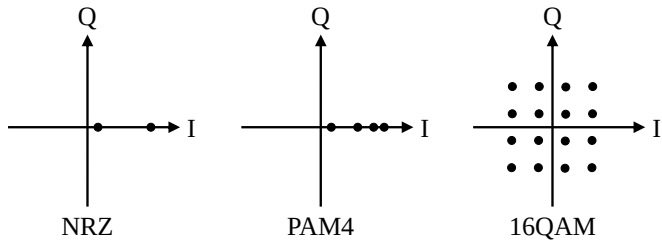

Figure 2.6: Symbol points of various modulation formats on the complex plane representing the magnitude and phase of the optical field.

External modulation provides system-level advantages too. Using a separate optical source allows to put the temperature sensitive laser away from the heat-dissipating electronics. And multiple optical modulators can be served from a single laser, given that the laser can provide sufficient power. Lastly, more complex modulator architectures and more functionality can be integrated on a single optical integrated circuit [13, 15, 22, 23].

2.3 Integrated Modulators

We will now shift our attention to integrated optical modulators. We distinguish two categories: phase modulators (PMs) and amplitude modulators (AMs). PMs rely on a change in effective index due to an applied electrical signal, causing the optical phase front to travel faster or slower trough the material, which results in a phase shift. AMs employs a signal dependent absorption to modulate the intensity of the optical wave passing through the modulator. Depending on the required constellation, both types can be used directly or incorporated in a larger transmit structure. The three most commonly encountered modulators are Mach-Zehnder modulators (MZMs), micro-ring modulators (MRMs) and electro-absorption modulators (EAMs). The first two consist out of PMs while the latter is based on intensity modulation. Next, we'll briefly discuss the three modulator types and highlight their advantages and disadvantages. Note that their availability also depends on the material platform that is used.

2.3.1 Mach-Zehnder modulators

The most common external modulator is the MZM, of which a typical implementation is shown in Fig. 2.7a. The versatility of this device is proven by it's common use in e.g. optical signal communication, optical switching, sensing ... The incoming light is split in two arms, one or both arms contain a phase modulator. Upon combination, the light in both arms interferes, resulting in phase and amplitude modulation. When driven correctly, only amplitude modulation is present at the output.

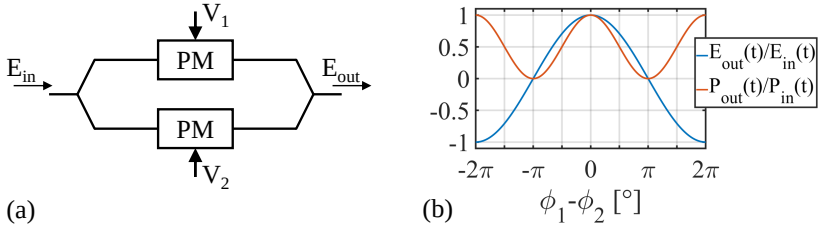

Figure 2.7: (a) a dual-arm Mach-Zehnder modulator and (b) the optical field and optical power response of the structure.

The phase modulators introduce a phase shift proportional to the applied voltage: $\phi \propto V_i$. As a first approximation, we assume that the PM does not introduce any additional insertion loss. The transfer function from the input of

the PM to the output is given by:

$$\frac{\mathrm{E_{PM,out}(t)}}{\mathrm{E_{PM,in}(t)}} = \exp\left(j\phi(t)\right) \tag{2.4}$$

Assuming that the splitters and combiners are perfect, i.e. they have no insertion loss and have a perfect 1/2 split ratio, the output field of this dual-arm MZM in Fig. 2.7(a) can be written as:

$$\begin{aligned}\frac{\mathrm{E_{out}(t)}}{\mathrm{E_{in}(t)}} &= \frac{1}{2}(\exp\left(j\phi_1(t)\right) + \exp\left(j\phi_2(t)\right)) \\ &= \exp\left(j\frac{\phi_1(t)+\phi_2(t)}{2}\right)\cos\left(\frac{\phi_1(t)-\phi_2(t)}{2}\right)\end{aligned} \tag{2.5}$$

Since power detection is used in an IM/DD link, it is also convenient to express the power transfer function:

$$\frac{\mathrm{P_{out}(t)}}{\mathrm{P_{in}(t)}} = \left|\frac{\mathrm{E_{out}(t)}}{\mathrm{E_{in}(t)}}\right|^2 = \frac{1}{2}(1+\cos\left(\phi_1(t)-\phi_2(t)\right)) \tag{2.6}$$

A graphical representation of both equations can also be found in Fig. 2.7(b). It can be observed from Eq. (2.5) that there is a phase-modulation term depending on $\phi_1(t) + \phi_2(t)$ and an amplitude modulation term depending on $\phi_1(t) - \phi_2(t)$. In order to avoid any chirp, the phase modulation term can be eliminated by driving the modulator such that $\phi_1(t) = -\phi_2(t)$, this is the so-called push-pull operation.

To analyse the response of the MZM, we can rewrite the phase difference $\phi_1(t) - \phi_2(t)$ to contain a AC and DC phase shift: $\phi_1(t) - \phi_2(t) = \phi_\mathrm{s}(t) + \phi_\mathrm{b}$. Where $\phi_\mathrm{s}(t)$ is the phase difference introduced by the AC component of the signal and ϕ_b is the fixed DC phase shift. Furthermore, since ϕ_1 and ϕ_2 are proportional to V_1 and V_2, we find that the driving voltage for a dual drive modulator is $\mathrm{V_s} = \mathrm{V}_1 - \mathrm{V}_2$.

In an IM/DD system, the MZM is biased in quadrature, that is $\phi_\mathrm{b} = \pi/2$, such that the power response is given by:

$$\frac{\mathrm{P_{out}(t)}}{\mathrm{P_{in}(t)}} = \frac{1}{2}(1-\sin\left(\phi_\mathrm{s}(t)\right)) \approx \left.\frac{1}{2}(1-\phi_\mathrm{s}(t))\right|_{\phi_\mathrm{s}(t)\ll 1} \tag{2.7}$$

Thus for sufficiently small signals, the output power swing is proportional to the induced phase shift and consequently to the applied voltage. The graphical representation of this biasing scheme is shown in Fig. 2.8(a). The power response is biased such that the optical output is half the optical input power and the electrical signal swing causes an optical power swing around this point. As

can be observed in the optical field response and the constellation diagram, the electric field does not change sign. Note that all quadrature points defined as $\phi_b = \pi/2 + i\pi$ with $i \in \mathbb{Z}$ yield the same response, expect for an inversion between even and odd i. For larger signal swings, compression will start to occur due to the sin-function. As can be observed in Eq. (2.7), there is an additional 3 dB insertion loss associated with quadrature biasing.

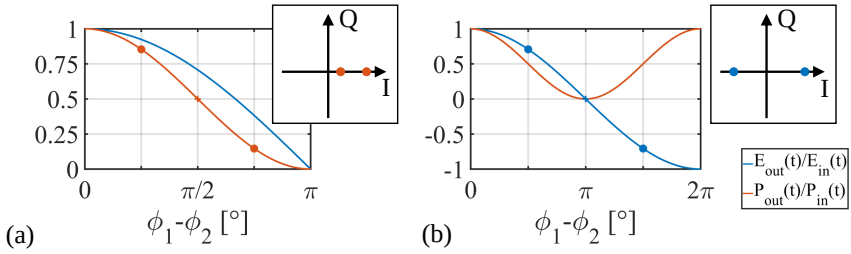

Figure 2.8: (a) MZM response at quadrature for IM/DD applications. (b) MZM response at minimum transmission for coherent applications.

In order to perform coherent modulation, full control over the electrical field is required. By biasing the modulator at the minimum transmission point, i.e. $\phi_b = \pi$, the amplitude and sign of the electrical field can be controlled, adjusting Eq. (2.5) yields:

$$\frac{E_{out}(t)}{E_{in}(t)} = -\sin\left(\phi_s(t)\right) \approx -\phi_s(t)|_{\phi_s(t)\ll 1} \tag{2.8}$$

If no signal is present, there is no optical signal at the output. This can also be observed in Fig. 2.8(b). An electrical signal swing causes the optical field to swing around the reference point and cover both the positive and negative I-axis. A second parallel MZM can be used in conjunction with a 90° phase-shift to cover the Q-axis and reach the full complex plane to recreate coherent constellations [21].

After this brief general description of the Mach-Zehnder operation, we can now consider the implementation. The phase modulators can be implemented in a wide variety of materials. Certain materials have a higher electro-optic effect, such that for the same voltage, a larger phase shift is introduced. A longer electro-optic interaction length, thus a longer phase shifter, will also introduce a larger phase shift. To this end, the voltage required for a π phase shift in a PM is used to characterize the efficiency of a phase shifter:

$$V_\pi = \frac{V_\pi L_\pi}{L} \tag{2.9}$$

With L the modulator length and $V_\pi L_\pi$ a technology dependent constant related to the material, composition and geometry of the phase shifter and the waveguides. The actual introduced phase shift is then given by:

$$\phi = \pi \frac{V}{V_\pi} \tag{2.10}$$

Historically, crystalline lithium niobate ($LiNbO_3$) was used to manufacture high-speed phase shifters [21]. The modulation efficiency varies depending on the crystallographic orientation and exact stackup, so the $V_\pi L_\pi$ is typically in the range of 8 to 12 V.cm [24]. As the importance of integration grew, III-V material systems like indium phosphide (InP) received more and more attention. The phase shifters can consist from a more simple PN junction design to complex multiple quantum wells (MQWs). The typical $V_\pi L_\pi$ is in the range of 0.3 to 0.6 V.cm [25–28] and decreases when a higher reverse bias voltage is applied to the junction or MQW [21]. Over the last years, silicon photonics has received tremendous attention since it offers low-loss, high-yield, high-volume production thanks to the compatibility with the complementary metal oxide semiconductor (CMOS)-platforms used for electronic chips [29]. The CMOS-compatibility also leads to an easier integration with (Bi)CMOS electronics. Silicon photonics allows for low-loss, compact structures as the large effective index between core (Si) and cladding (SiO_2) material features very good optical confinement. However, silicon has only limited electro-optic effects [30]. Therefore, the reverse biased PN junction based phase shifters have a higher $V_\pi L_\pi$ compared to other semiconductor material systems like III-V materials. The $V_\pi L_\pi$ is typically around 1.5 to 3.1 V.cm [13, 31–34]. In contrast to InP, the $V_\pi L_\pi$ in silicon increases with an increasing reverse bias voltage. More specialized implementations can reach up to 0.2 V.cm [35, 36], but at the cost of bandwidth, insertion loss and often also additional processing complexity.

Next to these 'pure' platforms, combinations are often used to boost specific performance metrics. For example, to boost the modulation efficiency while still being able to create compact, low-loss structures, III-V can be combined with silicon [37–39]. Lithium niobate has been integrated with silicon for a superior high speed performance [40, 41]. Even exotic polymers have been engineered to obtain a very strong electro-optic effect to obtain very efficient silicon-organic hybrids [42].

Of equal importance as the modulation efficiency is the loss introduced by the phase modulator. A very attractive feature for lithium niobate is the very low loss, depending on the exact dimensions, it can be as low as 0.2 dB/cm [21]. For InP, the loss are significantly higher: between 2.5 and 6 dB/cm [25–27]. Whether a junction-based design or an MQW is used, affects the losses. Furthermore, a higher reverse biasing voltage leads to higher attenuation in

InP. Losses in silicon vary between 5 and 20 dB/cm [13, 31–34]. Again, there is a very important dependence on the exact geometry, doping levels and on the biasing voltage. In silicon, the losses decrease with increasing reverse bias voltage. Interestingly, the more specialized, pure silicon modulators with a low $V_\pi L_\pi$ often have quite high losses, up to 65 dB/cm in [36]. The very high modulation efficiency fortunately allows to create very short modulators such that the losses remain manageable. In a modulator design, losses introduced by the routing of waveguides, splitters, combiners and fiber coupling should of course be taken into account.

Lastly, we consider the chirp of MZMs. As proven by Eq. (2.5), an ideal MZM can be chirp-free if driven correctly. In reality, deviations in the split ratio between both arms and asymmetric losses in the phase modulators can cause chirp [18]. Furthermore, indium phosphide and silicon phase modulators do exhibit some weak amplitude modulation [43], which also contributes to the chirp. We assumed earlier that the relationship between the introduced phase shift and voltage is linear, which is not the case for indium phosphide and silicon, while this relationship is linear in lithium niobate. This effect and the consequences on system-level performance were analyzed in [43]. It can be concluded that the chirp induced due to these effects is quite low. Such that typical chirp values are still much lower than those found in directly modulated transmitters.

MZMs offer very good performance in terms of bandwidth, modulation efficiency and loss. Their behavior shows limited wavelength dependency, and they can be easily made in both O- and C-band. Furthermore, they are well suited for IM/DD as well as coherent communication. However, to obtain a good modulation efficiency, quite large devices are required. Even when integrated on silicon, they can be several millimeter long. Such long devices start to show electrical traveling-wave effects [44]. This typically results in an increased power consumption as 50 Ω interfaces are required. However, later in this work, we will show that Mach-Zehnder based optical transmitters do have an important role to play in future datacenter interconnects due to their superior performance and coherent abilities.

2.3.2 Micro-ring modulators

A very compact and efficient amplitude modulator is the MRM, shown in Fig. 2.9. It consists of a waveguide ring in close proximity to a waveguide, such that a portion of the light can couple from the bus waveguide to the ring. Since light continuously couples into the ring, a resonance can occur if the light after a round trip in the ring constructively interferes with the light coupled into the ring. At this point, almost no power is present at the output waveguide.

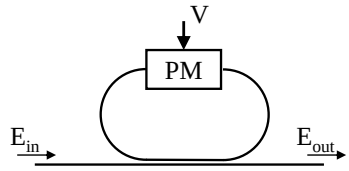

Figure 2.9: Micro-ring modulator with phase modulator inside the ring section.

An illustrative static response is given in Fig. 2.10, based on the models from [45]. It becomes clear that when the ring is resonating, in this case at λ_0, the output power is very low. Since the extinction is very good, a microring is perfectly suited for filtering in e.g. wavelength division multiplexing (WDM) systems.

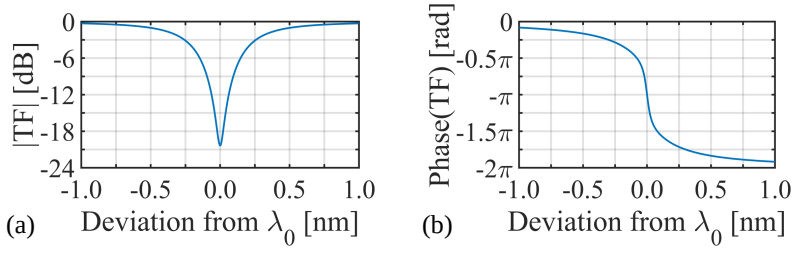

Figure 2.10: Illustrative intensity response (a) and phase response (b) of a microring.

The resonance wavelength is determined by the length of the ring, and is given by:

$$\lambda_0 = \frac{n_{\text{eff},\lambda 0} L}{i} \tag{2.11}$$

With $n_{\text{eff},\lambda 0}$ the effective index at the wavelength λ_0, L the physical ring length and $i \in \mathbb{N}_0$. Thus every time the effective ring length is a multiple of the wavelength, a resonance occurs. The difference in wavelength between two adjacent resonances is given by the free spectral range (FSR):

$$\text{FSR} = \frac{\lambda^2}{n_g L} \tag{2.12}$$

With n_g the group index of the waveguide. A sufficiently high distance is required between adjacent resonances, thus an FSR of more than 10 nm is not an exception. At 1550 nm and with a group index of 4, this results in a ring with a diameter of approximately 20 um. Such small waveguide bends with reasonable loss are only possible in materials with a very high index contrast

between the waveguide core and cladding, making silicon an ideal platform for ring resonators and modulators. The width and depth of the resonance are also determined by the losses in the ring and the coupling factor between the bus waveguide and the ring [45]. The full width at half maximum (FWHM) is linked to the Q-factor of the resonance as follows:

$$\mathrm{Q} = \frac{\lambda_0}{\mathrm{FWHM}} \tag{2.13}$$

To obtain a narrow resonance, a high Q-factor is required. A high Q-factor can be accomplished (in part) by minimizing the losses inside the ring. This again confirms the attractiveness of silicon photonics, as it provides low loss waveguides and low-losses at small bend radii.

The phase modulator in the ring can be used to adjust the resonance wavelength of the ring by changing the effective path length. This will result in amplitude modulation. An example of the static behavior when a phase shift is applied in the ring is shown in Fig. 2.11. Note that under modulation, a dynamic model is required as e.g. derived in [46, 47]. While this yields more accurate results, it significantly complicates the analysis. For the simple analysis here, a static model is already sufficient. Assuming our system is operating at a wavelength λ_0, shifting the resonance frequency causes amplitude modulation as shown by Fig. 2.11. It becomes clear that a high Q-factor is desirable: for the same shift in resonance wavelength, a much larger amplitude modulation can be obtained. However, this figure also highlights two important drawbacks of ring modulators: the intensity modulation is nonlinear and the phase of the optical field is also modulated. The nonlinear intensity modulation can be compensated, as shown by [14, 48]. Compensation can be done either directly in hardware, by adjusting the PAM-4 levels in the transmitter, or using digital signal processing (DSP). However, this comes at the cost of an increased complexity. The chirp of MRMs has been analyzed quite thoroughly [19, 47]. By optimizing the operating region of the MRM, the chirp can be minimized or negative chirp can be introduced such that the effect of dispersion is partially counteracted. While this is a good solution for IM/DD links, coherent links are very hard to implement using MRM.

Using a resonant device comes with certain advantages and disadvantages. An important advantage is that only a modest optical phase shift is required to obtain a considerable optical amplitude swing [49]. As small phase shifters can be used, the electrical load is relative easy to drive resulting in a very high bandwidth and low power consumption. Their wavelength selectivity also allows easy deployment in WDM systems [50]. At the downside, the device is also very sensitive to parasitic temperature variations and additional stabilization circuitry is required [14]. Locking the ring resonance to the operating

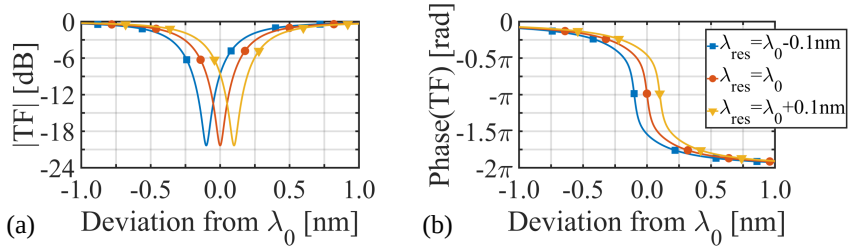

Figure 2.11: Illustrative intensity response (a) and phase response (b) of a microring.

wavelength, with or without a certain wavelength offset, is no easy feat. As a high Q-factor is required to obtain a narrow resonance and thus a high optical swing, the signal inside the ring is very strong. Which leads to additional non-linear effects in the waveguides that can alter the behavior of the MRM [51].

As explained before, since very small rings are required, and losses should be minimized, silicon photonics is an ideal candidate for ring modulators [14, 52]. Thanks to their very small size, they are ideally suited for monolithic integration with CMOS drivers [53]. A smaller footprint results in a much cheaper implementation together with electronics. To boost the optical swing, III-V on silicon and hybrid lithium niobate silicon platforms have been used for integrated ring modulators [41, 54].

2.3.3 Electro-absorption modulators

While previous modulators rely on phase modulation that gives rise to amplitude modulation, EAMs directly modulate the intensity of the optical carrier. Applying a voltage results in a change in the absorption spectrum, which gives rise to intensity modulation. Depending on the materials and buildup, the physical underlying effect can be the Franz-Keldish effect or the Quantum-Confined Stark Effect [21]. In both cases, an applied reverse bias voltage causes the absorption spectrum to shift towards longer wavelength, resulting in the transmission curves shown in Fig. 2.12. As can be observed, the response is nonlinear with applied voltage, thus compensation is required for higher-order modulation formats.

The electro-optical interaction length determines the modulation efficiency and the insertion loss. Most EAMs have an active region between 40 and 200 µm [55–57]. Making them very compact and ideal candidates for integration. Just as with MRMs, such a small device allows for a very high bandwidth and low power consumption. However, due to the change in absorption, there is also a change in the phase response, causing chirp. The introduced chirp

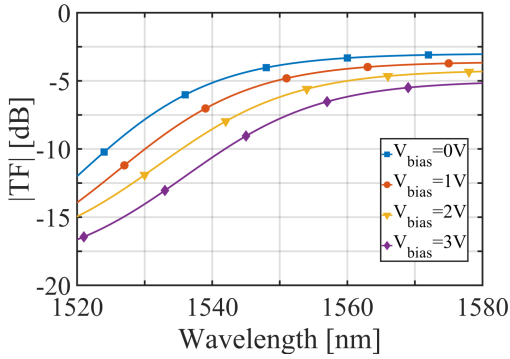

Figure 2.12: Illustrative static transmission curves for a C-band EAM at various biasing voltages.

is fortunately lower than caused in directly modulated systems [21]. Heavy optimization of III-V-based EAMs led to a decreased chirp factor and even to negative chirp [16, 58]. As also indicated in Fig. 2.12, the response varies over the C-band. Especially at the lower C-band, the insertion loss is much higher. While the response is not as sensitive to the operating wavelength as a MRM, it does impose some challenges in WDM systems. Apart from this dependency, since the absorption spectra are heavily material dependent, EAMs work in the O-band or the C-band. Switching from one band to the other requires different materials or a different composition.

As light is absorbed by EAMs, they act as a photodiode and generate a photocurrent. This is an important design consideration for the electronics: the driving electronics need to handle this photocurrent [59]. However it allows to use the same optical component both at the transmit and receive side [59].

Legacy electro-absorption modulators were integrated in III-V materials [21, 56, 58]. Later, interest in EAMs on silicon photonics grew. But as silicon does not exhibit the necessary physical effects for tunable absorption at telecom waveguides, new materials had to be introduced. First, pure germanium base modulators were integrated on silicon [55], germanium-silicon compounds were used later [57]. Since a new material is required, the pure CMOS-compatibility is (partially) lost, while MZMs and MRMs can be manufactured in a pure CMOS platform. However, germanium is not new in foundries for integrated electronic circuits: it's used in the high-performance BiCMOS platforms. While III-V based EAMs are demonstrated in both O-band and C-band, germanium-silicon EAMs operate only in the C-band.

2.4 Conclusion

In the previous sections, we outlined the advantages of external modulation and highlighted the most common integrated optical modulators: MZMs, MRMs and EAMs. The most popular platforms for integration were briefly discussed. While MZMs are larger and more power consuming, they offer superior signal quality, optical broadband operation, are easy to bias, are CMOS compatibile and are ideally suited for coherent communication. This make silicon Mach-Zehnder modulators a very attractive candidate for current and next generation datacenter interconnects. Due to their size and potentially high power consumption, very good co-design with the driving electronics is a crucial aspect in the design of a high-speed optical transmitter. This not only concerns the design of the phase shifter itself, but also the incorporation of the phase shifter in a traveling-wave structure, the electrode structure, biasing schemes ... As a result, it is also a very attractive field of research and part of this work. The following chapters will discuss the design of such high-speed traveling-wave silicon Mach-Zehnder modulators on imec's iSiPP50G silicon photonics platform [34].

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3

Traveling-wave Silicon Mach-Zehnder modulators

Silicon photonics is a key enabling technology for next generation datacenter interconnects. The outlook on closer integration and more complex modulation formats puts silicon Mach-Zehnder modulators (MZMs) in a pivotal position. Due to the limited electro-optic effect in silicon [1], phase modulators can easily measure several millimeters. At high-frequencies, where the device size is large compared to the wavelength of the electrical signal, traveling wave effects will occur [2]. To be able to provide high electro-optic bandwidths and a good modulation efficiency, the modulator electrodes should be designed with traveling-wave effects in mind while also paying attention to an optimal interfacing with the driving electronics. In this chapter, we will take a closer look to the modeling of silicon depletion phase shifters in the electrical domain and cover the analysis of traveling-wave modulators. Next, the design of a segmented traveling-wave modulator on imec's iSiPP50G platform will be discussed and verified using measurements [3].

3.1 Silicon depletion phase shifters

In silicon, most phase modulators rely on the plasma dispersion effect as it only requires doping of the waveguides. There are three different modes that can be used: carrier injection, carrier accumulation and carrier depletion. The latter

is most often used in high-speed phase shifters because of the superior bandwidth and ease of manufacturing [4, 5]. A cross section of the phase shifter in the iSiPP50G platform is shown in Fig. 3.1(a) [3]. A PN junction is formed inside a rib waveguide, the doping in the thin silicon slabs allows an electrical path from the outer contacts to the junction itself. The silicon is 220 nm thick while the silicon slabs are 60 nm thick. The buried oxide layer is 2 µm thick. By reverse biasing the PN junction ($V_S < 0$), a depletion layer is formed at the P-N transition. Applying a higher reverse bias increases the width of this region, resulting in a change in the effective index of the waveguide and consequently a phase shift. A simplified electrical circuit is Fig. 3.1(a) is shown in Fig. 3.1(b), the small-signal equivalent electrical circuit is given in Fig. 3.1(c). A general model would be that of a diode, but since the junction is reverse biased, we can use an RC series circuit as equivalent model. The reverse biased junction can be modeled as a capacitor, while the P and N doped region leading to the junction are modeled using resistors.

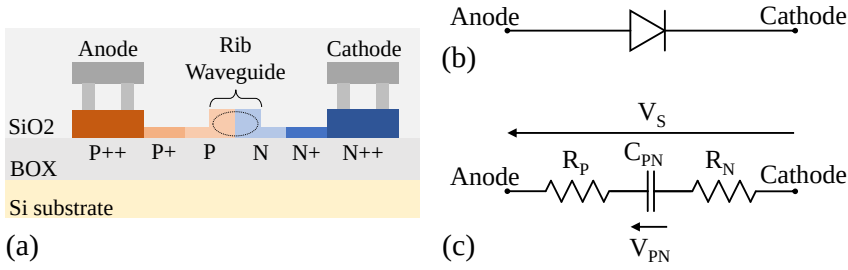

Figure 3.1: (a) Cross section of a PN-junction integrated in an optical rib waveguide. BOX: buried oxide layer, A: anode, C: cathode. (b) Equivalent electrical diagram of the cross-section. (c) Simplified small-signal electrical diagram of the reverse biased junction in (a).

The signal V_S is applied to the metal contacts, but the phase shift depends on the voltage V_{PN}. They relate to each other through the following transfer function:

$$V_{PN} = \frac{1}{1 + s(R_P + R_N)C_{PN}} V_S \tag{3.1}$$

As can be observed, a first order low-pass filter is obtained. To maximize the bandwidth of the modulator, the series resistance of the silicon slabs should be minimized. However, a higher doping close to the waveguide results in a higher insertion loss [6]. Decreasing the junction capacitance can be achieved using a lower doping, but at the cost of a worse modulation efficiency [7]. A second way to alter the junction capacitance is by adjusting the reverse bias voltage: a higher reverse bias voltage results in a wider depletion region and

a lower capacitance. But this also results in a degraded modulation efficiency and less insertion loss [7]. In this work, we are using the standard modulator of the iSiPP50G platform [3]. Thus doping optimization is not possible. We will also not optimize the dimensions of the waveguide and the doping, as this requires an in-depth analysis of the physics of the phase shifter. Instead, we will optimize the electrode structure and interfacing to the phase shifter to optimize the performance. The information available on the iSiPP50G phase shifter is summarized in Table 3.1

V_{bias} [V]	$V_\pi L_\pi$ [V.cm]	IL [dB/cm]	C_{PN} [fF/ µm]
0	1.4	15	0.42
-2	-	-	0.32

Table 3.1: Details on the Si depletion phase shifter at 1550 nm

As could be expected, the depletion capacitance drops with increasing reverse bias. The $V_\pi L_\pi$ and insertion loss are only given at a bias of 0 V. For a higher reverse bias voltage, the $V_\pi L_\pi$ will increase and the insertion loss will decrease.

While this information is sufficient for a low-speed phase shifter design, it is not detailed enough for a traveling wave modulator. A good electrical equivalent network is required to calculate the effect of the PN junction on the traveling wave electrodes. This not only includes the RC-series equivalent, but also the parasitic effects up to high frequencies. A small-signal equivalent circuit containing the substrate parasitics and parasitic capacitances is given in Fig. 3.2.

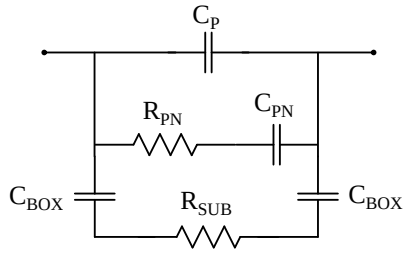

Figure 3.2: Improved equivalent small signal electrical circuit of the PN junction in Fig. 3.1(a).

In this circuit, C_{PN} resembles the depletion capacitance and R_{PN} is the resistance of the contacting up to the depletion layer. These are equivalent to the RC circuit in Fig. 3.1(a). The parasitic capacitances between the P- and N-doped silicon slabs, the contacts and the metal are summarized in C_P. The

substrate, which has a low resistivity, is modeled using R_{SUB}, while C_{BOX} is the capacitance formed between the doped silicon through the buried oxide to the silicon substrate.

To obtain the values of the various elements, one can measure the impedance of the phase shifter and fit the measurements on the equivalent circuit. As these devices were not available, Keysight's ADS Momentum® was used to perform electromagnetic simulations on the phase shifter. The results were fitted on the equivalent circuit to obtain all values. However, Momentum does not support full simulation of PN-junctions. The doped silicon parts can be replaced by conductors with the appropriate conductances as defined in the process development kit (PDK) documentation. In order to model the depletion region, a gap between the N- and P-doped regions filled with the surrounding material (SiO_2) can be used, as shown in Fig. 3.3. Since the gap width w is typically much smaller than the silicon thickness t, it acts as a parallel plate capacitor. Note that the depletion capacitance is typically calculated using a parallel-plate approximation.

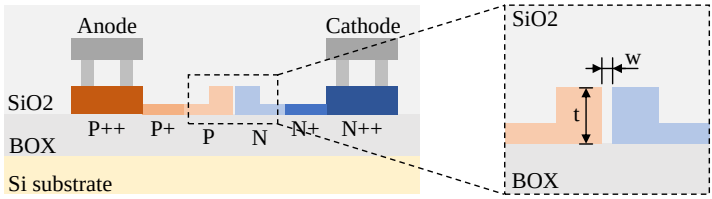

Figure 3.3: Cross section of the phase shifter used for simulation. The depletion layer is modeled as a SiO_2-gap of width w between the doped regions.

The gap width should be selected to correspond with the junction capacitance provided in the PDK, see Table 3.1. The layout of the standard phase shifter was transferred to Momentum and simulated for various gap widths. The total capacitance (including parasitics) was extracted at 100 kHz and is plotted in Fig. 3.4. In this case, a gap of 40 nm and 70 nm corresponds with a capacitance of 0.43 and 0.33 fF/ µm, respectively the capacitances stated by the documentation at a reverse bias of 0 and 2 V respectively.

In the next step, the cross section of the standard phase shifter was simulated up to 50 GHz. The simulations were done with a gap of 40 and 70 nm and the phase shifters themselves were 100, 200 and 300 µm long. These various lengths were chosen to obtain reliable results and isolate parameters that only depend on the device length. Each time, the circuit from Fig. 3.2 was fitted onto the simulated impedance. In order to remove the length dependence, the parameters were converted to per unit length parameters. The results can be found in Table 3.2. The maximal error between the simulation and the equiv-

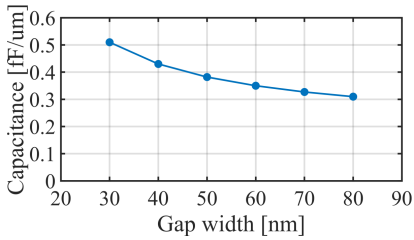

Figure 3.4: Total capacitance at 100 kHz as a function of gap width.

alent circuit was 3.1% and 0.8% (both for the 300 µm long device) on the resistance and capacitance directly extracted from the total impedance.

	w=40 nm	w=70 nm	
C_{PN}	0.283	0.182	[fF/ µm]
R_{PN}	9.720	9.370	[kΩ. µm]
C_P	0.117	0.115	[fF/ µm]
C_{BOX}	55.3	54.9	[aF/ µm]
R_{SUB}	1.006	1.027	[MΩ. µm]

Table 3.2: Component values for the standard phase shifter

Note that a similar procedure can be used if the phase shifter design is adjusted. As long as the waveguide and corresponding doping is not adjusted, the optical parameters will remain the same. The highly doped contacting slabs and metals can be redesigned to optimize the performance in the traveling-wave design.

3.2 Traveling wave modulators

In order to obtain a reasonable V_π, silicon depletion phase modulators are easily several millimeters long. For example, to obtain a reasonable V_π of 4 V using the standard iSiPP50G phase shifter (Table 3.1), the modulator should be 3.5 mm long. At high frequencies, this is a considerable fraction of the wavelength. Fore example at 30 GHz, the wavelength in vacuum is only 10 mm. Thus a proper design, taking care of traveling wave effects, is of utmost importance. An example layout of a traveling wave phase shifter is shown in Fig. 3.5. A transmission line is formed with the reverse biased PN junction in between. At every point on the modulator, the electrical signal modulates the local refractive index, which gives rise to a local phase shift. As the electrical

and optical signal are traveling in the same direction, the optical signal accumulates all local phase shifts. Such traveling-wave designs were pioneered in lithium niobate [8] in the late 70's, and found their application in high speed integrated modulators since then in various material systems including silicon [6, 9–16]. Many variations exists on the basic structure to improve certain performance metrics like modulation efficiency, area and others. We will first cover the analysis of the standard traveling-wave modulator.

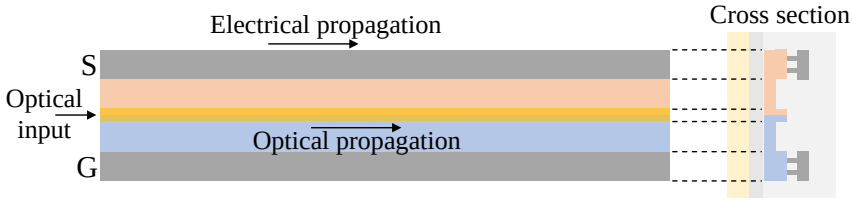

Figure 3.5: Basic layout of a traveling-wave phase-shifter. At the left side, the electrical and optical signals are launched into the phase shifter. At the right side, the electrical signal is terminated (not shown) on- or off-chip.

3.2.1 Derivation of the electro-optical response

The analysis can be split into 2 parts: the electrical part that results in the voltages that give rise to a phase shift and the electro-optical part that converts this voltages to actual phase shifts. To determine the voltages over the depletion layer, we can extend the RLCG model of the transmission line [2] to include the equivalent circuit of a reverse biased PN junction, see Fig. 3.6. Here, $\mathrm{R_U}$, $\mathrm{L_U}$, $\mathrm{C_U}$ and $\mathrm{G_U}$ are the RLCG parameters of the unloaded transmission line, while $\mathrm{R_{PN}}$, $\mathrm{C_{PN}}$ comprise the reverse biased PN junction.

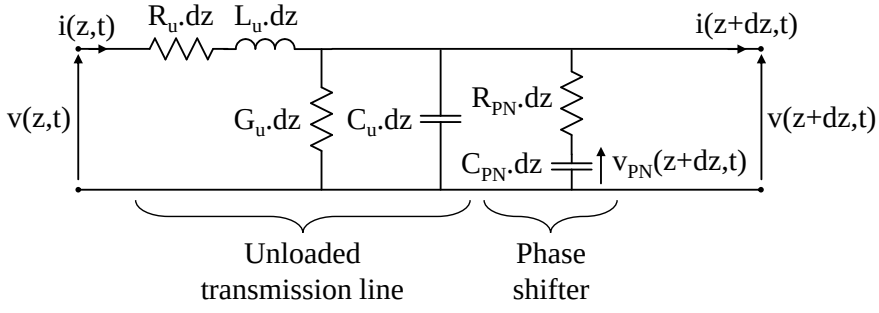

Figure 3.6: RLCG model of the unloaded transmission line extended with the small-signal circuit model of a reverse biased PN-junction.

This method has been proven by [14, 15] and others to yield very good results, under the condition that there is a quasi-transverse electro-magnetic wave propagation and that the loading of the PN junction does not alter the series resistance and inductance. The first condition was verified by [15], while the second condition is true as long as the current flowing in the doped areas along the propagation direction is negligble. By absorbing the phase shifter impedance in the conductance and capacitance, a conventional RLCG model is obtained again. Note that the RLCG-parameters are frequency-dependent and that the simplified RC-series circuit for the PN junction can be replaced by a more accurate circuit.

From the RLCG parameters, the characteristic impedance and propagation factor can be obtained. This way, we can predict how the PN-junction affects the loaded transmission line parameters. The unloaded transmission line parameters are given below [2]:

$$\begin{aligned} \mathrm{Z_{cu}} &= \sqrt{\frac{\mathrm{R_u} + \mathrm{j}\omega\mathrm{L_u}}{\mathrm{G_u} + \mathrm{j}\omega\mathrm{C_u}}} \\ \gamma_\mathrm{u} &= \alpha_\mathrm{u} + j\beta_\mathrm{u} = \sqrt{(\mathrm{R_u} + \mathrm{j}\omega\mathrm{L_u})(\mathrm{G_u} + \mathrm{j}\omega\mathrm{C_u})} \end{aligned} \tag{3.2}$$

Which under low-loss conditions ($\mathrm{R_u} \ll \omega\mathrm{L_u}$ and $\mathrm{G_u} \ll \omega\mathrm{C_u}$), can be simplified to the following expressions:

$$\begin{aligned} \mathrm{Z_{cu}} &\approx \sqrt{\frac{\mathrm{L_u}}{\mathrm{C_u}}} \\ \gamma_\mathrm{u} = \alpha_\mathrm{u} + j\beta_\mathrm{u} &\approx \frac{1}{2}\left(\frac{\mathrm{R_u}}{\mathrm{Z_{cu}}} + \mathrm{G_u Z_{cu}}\right) + j\omega\sqrt{\mathrm{L_u C_u}} \end{aligned} \tag{3.3}$$

So the losses α_u can be split in the conductor losses ($\propto \mathrm{R_u}$) and dielectric losses ($\propto \mathrm{G_u}$). From the propagation factor, we can obtain the phase velocity and the phase index of the propagating wave since the phase velocity is given by $\mathrm{v_p} = {}^{\omega}/_{\beta_\mathrm{u}}$:

$$\mathrm{n_u} = \frac{\mathrm{c}}{\mathrm{v_p}} = \mathrm{c}\sqrt{\mathrm{L_u C_u}} \tag{3.4}$$

In order to absorb the RC-series equivalent circuit of the phase shifter into the RLCG parameters, we first need to convert it to a RC-parallel equivalent

circuit:

$$\begin{aligned} \mathrm{R_{p,pn}} &= \mathrm{R_{pn}}\left(1+\frac{1}{(\omega \mathrm{R_{pn}C_{pn}})^2}\right) \\ \mathrm{C_{p,pn}} &= \mathrm{C_{pn}}\left(\frac{1}{1+(\omega \mathrm{R_{pn}C_{pn}})^2}\right) \end{aligned} \tag{3.5}$$

By inverting $\mathrm{R_{p,PN}}$, the conductance $\mathrm{G_{p,PN}}$ is obtained. The conductance and capacitance in the loaded RLCG model are then given by: $\mathrm{G_l} = \mathrm{G_u} + \mathrm{G_{p,PN}}$ and $\mathrm{C_l} = \mathrm{C_u} + \mathrm{C_{p,PN}}$. Which leads to the following loaded transmission line parameters:

$$\begin{aligned} \mathrm{Z_{cl}} &= \sqrt{\frac{\mathrm{R_u} + \mathrm{j}\omega \mathrm{L_u}}{\mathrm{G_l} + \mathrm{j}\omega \mathrm{C_l}}} \\ \gamma_\mathrm{l} &= \alpha_\mathrm{u} + j\beta_\mathrm{u} = \sqrt{(\mathrm{R_u} + \mathrm{j}\omega \mathrm{L_u})(\mathrm{G_l} + \mathrm{j}\omega \mathrm{C_l})} \end{aligned} \tag{3.6}$$

Again under low-loss conditions ($\mathrm{R_u} \ll \mathrm{j}\omega \mathrm{L_u}$ and $\mathrm{G_l} \ll \mathrm{j}\omega \mathrm{C_l}$), this can be simplified to the expression below. We have substituted the original expressions for $\mathrm{G_l}$ and $\mathrm{C_l}$:

$$\begin{aligned} \mathrm{Z_{cl}} &\approx \sqrt{\frac{\mathrm{L_u}}{\mathrm{C_u} + \mathrm{C_{p,PN}}}} \\ \gamma_\mathrm{l} = \alpha_\mathrm{l} + j\beta_\mathrm{l} &\approx \frac{1}{2}\left(\frac{\mathrm{R_u}}{\mathrm{Z_{cl}}} + (\mathrm{G_u} + \mathrm{G_{p,PN}})\mathrm{Z_{cl}}\right) + j\omega\sqrt{\mathrm{L_u}(\mathrm{C_u} + \mathrm{C_{p,PN}})} \\ \mathrm{n_u} &\approx \mathrm{c}\sqrt{\mathrm{L_u}(\mathrm{C_u} + \mathrm{C_{p,PN}})} \end{aligned} \tag{3.7}$$

As can be observed, the addition of capacitance and conductance from the phase shifter yields a decrease in characteristic impedance, an increase in the transmission line loss and an increase in the phase index. As the added capacitance can be quite significant, the change in parameters can be quite drastic, this will become clear later. In the design phase, various unloaded transmission line configurations can be simulated using, e.g. Keysight ADS Momentum®. The RLCG parameters can be extracted from the simulated S-parameters.

Using this model, we are now able to calculate the voltage giving rise to a phaseshift over the full modulator. A methodical approach towards an analytical solution is provided by [9]. Using the transmission line model, the voltage at each location on the transmission line electrodes can be calculated, given a certain termination impedance and source impedance. An electrical

diagram of the loaded transmission line is provided in Fig. 3.7. For illustrative purposes, the phase shifters are drawn here as distributed RC-series chains.

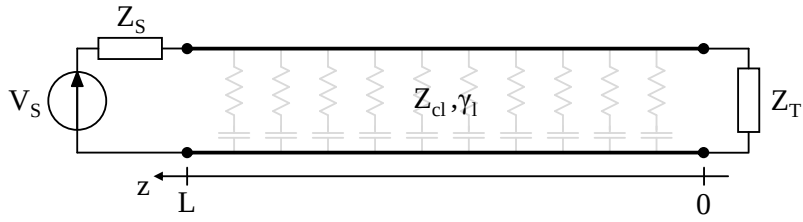

Figure 3.7: Loaded transmission line driven by a source with impedance $\mathrm{Z_S}$ and terminated with $\mathrm{Z_T}$. Both optical and electrical wave are assumed to be propagating in the negative z-direction.

The resulting voltage can now be calculated at each point and each frequency (the frequency variable is dropped to improve readability):

$$\mathrm{V(z)} = \mathrm{V_S}\frac{1+\mathrm{K_1}}{2}\frac{\exp\left(\gamma_\mathrm{l}\mathrm{z}\right)+\mathrm{K_2}\exp\left(-\gamma_\mathrm{l}\mathrm{z}\right)}{\exp\left(\gamma_\mathrm{l}\mathrm{L}\right)+\mathrm{K_1K_2}\exp\left(-\gamma_\mathrm{l}\mathrm{L}\right)} \tag{3.8}$$

Where $\mathrm{K_1}$ and $\mathrm{K_2}$ are the reflection coefficient at the input and termination of our transmission line respectively:

$$\mathrm{K_1} = \frac{\mathrm{Z_{cl}}-\mathrm{Z_S}}{\mathrm{Z_{cl}}+\mathrm{Z_S}} \text{ and } \mathrm{K_2} = \frac{\mathrm{Z_T}-\mathrm{Z_{cl}}}{\mathrm{Z_T}+\mathrm{Z_{cl}}} \tag{3.9}$$

Now, the voltage over the depletion capacitor can be calculated using the appropriate transfer function and the voltage from Eq. (3.8). As the equivalent phase-shifter network contains per-unit-length parameters (see sec. 3.1), the length-dependence can be omitted and all components can be combined as if they are a normal circuit, so we obtain:

$$\mathrm{V_{PS}(z)} = \mathrm{V(z).TF_{PS}} \tag{3.10}$$

Where $\mathrm{TF_{PS}}$ depends on the equivalent phase shifter circuit. While this expression yields the phase shift that is introduced at a specific location, we need to be able to combine all these phase shifts together. As a reference location to add all phase shifts, we choose the end of the phase shifter at $z = 0$. Thus the phase shift induced by the voltage $\mathrm{V_{PS}}$ at location z has to travel over a distance z through the optical waveguides to our reference point. This induces an additional delay $\beta_\mathrm{o}\mathrm{z}$, with $\beta_\mathrm{o} = {}^{\omega_\mathrm{m}}/_{\mathrm{c.n_o}}$. Where ω_m is the pulsation of the modulating signal and $\mathrm{n_o}$ is the group index of the optical waveguide. Applying this delay to $\mathrm{V_{PS}(z)}$ by multiplying with $\exp\left(\beta_\mathrm{o}\mathrm{z}\right)$ and integrating over

the full modulator length, yields the average voltage that gives rise to a phase shift:

$$\begin{aligned} \mathrm{V_{avg}} &= \frac{1+\mathrm{K_1}}{2}\mathrm{V_S}\frac{\exp\left(\mathrm{j}\beta_\mathrm{o}\mathrm{L}\right)\mathrm{TF_{PS}}}{\exp\left(\gamma_\mathrm{l}\mathrm{L}\right)+\mathrm{K_1K_2}\exp\left(-\gamma_\mathrm{l}\mathrm{L}\right)}\left(\theta_\mathrm{p}+\mathrm{K_2}\theta_\mathrm{m}\right) \\ \theta_\mathrm{p} &= \exp\left(\frac{(\gamma_\mathrm{l}-j\beta_\mathrm{o})L}{2}\right)\frac{\sinh\left(\frac{(\gamma_\mathrm{l}-j\beta_\mathrm{o})L}{2}\right)}{\frac{(\gamma_\mathrm{l}-j\beta_\mathrm{o})L}{2}} \\ \theta_\mathrm{m} &= \exp\left(-\frac{(\gamma_\mathrm{l}+j\beta_\mathrm{o})L}{2}\right)\frac{\sinh\left(-\frac{(\gamma_\mathrm{l}+j\beta_\mathrm{o})L}{2}\right)}{-\frac{(\gamma_\mathrm{l}+j\beta_\mathrm{o})L}{2}} \end{aligned} \tag{3.11}$$

The voltage $\mathrm{V_{avg}}$ can now directly be used to calculate the phase shift over the full frequency range. As this quite elaborate expression is unwieldy to work with, we derive the performance tradeoffs using well-chosen simplifications.

3.2.2 Performance tradeoffs in traveling-wave modulators

There are three important performance tradeoffs in the design, we will cover all of them using the previous analysis. These serve as the basis for almost any traveling-wave modulator design:

- Matching the characteristic impedance to the source and load impedance;
- Minimizing the electrical attenuation;
- Matching the velocities of the electrical and optical waves.

The characteristic impedance impacts $\mathrm{V_{avg}}$ through the parameter $\mathrm{K_1}$ and $\mathrm{K_2}$. When the characteristic impedance is too low, the voltage at the input terminals of the modulator will be lower, resulting in less optical swing. To illustrate this effect, Eq. (3.11) is evaluated in various configurations. The source impedance is kept fixed at 50 Ω, while the characteristic impedance and termination impedance were varied. The electrical and optical wave are assumed to be velocity matched (the electrical phase index and optical group index are both 4), the electrical attenuation is simplified to a linear loss model with 0.1 dB/mm.GHz attenuation. The transmission line is 3 mm long, the RC-effect of the phase shifters were omitted for simplicity. As can be observed in Fig. 3.8, for a perfectly matched transmission line with $\mathrm{Z_{cl}}$ and $\mathrm{Z_T}$ equal to 50 Ω, there is 6 dB loss due to the 50 Ω interfacing. If the characteristic impedance drops to 30 Ω, and $\mathrm{Z_T}$ drops accordingly to keep a good match, the loss increases to 8.5 dB. A $\mathrm{Z_{cl}}$ higher than $\mathrm{Z_S}$ might be a solution to obtain additional swing, but a higher voltage swing could cause breakdown in the

driver. Furthermore, due to the loading of the PN-junction, obtaining a high characteristic impedance is very difficult [6, 16, 17]. The interface between the driving electronics and the modulator can have a major influence: if an interconnecting transmission line is present, a mismatched modulator impedance will cause variations in the impedance seen by the driver. Consequently, the fluctuations in driving voltage can heavily affect the driver performance.

By matching the termination impedance to the characteristic impedance, any reflections on the modulator are suppressed, since K_2 is zero. So there is only a co-propagating electrical wave present. If there is a mismatched termination, a counterpropagating wave exists on the modulator which affects the frequency response. Interestingly, if the termination impedance is lower than the characteristic impedance, the mismatch causes an increase in bandwidth [15]. This effect is demonstrated in Fig. 3.8, where a significant increase in 3 dB bandwidth is observed. The low termination impedance causes a drop in modulation efficiency at low frequency, causing the higher bandwidth. Thus there is a tradeoff between modulation efficiency and bandwidth. This is a popular equalization technique to enhance the bandwidth, but causes variations in the modulator input impedance, which can cause a performance deterioration in the driving electronics. Similarly, a higher termination impedance yields a higher DC modulation efficiency at the cost of less bandwidth.

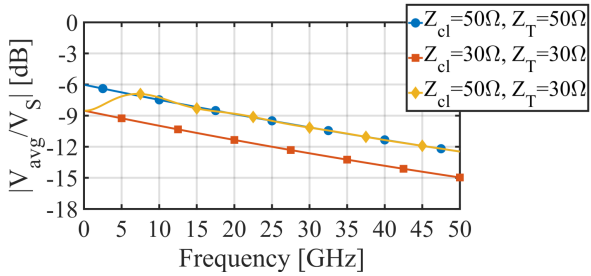

Figure 3.8: Effect on V_{avg} of the mismatch between the source impedance and transmission line and mismatch between the transmission line and termination. The source impedance is 50 Ω in all cases.

Minimizing the electrical attenuation, especially at high frequencies, is key to a high-speed modulator. This directly follows from Eq. (3.11), assuming a perfect matching on all interfaces ($K_1 = K_2 = 0$) and assuming the velocities of the electrical and optical wave are matched ($\beta_l = \beta_o$), we obtain:

$$V_{avg} = \frac{V_S}{2} \frac{1}{\alpha_l L} \left(1 - \exp\left(-\alpha_l L\right)\right) \tag{3.12}$$

Thus the 3 dB bandwidth highly depends on the product $\alpha_l L$. Higher attenua-

tion or a longer modulator translates into less bandwidth. As a long modulator is required for a high modulation efficiency, a tradeoff between bandwidth and modulation efficiency is established. Using our highly simplified model, the bandwidth-length curve of Fig. 3.9 is obtained. A high bandwidth can only be obtained with a short modulator, at the cost of modulation efficiency.

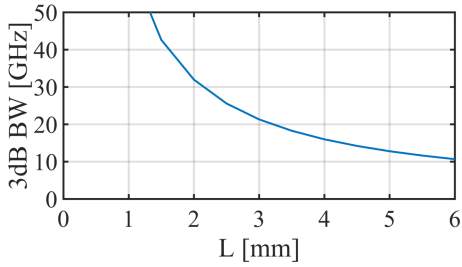

Figure 3.9: Bandwidth as a function of modulator length using a simplified linear loss model.

The attenuation on the transmission line is determined in Eq. (3.7). We can split the expression in a part related to the transmission line electrodes and a part related to the PN junction loading:

$$\alpha_{\mathrm{l}} = \underbrace{\frac{1}{2}\frac{\mathrm{R_u}}{\mathrm{Z_{cl}}}}_{\alpha_{\mathrm{l,e}}} + \underbrace{\frac{1}{2}(\mathrm{G_u} + \mathrm{G_{p,PN}})\mathrm{Z_{cl}}}_{\alpha_{\mathrm{l,pn}}} \tag{3.13}$$

The first part $\alpha_{\mathrm{l,e}}$ is related to the series resistance of the electrodes. Due to the skin-effect, the series resistance is proportional to the square root of the frequency [2, 14]. The second term depends mostly on the transmission line loading since the $\mathrm{G_u}$ term is relative small compared to $\mathrm{G_{p,PN}}$. As can be observed by Eq. (3.5), $\mathrm{R_{p,PN}}$ is inversely proportional to f^2 if the frequency is sufficiently below the RC cutoff. Consequently, $\mathrm{G_{p,PN}}$ is proportional to f^2. Note that for very high speed modulators, where the bandwidth is close to the RC cutoff frequency of the phase shifter, the frequency dependency changes again. As such, our linearized loss model is only a crude approximation, but given the complexity, it still provides insightful results. As the PN junction is the major contributor, we can decrease the loss by decreasing the PN junction resistance or capacitance. As explained section 3.1, decreasing the resistances requires doping closer to the waveguide, resulting in a higher optical insertion loss. While decreasing the capacitance requires lower doping and thus a penalty on the modulation efficiency.

Quite some solutions have been explored to minimize this loss. Decreasing the loss through optimization of the doping profile or complex doping pro-

files [5, 7], typically comes at the cost of modulation efficiency and more complex processing. Furthermore, commercial processes often don't allow such techniques. In [18], the substrate under the electrode is etched away, yielding less dielectric loss and as such an increase in bandwidth. But this is a quite complex additional processing step, which is again not supported by most commercial processes. Instead of loading the transmission line continuously with the phase shifter, slow-wave modulators only periodically load the transmission line. This gives an extra degree of freedom to control the transmission line parameters, at the cost of a slightly longer modulator [6, 14, 19, 20]. This technique has been proven quite successful and is used in most very-high speed designs. Next to these slow-wave modulators, a very effective technique is to place two phase shifters in series between two electrodes [14, 16]. As two phase shifters are required for an MZM, they can be directly integrated together. A cross section of such an series push-pull (SPP) architecture is shown in Fig. 3.10.

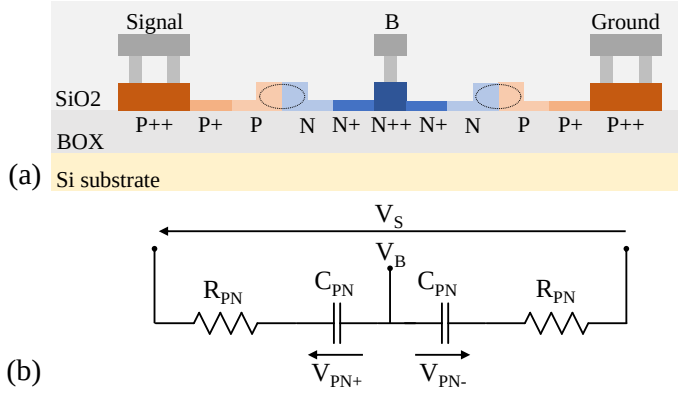

Figure 3.10: (a) Cross section of a SPP phase shifter with a center biasing line. (b) Equivalent electrical circuit with the signal and bias voltage V_S and V_B.

As both PN junctions are now placed in series between the transmission line electrodes, the total resistance doubles while the total capacitance halves. Using Eq. (3.7) and Eq. (3.5), we can observe that this leads to a higher characteristic impedance, a lower electrical phase index and less losses.

Using Fig. 3.10(b), we can derive the voltage over the PN junctions. Note that the voltages are defined such that a negative V_{PN} is required for a reverse bias. We assume that the signal voltage V_S has no DC-component and the bias connection has a high-impedance and therefore does not carry AC-signals. We then obtain $V_{PN+} = {}^{V_S}/_2 - V_B$ and $V_{PN-} = -{}^{V_S}/_2 - V_B$. Consequently, both arms induce an opposite phaseshift, such that a dual-arm push-pull MZM

can be formed, see section 2.3.1. Additionally, the separate line to bias the PN junctions means that the driving electronics don't have to bias the junctions. So the high-speed driver can be independently optimized [21].

A third parameter to consider is the velocity mismatch between the electrical and optical waves. If the phase index of the electrical wave and the group index of the optical wave are matched, a maximal phase shift can build up. Consider a point on the optical wave traveling through the modulator: when the optical and electrical wave are traveling at the same velocity, from our point we'll see the same amplitude throughout the modulator. Thus a peak in the electrical wave will be fully transfered to the optical domain. If the optical and electrical wave are traveling at different speeds, we will see a varying amplitude. This will result in a lower average phase shift induced on the modulator. At higher frequencies, where the wavelengths are much shorter, the average phase shift will drop faster. Thus velocity matching is crucial for the high-speed operation of a traveling-wave modulator. The analytical solution for V_{avg} in Eq. (3.11) takes this into account through the terms $\gamma_l - j\beta_o$ and $\gamma_l + j\beta_o$. Simulations with the same model used earlier, but with varying phase index and group index for the electrical and optical waves respectively are shown in Fig. 3.11. In this simplified simulation, we adjusted the optical group index from 4 to 1. This latter value is chosen as an extreme case. As can be observed, a significant drop in bandwidth is observed.

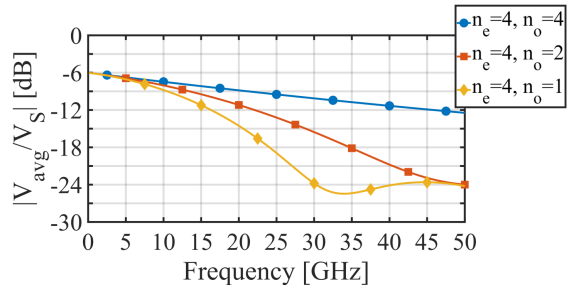

Figure 3.11: Effect of velocity mismatch on high-speed behavior of V_{avg}.

For a modulator with perfectly matched source & termination impedances, with negligible losses and neglecting the RC-effect of the phase shifter, the 3-dB bandwidth can be calculated as follows [22]:

$$f_{vm} = \frac{1.39c}{\pi \left| n_e - n_o \right| L} \tag{3.14}$$

While quite some assumptions are made, this equation still provides a straightforward way to verify if velocity mismatch might be a limiting factor for the

device bandwidth. As could be expected, a larger difference between the phase and group index and a longer device, both result in a lower bandwidth. As silicon phase shifters are relative short, in the orders of several millimeters, they typically do not suffer from bandwidth deterioration due to velocity mismatch. For example, a 3 mm long modulator with a group index of 4 can have a electrical phase index between 3.12 and 4.88 before the bandwidth according to Eq. (3.14) drops below 50 GHz. In most cases, obtaining a sufficiently good velocity match is straightforward.

In certain cases, due to the capacitive loading on the electrodes, the electrical wave is actually traveling too slow. Periodically loading the electrodes with phase shifters provides an elegant solution to this problem [14, 19, 20] as the effective capacitive load per unit length drops. Furthermore, it also provides a bandwidth enhancement due to the lower losses (see previous part). If that extra degree of freedom is still not sufficient, delay lines can be inserted in the phase shifter to slow down the optical wave [6].

3.3 Design of a traveling-wave modulator

Using the various performance tradeoffs from the previous section, we can apply these concepts to an optimized traveling-wave modulator design. The modulator is designed on imec's iSiPP50G platform [3].

3.3.1 Architecture

The architecture for the traveling-wave modulator is shown in Fig. 3.12. A differential electrode structure is used in order to combine the modulator with a differential driver. This results in advantages in driving voltage, bandwidth, linearity and inter-device crosstalk [23]. The PN-phase shifters are arranged in an SPP configuration between both signal lines. Placing the diodes of the upper and lower arm between the upper and lower ground-signal line pair would, electrically speaking, be the same for the differential mode. The DC-voltage for reverse biasing the diodes should be applied between the ground and signal line. Since this bias voltage is also applied over the terminations, a quite substantial current can flow. This results in a limited bias voltage, as the electrodes and termination resistor can only handle a limited current, but also causes a worse power efficiency of the complete transmitter. Furthermore, the electrical driver has to be able to deliver the relative high bias voltage and accompanying current. This interferes with the DC-configuration of the driver leading to a less optimal electrical driver. Therefore, by using the SPP circuit, a separate biasing line is used such that the high-speed driver-operation is isolated from the modulator biasing.

Instead of employing one long phase shifter, we have two traveling-wave segments. The advantage in this approach is that the microwave losses can be limited, resulting in a higher bandwidth per segment, see section 3.2.2 and [24]. At the same time, a 2-bit digital-to-analog converter (DAC) functionality is obtained. So two binary signals can be applied to the segments in order to generate a PAM-4 signal. As such, a power-hungry linear driver supporting PAM-4 can be avoided and two non-linear drivers can be used [21]. The optical power response of such a system becomes:

$$\frac{\mathrm{P_{out}(t)}}{\mathrm{P_{in}(t)}} = \frac{1}{2}\left(1 - \cos\left(\frac{\pi \mathrm{V_{MSB}}}{\mathrm{V_{\pi,MSB}}} + \frac{\pi \mathrm{V_{LSB}}}{\mathrm{V_{\pi,LSB}}} + \phi_{\mathrm{bias}}\right)\right) \tag{3.15}$$

With $\mathrm{V_{\pi,MSB}}$ and $\mathrm{V_{\pi,LSB}}$ the $\mathrm{V_\pi}$ of the longest (most significant bit (MSB)) and shortest (least significant bit (LSB)) segments. Their respective driving voltages are $\mathrm{V_{MSB}}$ and $\mathrm{V_{LSB}}$. The bias of the modulator is incorporated in the term ϕ_{bias}. Assuming we use the same driving voltage for both segments, then $\mathrm{V_{\pi,LSB}}$ should be twice as high as $\mathrm{V_{\pi,MSB}}$ to obtain a 2-bit DAC in the optical power domain. Thus the LSB segment should be half the length of the MSB segment, as shown in Fig. 3.12. When driving both segments with digital signals that have the same amplitude, 4 equidistant levels can be obtained in the optical power domain. In the electrical field domain, these 4 levels will not be equidistant.

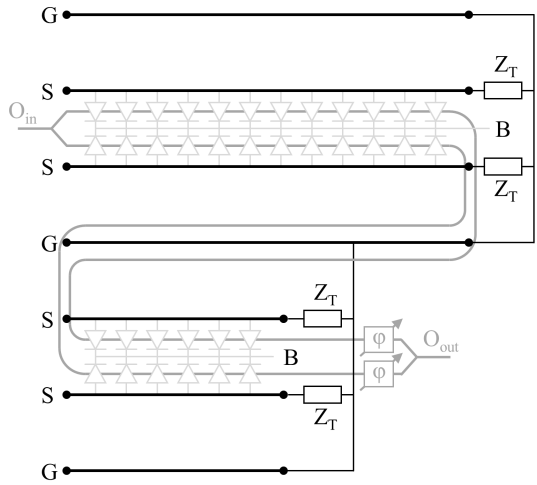

Figure 3.12: Architecture of the traveling-wave modulator using differential electrodes, an SPP phase shifter and traveling-wave segments to implement an electro-optical 2-bit digital-to-analog conversion.

Note that to be able to interface with a driver IC containing multiple drivers, the high-speed bondpads of the modulator need to be aligned in one column. In our architecture, the adjacent segments share the ground-bondpad. When this modulator was designed, only C-band phase shifters were available. Therefore, the modulator is designed to operate in the C-band. Note that a conversion to the O-band is straigthforward for MZMs.

In order to bias the MZM at its quadrature point, thermo-optic phase shifters are used. In each arms a thermo-optic phase shifter of 100 µm is inserted to maintain perfect balance between both arms. These phase shifters consist of a 100 µm long strip of doped silicon next to the strip waveguide. The doped silicon acts as a resistor which heat the waveguide when electrical power is applied. The temperature dependency of the effective index causes a phase shift [3].

The cross section of the structure in Fig. 3.12 is given in Fig. 3.13. As two metal layers are available, both are used to minimize the resitive losses. Note that the cathodes of the diode are both connected to the bias line, thus the bias line should have a higher voltage than the signal lines in order to obtain a reverse biased junction.

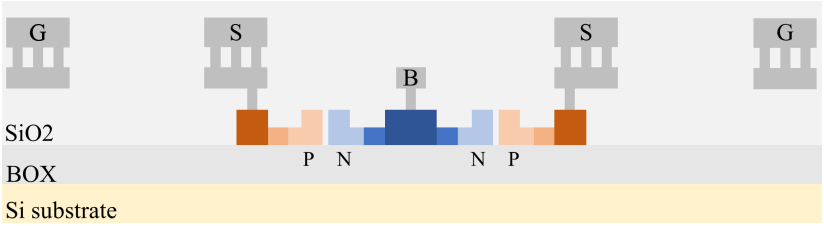

Figure 3.13: Cross section of the modulator architecture from Fig. 3.12 with differential electrodes and SPP phase shifters on the iSiPP50G technology.

3.3.2 Static optimization

First, we will optimize the length of both segments to obtain the desired extinction ratio (ER). From Table 3.1, we find that the $V_\pi L_\pi$ is 14 V.mm and the insertion loss is 1.5 dB/mm. Our driver will generate a differential voltage swing of 2 V, see chapter 5. The modulator will be interfaced using fiber grating couplers, each with an insertion loss of 3 dB [3]. The insertion loss of the on-chip splitters, combiners and waveguides will be neglected for now, as they are low in comparison with the other losses. We'll assume a laser power of 13 dBm. For the static response, the lengths of both segments are added to obtain the full modulator length L. We can now calculate the ER, optical mod-

ulation amplitude (OMA) and average launch power as a function of modulator length. The results are shown in Fig. 3.14. As each fiber grating coupler has 3 dB insertion loss, the total loss associated with coupling light in and out of the modulators is 6 dB. Evidently, a longer modulator has a lower V_π and more insertion loss, and thus a higher extinction ratio while also having a decreasing average launch power. Interestingly, the OMA first increases with modulator length and starts to decrease when the losses become dominant. The maximal OMA is achieved around 2.6 mm. This simulation also nicely demonstrates that a high ER does not necessarily translates into a high OMA.

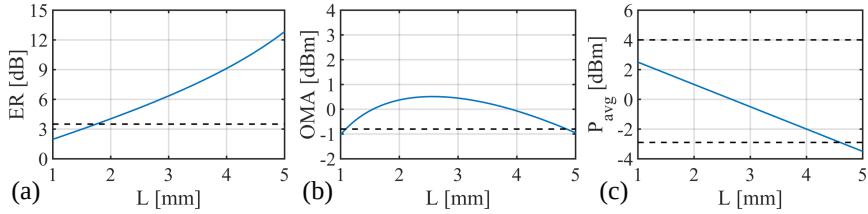

Figure 3.14: Static performance of a MZM with the standard phase shifter: (a) ER, (b) OMA and (c) average launch power. The black dashed line show the specifications according to the IEEE 400GBASE-DR4 [25] standard.

We aim to develop a 53 Gbaud PAM-4 optical transmitter, so it makes sense to check the specifications of the appropriate standard being IEEE 400GBASE-DR4 [25]. The ER should exceed 3.5 dB, the OMA should be between -0.8 and 4.2 dBm while the average launch power should be between -2.9 and 4 dBm. These are all annoted using black dashed lines in Fig. 3.14. Applying these specifications leads us to a modulator length between 1.75 and 4.6 mm, respectively limited by the minimal extinction and minimal launch power.

However, the employed $V_\pi L_\pi$ are for a bias voltage of 0 V. PN junctions are typically biased at a reverse bias of several volt to maximize their bandwidth, which also results in a higher $V_\pi L_\pi$ and lower insertion loss, see section 2.3.1. Due to the higher $V_\pi L_\pi$, the ER will decrease for a fixed length, thus a higher minimal length will be required. At the same time, the average launch power will increase for the same length due to the lower insertion loss. Thus the maximal modulator length can increase. The effect on the OMA-curve is more difficult to predict, as the higher $V_\pi L_\pi$ is partially counteracted by the lower insertion loss. Additionally, the length of the modulator should be minimized to maximize its bandwidth. Given these constraints and given the available space on the photonic IC, we selected the MSB and LSB to be 2.25 and 1.2 mm, thus the total length is 3.45 mm. This is still sufficiently close to the maximal OMA-point, while having a sufficiently high ER. Furthermore,

if the final devices has slightly too much insertion loss but a sufficiently high ER, experiments are still possible albeit using higher laser powers or additional optical amplification. An ER that is too low can only be fixed by increasing the driving voltage, but our driver has a maximal output swing of 2 V. As will be shown in the next section, a sufficiently high bandwidth can be achieved using these modulating sections. The equalization capabilities in the driver, combined with the relative slow roll-off in modulator frequency response can help significantly.

With these lengths, we find that the MSB and LSB have a V_π of 6.2 and 11.7 V at a bias voltage of 0 V. The insertion loss of the MSB and LSB segment are 3.4 and 1.8 dB at 0 V. Combined, they have a V_π of 4.1 V and a total insertion loss of 5.2 dB. When coupled to our driver with 2 V swing, the ER will be 6.7 dB. The total modulator insertion loss, comprising the phase shifters and the grating couplers is 11.2 dB.

3.3.3 Dynamic optimization

Next, we can optimize the electrode dimensions to maximize the bandwidth. As outlined in section 3.2.1, we need the RLCG parameters of the unloaded line and the equivalent circuit of the phase shifter to start. Both can be obtained by separate simulation in Keysight ADS Momentum®. The cross-sectional dimensions of the unloaded line can be swept to find the optimal modulator. A more accurate method would be to directly simulate the loaded line. However, the simulation time is significantly higher, such that optimizing becomes very tedious. The full simulation technique is shown in Fig. 3.15.

The width of the signal lines W and clearance C is swept. The width is swept from 5 to 15 µm in 5 µm steps while the clearance is swept from 20 to 60 µm in 10 µm steps. The phase-shifter was already simulated in section 3.1. However, that simulation did include the metal contacts, which actually are part of the the unloaded transmission line. Thus the phase shifter without electrode contacting is simulated, as shown in Fig. 3.15. The adjusted component values for the phase shifter are given in Table 3.3. As can be observed, the parallel capacitance C_P drops significantly.

The loaded transmission line parameters for selected widths and clearances are shown in Fig. 3.16. The PN junction was reverse biased at 2 V. While static optimization at a reverse bias of 2 V was not possible since no data was available from the PDK documentation, dynamic optimization is possible since the junction capacitance is given, see Table 3.1. Only the most extreme clearances are shown. For matching, we aim at a differential characteristic impedance close to 100 Ω. This can be achieved using a small trace width and large clearance, but at the cost of a high attenuation. Lowering the attenuation

	w=40 nm	w=70 nm	
C_{PN}	0.282	0.180	[fF/ µm]
R_{PN}	10.04	9.890	[kΩ. µm]
C_P	71.6	70.8	[aF/ µm]
C_{BOX}	16.2	15.9	[aF/ µm]
R_{SUB}	2.971	3.085	[MΩ. µm]

Table 3.3: Component values for the standard phase shifter without electrode contacts

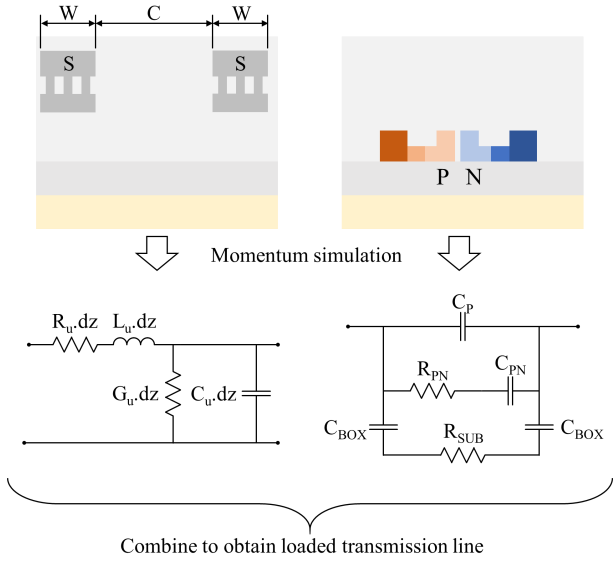

Figure 3.15: The electrodes and reverse biased PN junction are simulated seperately to obtain the equivalent electrical circuits. Both are combined to obtain the loaded transmission line parameters

by increasing the electrode width and decreasing clearance yields a decrease in characteristic impedance. Thus an optimum has to be found. Note that the attenuation shows some distinct changes when sweeping, but the losses are predominantly determined by the phase shifter. In all cases, the phase index is sufficiently close to the optical group index of 4.26 to not cause the main bandwidth limitation.

From these loaded transmission line parameters, combined with the lengths of both segments, we can calculate the electro-optic response as outlined in section 3.2.1. The differential source impedance is 100 Ω. As differential

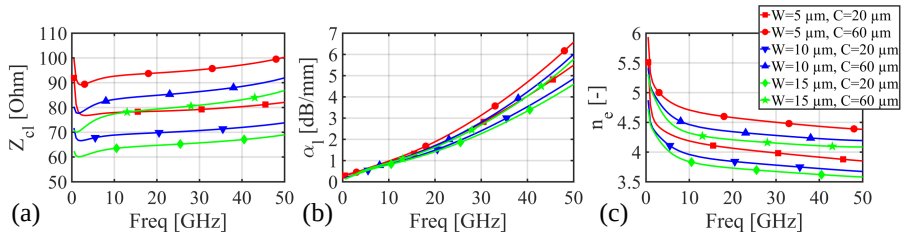

Figure 3.16: Loaded transmission line parameters: differential characteristic impedance (a), attenuation (b) and phase index (c).

termination impedance, we select 100 Ω, as our driver is optimized for this impedance. In line with the previous simulations, the PN junction was biased at a reverse voltage of 2 V. The electro-optic responses for selected widths and clearances are shown in Fig. 3.17(a) for the MSB and (b) for the LSB. For both segments, increasing the width while keeping the clearance fixed decreases the bandwidth. This contradicts the conclusion from Fig. 3.16, where smaller widths yield a higher microwave attenuation and thus should yield a lower bandwidth. This earlier finding assumes however that the modulator is perfectly terminated such that there are no reflections. Here, the modulator is terminated with a fixed impedance Z_T of 100 Ω, which can be quite different from the characteristic impedance Z_{cl}, see Fig. 3.16. In section 3.2.2, it was shown that a larger mismatch between Z_T and Z_{cl}, with Z_T higher than Z_{cl} can cause a large drop in bandwidth. Indeed, a higher electrode width yields a considerable decrease in Z_{cl}, while Z_T remains fixed and thus leads to the observed drop in modulation bandwidth.

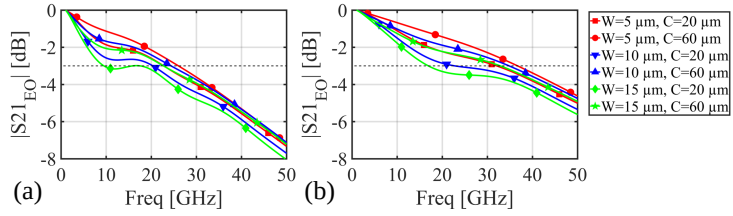

Figure 3.17: Electro-optic response of the MSB (a) and LSB (b) for selected electrode configurations and at a bias voltage of 2 V. Normalized at 1 GHz.

Similarly, a higher clearance for a fixed width, should yield a lower bandwidth due to the higher microwave attenuation. However, this also causes the characteristic impedance to increase such that there is a net increase in bandwidth.

In Fig. 3.18, the 3dB electro-optical bandwidth of all swept configurations is shown. As expected, the LSB has a higher bandwidth than the MSB and the highest bandwidth is achieved for the most narrow electrodes with the largest clearance in the sweep range. While this points yield the highest bandwidth, our models do not include all additional parasitics at the largest clearances. A larger C means that the center n-doped region (see Fig. 3.13) becomes wider. While it is preferred to increase the size of the n-doped region over the p-doped region, since the p-doped region has a worse conductivity, it does introduce additional resistance that is not included in our models. Only the cross-section of the phase shifter in Fig. 3.15 is used. Furthermore, there will be additional stray capacitance between the both sides of the PN-junction and between the n-doped layer and the electrodes. Therefore, a clearance of 40 µm is chosen to be on the safe side. Secondly, a width of 10 µm is chosen to ensure the traces can carry sufficient current. This results in an electro-optic bandwidth of 23 GHz and 33 GHz for the MSB and LSB respectively.

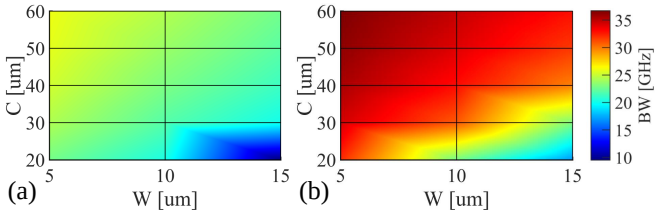

Figure 3.18: Normalized electro-optic bandwidth of the MSB (a) and LSB (b) for all electrode configurations and at a bias voltage of 2 V.

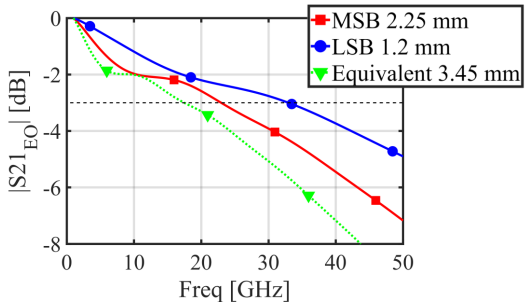

Figure 3.19: Electro-optic response of the MSB, LSB and a modulator consisting of one single segment with a length equal to that of the MSB and LSB combined. With W=10 µm and C=40 µm, reverse bias of 2 V, normalized at 1 GHz.

The final electro-optic responses are shown in Fig. 3.19, for a reverse bias of 2 V. To observe the effect of using two segments, the response of a modulator with a length of 3.45 mm is also shown. Compared to the MSB and LSB, this long segment only achieves a bandwidth of 17.5 GHz

3.3.4 Final modulator design

With the simulated devices, we can now code the full layout. The full schematic and layout are shown in Fig. 3.20. We have included two identical MZMs, both with two traveling-wave segments. All DC optical phase shifts are implemented using thermo-optic phase shifters. The optical splitting and combining is done through multimode interferometers (MMIs), offering broadband splitting and combining from 1530 nm to 1570 nm with an excess loss less than 0.1 dB. Optical interfacing is done through fiber grating couplers with, according to the PDK-documentation, a peak insertion loss of 2.4 dB at 1565 nm and a 1-dB optical bandwidth of 35 nm. Given the sensitivity of alignment, we assume 3 dB insertion loss per device in our static optimization. If both MZMs are at maximum transmission and their outputs interfere constructively, the total insertion loss becomes: $2\times$ 3 dB from the grating couplers, 3.1 dB from the MSB and 1.8 dB from the LSB thus 11.2 dB in total. Waveguide losses, at 0.14 dB/mm, are negligible compared to other losses.

By including two MZMs, we can perform both the envisioned intensity modulation and direct detection (IM/DD) experiments, but later also extend to coherent communication. For IM/DD experiments, one MZM is biased at quadrature, while the other is biased at minimum transmission. The MZM at quadrature is used for modulation. For coherent experiments, both MZMs are at minimum transmission and both are used to modulate the data. Note that if one MZM is at minimum transmission, there is 6 dB additional insertion loss: 3 dB from the splitting and 3 dB from the combining. As the MZM biased at it's quadrature point also introduced 3 dB modulation loss. This increases the total insertion loss with 9 dB.

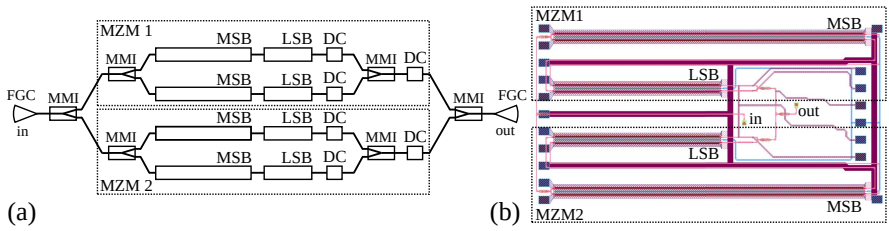

Figure 3.20: (a) Optical schematic of the full structure. (b) Layout of the full structure with the high-speed bondpads left and DC-control bondpads right.

To summarize, we have listed the simulated specifications of the device below:

- V_π of the MSB, LSB and combined (at V_{bias} 0 V): 6.2, 11.7 and 4.1 V;
- IL of the MSB, LSB and combined (at V_{bias} 0 V): 3.1, 1.8 and 5.2 dB;
- Bandwidth of the MSB and LSB (at V_{bias} 2 V): 23 and 33 GHz;
- Total insertion loss, both MZMs at MATP (at V_{bias} 0 V): 11.2 dB;
- Total IL with one MZM at QP & one MZM at MITP (at V_{bias} 0 V): 20.2 dB;
- High speed bondpads: GSSG configuration with 125 µm pitch;
- Total structure size: 1300 by 2550 µm.

3.4 Measurement Results

The manufactured die is shown in Fig. 3.21. We can now perform the static and dynamic characterization of the phase shifters, verify our modeling and if necessary, optimize it.

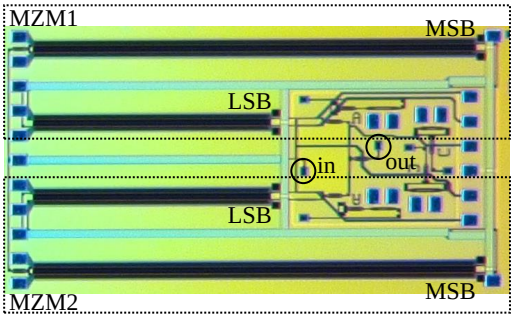

Figure 3.21: Micrograph of the full modulator die

To characterize the insertion loss, we first measured a direct connection between two grating couplers to deduce the grating coupler loss. A loss of 5 dB per coupler was found at 1550 nm. This deviation could be caused by a suboptimal probing setup, e.g. fiberprobe too far from the grating coupler, under a slightly wrong angle, or due to process variations. However, all future measurements were done using the same setup, thus this coupler loss is used for the remainder of this section. Thereafter, the insertion loss on a 1.3 mm long piece of phase shifter was measured for various biasing voltages. The losses are summarized in Table 3.4. As expected, a higher reverse bias voltage lowers the insertion loss. However, the observed insertion loss at 0 V is higher than

disclosed in the PDK documentation: 1.85 dB/mm instead of the anticipated 1.5 dB/mm.

Vbias [V]	IL [dB/mm]	$V_\pi L_\pi$ [V.mm]
0	1.85	-
-1	1.77	19.2
-2	1.69	22.1
-3	1.61	23.5

Table 3.4: Measured attenuation and $V_\pi L_\pi$ of the phase shifter at 1550 nm

To determine the $V_\pi L_\pi$, a differential DC voltage is applied to an MZM with a 1.3 mm long phase shifter, the MZM is biased at quadrature. A separate DC-test MZM was used as this eases measurements compared to performing measurements on the full structure. The obtained $V_\pi L_\pi$ is given in Table 3.4. Note that no measurements were conducted at 0 V, since one of the PN junctions would be forward biased. Again as expected, a higher reverse bias yields a higher $V_\pi L_\pi$. The PDK documentation stated a $V_\pi L_\pi$ of 14 V.mm at 0 V. While an increase in $V_\pi L_\pi$ is expected at higher reverse biases, a $V_\pi L_\pi$ of 19.2 V.mm at -1 V is a relative large step. We expect that this higher $V_\pi L_\pi$ is related to process variations.

From these measurements, we can derive the following specifications:

- V_π of the MSB, LSB and combined (at V_{bias} 2 V): 9.8, 18.4 and 6.4 V;
- IL of the MSB, LSB and combined (at V_{bias} 2 V): 3.8, 2 and 5.8 dB.

The higher V_π will result in a lower modulation efficiency. We expect still to obtain an ER of 4.5 dB with a V_π of 6.4 V at a reverse bias of 2 V.

Next, high-speed measurements are conducted to characterize the electro-optic response and determine the device bandwidth. The measured electro-optic transfer functions for both segments at a reverse bias voltage of 0 and 2 V are shown in Fig. 3.22. These measurements are conducted with a 70 GHz high-speed photodiode, such that the measured S-parameter response is proportional to the OMA.

It immediately becomes apparent that the electro-optic bandwidth is significantly lower than anticipated. For the MSB at a reverse bias of 2 V, we expected a bandwidth of 23.4 GHz but we only obtained 12.1 GHz in the actual device. Similarly, at a reverse bias of 0 V, the obtained bandwidth is only 8.1 GHz compared to the simulated 11.2 GHz. A lower bandwidth for a lower reverse bias is to be expected, as the PN junction has a higher capacitance. This results in a lower characteristic impedance and more microwave losses.

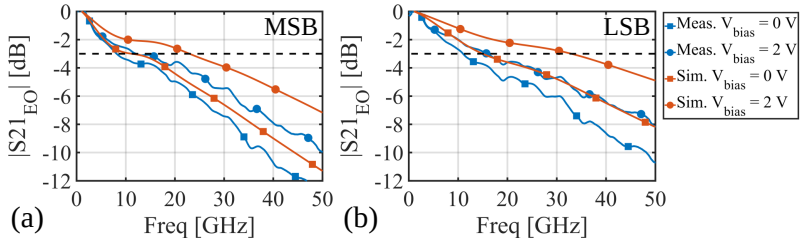

Figure 3.22: Measured and simulated electro-optic response of the MSB (a) and LSB (b) at a reverse bias of 0 and 2 V. Normalized at 1 GHz, measurements smoothed over a 1 GHz window.

For the LSB, a comparable trend is observed. The bandwidth at 2 V was expected to be 33 GHz and turned out to be 15.9 GHz. At a reverse bias of 0 V, the simulation predicted 15 GHz, while 11 GHz was measured.

In a first step to let the simulation and measurement converge, we take a look at the simulations of the electrodes and phase shifters. As these were simulated separately, coupling between the electrodes and the phase shifters is not included. Furthermore, if electrical currents along the modal propagation direction exist in the doped silicon of the phase shifter, our additive approach of section 3.2.1 is not entirely correct. In that case, the addition of the phase shifter not only alters the shunt conductance and capacitance, but also the series resistance and inductance. In order to improve our simulation models, the full cross section with electrodes and phase shifters combined (see Fig. 3.13) is simulated with the correct dimensions (electrode width of 10 µm and clearance of 40 µm). This directly yields the loaded transmission line parameters. Next, the phase shifter used in this simulation was isolated and the equivalent circuit was refitted to account for the larger N-doped region in the phase shifter transfer function. From this data, a new electro-optic response could be derived. The results are shown in Fig. 3.23.

The main difference is the decreased response at higher frequencies, while the lower frequency range is largely unaffected. Consequently, the simulated electro-optic bandwidths do not change significantly. The RLGC parameters of the loaded line obtained using the original simulation technique and optimized simulation technique (where the full cross section of the loaded line was simulated) is shown in Fig. 3.24. The inductance, conductance and capacitance match very well. However, the series resistance of the optimized simulation is higher at higher frequencies, indicating that indeed currents flow in the doped regions along the propagation direction. This leads to the higher attenuation at high frequencies.

Observing the discrepancies between measurement and simulation in

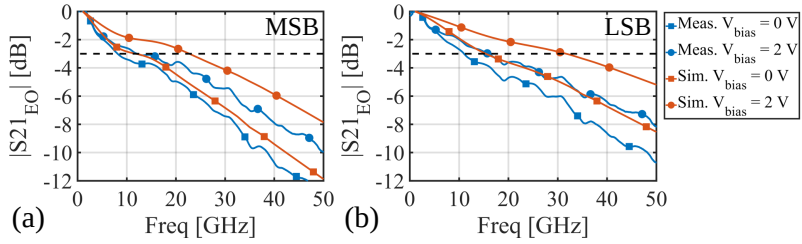

Figure 3.23: Measured and optimized simulated electro-optic response of the MSB (a) and LSB (b) at a reverse bias of 0 and 2 V. Normalized at 1 GHz, measurements smoothed over a 1 GHz window.

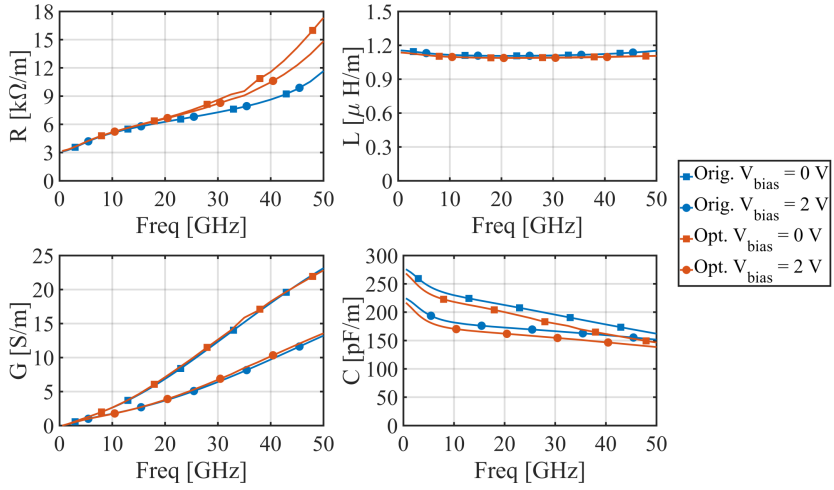

Figure 3.24: RLGC parameters of the loaded line using the original simulation technique and the optimized simulation technique.

Fig. 3.23, it becomes apparent that the measurements show a sharper roll-off at low frequencies. This can be caused by a termination resistance that is higher than expected. DC-measurements indicate a termination resistance of around 110 Ω. The adjusted electro-optic responses are shown in Fig. 3.25.

Increasing the termination resistor indeed yields a better match at lower frequencies. The simulated bandwidths for the MSB segment at a reverse bias of 0 and 2 V is 8.2 and 20.5 GHz respectively, whereas the measurements yield a bandwidth of 12.1 and 8.1 GHz. For the LSB segment, the simulated bandwidths at a reverse bias of 0 and 2 V is 26.8 and 13.3 GHz respectively, whereas the measurements yield a bandwidth of 15.9 and 11 GHz. The input impedance of the measurements and optimized simulations are shown in

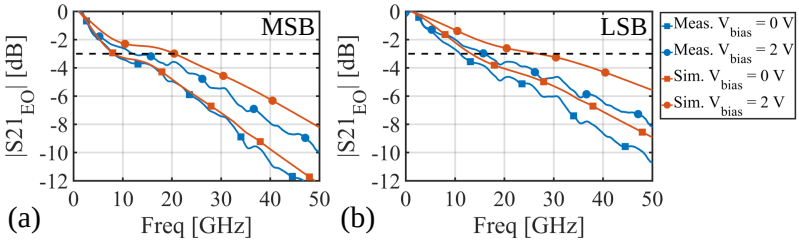

Figure 3.25: Measured and optimized simulated (with 110 Ω termination) electro-optic response of the MSB (a) and LSB (b) at a reverse bias of 0 and 2 V. Normalized at 1 GHz, measurements smoothed over a 1 GHz window.

Fig. 3.26. A relative good correspondence is obtained, albeit some deviations exist at low frequencies. This is caused by suboptimal landing of the RF-probes during the measurement.

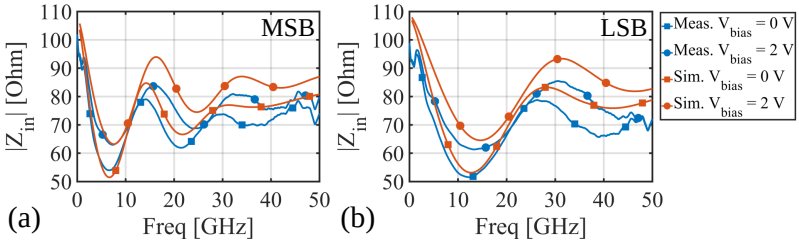

Figure 3.26: Measured and simulated (optimized, with 110 Ω termination) input impedance of the MSB (a) and LSB (b) at a reverse bias of 0 and 2 V. Measurements smoothed over a 1 GHz window.

While the final results are relative close to the measured waveforms, still some discrepancies exist. While these electro-optic bandwidths are low, the roll-off is quite slow. Assuming we want to generate 53 Gbaud data, a device bandwidth of at least 27 GHz is desired. At 27 GHz, the MSB and LSB still only have a 5.2 dB and 4.6 dB drop with respect to their DC-value. Thus using a limited amount of peaking from an equalizer, i.e. 2.2 and 1.6 dB respectively, the bandwidth can be significantly extended.

An important step in further research would be to further investigate the origin of this discrepancies. This would require additional measurements on electrode structures, loaded transmission lines without termination and the phase shifter. On our photonic IC, a loaded transmission line, where both ends could be probed using RF probes, was available. But as this line was relative short, only 1.3 mm, the measurement is very prone to errors in calibration and

probing. The data was unfortunately too degraded to extract useful results. Furthermore, a lower termination impedance would be key to mitigate the unexpected additional resistance we encountered. Lowering the impedance will also help to increase the bandwidth, with some minor adaptations on the driver side, this will not have any large side-effects.

3.5 Conclusion

In this chapter, we discussed the analysis of traveling-wave MZMs. An analytical theory was presented and the most important performance tradeoffs were qualitatively and quantitatively discussed. Using the available data from the PDK documentation, and additional high-speed simulations, a simulation model for a MZM was designed. This model allowed to optimize the electrode dimensions in order to reach the desired modulation efficiency and maximize the bandwidth. A segmented traveling-wave structure was designed and characterized. The complete modulator consists of two child MZMs each with two segments. The segment lengths are designed to achieve a 2-bit electro-optical DAC operation when both are driven with signals having the same swing. The MSB and LSB have a V_π of 9.8 and 18.4 V (reverse bias of 2 V) and an insertion loss of 3.8 and 2 dB (reverse bias of 2 V). The MSB and LSB have a bandwidth of 12.1 and 15.9 GHz. The simulation model was verified with these simulations. Given the simplifications in the model, a relative good match was obtained. Further optimization of the simulation model yields a more accurate prediction of the resulting electro-optic transfer function. However, still some discrepancies exist. In further research, the nature of this discrepancies has to be assessed using measurements on well-designed test structures. This will allow to further optimize the Keysight ADS Momentum® simulations as well as the fitted equivalent circuits and the subsequent analysis.

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4

Frequency Response Shaped Mach-Zehnder Modulators

In this chapter, a novel method is presented to embed finite impulse response (FIR) filters in slow-wave Mach-Zehnder modulators. By choosing the desired FIR filter, the electro-optic frequency response can be adjusted to enhance the modulator bandwidth or counteract bandwidth limitations from other link components. The embedded FIR filters can take over the electrical equalization partially or completely in certain cases to provide a power and area-efficient way of equalization. This chapter is based on the following publication:

> **L. Breyne**, J. Lambrecht, M. Verplaetse, X. Yin, G. Roelkens, P. Ossieur, and J. Bauwelinck, "Electro-Optic Frequency Response Shaping using Embedded FIR Filters in Slow-Wave Modulators," *Journal of Lightwave Technology*, vol. 39, no. 6, pp. 1777–1784, 2020.

4.1 Introduction

The ever-increasing growth in network traffic drives both industry and academia to push the capacity of optical interconnects to support astounding data rates. The last decade has proven that integrated photonic systems have a key role to play in this evolution by allowing compact, fast, innovative and cheap devices to be manufactured in large volumes. The devices can be used both in

externally intensity-modulated/direct-detection (IM/DD) as well as coherent communication systems. Especially silicon photonic systems gained a lot of interest. Thanks to the large effective index difference between the silicon core and silicon dioxide cladding, compact, low-loss structures are possible. The compatibility with CMOS manufacturing lines provides high-volume, high-yield and low-cost production while also allowing easy integration with e.g. (Bi)CMOS driver circuits.

Three types of silicon optical modulators have gained particular interest: Mach-Zehnder modulators (MZMs) [1–10], electro-absorption modulators (EAMs) [11, 12] and micro-ring modulators (MRMs) [13]. EAMs and MRMs offer a very compact footprint and high bandwidth, which has led to recent demonstrations at 112 and 128 Gb/s PAM-4 [12, 13]. But MRMs are challenging to bias and introduce significant chirp. While EAMs require additional materials in the process, they also do show wavelength dependency and cannot be easily ported from C- to O-band. MZMs are typically larger and more power consuming but they operate in both O- and C-band, are easy to bias, can be made without additional materials, have a higher linearity and are more suited for coherent communication. This makes them a popular choice as modulators.

Of the various physical mechanisms available to perform modulation in silicon MZMs, the plasma dispersion effect is most employed. It only requires doping the silicon waveguides. Three modes can be used to introduce phase shift: carrier injection, accumulation or depletion [14]. The latter is most often used because of the straightforward manufacturability and high-speed operation [15]. Note that by using other materials, higher modulation efficiencies and bandwidths may be obtained [8–10]. However, these approaches come at the cost of CMOS compatibility.

A myriad of innovative solutions have been demonstrated in recent years [1–7] to push the performance of silicon MZMs. Since the electro-optic effect in silicon is rather weak, long phase shifters are required [16]. Thus most high-speed designs incorporate traveling-wave structures to reach high bandwidths. The authors of [1] show that optimization of the doping levels and PN-junction itself can be used to optimize the bandwidth-V_π trade-off, while [2] shows how termination mismatch of the traveling wave electrode can be used to enhance the electro-optic bandwidth. In [3] and [4], two PN-junctions are placed in series between two electrodes to half the load capacitance. This decreases the microwave attenuation and enhances the bandwidth. The advantage of loading a traveling-wave structure periodically with short phase-shifter segments instead of continuous loading is demonstrated in [5]. This technique leads to a so-called slow-wave modulator which offers superior high-speed performance [5, 17]. A very interesting approach is taken in [7]. Instead of using a

traveling-wave concept, the MZM is split into separate lumped segments that are driven separately. The authors of [7] drive the segments in such a way that a feed-forward equalizer (FFE) structure is obtained to improve the modulator bandwidth.

We proposed a novel slow-wave modulator design using carrier-depletion PN junctions in [18]. By careful analysis and design, a finite-impulse response (FIR) filter can be integrated in the structure. The frequency response of the FIR filter is applied onto the slow-wave modulator response allowing a wide range of FIR filter shapes. This allows to enhance the electro-optic bandwidth of the modulator or to introduce peaking to counteract bandwidth limitations in the driver, link or receiver. By adding FIR filters in the modulator, equalization elsewhere in the link can be minimized or even omitted. Making this technique very attractive for short-reach datacenter interconnects. The FIR filter can be integrated without introducing additional processing steps or by adjusting the electrical operation of the modulator. While the technique is demonstrated here on silicon photonics, it can be easily ported to other technology platforms.

In section 4.2, we analyze the slow-wave modulator structure and explain how a FIR filter can be integrated in the structure. In section 4.3.1 and 4.3.2, we cover the design and simulation of a standard and a shaped modulator. Electro-optic characterization of manufactured devices is covered in 4.3.3. An optical link experiment is described in section 4.4.

4.2 Slow-wave modulator as FIR filter

We start from the standard slow-wave modulator design, as described in [17] and [19]. A differential drive push-pull MZM is chosen with series-push-pull (SPP) phase shifters to separate high-speed operation from the junction bias voltage. The electrodes are in a GSSG configuration as this provides advantages in drive voltage, inter-device crosstalk and driver integration [19, 20]. An example layout of such an MZM is given in Fig. 4.1.

4.2.1 Standard slow-wave modulator

A very convenient way to analyze the electro-optic response of slow-wave modulators is provided by [17]. However, the ABCD-matrix approach only operates on 2-port structures, while a differential transmission line is modeled as a 4-port structure. In [19], it is shown that a differential MZM that is perfectly symmetrical and driven differentially can be fully described using its differential transmission line parameters. This simplifies the 4-port device to a 2-port device allowing the ABCD-matrix formalism to be applied. Since the proposed modulator structure from Fig. 4.1 is perfectly symmetrical and will

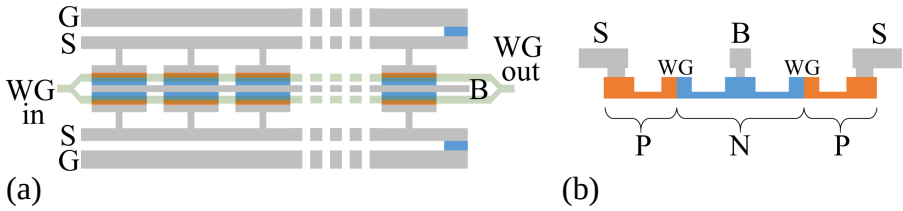

Figure 4.1: (a) Layout of a differential drive push-pull MZM with SPP phase shifters, a GSSG electrode configuration and on-chip termination. The PN-junctions are biased using the B-line that does not carry any AC-signal. (b) Simplified cross section of a segment with PN-doped rib waveguides.

be driven differentially, this technique can be applied. Converting the general MZM with N segments from Fig. 4.1 to its electrical equivalent leads to the circuit in Fig. 4.2.

The transmission line differential characteristic impedance and propagation factor are Z_{cdiff} and γ_{diff}. The pieces of transmission line between adjacent phase shifter segments have length L, while at the beginning and end of the first and last segment the length is L/2. The differential source impedance, source voltage and termination impedance are denoted Z_{Sdiff}, V_{Sdiff} and Z_{Tdiff}. Each phase shifter is modeled as an RC series circuit $R_{PN}C_{PN}$. As they are placed in series, we find R_M and C_M equal to $2\times R_{PN}$ and $C_{PN}/2$ respectively. Note that it is also possible to include more elaborate equivalent circuits for the phase shifters.

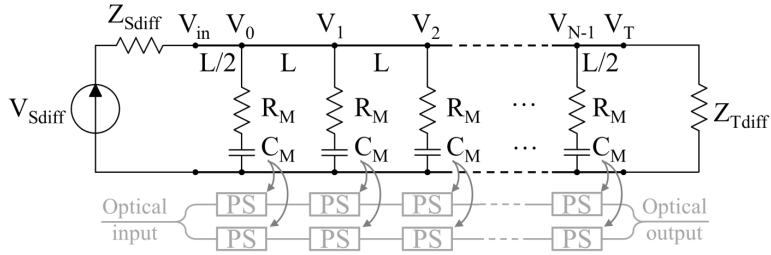

Figure 4.2: Equivalent electrical and optical circuit of the slow-wave modulator in Fig. 4.1 with N segments. The electrical part only contains the differential mode parameters. The transmission line segments have a characteristic impedance Z_{cdiff} and propagation factor γ_{diff}. Both phase shifters are taken together in the equivalent RC series network R_MC_M.

As described in [17] and [19], we can now use the ABCD-matrix formalism to calculate the voltage over each C_M. The ABCD matrix T_L of the L/2 piece

of transmission line at the input is given by [21]:

$$\begin{pmatrix} V_{in} \\ I_{in} \end{pmatrix} = \underbrace{\begin{pmatrix} \cosh(\gamma_{\text{diff}} \frac{L}{2}) & Z_{\text{cdiff}} \sinh(\gamma_{\text{diff}} \frac{L}{2}) \\ Z_{\text{cdiff}}^{-1} \sinh(\gamma_{\text{diff}} \frac{L}{2}) & \cosh(\gamma_{\text{diff}} \frac{L}{2}) \end{pmatrix}}_{T_L} \begin{pmatrix} V_0 \\ I_0 \end{pmatrix} \tag{4.1}$$

Since the L/2 piece of transmission line at the output has the same length, the ABCD matrix $\mathrm{T_T}$ of that piece is equal to $\mathrm{T_L}$:

$$\begin{pmatrix} V_{N-1} \\ I_{N-1} \end{pmatrix} = T_L \begin{pmatrix} V_T \\ I_T \end{pmatrix} = T_T \begin{pmatrix} V_T \\ I_T \end{pmatrix} \tag{4.2}$$

Analogously, the ABCD matrix $\mathrm{T_C}$ of the transmission lines segment between the phase shifters is given by:

$$\begin{pmatrix} V_n \\ I_n \end{pmatrix} = \underbrace{\begin{pmatrix} \cosh(\gamma_{\text{diff}} L) & Z_{\text{cdiff}} \sinh(\gamma_{\text{diff}} L) \\ Z_{\text{cdiff}}^{-1} \sinh(\gamma_{\text{diff}} L) & \cosh(\gamma_{\text{diff}} L) \end{pmatrix}}_{T_C} \begin{pmatrix} V_{n+1} \\ I_{n+1} \end{pmatrix} \tag{4.3}$$

To complete, the ABCD matrix of the impedance of the phase shifters is given by [21]:

$$T_M = \begin{pmatrix} 1 & 0 \\ \left(R_M + \frac{1}{sC_M}\right)^{-1} & 1 \end{pmatrix} \tag{4.4}$$

With $s = j\omega_m$ and ω_{m} the pulsation of the modulating signal. The voltage at the $\mathrm{n^{th}}$ segment can now be calculated by cascading the ABCD matrices of the elements preceding that specific segment, thus we find:

$$\begin{pmatrix} V_{in} \\ I_{in} \end{pmatrix} = T_L (T_M T_C)^n \begin{pmatrix} V_n \\ I_n \end{pmatrix} \tag{4.5}$$

With n from 0 to N-1. Note that a matrix inversion is required to solve for $\mathrm{V_n}$. Both the voltage and current at the input terminal of the modulator can be derived as follows:

$$V_{in} = \frac{Z_{\text{in}}}{Z_{\text{Sdiff}} + Z_{\text{in}}} V_{\text{Sdiff}} \qquad I_{in} = \frac{1}{Z_{\text{Sdiff}} + Z_{\text{in}}} V_{\text{Sdiff}} \tag{4.6}$$

The input impedance $\mathrm{Z_{in}}$ of the modulator can be derived from the ABCD matrix of the full modulator:

$$Z_{in} = \frac{A_{tot} Z_{\text{Tdiff}} + B_{tot}}{C_{tot} Z_{\text{Tdiff}} + D_{tot}} \tag{4.7}$$

With the ABCD matrix of the full modulator given by:

$$\begin{pmatrix} A_{tot} & B_{tot} \\ C_{tot} & D_{tot} \end{pmatrix} = T_L(T_M T_C)^{N-1} T_M T_T \tag{4.8}$$

Note that $\mathrm{V_n}$ is the voltage over the $\mathrm{n^{th}}$ modulator segment. In the phase shifter, the voltage over $\mathrm{C_M}$ gives rise to the optical phase shift. Thus the voltage divider $\mathrm{R_M C_M}$ needs to be taken into account using the following transfer function:

$$V_n' = \frac{1}{1 + sR_M C_M} V_n \tag{4.9}$$

Each phase shifter introduces the phase shift at a different location on the modulator. To calculate the total introduced phase shift, a reference location on the MZM should be chosen at which all separate contributions can be combined. The most obvious location is the last segment. Thus the phase shift introduced in the $\mathrm{n^{th}}$ segment has to travel through N-1-n segments of physical length L with group index $\mathrm{n_o}$. Since the optical waveguides run parallel along the electrodes, the physical distance between adjacent segments in the electrical and optical domain is both L. This results in the following delay correction factor:

$$V_n'' = V_n' \exp(-j\beta_o(N-1-n)L) \tag{4.10}$$

With the propagation factor β_o given by:

$$\beta_o = \frac{\omega_m n_o}{c} \tag{4.11}$$

The resulting voltage that introduces phase shift is then:

$$V_{tot} = \frac{1}{N} \sum_{n=0}^{N-1} \frac{\exp(-j\beta_o(N-1-n)L)}{1 + sR_M C_M} V_n \tag{4.12}$$

Which is the same as found in [17]. The phase shift (in radians) between both arms at the MZM output is now given by:

$$PS_{tot} = \pi \frac{V_{tot}}{V_\pi} \tag{4.13}$$

With $\mathrm{V_\pi}$ calculated over the full MZM, not a single segment. This total phase shift gives rise to the intensity modulation at the output of the MZM. Using this analysis, the small-signal electro-optic response of a slow-wave modulator can be derived. Moreover, using some minor adjustments, a FIR filter structure can be identified.

4.2.2 FIR filtering in slow-wave modulators

The equivalent electrical schematic from Fig. 4.2 can be further abstracted. To be able to calculate the full phase shift introduced by the segments, an additional delay correction was introduced at the optical side. This delay is linked to the distance in the optical domain between two adjacent segments. In the electrical domain, a similar delay is present due to the transmission lines. This delay is already accounted for in the ABCD matrices. If we draw a block diagram of the modulator that only includes these electrical and optical domain delays and the phase shifters, we obtain Fig. 4.3. This diagram only describes the behavior of one arm of the MZM, the other arm is identical, but is driven by opposite signals such that opposite phase shifts are introduced. Some simplifications were used for this description: the transmission line segments are replaced by fixed delays (no attenuation, perfectly matched to the source impedance), the transmission lines are perfectly terminated (no reflected waves) and each phase shifter introduces a frequency-independent phase shift PS at its output. No simplifications are carried out at the optical side: the optical delays are the same as those derived in the previous section.

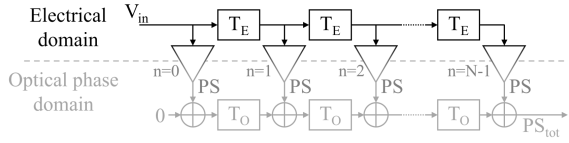

Figure 4.3: Simplified block diagram of a single arm in a slow-wave modulator.

From this block diagram, the equivalency to a FIR filter becomes apparent [22]. In a typical modulator design, the velocity of the electrical and optical wave are matched such that they simultaneously arrive at subsequent segments. In that case, $\mathrm{T_E}$ is equal to $\mathrm{T_O}$ and the full phase shift is the sum of all individual phase shifts. If no velocity match is achieved, a delay factor $\mathrm{T_O}$-$\mathrm{T_E}$ is present between subsequent segments. Thus the total phase shift is given by:

$$\mathrm{PS_{tot}} = \sum_{\mathrm{n=0}}^{\mathrm{N-1}} \exp(-\mathrm{j}(\mathrm{N}-1-\mathrm{n})(\mathrm{T_O}-\mathrm{T_E})\omega_\mathrm{m}) \cdot \mathrm{PS} \tag{4.14}$$

This transfer function consists of a sum of delays yielding the well-known low-pass filtering due to velocity mismatch [6]. In order to add fully controllable FIR filters, we need to create 'taps' with a specific weight and delay [22]. Starting from a velocity matched modulator, one can add an optical delay line with delay $\mathrm{T_D}$ between the $\mathrm{m^{th}}$ and $\mathrm{m}+1^{\mathrm{th}}$ phase shifter. This yields the

equivalent block diagram of Fig. 4.4. Note that adding delay in the optical domain is preferred: the optical waveguides have a smaller bend radius, lower losses and much higher bandwidth than the transmission line electrodes.

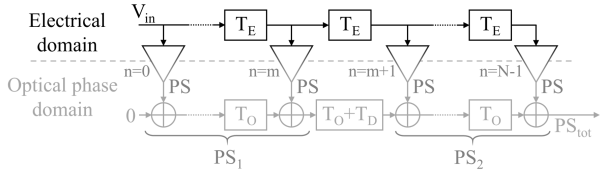

Figure 4.4: Simplified block diagram of a velocity matched modulator (T_E=T_O) where an additional optical delay line is incorporated between the m^{th} and $m + 1^{th}$ segments.

As the modulator is velocity matched, all phase shifts introduced before the delay T_D can be added together to obtain a total phase shift PS_1 of (m+1)×PS. The same can be done with all phase shifts introduced after the delay, resulting in a total phase shift PS_2 equal to (N-m-1)×PS. At the transition between the m^{th} and $(m + 1)^{th}$ segments, a net delay of T_O+T_D-T_E is introduced. Since T_E=T_O, this simplifies to T_D. When observed at the output, PS_2 directly contributes to PS_{tot} while PS_1 experiences an additional delay of T_D, this results in the following total phase shift:

$$PS_{tot} = (N - m - 1)PS + (m + 1)PS \cdot \exp(-jT_D\omega_m) \tag{4.15}$$

This corresponds to a z-domain representation of a FIR filter by substituting $z = \exp(jT_D\omega_m)$:

$$PS_{tot} = (N - m - 1)PS + (m + 1)PS \cdot z^{-1} \tag{4.16}$$

By tuning the position m of the optical delay line, the relative tap coefficients can be set. Tuning the length of the optical delay line changes T_D. Note that multiple optical delay lines can be added to create higher order transfer functions. The optical delay line should be inserted in both arms of the MZM.

However, only positive coefficients can be made this way. By using negative coefficients in FIR filters, peaking in the frequency response can be introduced. Note that the proposed block diagrams only describe the behavior of one arm. As the modulator is symmetrical and driven differentially, the other arm introduces exactly the opposite phase shift (optical delay lines should be introduced in both arms). By crossing the optical waveguides of both arms while keeping the electrodes unaltered, negative coefficients can be achieved. This is demonstrated in the block diagram of Fig. 4.5 where a crossing between the arms and a delay line in each arm are inserted between the m^{th}

and $(\mathrm{m}+1)^{\mathrm{th}}$ segments. Low-loss, low-cross-talks crossings are available in silicon photonics [23].

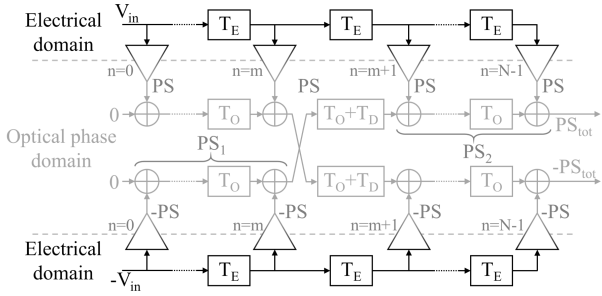

Figure 4.5: Simplified block diagram of both arms of a velocity matched modulator ($\mathrm{T_E}$=$\mathrm{T_O}$) where an additional crossing and delay line are incorporated between the m^{th} and $\mathrm{m}+1^{\mathrm{th}}$ segments.

We now determine the phase shift $\mathrm{PS_{tot}}$ at the output of the top arm. All phase shifts introduced after the crossing can still be added together to obtain a total phase shift $\mathrm{PS_2}$ of (N-m-1)×PS. Before the crossing, the individual phase shifts can also be added, but because of the crossing, the sign is inverted. This yields a negative phase shift $\mathrm{PS_1}$ for the top arm of -(m+1)×PS. So we obtain:

$$\mathrm{PS_{tot}} = (\mathrm{N}-\mathrm{m}-1)\mathrm{PS} - (\mathrm{m}+1)\mathrm{PS}\cdot\mathrm{z}^{-1} \tag{4.17}$$

The crossing and delay lines introduce additional delays. This had to be adjusted to obtain the same delay as when only a delay line without crossing is inserted between two segments. Similar to the delay-line-only case, the position of the crossing determines the tap weights while the length of the delay line determines $\mathrm{T_D}$. Furthermore, the delay from Fig. 4.4 and crossing from Fig. 4.5 can be used on different locations to obtain higher-order transfer functions with both positive and negative taps. The maximal order transfer function is limited to the number of segments minus one, the sum of the absolute values of the tapweights will always be equal to the total number of segments and the smallest value in which a tap can be adjusted is one over the number of taps.

As outlined at the beginning of this subsection, several simplifications were used in this block diagram approach. We can now adjust Eq. (4.12) from subsection 4.2.1 to incorporate the FIR filtering without the simplifications. For each segment, an additional phase factor is required to account for the added optical delay between that segment and the last segment, as the reference position to combine all phase shifts is this last segment. An additional sign is required to account for the arm in which the phase shift was introduced. We

obtain the following adjusted equation:

$$V_{tot} = \frac{1}{N}\sum_{n=0}^{N-1}\frac{\exp(-j\beta_o(N-1-n)L - jT_d D(n))}{1+sR_M C_M}(-1)^{C(n)}V_n \tag{4.18}$$

with D(n) and C(n) the number of delay lines and crossings that follow on the n^{th} segment. Note that each crossing also includes a delay line. We assume all delay lines to have the same delay $\mathrm{T_D}$. The total induced phase shift (in radians) between both arms can still be calculated using Eq. (4.13).

4.3 Design of a shaped slow-wave modulator

A slow-wave modulator operating in the C-band is designed on imec's iSiPP50G technology platform [24] to validate the concept, the electro-optic modeling and the design procedure. The electrical characteristics of both the transmission line pieces and the phase shifters have been simulated using ADS Momentum. Those simulation results are combined afterwards to obtain the electro-optic response of the slow-wave modulator. First, we will briefly discuss the design of the standard modulator, then we will apply and analyze the FIR filter technique.

4.3.1 Standard slow-wave modulator design

Using ADS Momentum, a piece of differential transmission line was simulated. The S-parameters from this simulation are exported to extract the differential characteristic impedance and differential propagation factor. From this, the ABCD matrices of all transmission line segments can be derived for an arbitrary length. The length of the electrodes can be easily adjusted afterwards without having to resimulate, the other dimensions are fixed when simulating in ADS. To incorporate the phase shifter with the cross section given in Fig. 4.6(a), the impedance can be measured and fitted on the equivalent electrical circuit of Fig. 4.6(b). However, as no measurement was available in our case, a phase shifter with the cross section of Fig. 4.6(a) was simulated using ADS Momentum. The doped layers are modeled as conductors, the conductivity is provided in the platform documentation. As the simulator cannot fully model a carrier-depleted PN-junction, the depletion region is modeled as a gap between the P and N doped layers which is filled with silicon dioxide. The width of the gap is adjusted to obtain the correct junction capacitance for a certain reverse bias voltage. This junction capacitance is also provided in the platform documentation. The gap behaves like a parallel plate capacitor, as the width (40-60 nm for a reverse bias between 0 and 2 V) is typically much lower than the height of the doped layers (220 nm). The dimensions of the

doped layers are identical to the default phase shifter as provided in the process design kit (PDK). The impedance found in the ADS simulation is fitted onto the equivalent electrical network from Fig. 4.6(b). Where L_s is the contacting inductance, C_P resembles parallel capacitance over the phase shifter, R_{PN} and C_{PN} resemble the resistance towards the PN-junction and the actual junction capacitance, C_{BOX} the buried oxide capacitance and R_{SUB} the substrate resistance. This equivalent network is combined with the transmission line parameters to calculate the full slow-wave modulator response. Note that Eq. (4.4) and Eq. (4.9) should be adjusted to accommodate the network of Fig. 4.6(b).

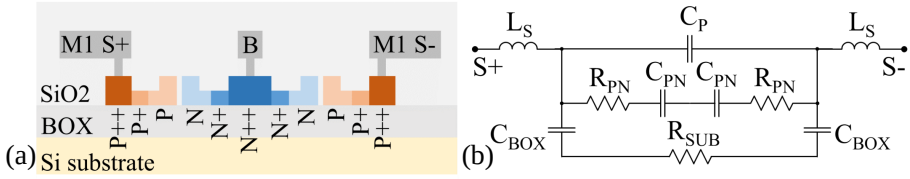

Figure 4.6: (a) Cross section of the simulated segment with the SPP phase shifters. (b) Equivalent electrical schematic for the cross-section in (a).

The phase shifter with the cross section of Fig. 4.6 is simulated with a length of 100, 150 and 200 µm in ADS. Each time a fit with the equivalent network has been made. For a fixed gap width (i.e. fixed reverse bias voltage), C_P, R_{PN}, C_{PN}, C_{BOX}, R_{SUB} were proportional to the segment length and L_s was independent on segment length. This allows to optimize the segment length based on the developed equivalent network without having to resimulate the segment in ADS.

The unloaded transmission lines and segments were combined and transmission line dimensions and segment length were optimized to obtain a high-bandwidth modulator with a matched input: a differential characteristic impedance of 100 Ω, minimal attenuation and a phase index close to 4.26, to velocity match the electrical and optical wave. The group index of the C-band optical waveguide is 4.26. Furthermore, there should be sufficient place between two subsequent segments to insert the delay and crossing. In our case, this is at least 75 µm. The optimal dimensions for both the traveling-wave electrodes and the phase shifter segments are shown in Fig. 4.7. The PN-junctions are simulated for a reverse bias voltage of 0 and 2 V. For the optimization, we assume a reverse bias of 2 V.

The phase shifter segments are 175 µm long and have a pitch of 250 µm, this provides a tradeoff between modulation efficiency, characteristic impedance, attenuation and phase index. Shorter segments result in a higher characteristic impedance and lower attenuation, but also a worse modulation

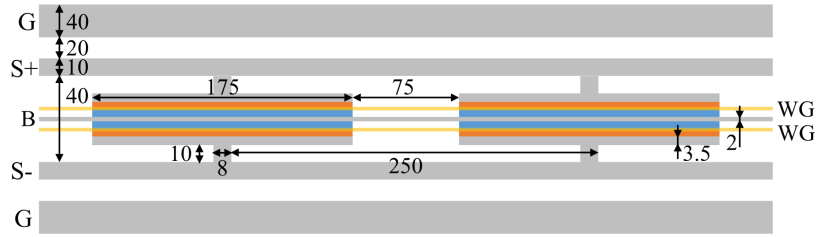

Figure 4.7: Dimensions of segments and traveling-wave electrodes of the modulator. All dimensions are in μm.

efficiency. The simulated characteristic impedance of the loaded transmission line is around 75 Ω, as shown in Fig. 4.8. While this is lower than the intended 100 Ω differential impedance, when properly terminated this will still yield a low reflection coefficient. The phase index of the electrical signal is close to the group index of the optical signal, being 4.26.

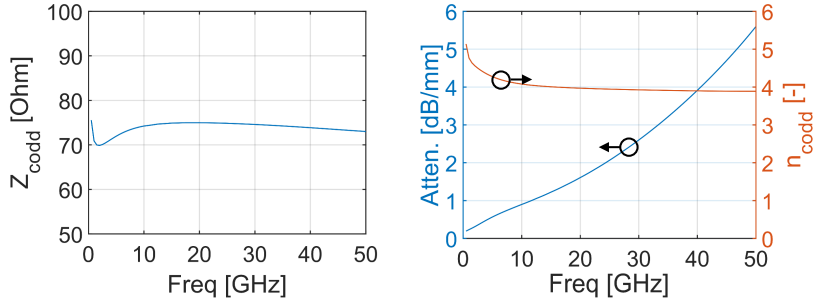

Figure 4.8: Differential characteristic impedance, microwave attenuation and phase index of the slow-wave modulator with the electrode layout of Fig. 4.7.

For the standard slow-wave modulator design, we chose a modulator with 10 segments. Thus the total modulator length is 2.5 mm of which 1.75 mm effective phase shifters. The $V_\pi L_\pi$ of the phase shifters is 24.6 V.mm at a reverse bias of 2 V at 1550 nm, resulting in a V_π of 14 V. The optical attenuation of the phase shifters is 1.5 dB/mm, thus a total insertion loss of 2.6 dB is expected. Given the characteristic impedance of 75 Ω, a differential termination impedance of 70 Ω is chosen. The simulated electro-optic response of this configuration is given in Fig. 4.10 ("Standard" curve). The 3 dB bandwidth is 30.6 GHz and the simulated input reflection coefficient (for a 100 Ω source impedance) is below -15 dB up to 50 GHz.

4.3.2 Embedding FIR filtering

As explained in section 4.2.2, by adding optical delay lines and crossings between subsequent phase shifting segments, a FIR filter can be created. An implementation of how such a delay line and crossing can be implemented is shown in Fig. 4.9. The delay lines are implemented using the PDK strip waveguides. The C-band waveguides have a low loss of 0.14 dB/mm. The PDK crossings feature 0.3 dB insertion loss and -30 dB crosstalk. Remark that no other changes are required, thus the electrical part of the modulator is untouched.

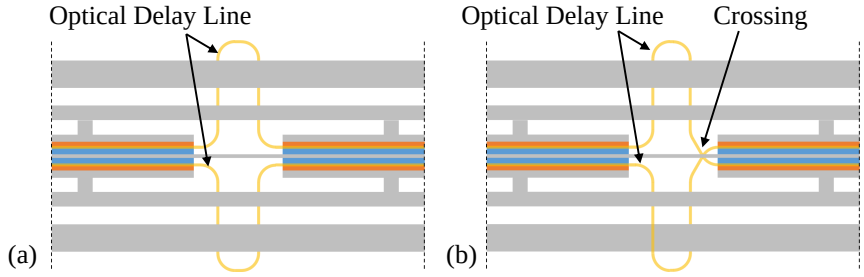

Figure 4.9: (a) Implementation of a delay line between two segments, (b) implementation of a delay line and crossing between to segments.

In order to demonstrate the effect of the FIR filter, the slow-wave modulator designed in the previous section is adapted. The simulated electro-optic response for the standard modulator and modulator with the crossing on various positions is given in Fig. 4.10(a). In all three cases, the delay line length is 500 µm, which is equivalent to 7 ps. Using the block-diagram approach of section 4.2.2, we can derive the transfer function for the various crossing positions. When the crossing is between the 1^{st}-2^{nd}, 2^{nd}-3^{rd} and 3^{rd}-4^{th} segments, the transfer functions are respectively $9\text{PS} - \text{PS} \cdot \text{z}^{-1}$, $8\text{PS} - 2\text{PS} \cdot \text{z}^{-1}$, $7\text{PS} - 3\text{PS} \cdot \text{z}^{-1}$. Thus placing the crossing further down the modulator increases the negative tap in the FIR filter, which results in more peaking but also a lower DC-response. This is confirmed in the simulation of Fig. 4.10(a). By adjusting the delay line length, the peaking frequency can be shifted. This is demonstrated in Fig. 4.10(b). The crossing is placed between the 2^{nd}-3^{rd} segments and the delay length is swept from 250 µm to 1000 µm. All electro-optic responses in Fig. 4.10(b) have been normalized at 1 GHz to ease comparison. By increasing the delay line length, the peaking frequency drops as expected. By adjusting the crossing position and the delay line length, both the amount of peaking and the peaking frequency can be controlled.

A popular way to enhance the bandwidth of traveling wave modulators is

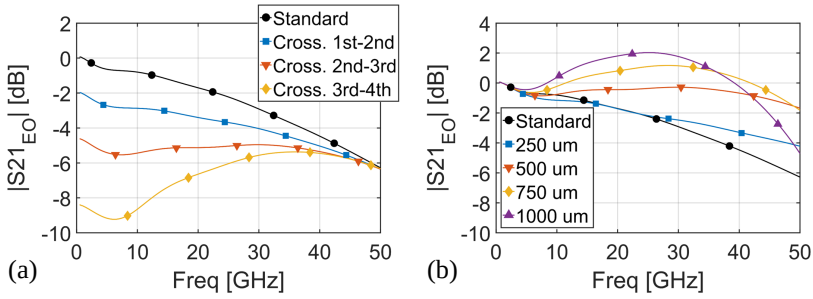

Figure 4.10: (a) Simulated electro-optic response for the standard modulator, for a crossing between the 1^{st}-2^{nd}, 2^{nd}-3^{rd} and 3^{rd}-4^{th} segments (delay line length 500 µm). (b) Normalized Electro-optic response of the modulator with crossing between the 2^{nd}-3^{rd} segments for various lengths of delay line. All simulations assume a reverse bias of 2 V.

by lowering the termination impedance [2]. To compare with our technique, we have simulated the standard modulator and the modulator with a crossing between the 1^{st}-2^{nd} segment. Both the FIR filter technique as well as lowering the termination impedance impose a penalty on the modulation efficiency. To compare, we have lowered the termination impedance of the standard modulator from 70 Ω to 46 Ω in order to obtain the same penalty as placing a crossing between the 1^{st}-2^{nd} segment. The resulting electro-optic responses are shown in Fig. 4.11(a). With the crossing and optimized delay line (750 µm), the electro-optic bandwidth is 43.7 GHz, compared to 42.9 GHz with the lower termination impedance. Both cases provide a significant improvement compared to the original standard modulator (30.6 GHz). However, the response obtained by lowering the termination impedance shows 1.5 dB peaking, while the response obtained by FIR filtering is much smoother. Moreover, by adjusting the termination impedance, the input impedance of the modulator shows significant variation ($> 25\%$), see Fig. 4.11(b). This complicates integration with a driver while also affecting the driver performance. If even higher bandwidths are required, the FIR filter technique can be easily adjusted while lowering the termination impedance will lead to excessive peaking and variations in input impedance.

In our technique, the accuracy of the tap weights and number of taps are limited by the number of segments. Furthermore, the filter is fixed in the layout. Electrical feed-forward equalizers can provide high accuracy tap weights, scale better to more taps and are reconfigurable. However, as the FIR filters are integrated in the modulators, they can take over the electrical equalization partially or completely in certain cases to provide a power and area-efficient

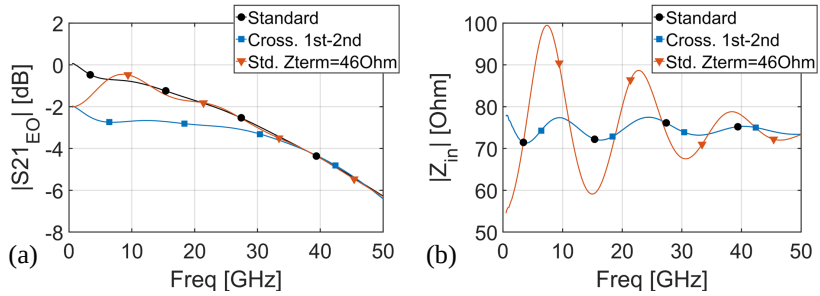

Figure 4.11: (a) Electro-optic response for the standard modulator, modulator with a crossing between the 1^{st}-2^{nd} segments and standard modulator with lower termination(b) Input impedances of the modulators used in (a). All simulations assume a reverse bias of 2 V.

way of equalization.

4.3.3 Final designs and electro-optic characterization

Two designs have been manufactured in imec's iSiPP50G platform [24], both are shown in Fig. 4.12(a). The standard design and a shaped design which includes a crossing between the 3^{rd}-4^{th} segments and a delay between the 4^{th}-5^{th} segments. The realized transfer function is $6\text{PS} + \text{PS} \cdot \text{z}^{-1} - 3\text{PS} \cdot \text{z}^{-2}$, while the delay line length is 500 µm (7 ps). The simulated electro-optic responses are shown in Fig. 4.12(b). The 3 dB bandwidth of the standard modulator is 30.6 GHz. The shaped modulator introduces 4.8 dB peaking at 25.7 GHz.

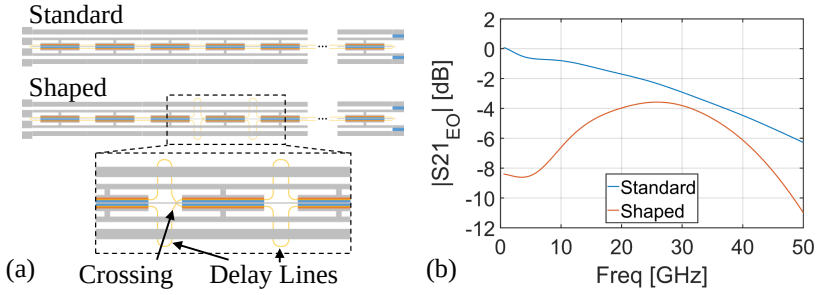

Figure 4.12: (a) Layout of the fabricated designs (b) Simulated electro-optic response of the designs in (a) for a reverse bias of 2V.

The manufactured devices are shown in Fig. 4.13. Both feature the GSSG

driving scheme, the separate biasing line for the PN-junctions, the 70 Ω on-chip termination (OCT) and thermo-optic heaters to bias the modulator at the quadrature point. The insets show the details of the crossing and delay lines. As these were partially hidden below the metal, a view of the designed layout is given.

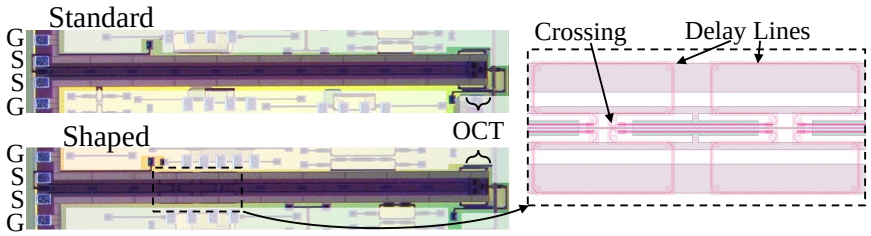

Figure 4.13: Micrograph of the layout of both modulators with an inset of the crossing and delay.

The measured V_π at a reverse bias of 1 and 2 V is respectively 11.8 and 14.0 V for the standard modulator, while being 29.6 and 35.1 V respectively for the shaped design. From the FIR transfer function, it can be observed that only 4 segments are actually contributing in DC instead of 10. This results in a V_π that is 2.5 times higher. Note that if a lower negative tapweight is used, the V_π penalty will be lower. The insertion loss at a reverse bias of 1 and 2 V is respectively 2.6 and 2.5 dB for the standard modulator while being 3.1 and 3.0 dB respectively for the shaped modulator. The additional insertion loss of the shaped modulator is attributed to the delay lines and the crossings.

The measured electro-optic response of the standard and shaped modulator at a reverse bias of 0 and 2 V is given in Fig. 4.14. The agreement between the simulations and measurements is good. Only for the standard modulator at lower frequencies, there is some deviation. We expect that this is caused by the termination impedance that is slightly higher than expected, causing this additional ripple and roll-off in the low-GHz region. Increasing the termination impedance from 70 Ω to 90 Ω in simulation results in a much better fit. The bandwidth of the standard modulator is 21 GHz at 0 V and 25.1 GHz at 2 V reverse bias. The shaped modulator has 3.2 dB peaking at 23.2 GHz at 0 V reverse bias and 4.8 dB peaking at 23.8 GHz at 2 V reverse bias.

4.4 Transmission Experiment

To finalize, we briefly go through a C-band transmission experiment using 56 Gb/s non-return-to-zero (NRZ) data (PRBS 2^{15}-1) and compare the per-

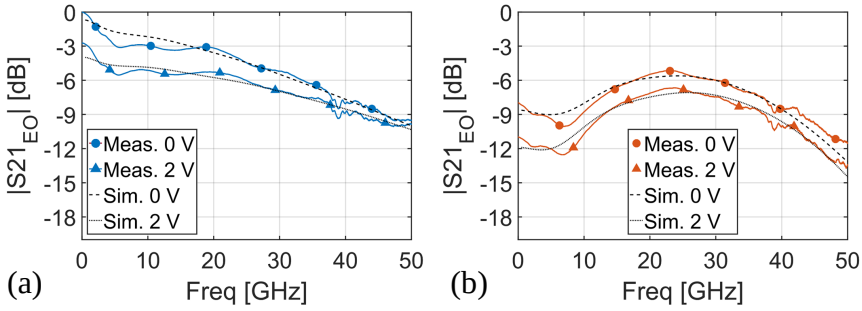

Figure 4.14: Measured and simulated electro-optic response of the standard modulator (a) and the shaped modulator (b). The EO-response of the standard modulator is normalized to 0 dB at DC, all other EO responses are referenced to this response.

formance of the standard and shaped design. Due to the bandwidth limitation imposed by chromatic dispersion, it is expected that the shaped design will have a lower bit-error-rate (BER) in the dispersion limited case. The experiment setup is shown in Fig. 4.15.

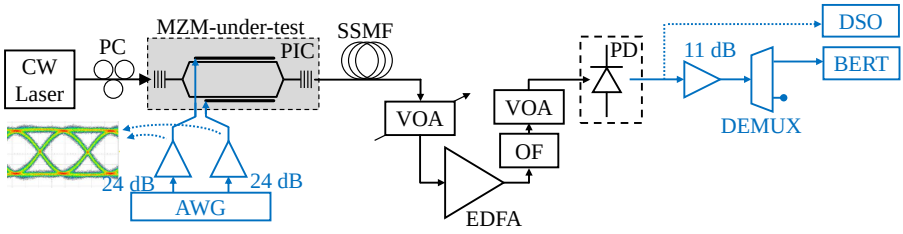

Figure 4.15: Experiment setup for the transmission experiment. CW: continuous-wave laser, PC: polarization controller, AWG: arbitrary waveform generator, VOA: variable optical attenuator, OF: optical filter, DSO: digital sampling oscilloscope, BERT: bit error rate-tester

A laser is set to emit 13 dBm of power at 1550 nm. The light is sent into the PIC through a polarization sensitive grating coupler, a polarization controller is used to minimize the insertion loss. The AWG generates a differential NRZ signal, the amplifiers boost this to 4 $V_{pp,diff}$ for a 100 Ω differential load. The simulated input impedance of our MZM is around 70 Ω, thus the voltage at the input of the modulator will be around 3.3 $V_{pp,diff}$. The average power launched into the fiber is around 1 dBm. The 12 dB insertion loss is caused by the grating couplers (2x3 dB), the modulator biased at quadrature (3 dB) and

the insertion loss of the phase shifters (3 dB). Fiber reaches of 0, 2 and 3 km were used. A VOA before the EDFA is used to control the input power. The EDFA, optical filter (1.2 nm BW), VOA and 70 GHz photodiode (PD) act as a reference receiver. The signal is sent to a DSO to capture the eye diagrams, or demuxed into 2x28 Gb/s of which one stream is used for BER analysis. The 11 dB linear, broadband amplifier with 67 GHz bandwidth is used to amplify the signal before demuxing.

In Fig. 4.16, we have cascaded the measured electro-optic response of the modulators with the analytical transfer function of a chromatic dispersive channel from [25]. The dispersion parameter used for the simulation was 17 ps/(nm.km) at 1550 nm, fiber loss was omitted to ease the comparison. At the Nyquist frequency of the 56 Gb/s signal, thus 28 GHz, the response of the standard modulator cascaded with 3 km fiber has dropped 10 dB with respect to the DC value. While the response of the shaped modulator and 3 km fiber only dropped by 3 dB with respect to its corresponding DC value, thanks to the additional peaking.

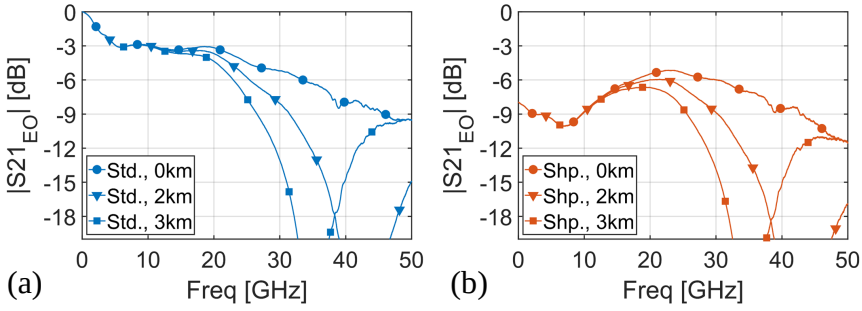

Figure 4.16: Cascade of the measured electro-optic response of the modulator and the simulated fiber channel (0, 2 and 3 km fiber) for the standard modulator (a) and the shaped modulator (b). The EO-response of the standard modulator is normalized to 0 dB at DC, all other EO responses are referenced to this response. The modulators were biased at 0 V.

The measured eye diagrams and BER measurements for the standard and shaped modulator over 0, 2 and 3 km fiber are shown in Fig. 4.17(a) and (b). The average optical receive power is measured at the input of the EDFA. The reverse bias was 0.5 V to optimize the extinction ratio. As could be expected, the eyes of the shaped modulator are smaller due to the lower modulation efficiency, but they do show more peaking resulting in a cleaner eye after 3 km fiber. This is also observed in the BER measurements: at low optical receive powers, the link is noise limited such that the standard modulator has a better BER. The power penalty between the standard and shaped modulator without

fiber (0 km) is slightly higher than 4 dB at a BER of 3.8×10^{-3}. At these low powers, the BER is dominated by the SNR and not by ISI. As the noise is identical in both cases, this 4 dB difference can be traced back to the 4 dB (factor 2.5) difference in V_π between the standard and shaped modulator. At higher optical receive powers and longer fiber reaches (2 and 3 km), the peaking of the shaped modulator results in a significantly better BER.

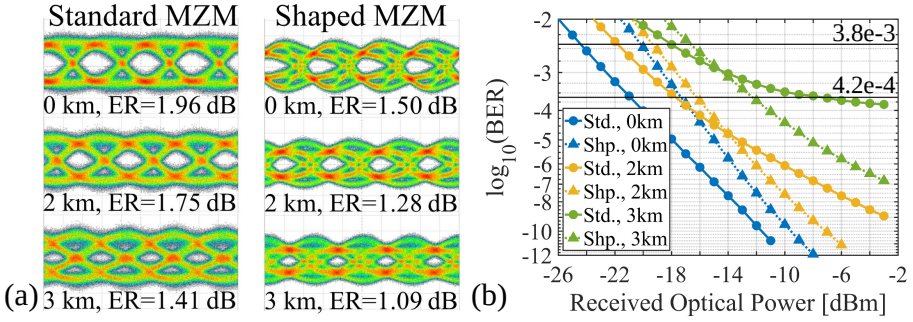

Figure 4.17: (a) Measured eye diagrams at 56 Gb/s NRZ, (b) corresponding BER measurements as a function of average receive power.

4.5 Conclusion

In this chapter, we described how FIR filters can be embedded in slow-wave Mach-Zehnder modulators by adding optical delay lines and optical crossings between phase shifter segments. The proposed technique does not require any changes to the electrical part of the modulator, nor does it require additional processing. Simulation models were devised to analyze and design shaped slow-wave MZM designs. Various cases were considered and compared to show how the response of the modulator could be optimized. A standard and shaped MZM were designed in imec's iSiPP50G silicon photonic platform to verify the modeling approach. Finally, a C-band transmission experiment with 56 Gb/s NRZ data over 3 km fiber was conducted to compare a standard and shaped modulator. The shaped modulator was designed to introduce peaking in order to counteract the bandwidth limitation of the fiber chromatic dispersion. Eye diagrams and BER measurements show the advantage of adding shaping in the MZM.

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Part II

Mach-Zehnder Modulator Drivers

5

Four channel limiting Mach-Zehnder Modulator driver

While the previous part of this dissertation covered optical devices, this part focuses on the driving electronics. The requirements on a high-voltage swing, high-speed operation and a low-power consumption create a challenging design environment for electrical driver integrated circuits (ICs). A carefully designed driver might yield good results, but thorough co-design between the driver and modulator is key to maximize the performance. This can be done in the high-speed regime by e.g. optimizing the impedances at the interface or absorbing interconnection parasitics. But equally important is the DC regime, where we can for example apply the bias voltage for the phase shifters via a separate contact on the photonic integrated circuit (PIC), relaxing the output voltage range of the driver IC. In chapter 3, the design of a silicon photonic Mach-Zehnder modulator (MZM) was discussed. Certain design choices were made in order to optimize the interfacing between driver and modulator. Here, we'll discuss the design of a four channel differential driver where each channel can operate at 53 Gb/s non-return-to-zero (NRZ) and deliver 2 $V_{pp,diff}$ swing over a 100 Ω differential load. The driver output is matched to this 100 Ω differential impedance. All channels can be DC-coupled to the modulator. Through a digital control block, the driver output swing is adjustable and peaking can be added to both the input and output. A well-chosen biasing scheme allows to apply an independent termination voltage to the modulator to further optimize the performance.

Later in this chapter, we will demonstrate a 2-bit electro-optic digital-to-analog converter (DAC) using this driver and the modulator from chapter 3. We'll show that a switching (so 2-level, non-linear) driver and a segmented modulator provide a competitive PAM-4 transmitter in terms of both baudrate and power consumption compared to transmitters employing linear drivers. Using switching output stages helps to keep the power consumption low while the modulator segmentation helps to reach high baudrates.

5.1 Introduction

The block diagram of the driver is shown in Fig. 5.1. It features a input stage with 100 Ω differential impedance followed by a continuous time linear equalizer (CTLE). The CTLE introduces peaking to counteract bandwidth limitations at the input, i.e. from the printed circuit board (PCB) traces leading up to the IC or caused by the bondwires. The duty-cycle distortion (DCD) block is incorporated in the CTLE and cancels potential offset induced by device mismatch and layout asymmetry. The predriver classically serves as the buffer towards the output stage. The output stage has adaptable swing to fine-tune the levels in e.g. a 2-bit electro-optical DAC and can introduce a limited amount of peaking.

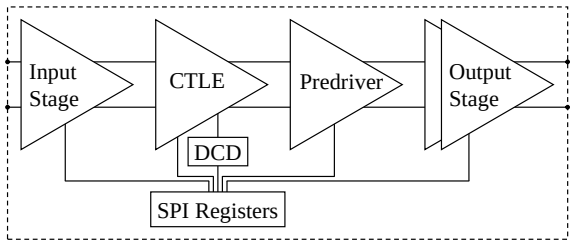

Figure 5.1: Block diagram of a single driver channel with the input stage, CTLE, DCD, predriver and output stage. All blocks are controlled through the SPI registers.

Various parameters of the high-speed blocks are controlled by digital settings in the serial peripheral interface (SPI). Each channel can be independently adjusted. This block contains all the registers for all channels.

5.2 Output Stage Considerations

Given the challenges on swing, speed and power consumption in output stages, quite some work has been put into optimizing towards these requirements

[1–10]. A first important distinction is whether a distributed or lumped output stage is selected, see Fig. 5.2. In a lumped architecture, the output stage works as one large amplifier that directly drives the load. A distributed architecture consists of a cascade of small amplifiers that are interconnected using transmission lines. While a distributed amplifier is superior in terms of bandwidth and voltage swing [1–4], thanks to the parasitics of the small cells that can be absorbed in the transmission lines, they are very power hungry and occupy quite some area. Especially the interconnecting transmission lines, which are sometimes replaced by inductors to obtain an artificial transmission line architecture, require quite some expensive chip area. Given the high bit rate requirement of 53 Gb/s, the moderate voltage swing of 2 $V_{pp,diff}$, the low-power requirement, the availability of high-speed transistors, and the fact that we want to integrate four channels on a die, a lumped driver is a more attractive option.

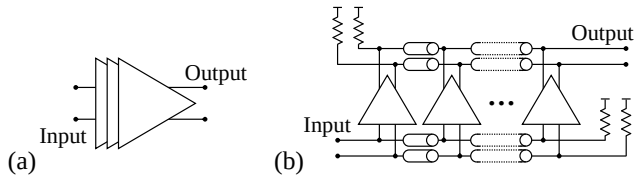

Figure 5.2: (a) Illustration of a differential lumped driver and (b) a differential distributed amplifier.

Most lumped driver designs use a current steering topology as they can achieve high bandwidths [5–11]. Two fundamental circuits are shown in Fig. 5.3: the output stage with back termination (a) and with open-collector circuit (b). The differential modulator is simplified to two lumped resistors R_M. In the topology with back termination, the current is split over the internal termination R_T and the modulator R_M. If both are equal (typically 50 Ω), the swing is divided by two. The open-collector configuration seems much more attractive, as all the current goes to the modulator. Thus a good power efficiency can be obtained [6, 8]. However, this structure is very sensitive to packaging interconnections and load impedance variations. If relatively long interconnections exists, reflections from the load towards the driver are not absorbed by the driver, but reflected back. If a back termination is present, the reflections from the load towards the driver are absorbed at the driver side such that they cannot cause any further distortion.

We prefer a back-terminated driver, as this is a more flexible solution: it is not specifically designed for a certain interconnect or load impedance. As such, good performance is still possible with longer interconnects or other modulators.

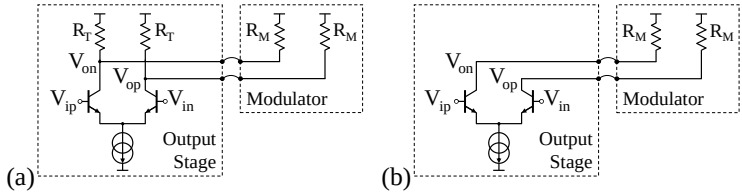

Figure 5.3: Current steering output stages with back termination (a) and with open-collector (b).

Using clever changes, the performance can be further optimized. Cascodes can be added to divide the output voltage swing over both transistors and achieve higher output voltage swings without risking breakdown [7], see Fig. 5.4(a). The cascode transistors can even be driven [10], see Fig. 5.4(b). Remark that additional cascodes come at a certain cost in power: to preserve sufficient voltage headroom, the power supply voltage has to be increased. The cascodes can also be used in an open-collector circuit. A last variation is the switched emitter follower [7, 9], in which the terminations are replaced by emitter followers to boost the high-speed performance at the cost of gain, see Fig. 5.4(c).

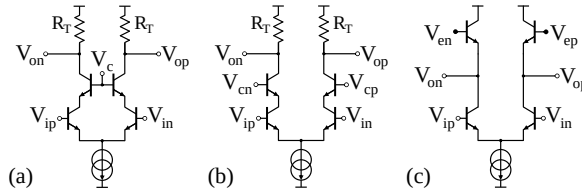

Figure 5.4: (a) Cascoded output stage. (b) Output stage with driven cascoded. (c) Switched emitter follower output stage.

Given the high-speed and relative high breakdown voltage, we opt to design our driver in a 55 nm SiGe bipolar CMOS (BiCMOS) technology [12]. The heterojunction bipolar transistors (HBTs) feature an f_t of 320 GHz. As we aim for a voltage swing of 2 $V_{pp,diff}$, the breakdown voltage of the HBTs is sufficiently large such that no additional cascoding is required. We will employ inductive peaking [13] and capacitive degeneration [11] as low-power means to optimize the bandwidth.

A simplified schematic of the output stage with DC-coupled modulator is shown in Fig. 5.5. The full schematic with simulations will be discussed in section 5.3.3. We prefer DC-coupling over AC-coupling as it doesn't require additional series capacitors to be inserted in the data path. These can harm the

performance due to additional parasitics. Furthermore, with AC-coupling, all DC-current flows through the internal 50 Ω back termination instead of being split over the back termination and the load. As a minimal collector voltage is required at the HBTs, the power supply voltage has to be increased to account for the larger voltage drop over the back termination. Consequently, the power consumption rises.

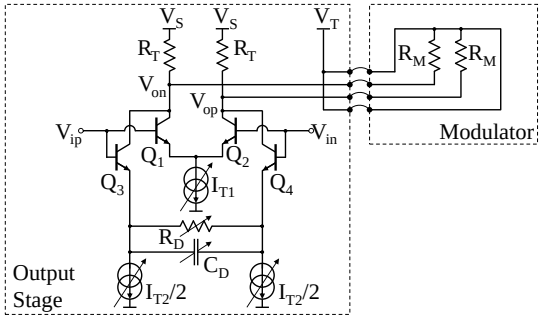

Figure 5.5: Simplified schematic of the output stage with the dual differential pairs connected to a simplified differential modulator. R_T and R_M are 50 Ω.

In order to obtain 2 $V_{pp,diff}$ swing over a 50 Ω load (100 Ω differential) and taking into account the back termination, a total tail current of 40 mA is required. Since binary signals will be generated, the differential pair can be switched without having to worry about linearity. The current is split over two differential pairs, each having a tail current of 20 mA. The pair Q_3-Q_4 introduces additional peaking through the emitter degeneration formed by R_D and C_D. By decreasing the tail current of the standard pair I_{T1} and by increasing the tail current of the degenerated pair I_{T2}, more peaking can be introduced in the total response while the output voltage swing is kept constant. As a high resolution current DAC can be used for I_{T1} & I_{T2}, the peaking can be tuned with high accuracy without affecting the high-speed performance. Ideally, the degeneration would be in series with the emitter of Q_3 and Q_4. However, given the substantial current, this would cost additional voltage headroom. Therefore, the tail current source was split.

Another important point is the voltage connected to the load, see Fig. 5.5. In contrast to most circuits where the load is connected to the same supply as the output stage, we connected the load to a separate supply voltage V_T. In the event that R_M deviates, the common-mode output voltage of the stage changes which may lead to suboptimal performance. In that case, V_T can be adjusted to optimize the performance. If this additional degree of freedom is not required, V_T can be connected to V_S externally. Sufficient decoupling is added on-chip to the V_T net in order to have a well-defined return path for the AC-signals inside the IC.

Given the 2 $V_{pp,diff}$ swing, the minimal voltage at V_{op} and V_{on} is $V_S - 1V$. Assuming the tail current sources need at least 500 mV to function well and we need a V_{CE} of at least 1 V, then we require a power supply voltage of 2.5 V. Consequently, the power consumption of the output stage itself will be around 100 mW. The collector voltage should not drop too far below the base voltage to avoid additional distortion and slew. As V_C is around 1.5 V, an input common-mode voltage of 1.4-1.5 V is required.

5.3 Chip implementation

The driver architecture and output stage architecture are now fixed, so we can shift our attention to the actual implementation. The driver is designed in a 55 nm SiGe BiCMOS technology [12]. HBTs are used in the data path, given their superior high-speed performance. The MOS transistors will mainly be used for biasing circuits and control.

5.3.1 Input Stage and Continuous Time Line Equalizer

The input stage circuit, consisting of two emitter followers is given in Fig. 5.6. The main goal of this part is to act as a buffer and provide a differential 100 Ω input impedance to interface with the preceding signal generation blocks. The resistors R_{iT} are each 50 Ω. These resistors also provide the base currents to Q_1 and Q_2. The dimensions of the transistors are chosen to let them operate near maximal f_T, I_{iT} is 2 mA. With this configuration, AC-coupling is most simple since the transistors are biased through R_{iT}. However, DC-coupling with a correct common-mode voltage (i.e. equal to the 2.5 V supply) is also possible.

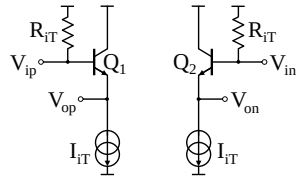

Figure 5.6: Driver input stage with 100 Ω differential termination.

Interconnections leading up to the IC, such as connectors, PCB-traces and bondwires, can already impose a bandwidth limitation. Therefore, the CTLE is added to introduce peaking and alleviate such bandwidth limitations. Getting a large eye-opening is critical at this point, as the subsequent predriver and output stage will be fully switching. Signals with insufficient bandwidth being

fed into predriver and output stage will result in a large amount of jitter, which is very hard to compensate for.

The circuit of the CTLE is shown in Fig. 5.7. It consists of two differential pairs, Q_1-Q_2 and Q_3-Q_4, both with emitter degeneration. They have the same degeneration resistor R_D but Q_1-Q_2 has a larger degeneration capacitance C_{D1}. So Q_1-Q_2 introduces quite a lot of peaking while the pair Q_3-Q_4 introduces only a very small amount of peaking. Using Q_5 to Q_{12}, the relative contributions of Q_1-Q_2 and Q_3-Q_4 to the output can be tuned. In a default case, the voltage V_{LEp} is low and V_{LEn} is high, such that the signal from Q_1-Q_2 is rerouted to the supply and the signal from Q_3-Q_4 goes to the output. Thus almost no peaking is present at the output signal. By increasing V_{LEp} and decreasing V_{LEn}, the pair Q_1-Q_2 contributes more to the output signal such that more peaking is present at the output signal while Q_3-Q_4 contributes less. By increasing V_{LEp} and simultaneously decreasing V_{LEn} with the same amount, the DC current in the termination resistors R_T remains the same. Thus the common-mode output voltage remains fixed. In the most extreme case with maximal peaking, no contribution of Q_3-Q_4 is present at the output.

An alternative solution would be to use a single differential pair and directly tune the capacitive degeneration. The disadvantages of such a capacitor bank is that there is quite some parasitic capacitance causing more peaking in the 'off'-state. As peaking induces group delay variations, undesired peaking can lead to additional jitter. Furthermore, fine digital tuning over a large range (in Fig. 5.7, C_{D1} and C_{D2} are 35 and 500 fF respectively) requires a large number of capacitors, leading to even more parasitics. In the proposed circuit, the control voltages V_{LEp} and V_{LEn} can be generated with a high accuracy and without affecting the high-speed performance of the circuit. The cost is a slightly higher circuit complexity and a DAC with sufficiently high accuracy is required.

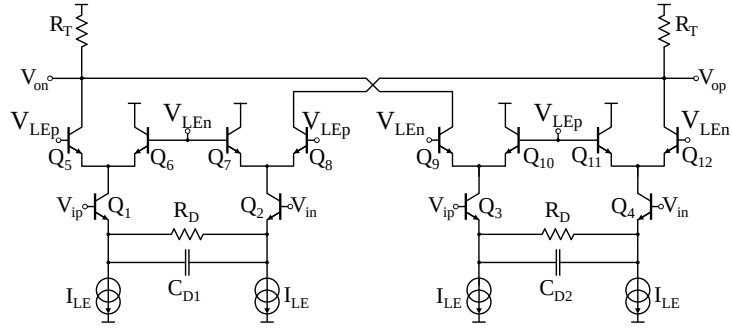

Figure 5.7: Continuous time line equalizer using a Gilbert-cell architecture with two differential pairs having different emitter degeneration (C_{D1}>C_{D2}).

The circuit in Fig. 5.8 demonstrates how the voltages V_{LEp} and V_{LEn} are generated using a differential current DAC. When the term a is zero, virtually no current flows through Q_p and all current flows through Q_n such that V_{LEn} is high and V_{LEp} is low. When a increases, V_{LEn} decreases and V_{LEp} increases causing more peaking. A 7-bit IDAC is used to generate the differential currents aI_B and $(1-a)I_B$, thus a high tuning resolution is obtained. The circuit allows to generate a constant common-mode voltage $((V_{LEp}+V_{LEn})/2)$ such that the transistors Q_1-Q_4 in Fig. 5.7 remain properly biased. The actual common-mode voltage is nominally around 2.2 V (for $a = 0.5$) and is determined by the current I_B, which is 150 µA, the sizing of Q_p and Q_n and the resistor R_E.

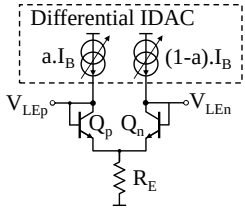

Figure 5.8: Generation of the control voltages V_{LEp} and V_{LEn} for the CTLE.

In Fig. 5.7, the tail current sources I_{LE} generate 2 mA of current. The termination resistance R_T is 170 Ω, while R_D is 150 Ω. The capacitances C_{D1} and C_{D2} are 500 fF and 35 fF. Simulation results over various peaking settings are shown in Fig. 5.9. The voltage transfer function from the driver input to the output of the CTLE is shown from minimal peaking to the maximum of 10 dB in steps of approximately 2 dB. The peaking frequency is 15 GHz. Note that this simulation already contains a 200 pH bondwire and bondpad parasitics at the input stage.

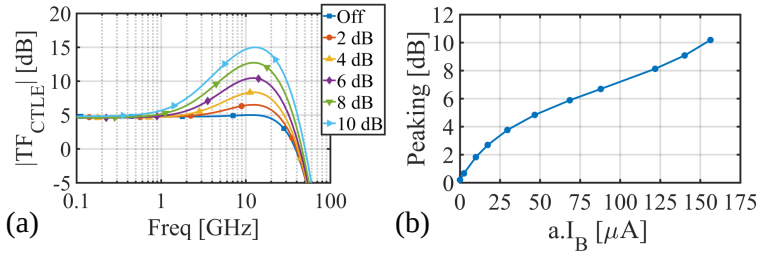

Figure 5.9: (a) Voltage transfer function from the input of the driver channel to the output of the CTLE for various peaking settings. (b) Peaking as a function of the current from the differential IDAC in Fig. 5.8.

Before the signal is fed into the predriver, the offset between the differential lines is adjusted using the DCD. Offset can be caused by asymmetry in layout, e.g. a voltage drop in the power supply between the left and right side of a differential pair, or due to device mismatch. As we employ limiting amplifiers, this offset is amplified and causes additional distortion. To compensate this, the DCD circuit of Fig. 5.10 is used. The circuit comprises a tunable current source $\mathrm{I_{OF}}$, a differential pair of metal-oxide-semiconductor (MOS) transistors and HBT-cascodes. By enabling $\mathrm{M_1}$ or $\mathrm{M_2}$, the offset current is subtracted from one of the signal lines. Since these lines are connected to the output of the CTLE, the current causes a voltage drop over the termination resistors $\mathrm{R_T}$ (see Fig. 5.7). As such, the voltage on the positive or negative line can be decreased to tune the differential offset at the output of the driver to zero.

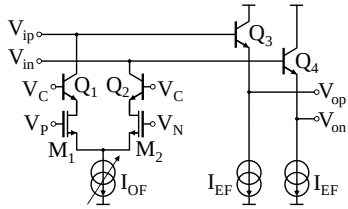

Figure 5.10: Duty cycle distortion circuit subsequent to the CTLE.

The current source $\mathrm{I_{OF}}$ is a 4-bit current DAC capable of generating a maximal current of 1.5 mA. Given the 170 Ω termination, this results in an offset compensation range from -250 to +250 mV in 17 mV steps. The HBT-cascodes help shielding the biasing part from the high-speed part. The emitter followers act as a buffer towards the predriver, but also help lowering the common-mode output of the CTLE, which is around 2.1 V, to more suitable levels for the predriver. The emitter followers are each biased with 2 mA.

Next to offset correction, the circuit can also be used to induce offset. For example, if an MZM has an insufficient extinction ratio (ER), the modulator bias can be slighly shifted from the quadrature point closer towards the minimum-transmission point. This results in a slight increase in insertion loss and an asymmetric eye-crossing. By introducing additional offset in the driver, the asymmetry introduced by the MZM can be precompensated. This principle is shown in Fig. 5.11. Without any offset, see (a), the eye is amplified by the limiting amplifier while the eye-crossing remains in the middle of both levels. In (b), the DC-voltage of $\mathrm{V_{OP}}$ is dropped, causing the eye-crossing to shift upwards. Remark that without any offset circuit, and in the presence of offset due to layout asymmetry or device mismatch, the output eye of Fig. 5.11(b) would be observed at the output of the driver. By adding the offset circuit, the eye-crossing can be tuned to counteract the effect of the present offset in order to reach the situation in Fig. 5.11(a).

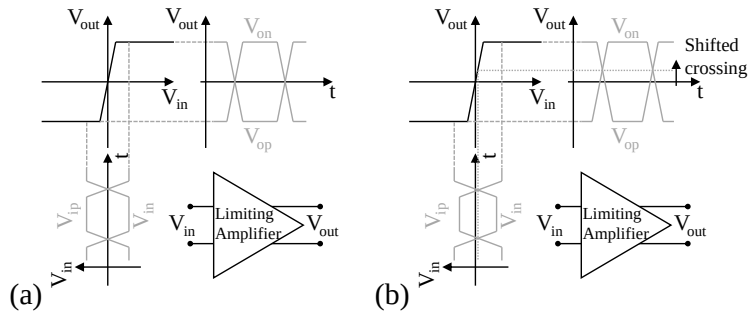

Figure 5.11: (a) Standard operation of a limiting amplifier (b) Adding offset to one signal to shift the eye-crossing.

5.3.2 Predriver

Next, the signal is boosted by the predriver before it is passed on to the output stage. As the output stage has quite large transistors, the predriver serves as a buffer while also ensuring that the output stage receives the optimal voltage swing at its input. Practically, the predriver and output stage are designed together in order to reach optimal designs. Hence, note that some results already rely on the output stage.

The predriver schematic is shown in Fig. 5.12. The tail current $\mathrm{I_{PRE}}$ and termination resistors $\mathrm{R_{T1}}$ and swing are chosen to obtain the optimal swing for the output stage, in this case 800 $\mathrm{mV_{pp,diff}}$. During the switching operation of the output stage, quite some current has to be sourced (or sunk) to the output stage, therefore, the predriver is biased with a sufficient tail current $\mathrm{I_{PRE}}$ of 10 mA. The termination resistors $\mathrm{R_{T1}}$ are chosen to be 40 Ω. As the output stage imposes a large capacitive load on the predriver, $\mathrm{R_{T1}}$ should be kept low to ensure the bandwidth of the predriver is sufficiently high. The 40 Ω resistor in combination with the 10 mA tail current are sufficient to obtain the required swing to drive the output stage. The resistor $\mathrm{R_{T2}}$ helps lowering the output common-mode voltage of the pre-driver. As already explained at the end of section 5.2, an input common-mode voltage of 1.5 V is desired. Without $\mathrm{R_{T2}}$, the output common-mode would be 2.3 V (2.5 V supply minus the DC current through the 40 Ω $\mathrm{R_{T1}}$). A higher common-mode voltage supplied to the output stage would cause the collector voltage of the transistors to drop below the base voltage, causing the HBTs to saturate and cause distortion. Therefore, a 80 Ω resistor $\mathrm{R_{T2}}$ is inserted to obtain a common-mode output voltage of 1.5 V. Note that if a 1.7 V supply would be available, e.g. using a high-efficiency on-chip DC-DC converter, $\mathrm{R_{T2}}$ could be omitted, saving 8 mW in power consumption. Good decoupling is required in this circuit at node A to avoid a high common-mode gain in the driver.

An alternative solution would be to use emitter followers to lower the common-mode output voltage. However, to supply the switching currents, the tail current required for the emitter followers is quite high, resulting in a higher power consumption than the technique used in our predriver.

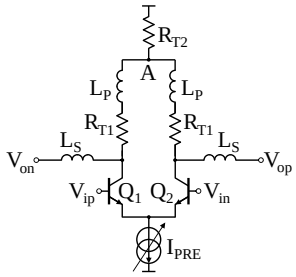

Figure 5.12: Schematic of the predriver stage

To be able to adjust the swing and common-mode output voltage in the final design, the current source I_{PRE} is made adjustable. The default current is 10 mA but can be adjusted between 0 mA and 16 mA in steps of 1 mA.

In order to reach the desired bandwidth, both shunt- as well as series peaking is employed [13]. First, we add shunt peaking by placing L_P in series with R_{T1} and sweeping L_P from 0 to 250 pH. The resulting voltage transfer function of the predriver is shown in Fig. 5.13(a). Note that the predriver is already loaded with the output stage. The flattest response is obtained at 150 pH, at 200 pH about 1.1 dB of peaking at 22 GHz is obtained. This increases further to 2.3 dB when L_P reaches 250 pH. The 3 dB bandwidth reaches a maximum of 48.3 GHz at 200 pH. According to [13], a maximal bandwidth enhancement of a factor 1.84 is to be expected. In our case, the bandwidth without shunt peaking is approximately 24 GHz, so we can expect a maximal bandwidth of 44.2 GHz, which is very close to our final result. Remark that these simulations are schematic simulations, the bandwidth and peaking are expected to drop after layouting due to additional parasitic capacitances on the interconnections. So we select 200 pH as our shunt inductance.

Next, we sweep L_S from 0 to 150 pH to optimize the series-peaking. Due to the relatively large size of the output stage, we cannot directly connect the output of the predriver to the input of the outputstage. An interconnection will be at least 50 µm, so the case with $L_S = 0$ is actually not realistic. Furthermore, since this concerns the interconnection between the predriver and output-stage, it makes more sense to analyze their combined transfer function or the transfer function of the complete data path. The transfer function of the full data path, including bondwires is shown in Fig. 5.13(b). For all subblocks, i.e. input stage, CTLE, predriver and output stage, the schematics are used. Thus

some changes are to be expected after layout. With L_S zero, around 0.9 dB of peaking is already present while the 3 dB bandwidth is 29.9 GHz. By increasing L_S to 100 pH, the peaking increases to 1.7 dB with a 3 dB bandwidth of 30.6 GHz. A higher series peaking inductance introduces more peaking at the cost of bandwidth. Therefore, the series peaking inductance of 100 pH is selected.

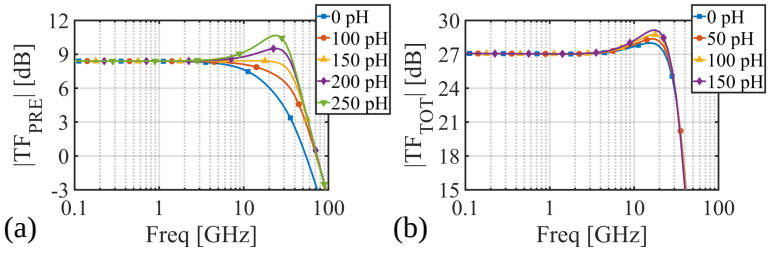

Figure 5.13: (a) Effect of adding shunt peaking (L_P swept, $L_S = 0$) on the transfer function of the predriver. (b) Effect of adding series peaking (L_S swept, $L_P = 200$ pH) on the total driver transfer function.

To confirm that these component values do not introduce excessive jitter, transient simulation were used to confirm that this jitter is within bounds.

5.3.3 Output stage

The architecture of the output stage was already discussed in section 5.2. Now, we cover the circuit implementation more in detail. The full schematic is shown in Fig. 5.14. As described earlier, the resistors R_T are 50 Ω, the total tail current is 40 mA of which 20 mA is supplied by I_{T1} and two times 10 mA by I_{T2}. Both I_{T1} and I_{T2} are tunable in steps of 1 mA up to 32 and 16 mA respectively, this helps to control the swing and to introduce peaking.

Let us first take a closer look to the tunable degeneration, the circuits are shown in Fig. 5.15. The tunable capacitor in Fig. 5.15(a) consists of NMOS transistors connected as capacitors in a 4-bit capacitor bank. The digital control voltages V_{Cdc0}, V_{Cdc1}, V_{Cdc2} and V_{Cdc3} drive the gates of 1, 2, 4 or 8 devices in parallel, to obtain a binary weighted DAC. The control voltages are 0 or 2.5 V. Gate-control was chosen over drain/source-control as this yields a higher difference between the on and off capacitance. As stray capacitances scale with the device width, a small W and large L was chosen to maximize the difference between C_{on} and C_{off}. Since the common-mode voltage over the capacitor terminals is relative low, around 500 to 600 mV, NMOS devices were chosen over PMOS devices as a much larger V_{GS} can be applied to the NMOS

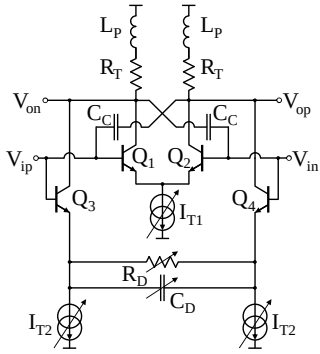

Figure 5.14: Schematic of the output stage

devices, yielding a higher $\mathrm{C_{on}}$. The total capacitance between $\mathrm{V_{Cdp}}$ and $\mathrm{V_{Cdn}}$ can be tuned between 60 fF and 390 fF with an accuracy of 4-bit, resulting in steps of 22 fF. By default, the lowest capacitance is used. After measurements, it was found that the capactive degeneration did not create as much peaking as expected. Upon further investigation, we found that a wrong model was used to determine the capacitance of the NMOS transistor. The finite transit time of carriers inside the channel was incorrectly modeled. With the correct models, the maximal capacitance drops from 390 fF to 260 fF at 10 GHz and to 140 fF at 30 GHz. This is not an immediate problem, as there are sufficient other means to induce some additional peaking (resistive degeneration, tuning the tail currents). However, when redesigned, care should be taken to ensure correct models are used. With proper sizing, a similar maximal capacitance can be obtained.

The tunable resistor is created using a fixed resistor in parallel with a NMOS transistor in triode. By switching the gate of $\mathrm{M_1}$, the resistance between $\mathrm{V_{Rdp}}$ and $\mathrm{V_{Rdn}}$ can be switched between 20 and 30 Ohm. Default, the lowest resistance is used.

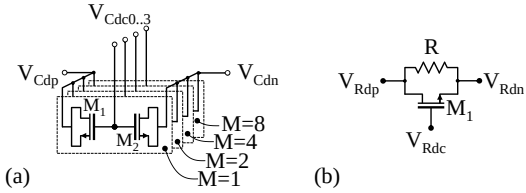

Figure 5.15: Circuit implementation of the tunable capacitor $\mathrm{C_D}$ (a) and tunable resistor $\mathrm{R_D}$ (b) from Fig. 5.14.

The effect of the various values of R_D and C_D on the total transfer function of the modulator is shown in Fig. 5.16(a). The circuit has been simulated with 200 pH bondwires and a 100 Ω differential load. As expected, increasing C_D causes the peaking to increase from 1.1 dB to 1.8 dB. Increasing R_D causes the peaking to increase even further (up to 2.4 dB when C_D is maximal), but at the cost of DC-gain. However, we drive the output stage in a switching regime, so the concept of DC-gain is somewhat alien. Nevertheless, increasing the resistance at the emitter causes the V_{BE} voltage of the HBT to decrease. Such that a higher input voltage is required to fully switch the differential pair. As such, increasing R_D will cause a small decrease in signal swing [11]. Thanks to the tunable tail current sources, this decrease can be easily compensated for.

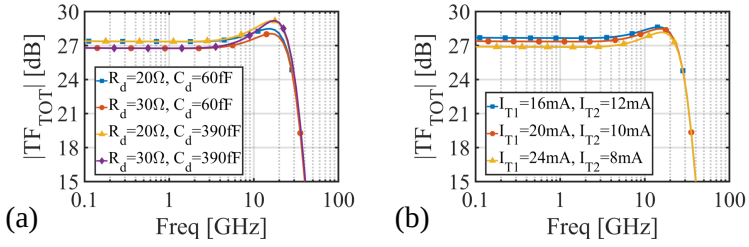

Figure 5.16: (a) Effect of tuning R_D and C_D with the nominal settings for I_{T1} and I_{T2}. (b) Effect of tuning I_{T1} and I_{T2} with the nominal settings for R_D and C_D.

An additional degree of freedom is found in the tail current sources I_{T1} and I_{T2}. Their nominal values are 20 mA and 10 mA respectively to obtain a full tail current of 40 mA leading to 2 $V_{pp,diff}$ swing. By decreasing I_{T1} and increasing I_{T2}, the relative contribution of the degenerated pair increases, leading to more peaking. This effect is demonstrated in Fig. 5.16(b), degeneration is disabled in this case. Nominally, around 1.1 dB peaking is present while the DC-gain is 27.4 dB. By increasing I_{T1} while decreasing I_{T2}, there's less emphasis on the degenerated pair such that the DC-gain increases and the peaking decreases. The other way around leads to a less gain and more peaking.

Looking back to our output stage schematic, Fig. 5.14, cross-coupling capacitors C_c have been used to alleviate the effect of the Miller capacitance. However, care should be taken that C_c does not exceed the Miller capacitance, as this would lead to instability. Additional simulations were carried out to ensure the employed cross-coupling capacitors do not lead to insufficient phase margin. The previous simulations already included the cross-coupling

A last measure to optimize the high-speed performance of the output stage is the shunt peaking introduced by L_P. No series peaking is added, as a 200 pH

bondwire is already present. The data path transfer function, including bondwires, is shown in Fig. 5.17 for various values of L_P. From 100 pH to 200 pH to 300 pH, we'll see the peaking increasing from a mere 0.6 dB to 1.1 dB to 1.9 dB, while the bandwidth increases from 26.8 GHz to 29.4 GHz to 30.6 GHz. As already quite some peaking can be introduced by the degeneration, we'll choose 200 pH to be on the safe side as excessive peaking leads to too much jitter. The previous simulations already include the effect of the selected shunt inductor.

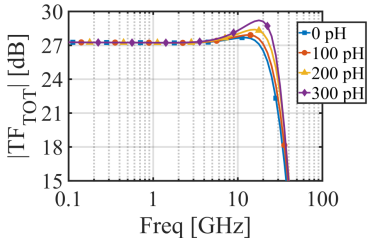

Figure 5.17: Effect of adding shunt peaking to the output stage.

Given the nonlinear behavior of the output stage, transient simulations of the data path were carried out. To assess the effect of the degeneration, various settings were simulated and are shown in Fig. 5.18. Except for R_D and C_D, all other settings are set to their nominal values. Note that these transient simulations are carried out on the schematics, so post-layout effects are not included yet. The input signal swing was 400 $mV_{pp,diff}$ in all cases, and an output swing of approximately 2 $V_{pp,diff}$ is obtained in all three cases. In line with earlier conclusions from the AC simulations, we indeed see an increase in peaking when R_D or C_D increase. An increase in jitter, due to the higher group delay variation is also expected. Furthermore, raising R_D indeed leads to a slightly lower swing.

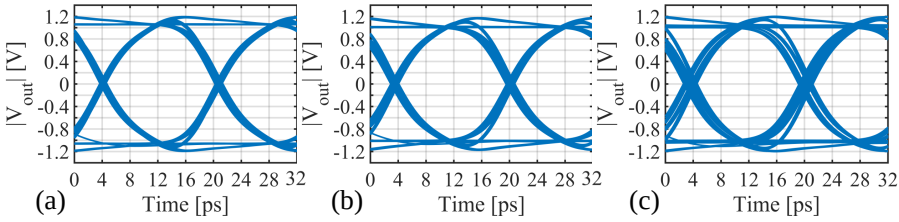

Figure 5.18: Eye diagrams of the driver output at 60 Gb/s at nominal settings for (a) $R_D = 20\ \Omega$, $C_D = 60$ fF, (b) $R_D = 30\ \Omega$, $C_D = 60$ fF and (c) $R_D = 30\ \Omega$, $C_D = 390$ fF.

In Fig. 5.19, the eye diagrams at nominal settings for various I_{T1} and I_{T2} are shown. From (a) to (c), the tail current of the default pair (I_{T1}) decreases while the tail current of the degenerated pair increases (I_{T2}), their sum is kept constant at 40 mA. As expected, the peaking increases and the voltage swing decreases slightly.

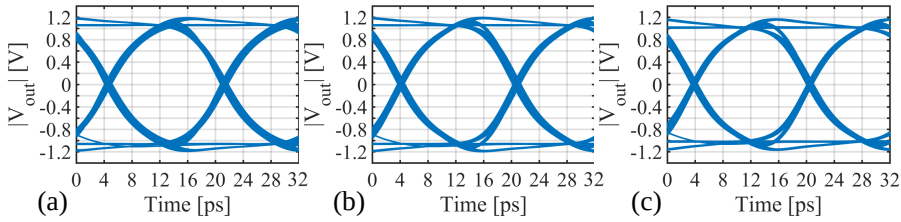

Figure 5.19: Eye diagrams of the driver output at 60 Gb/s at nominal settings for (a) $I_{T1} = 24$ mA, $I_{T2} = 8$ mA, (b) $I_{T1} = 20$ mA, $I_{T2} = 10$ mA and (c) $I_{T1} = 16$ mA, $I_{T2} = 12$ mA.

The tail current sources need to deliver quite some current, two times 10 mA to the degenerated pair and 20 mA to the standard pair. To minimize the power consumption of the biasing network, a high mirror-ratio is desired. Both mirrors are designed to work with an input current of 1 mA. An important design restriction is the low compliance voltage. Nominally, this is set to around 600 mV, but due to process corners, temperature, drops in power supply and predriver settings, this value can quickly decrease below 400 mV. Therefore, a current mirror using a regulated cascode was used [14], as shown in Fig. 5.20. A single-stage opamp was used in this circuit. To minimize the parasitic capacitances at the output node, the thin-oxide MOS transistors were used as these allow a much lower channel length. However, these have a breakdown voltage that is significantly lower than the 2.5 V supply voltage. As the output voltage decreases, the opamp output increases and could cause breakdown. This was thoroughly checked over all corners and no issues were found. When checking the start-up of the full chip, potential issues were detected. To ensure that no breakdown occurs, the MOS transistors M_5 and M_6 were added to avoid that the opamp output voltage exceeds the breakdown voltage.

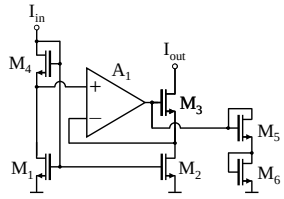

Figure 5.20: Circuit of the tail current mirror using a regulated cascode.

5.3.4 Layout

The layout of a full channel is given in Fig. 5.21. A bondpad pitch of 125 µm is selected and the channels share their ground bondpads with their adjacent channels, so a channel pitch of 375 µm is obtained. The total channel length is 1080 µm, excluding sealring. As the actual high-speed data path is much shorter, only around 350 µm, the remaining distance to the bondpads is covered using transmission lines. The actual output stage measures 220 by 140 µm. The remaining area is covered by power distribution planes and decoupling to ensure that a high quality supply is available throughout the channel.

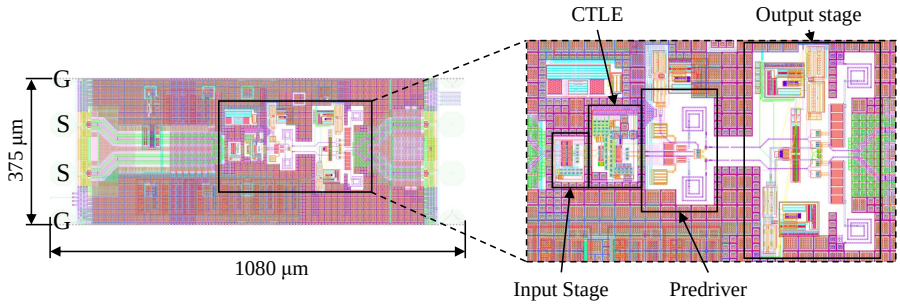

Figure 5.21: Layout of a full channel with an inset of the data path circuitry.

After layout, the additional parasitics can be extracted to verify whether the circuits perform as intended. The transfer functions of the various blocks and the full driver have been simulated using the schematics and the extracted layouts, see Fig. 5.22. All settings are nominal. The input buffer and CTLE show very similar behavior. The predriver has slightly less peaking, likely because additional parasitic capacitances were introduced in layout that were not accounted for in the schematic. However, the deviation is relative small and can be easily compensated for by introducing some additional peaking in the CTLE For the output stage, we see a drop of 1 dB in gain, caused by a higher-than-anticipated emitter resistance. While care has been taken to minimize the trace lengths, some additional trace resistance is always possible, leading to a small drop in gain. As such, the total transfer function shows a slightly lower gain and peaking. The total bandwidth is still 26.2 GHz (while schematic predicted 29 GHz). While this bandwidth seems a bit low for 53 Gb/s NRZ signals, remark that this is the small-signal bandwidth. In the large signal regime, the bandwidth will be larger due to the switching behavior.

We can now also simulate the post-layout transient performance of the driver, the results are shown in Fig. 5.23. This also captures all nonlinear effects in our circuits. The required swing of 2 $V_{pp,diff}$ is clearly obtained, the effect of the slightly lower bandwidth and peaking is limited. While no device

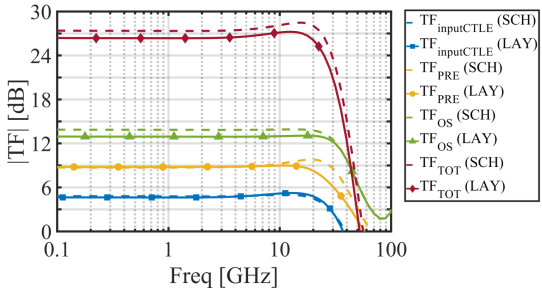

Figure 5.22: Transfer function of the various block before and after layout.

mismatch was assumed in this simulation, we see around 200 mV DC-offset at the output, caused by layout asymmetry. Due to the strong nonlinear behavior of the predriver and output stage, a small input offset is easily converted in a larger output offset. Given the 2 V_{pp} swing, no issues are expected with this offset. However, the DCD circuit can be used to compensate.

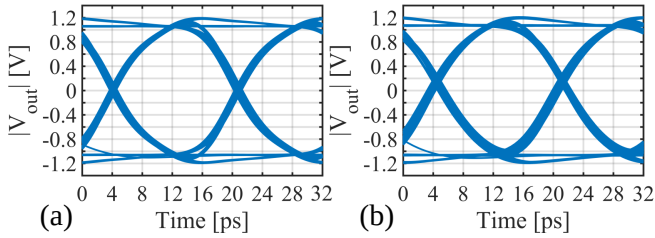

Figure 5.23: Eye diagrams at 60 Gb/s measured at the output of the driver before (a) and after layout (b).

The total power consumption of a single channel operating at a supply of 2.5 V is 180 mW, of which 100 mW in the output stage, 25 mW in the predriver, 30 mW in the CTLE and 10 mW in the input stage. The remainder is used for the biasing network. The power consumption of the full chip is 720 mW.

An annotated micrograph of the chip is shown in Fig. 5.24. The full chip measures 1.2 by 2.5 mm. Note that most features are hidden due to the required metal tiling. Four channels are replicated next to each other. The area at the left and right side is used for power distribution and decoupling. All registers are controlled by the SPI block situated in the bottom right corner.

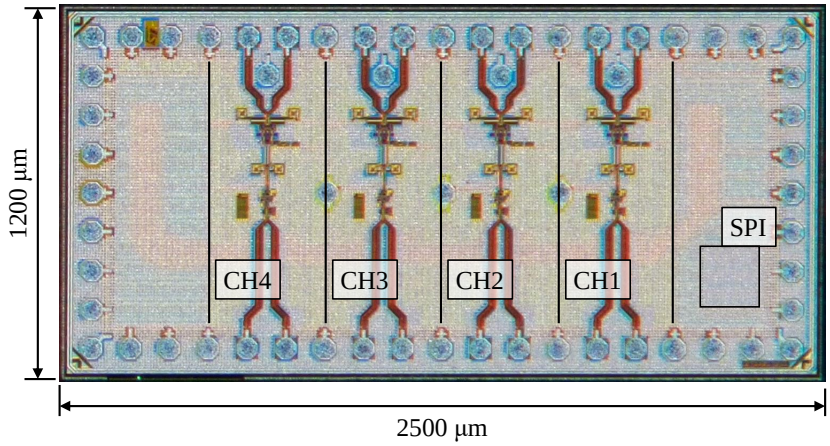

Figure 5.24: Annoted micrograph of the full die.

5.4 Experimental results

The driver IC was used in several assemblies. Here, we briefly cover the electrical characterization of the driver itself and discuss our PAM-4 generation experiments using the modulators from chapter 3. This section is also based on the following publication [15].

5.4.1 Electrical characterization

To perform the pure electrical testing, all DC and control lines of the IC were wirebonded to traces on a PCB while the RF bondpads where probed using a GSSG-probe with 125 µm pitch. The large-signal S-parameters were measured using a vector network analyzer (VNA) and are shown in Fig. 5.25(a). As signals get clipped due to the limiting driver, the large signal gain decreases for increasing signals. Furthermore, as the driver has quite some gain, clipping occurs already for very small input signals. Thanks to this clipping, the bandwidth increases from 34 GHz at -12 dBm to 45 GHz at -4 dBm. The measured differential input- and output impedance are shown in Fig. 5.25(b) at a power of -12 dBm. A good match is obtained over the full frequency band.

The initial eye diagrams are shown in Fig. 5.26. With an input voltage swing of 300 mV_{pp}, clear eyes are obtained at 50 and 56 Gb/s. Every other eye in each diagram is slightly smaller, this is caused by the mux in the signal generator (SHF10001B). The measured voltage swing is around 2 $V_{pp,diff}$, as designed. All settings are nominal, however, the supply voltage was increased to 2.75 V in order to full maximize the performance.

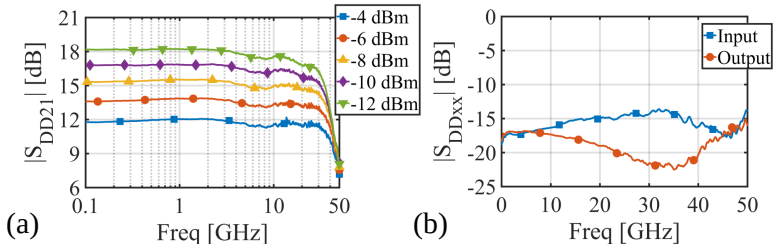

Figure 5.25: (a) Large signal S-parameter measurements on the driver for various input powers. (b) Differential input- and output impedance at an input power of -12 dBm.

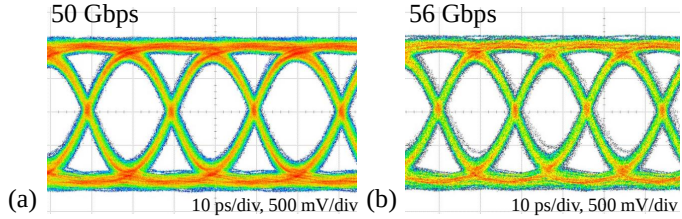

Figure 5.26: Eye diagrams at 50 Gb/s and 56 Gb/s. 10 ps/div and 500 mV/div.

5.4.2 Electro-optical experiments

By combining the driver with the segmented modulator from chapter 3, a 2-bit electro-optical DAC is obtained. As explained in that chapter, by splitting the long traveling-wave (TW) modulator into two shorter TW segments, the total loss on the segment electrodes can be decreased. Hence the bandwidth of each segment is higher than the bandwidth of the initial long TW MZM. Compared to driving a single TW MZM (of length L) with a PAM-4 signal, higher data rates can now be achieved by driving both segments (with a combined length L) using two binary signals. This technique also avoids a linear modulator driver for the long TW modulator. A linear driver consumes more power for the same voltage swing at the same data rate, while also requiring additional equalization to counteract the lower bandwidth of the longer modulator. This segmented approach was already demonstrated in [16]: 50 and 84 Gbaud PAM-4 is generated using a TW MZM with two segments driven by binary signals. However, no dedicated modulator driver is integrated and digital signal processing is used to reach 84 Gbaud. We show >56 Gb/s NRZ and >50 Gbaud PAM-4 generation using a two segment TW silicon photonic MZM co-packaged with a limiting SiGe BiCMOS driver.

The driver was wirebonded together with the modulator on a PCB. This

allows to easily connect all power supplies, control signals and RF-signals without having to probe, see Fig. 5.27. Thanks to the careful co-design, the interface between driver and modulator is only consist of a bondwire with an approximate length of 250 µm. So the high-speed data path contains a minimal amount of parasitics that can deteriorate the performance. The driver power supply V_S and termination of the modulator V_T are kept separate, see Fig. 5.5, in order to independently optimize the collector voltage of the output stage transistors.

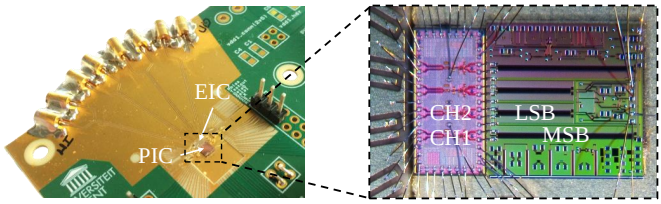

Figure 5.27: Assembly with the driver wirebonded to the modulator. Inputs to the driver are supplied through high-speed connectors

To assess the effect of the integration and the loading of the modulators on the driver channels, the measured large-signal S-parameters of the driver (see Fig. 5.26) were combined with the EO-response measurements of the modulators (see Fig. 3.26). The interconnecting bondwires were assumed to be 250 pH. As such, the whole cascade could be simulated using measured data for the driver and modulators. The results can be found in Fig. 5.28.

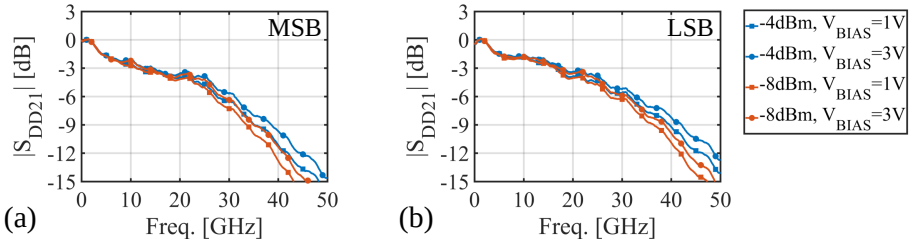

Figure 5.28: Cascade of the measured large-signal S-parameters of the driver with the MSB segment (a) and the LSB segment (b). Each time with an interconnection inductance of 250 pH.

Fig. 5.28(a) shows the cascade of the driver with the MSB segment. At -4 dBm input power to the driver, the bandwidth is between 11.2 and 13 GHz for a reverse bias between 1 and 3 V over the PN junction. However, the roll-off is very slow: the 6 dB bandwidth is 27.6 and 31.1 GHz for a reverse

bias of 1 and 3 V respectively. At 25 GHz, the response dropped between 3.8 and 4.7 dB with respect to DC. Thus by configuring the driver to introduce around 1-2 dB of peaking at 25 GHz, the 3dB-bandwidth of the cascade can be increased to 25 GHz. The results of the cascade of the driver with the LSB segment interconnected using 250 pH bondwires show a similar trend: the 3 dB bandwidth is between 14.8 and 16.8 GHz. The 6 dB bandwidth is 31.6 and 32.7 GHz for 1 and 3 V reverse bias. At 25 GHz, the response dropped only between 3.8 and 4.3 dB with respect to DC, thus 1-1.5 dB of peaking introduced by the driver at 25 GHz is sufficient to obtain a bandwidth of 25 GHz for the full cascade.

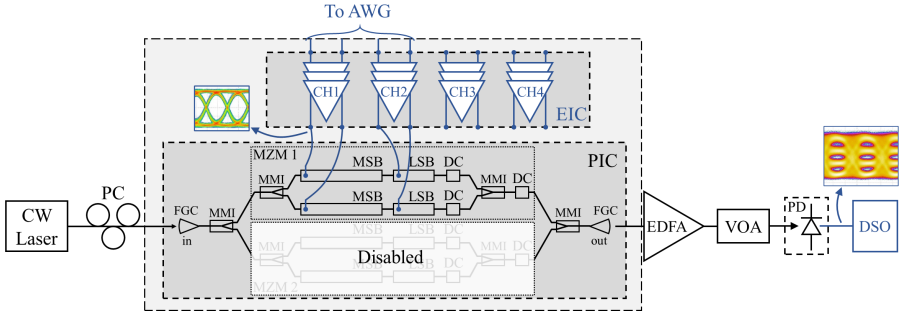

Figure 5.29: Experiment setup: CW laser set to 1550 nm, PC: polarization controller, AWG: arbitrary waveform generator, EDFA: erbium doped fiber amplifier, VOA: variable optical attenuator, PD: DC-coupled 70 GHz photodiode, DSO: 70 GHz digital sampling oscilloscope.

The setup used for our data generation experiments is shown in Fig. 5.29. Only the top MZM is used, the bottom one is biased at minimum transmission. A CW laser is set to 1550 nm and 13 dBm output power. As the fiber grating couplers (FGCs) of the PIC are polarization dependent, a polarization controller is added before the fiber probe. The output of the PIC goes to an EDFA and VOA that amplifies the optical signal to an average power of 8 to 9 dBm, and is then coupled into a DC-coupled 70 GHz photodiode. The total insertion loss of the PIC is around 24.8 dB with a reverse bias of 2 V on the PN junctions, of which 2x5 dB from the FGCs, 2x3 dB because one child MZM is not used, 3 dB because the active MZM is biased at the quadrature point and 5.8 dB attenuation from the PN junctions reverse biased at 2 V. Note that by using more efficient edge couplers (typ. 2 dB loss [17]) and by omitting the unused child MZM, the insertion loss can be improved by 12 dB. With the given laser output power of 13 dBm, this would result in a launch power of 0.2 dBm, which is compliant with both the IEEE 802.3bs 400-GBase DR-4 standard [18] (launch power between -2.9 and 4.2 dBm) and the MSA 400G-

FR4 standard [19] (launch power between -3.3 and 3.5 dBm). The 70 GHz photodiode used in the setup is internally matched to 50 Ω and connected to a 70 GHz digital sampling oscilloscope (DSO). The 92 GS/s arbitrary waveform generator (AWG) generates two identical PRBS15 streams with a Gaussian pulse shape. We have selected the PRBS15 sequence as this is the longest sequence that still fits in the AWG memory. The AWG is set to an output voltage of 400 $\mathrm{mV_{pp,diff}}$.

For the data experiments, the transmitter was first tested by generating 50, 56 and 60 Gb/s NRZ using only one driver channel and the MSB segment (length 2.25 mm). The adjustable input peaking of the driver is used to compensate for the RF attenuation of the cables, connectors and PCB traces. The eye diagrams can be found in Fig. 5.30. The average optical input power to the PD is 8 dBm. For 50, 56 and 60 Gb/s, $\mathrm{V_T}$ and $\mathrm{V_S}$ are 2.75 V. The PN junction was biased around 1 V for 50 and 56 Gb/s to maximize the extinction ratio (ER) by keeping $\mathrm{V_\pi L_\pi}$ as low as possible. As the low reverse bias voltage of 1 V decreases the EO-bandwidth of the modulator, the driver is configured to introduce some peaking at its output. At 60 Gb/s, the driver cannot introduce sufficient peaking, so we increase the reverse bias of the PN junction to 2 V in order to raise the modulator bandwidth. The power consumption of the active driver channel and MZM is 205 mW for 50 and 56 Gb/s, resulting in a power efficiency of 4.1 and 3.7 pJ/bit respectively. At 60 Gb/s, the power efficiency improves to 3.5 pJ/bit.

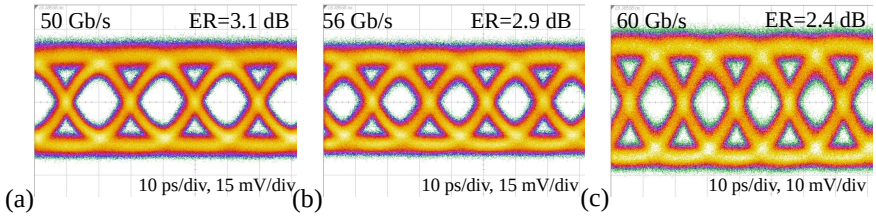

Figure 5.30: Eye diagrams of NRZ generation using the MSB only at (a) 50 Gb/s, (b) 56 Gb/s and (c) 60 Gb/s.

In the next step, both the MSB and LSB segments are driven by the same PRBS15 sequence. The delay between the MSB and LSB is sufficient to decorrelate both NRZ streams for the PAM-4 signal. Some skew is added between the signals to align the edges of the LSB bitstream with the MSB bitstream. In our experiment, this skew was tuned using the AWG, however, delay cells could be added to the driver input to align the edges [20]. In a transceiver, additional control loops will be required to tune both the gain and delay of the MSB. A system similar as demonstrated in [21] could be used. A moni-

tor photodiode can be added to the modulator, the output of this photodiode is typically used to keep the modulator biased at its correct operating point. But it can also be used to align the MSB and LSB and even to calibrate the MSB and LSB signal swing. To quantify the quality of the generated PAM-4 signal, transmitter and dispersion eye closure quatenary (TDECQ) is used [18]. This is a measure of the vertical eye closure of an optical transmitter when the signal is sent through a worst-case optical channel and is measured through an optical to electrical (O/E) converter. It can be shown that TDECQ is roughly proportional to the receiver power penalty [18]. An in-depth discussion about TDECQ can also be found in [22]. The IEEE 802.3bs 400-GBase DR-4 standard and the MSA 400G-FR4 standard require a TDECQ below 3.4 dB [18, 19], the target symbol error rate for minimizing the TDECQ was 4.8×10^{-4}. The complete procedure of determining the TDECQ is done automatically in the Keysight DCA-X 86100D. The eye diagrams at 40 Gbaud before and after the TDECQ processing are shown in Fig. 5.31. During the measurements, no detrimental impact from crosstalk between the MSB and LSB was observed.

The eye diagrams at 40 Gbaud before and after the TDECQ processing are shown in Fig. 5.31. The significant improvement can be explained by the slow roll-off of the electro-optic response of the modulator, which can be readily compensated with the 5-taps feedforward equalizer (FFE). This FFE is part of the TDECQ measurement procedure applied by the measurement equipment. Remark that the FFE has a DC-gain of 1.

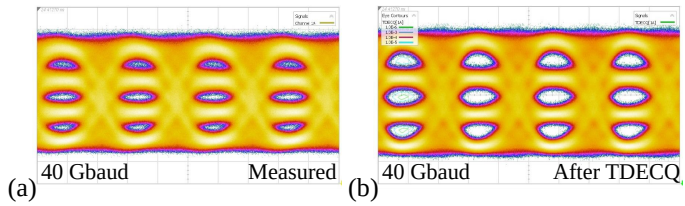

Figure 5.31: 40 Gbaud PAM-4 before (a) and after the 4^{th} order Bessel filter and 5-taps FFE for TDECQ measurements (b). The ER before processing is around 4.5 dB.

The eye diagrams at 40, 50 and 53 Gbaud after TDECQ analysis are shown in Fig. 5.32. Again, V_S was 2.75 V, but V_T and the reverse bias of the PN junction were set to 3.1 V and 3.5 V respectively to maximize the transmitter bandwidth. Compared to a reverse bias of 3 V, this led to a rather modest improvement of 0.1-0.2 dB in TDECQ, leading us to the conclusion that the changes in V_π, loss and bandwidth are very small. Remark that the output swing of the LSB driver channel was optimized to obtain equally-spaced PAM-4 levels, this results in an level separation mismatch ratio (RLM) higher than

0.92 for all cases. The ER was in all cases around 4.5 dB, compliant with both IEEE 802.3bs 400-GBase DR-4 standard [18] and the MSA 400G-FR4 standard [19], both require and ER of at least 3.5 dB. The average optical power on the PD was 8 dBm for 40 and 50 Gbaud and 9 dBm for 53 Gbaud.

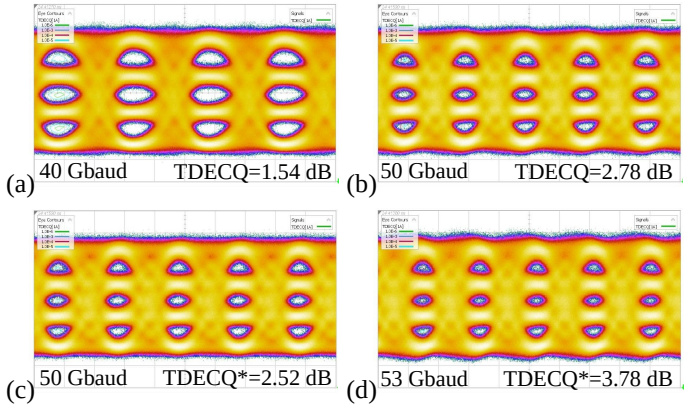

Figure 5.32: Eye diagrams and TDECQ of (a) 40, (b)-(c) 50 and (d) 53 Gbaud. TDECQ* means the PAM-4 thresholds were optimized for minimal TDECQ.

At 40 and 50 Gbaud, the TDECQ is 1.54 dB and 2.78 dB with a total power consumption of 374 and 386 mW. At 40 Gbaud, the MSB and LSB driver channels are consuming 199 mW and 175 mW respectively. While at 50 Gbaud, the MSB and LSB driver channels are consuming 201 mW and 184 mW. The LSB channel is consuming less power as the swing has been slightly decreased to tune the PAM-4 levels and peaking is decreased since the LSB modulator has a higher bandwidth. This results in a power efficiency of 4.7 pJ/bit and 3.9 pJ/bit at 40 and 50 Gbaud. The measurement at 50 Gbaud was redone with TDECQ threshold optimization for the PAM-4 levels. The thresholds were allowed to deviate from their ideal levels over a range equal to 1% of the outer OMA. This improves the TDECQ from 2.78 dB to 2.52 dB. For 53 Gbaud, with threshold optimization, a TDECQ of 3.78 dB was measured, the power efficiency is 3.6 pJ/bit. The driver uses the same settings at 50 and 53 Gbaud, thus the power consumption is identical. Both the IEEE 802.3bs 400-GBase DR-4 standard [18] and the MSA 400G-FR4 standard [19] require a TDECQ below 3.4 dB. While the 40 Gbaud and 50 Gbaud PAM-4 comply, the TDECQ at 53 Gbaud is 0.4 dB too high. However, by redesigning the MZM as explained in chapter 3 the TDECQ can be enhanced.

One of the first steps to enhance the bandwidth would be to lower the termination impedance of the MZM. On one hand, the power consumption decreases as the driver needs to introduce less peaking and V_T can be lowered

to keep the collector voltage of the output stage constant. On the other hand, the lower load impedance causes the voltage swing to drop. This will have to be compensated by increasing the output stage current and hence the power consumption. We expect that these effects will cancel each other out almost completely. By using lower-loss edge couplers and by omitting the unused child MZM, the insertion loss can be decreased. Improving the insertion loss does not affect the driver performance, but enhances the noise performance of the link. These changes should enhance both the OMA at the output of the transmitter as well as the TDECQ such that OMA, TDECQ and OMA-TDECQ specification of the referred standards are all met.

A benchmark comparison to several implementations of optical transmitters employing integrated MZMs co-packaged with drivers is presented in Table 5.1. As can be observed, the transmitter presented in this paper features the best power efficiency for the given data rate. This shows the potential of the electro-optic DAC solution to reach high bandwidths with low power consumption. In [5], a full transceiver is demonstrated at 28 Gbaud PAM-4 using the same BiCMOS technology, only the power of the output stage was taken into account to calculate the efficiency here. The authors of [6] show a very good power efficiency, but reach only up to 40 Gbaud using a linear driver in a 65 nm CMOS technology. However, an open-drain output stage is used. While saving on power consumption, the driver is much more sensitive to interconnection parasitics and variations in the load impedance. A linear driver without modulator is presented in [4]. The driver achieves a similar data rate and swing as our architecture, but at a much higher power consumption. A large-swing linear driver capable of 64 Gbaud PAM-4 and 56 Gbaud PAM-8 is demonstrated in [7]. However, no experiments with integrated MZMs are shown. While a better power efficiency for a higher data rate is obtained for the coherent transmitter with open-collector output in [8], the transmitter has around 3 dB peaking in its EO response, and quite some equalization will be required to flatten this response and avoid degradation in the PAM-4 eye. In the case of [8], this equalization is provided by the digital signal processing required for the coherent experiments. This is undesired for short-reach datacenter interconnects employing PAM-4, as additional equalization increases the total link power consumption and the link latency. No transmission experiments without additional DSP are shown in [8], prohibiting a correct comparison.

Ref.	Implementation Details	Data rate [Gbaud]	Output [$V_{pp,diff}$]	Efficiency [pJ/bit]	Driver Technology
[5]	3 seg. Si TW MZM, flip-chip integrated driver	28	-	5.2	55 nm BiCMOS
[23]	2 seg. Si TW MZM, monolithic integrated driver	28	2.2	4.8	90 nm CMOS
[24]	2 seg. lumped Si MZM, flip-chip integrated driver	28	1	1.59	28 nm CMOS
[6]	Single Si TW MZM, wirebonded linear driver	40	2	2.25	65 nm CMOS
[4]	Linear driver only	56	1.8	7.5	0.25 um InP DHBT
[7]	Linear driver only (PAM-4/PAM-8)	64/56	4.8/3.8	6.4/4.9	55 nm BiCMOS
[8]	InP TW MZM, wirebonded linear driver	64	2	1.4	65 nm CMOS
This work	2 seg. Si TW MZM, wirebonded driver	50	2	3.9	55 nm BiCMOS
		53	2	3.6	

Table 5.1: Comparison between PAM-4 transmitters using integrated Mach-Zehnder modulator and drivers.

5.5 Conclusion

In this chapter, the design of a four channel limiting driver in a 55 nm SiGe BiCMOS technology was covered. The driver is capable of generating 2 $V_{pp,diff}$ signals at bit rates exceeding 50 Gb/s and employs an output stage with flexible tuning of both the swing and the peaking. Furthermore, using a separate biasing line for the MZM PN-junctions, the performance can be further optimized. Each driver channel also includes a CTLE to compensate for bandwidth limitations induced by the connectors, traces and wirebonds leading to the driver. Using a SPI interface, all channels can be controlled separately. A complete driver channel uses approximately 180 mW and 200 mW per channel at a supply of 2.5 V and 2.75 V respectively.

The driver has been integrated on an assembly with the MZM from chapter 3 to demonstrate a 2-bit electro-optical DAC. Using the MSB only, generation of 56 Gb/s and 60 Gb/s NRZ with an ER of 2.9 dB and 2.4 dB was shown. By using both segments, generation of 50 Gbaud PAM-4 and 53 Gbaud PAM-4 can be achieved with a power efficiency is 3.9 pJ/bit and 3.6 pJ/bit respectively. With this work, we have shown the potential of segmenting silicon optical modulators to enhance the bandwidth for high-baudrate signal generation. When combined with limiting drivers, 400G capable short-reach optical interconnects employing PAM-4 with a very competitive power consumption can be obtained.

Future work can focus on several tracks. As mentioned in section 5.4.2, the experiments can be conducted using an improved modulator to fully showcase 53 Gbaud PAM-4 according to established standards. Given that the driver has back termination, experiments using longer MZMs are an interesting option to explore. Furthermore, the experiments can be extended toward 53 Gbaud 16QAM.

At the driver side, certain optimizations are possible. The power consumption of the CTLE can be lowered by redesigning the circuit and avoid half of the tail currents being switched to the supply net. The capacitive degeneration in the output stage should be redesigned using the correct models to improve the peaking of the output stage. An open-collector output stage is a tempting option to lower the power consumption. Switching to such an architecture would enhance the power consumption of a single channel from 180 mW at 2.5 V to 130 mW per channel. Nevertheless, this comes at the cost of a much higher sensitivity to interconnection parasitics and deviations in load impedance. So such a stage has to be designed for a specific assembly and modulator, leading to a suboptimal performance if other MZMs are used.

Additional feedback circuits to control the modulator biasing, MSB-LSB delay and MSB-LSB swing can be integrated into one assembly and into the driver to obtain a more complete optical transmitter. The challenge of this track is to implement these circuits without raising the power consumption and without deteriorating the high-speed performance.

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6

Four channel PAM-4 Mach-Zehnder Modulator driver

This chapter extends our work on Mach-Zehnder modulator driver integrated circuits (ICs) to support PAM-4 modulation. While the 2-bit electro-optic digital-to-analog converter (DAC) solution proposed in the previous chapter provides a power efficient way to generate PAM-4, two NRZ limiting channels are required for one PAM-4 line. As a result, two driver ICs each with four channels are required to support a full 400 Gb/s transmitter. So the solution does not scale well to higher numbers of lines, either parallel fibers or wavelengths. Especially with upcoming 800 Gb/s standards, where first implementations will double the number of lanes compared to 400 Gb/s modules [1]. Furthermore, the coherent 400-GBase ZR standards for inter-datacenter interconnects will employ 60 Gbaud DP-16QAM transmission [2]. Creating such a module with one driver IC in a small package requires four PAM-4 channels on a single IC.

Low-power PAM-4 driver ICs, preferably with four channels, are key to keep up with increasing bit rates and allow highly integrated transmitter modules. Quite some $>$ 53 Gbaud PAM-4 drivers have been shown [3–7]. In [3], 56 Gbaud PAM-4 is demonstrated using an open-drain CMOS driver coupled to a micro-ring modulator (MRM). The driver contains a pattern generator, muxing, biasing control, nonlinear equalization while outputting 3 V_{pp} swing. The total driver power consumption is 676 mW. In [4], eight driver channels, each capable of 53 Gbaud PAM-4 are coupled to MRMs. The same assembly

also contains the eight channel receiver, the required serializers, deserializers, controls and lasers. The drivers consume only 325 mW per channel, excluding additional biasing of the ring modulators. However, both employ ring modulators, which are highly wavelength sensitive and are also not suited to be used for coherent communication. In [5], a 64 Gbaud PAM-4 electrical driver for Mach-Zehnder modulators (MZMs) is demonstrated capable of 4.8 V_{pp} output swing. However, the total power consumption is 820 mW. Similarly, the authors of [6] demonstrate a 64 Gbaud PAM-4 driver with 4.4 V_{pp} swing consuming 1.1 W.

A number of DP-16QAM transmitters employing PAM-4 drivers have been shown as well, [8, 9] show 64 and 69 Gbaud DP-16QAM respectively. The authors of [8] designed a four channel open-drain driver IC, consuming only 225 mW per channel and achieve 1.5 $V_{pp,diff}$ swing. Their assembly however contains an indium phosphide MZM with a very low V_π of only 1.5 V_{pp}. While having a very low $V_\pi L_\pi$ compared to silicon, silicon has a lower cost, higher yield and can be manufactured in high volumes, see also section 2.3.1. Furthermore, the driver shows 5.5-6 dB of peaking and a high group delay variation of around 8.5 ps. In coherent links, this is less of an issue as quite some digital signal processing (DSP) is available to compensate this. Nevertheless, for intra-datacenter intensity modulation and direct detection (IM/DD) interconnects, DSP is minimized as it introduces quite a lot of latency and additional power consumption. The assembly demonstrated in [9] uses two ICs each containing two channels that are assembled with a silicon MZM. For the DP-16QAM experiments at 69 Gbaud, the output swing is 2.4 $V_{pp,diff}$. For the 45 Gbaud DP-16QAM and below experiments, the swing was 6 $V_{pp,diff}$. The power consumption is 1 W per channel.

In this chapter, we will cover the design of a low-power four channel 64 Gbaud PAM-4 driver for MZMs, capable of generating 2 V_{pp} PAM-4 and 3 V_{pp} NRZ over a 50 Ω load (100 Ω differential) with a power consumption of 350 mW. A 2 V_{pp} swing on the modulator designed in chapter 3, yields an extinction ratio (ER) of 4.5 dB. Similar to the previous driver, all channels allow DC-coupling to the modulator to simplify the driver-modulator interface. Tunable peaking is added to partially alleviate input and output bandwidth limitations. A nonlinear circuit block helps precompensating for symmetric compression of the PAM-4 levels. The driver is designed in a 130 nm SiGe BiCMOS technology (f_T of 300 GHz), heterojunction bipolar transistors (HBTs) are used for the data path, while the metal-oxide-semiconductor (MOS) transistors are mainly used for biasing and control signals.

6.1 Introduction

The block diagram of a single driver channel is shown in Fig. 6.1. An input buffer with a 100 Ω differential input impedance takes the signals in. Next, a continuous time linear equalizer (CTLE) is used to introduce up to 7 dB of peaking. Since the complete data path is linear, this peaking can be used to partially counteract bandwidth limitations before or after the driver. This includes for example high-frequency losses due to printed circuit board (PCB) traces or connectors before the driver. But the peaking can also be used to enhance the modulator bandwidth if required. Note that the introduced peaking introduces also additional variation to the group delay (and thus jitter), which eventually deteriorates the performance. The next block operates both as a variable gain amplifier (VGA) and nonlinearity compensation (NLC). As VGA, it ensures that the optimal input voltage is always present at the input of the output stage, the gain can be varied over a range of 6 dB. If the circuit is being used as NLC, the inner PAM-4 levels are compressed. This allows to precompensate for symmetric compression by the output stage and the MZM. The duty-cycle distortion (DCD) block is integrated with the VGA/NLC to compensate for DC-offsets in the data path. Similar to the previous driver, the DCD can also intentionally add offset to counteract duty-cycle distortion induced by an MZM that has been biased off the quadrature point to enhance the ER. The predriver and output stage are integrated into one larger circuit. Through digital settings, the output voltage swing can be finetuned to the desired level.

There are 3 different power nets: the net for the digital controls (SPI registers), the net for the input stage, CTLE and VGA/NLC and the net for the output stage. As the latter requires a higher supply voltage, we chose to separate this from the preceding stages to minimize the power consumption. The digital voltage V_{dig} is 1 V, V_S is 2.5 V and V_{DRV} is 3.4 V.

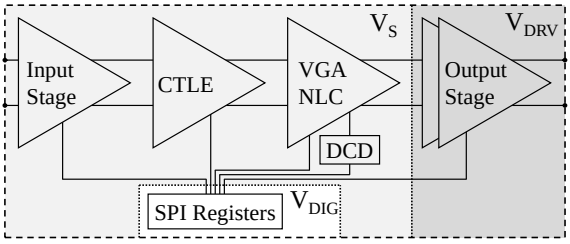

Figure 6.1: Block diagram of a single driver channel with the input stage, continuous time linear equalizer (CTLE), variable gain amplifier (VGA) and nonlinearity compensation (NLC) combined with the duty-cycle distortion (DCD) and the predriver and output stage integrated into one block. All blocks are controlled through the SPI registers.

6.2 Output Stage Considerations

Similar to the previous driver and given the symbol rate of 64 Gbaud, a lumped design is chosen over a distributed design as it allow a smaller footprint and has a lower power consumption. A lumped design should have sufficient bandwidth to support this data rate. Internal back-termination, as shown in Fig. 5.3(a) (page 102) is chosen over an open-collector design to avoid the high sensitivity to interconnection parasitics between the driver and the modulator and the modulator input impedance. While this comes at the cost of an increased power consumption, it allows a higher flexibility in integration and choice of the Mach-Zehnder modulator.

Compared to the previous design, this driver is not operated in a switching regime to ensure a sufficiently high linearity. However, when operated in a switching regime, a higher output swing can be obtained compared to our previous driver. With this driver, we aim at a full swing of up to 3 $V_{pp,diff}$ for NRZ signals. At such high output voltage swings, the collector-emitter or collector-base junction breakdown becomes of concern in the output differential pair. Faster technologies, with a higher f_T, have led to a decrease in breakdown voltages [10]. In this technology, the collector-emitter breakdown voltage in an open base configuration BV_{CEO} is 1.6 V, while the collector-base breakdown for an open emitter configuration BV_{CBO} occurs at 4.8 V. A collector-base breakdown is irreversible and independent of the circuit topology and other operating conditions. When V_{CB} exceeds BV_{CBO} the device breaks down [11]. In contrast, the BV_{CEO} breakdown does depend on circuit topology and exact operating conditions, often V_{CE} may exceed BV_{CEO} while not causing an irreversible breakdown. Using the models from [11], it can be understood that increasing V_C yields an increasing (avalanche) current through the base-collector current. This avalanche current is opposed to the base current for biasing the transistor. When the net base current reaches zero, BV_{CEO} breakdown is reached and biasing instabilities can occur [12]. This definition however applies for an open-base configuration. When a low impedance is present at the base, a bias instability can be delayed such that the breakdown shifts towards higher V_{CE}, denoted as BV_{CER} [9, 11, 13]. Given that we will drive the output stage with a low impedance at the base of the HBTs, a maximum V_{CE} of 2 to 2.2 V is assumed.

To avoid breakdown of the differential pair, additional protection is required. The most straightforward way to implement this is using a cascode, see Fig. 6.2(a). The cascode transistors Q_3 and Q_4 protect the differential pair Q_1-Q_2. However, the cascodes only keep the collector voltage of Q_1-Q_2 (almost) constant. Thus a large portion of the voltage swing is still present on the transistors Q_3 and Q_4. A DC-simulation help visualizing this, see Fig. 6.3(a).

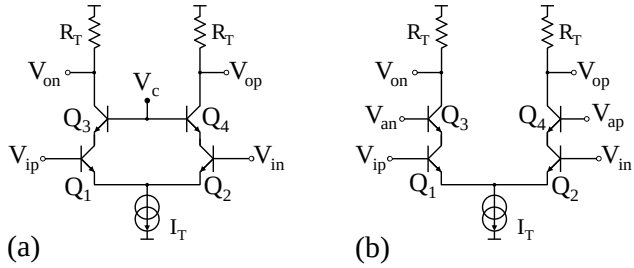

Figure 6.2: (a) Cascoded differential pair to enhance the output swing. (b) Breakdown voltage doubler architecture.

The circuit of Fig. 6.2(a) was simulated with I_T equal to 60 mA, R_T 25 Ω (two times 50 Ω in parallel), a supply voltage of 3.3 V and an ideal current source. As expected, the collector voltage of Q_2 is nearly constant at 1 V (Casc. $V_{C,Q2}$). The associated collector-emittervoltages are plotted in Fig. 6.3(b), which demonstrates that the V_{CE} voltage of Q_2 is in the safe area while most of the output swing is present over Q_4.

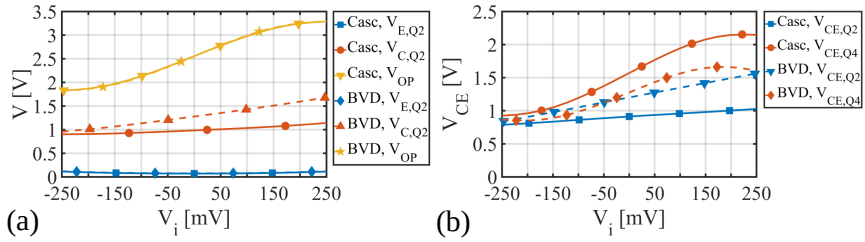

Figure 6.3: DC simulation of a differential input voltage applied to the circuits from Fig. 6.2: (a) Voltage at various nodes, (b) collector-emitter voltages of the Q_2 and Q_4.

A more effective technique is to drive the cascode transistors with a scaled version of the output voltage to divide the full voltage swing over both transistors. This technique is called the breakdown voltage doubler [9, 13, 14]. The circuit is shown in Fig. 6.2(b). An additional amplifier is required to generate V_{an} and V_{ap}, this can be a separate differential pair. Now we can understand that if e.g. V_{op} increases with a certain voltage V while V_{ap} increases with $V/2$, then this increase is divided over the collector-emitters of both Q_2 and Q_4. The same simulation as for the cascode was conducted with the breakdown voltage doubler, the results can be found in Fig. 6.3. In Fig. 6.3(a), we see that the collector voltage of Q_2 is not constant anymore, but rises with increasing output voltage due to the cascode Q_4 being driven. Consequently in

Fig. 6.3(b), the V_{CE} of both transistors increase, but remain well within the safe operating area.

The complete schematic of the breakdown voltage doubler is shown in Fig. 6.4. The differential pair Q_7-Q_8 drives the cascodes Q_3-Q_4 with a scaled version of the output voltage. The emitter followers Q_5-Q_6 act as a buffer for the larger Q_1-Q_2 while also providing a required level shift to keep all HBTs biased correctly.

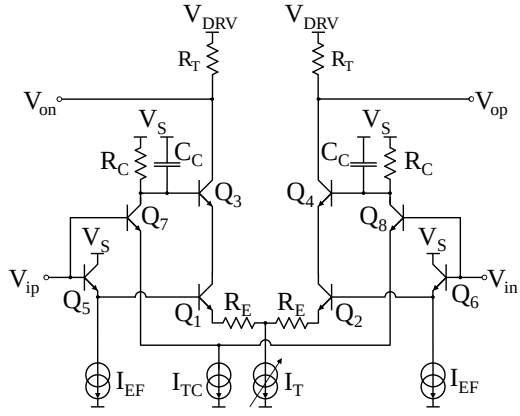

Figure 6.4: Schematic of the breakdown voltage doubler.

To enhance the linearity of the output stage, the resistors R_E are added. The presence of the capacitor C_c might seem counter intuitive, as this slows down the driving circuit for the cascodes Q_3-Q_4. In order to analyze the circuit, it can be split into a main path, formed by the emitter followers Q_5-Q_6 and the differential pair Q_1-Q_2 and an auxiliary path formed by the differential pair Q_7-Q_8 and the cascodes Q_3-Q_4. Furthermore, we assume that both paths have no influence on each other. In reality, this is not entirely true: the signal at the emitters of the cascodes can couple through the base-collector capacitances and modulate the differential pair. As we would like to keep our analysis simple and insightful, we will neglect this feedback path by omitting all base-collector capacitances. Later, when the circuit is implemented, simulations will be used to capture all effects and optimize the circuit response.

The single-ended small-signal equivalent of the main path is given in Fig. 6.5. The emitter follower Q_5 has been replaced by an ideal voltage source and a source impedance R_{s1} equal to $1/g_{m5} + r_{e5}$. Similar for the cascode Q_3, the driving differential pair has been replaced by the resistance R_{s3}. The HBT Q_1 works as a common-emitter amplifier, while the cascode Q_3 serves as a current buffer. Calculating the response and performing some simplifications (e.g. omitting non-dominant poles and zeros), results in the following expression:

$$V_{o,main} = -\frac{R_L}{(1+sR_LC_L)}\frac{g_{m1}}{(1+g_{m1}R_{E1}+s\,(R_{s1}+R_{b1})\,C_{\pi 1})}V_i \quad (6.1)$$

So we find, as expected, a DC-gain of $-g_{m1}R_L$ and two poles: one determined by the input of Q_1 and the other determined by the load. Note that we have absorbed r_{e1} into R_E for readability. We can rewrite this expression by choosing the DC-gain A_{main} equal to ${}^{g_{m1}R_L}/_{(1+g_{m1}R_{E1})}$, expressing the time constants associated with the input pole of Q_1 as τ_1 and the output pole as τ_L:

$$V_{o,main} = -\frac{A_{main}}{(1+s\tau_L)\,(1+s\tau_1)}V_i \quad (6.2)$$

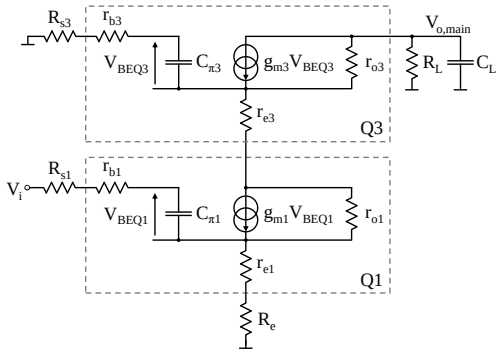

Figure 6.5: Simplified small-signal equivalent circuit of the main path in the breakdown voltage doubler of Fig. 6.4.

Analogously, the small-signal equivalent of the auxiliary path is given in Fig. 6.6. The common-emitter amplifier Q_7 drives the cascode transistor Q_3, which now operates as a common-emitter amplifier. The transistor Q_1 has been replaced by its equivalent output impedance Z_{oQ1}, equal to r_{o1} with a parasitic capacitance C_{par} in parallel. Since Z_{oQ1} is very high, the common-emitter amplifier formed by Q_3 is heavily degenerated and the gain of the auxiliary path to the output will be low. When calculating V_C, we can omit the influence of Q_3 as its input impedance is very high. Using similar simplifications as for the main-path calculation, we find:

$$V_c = -\frac{R_C}{(1+sR_CC_C)}\frac{g_{m7}}{(1+g_{m7}R_{e7}+s\,(R_{s7}+R_{b7})\,C_{\pi 7})}V_i \quad (6.3)$$

We find a small-signal gain of $-g_{m7}R_C$ and two poles: one determined by the input and one due to R_C and C_C. Calculating the response from V_C to

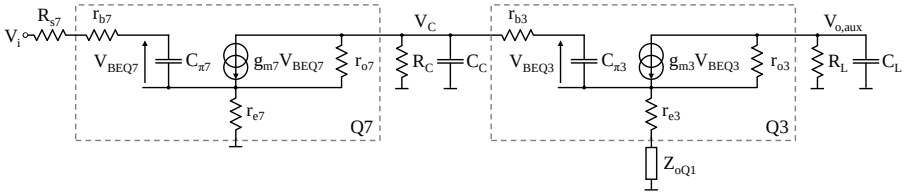

Figure 6.6: Simplified small-signal equivalent circuit of the auxiliary path in the breakdown voltage doubler of Fig. 6.4.

$\mathrm{V_{o,aux}}$ through $\mathrm{Q_3}$ yields the following simplified expression:

$$\mathrm{V_{o,aux}} = -\frac{\mathrm{R_L}}{(1+\mathrm{sR_LC_L})}\frac{1}{\mathrm{Zo,Q1}}\mathrm{V_c} \tag{6.4}$$

As expected, the small signal gain of $\mathrm{Q_3}$ is very low due to the high $\mathrm{Z_{o,Q1}}$. Furthermore, due to capacitances included into $\mathrm{Z_{o,Q1}}$, a zero is present in the response. Combining Eq. (6.3) and Eq. (6.4), substituting $\mathrm{Z_{o,Q1}}$ as $\mathrm{R_{o,Q1}}/(1+s\tau_z)$, rewriting the DC-gain $\mathrm{A_{aux}}$ as $\mathrm{g_{m7}R_CR_L}/(\mathrm{R_{o,Q1}}\,(1+\mathrm{g_{m7}R_{E7}}))$, the time constants associated with input pole of $\mathrm{Q_7}$ as τ_7 and the pole from $\mathrm{R_C}$-$\mathrm{C_C}$ as τ_C, we obtain:

$$\mathrm{V_{o,aux}} = -\frac{\mathrm{A_{aux}}\,(1+\mathrm{s}\tau_\mathrm{z})}{(1+\mathrm{s}\tau_\mathrm{L})\,(1+\mathrm{s}\tau_\mathrm{C})\,(1+\mathrm{s}\tau_7)}\mathrm{V_c} \tag{6.5}$$

Combining the expression in Eq. (6.2) and Eq. (6.5), leads to the following expression for the system:

$$\mathrm{V_o} = \left(-\frac{\mathrm{A_{main}}}{1+\mathrm{s}\tau_1} + \frac{\mathrm{A_{aux}}\,(1+\mathrm{s}\tau_\mathrm{z})}{(1+\mathrm{s}\tau_\mathrm{C})\,(1+\mathrm{s}\tau_7)}\right)\frac{1}{1+\mathrm{s}\tau_\mathrm{L}}\mathrm{V_i} \tag{6.6}$$

The main path contributes most to the final output signal. Nonetheless, there's also quite some peaking present due to the heavy emitter degeneration in the auxiliary path. This can have a detrimental impact on the output signal and on the distribution of the output swing over $\mathrm{Q_1}$ and $\mathrm{Q_3}$ at high frequencies. Therefore, the capacitor $\mathrm{C_C}$ is required to slow-down the auxiliary path and flatten out the peaking. For the circuit implementation described in section 6.3.3, we will make use of simulations to find the optimal component values in terms of bandwidth and linearity.

6.3 Chip Implementation

6.3.1 Input Stage and Continuous Time Line Equalizer

The input stage of this driver consists of two emitter followers that act as a buffer to shield the subsequent stages and provide a 100 Ω differential input impedance. While AC-coupling the input is most convenient, DC-coupling with a correct common-mode voltage is also possible. The HBTs are biased near their maximal f_T point using a current I_{iT} of 2.4 mA.

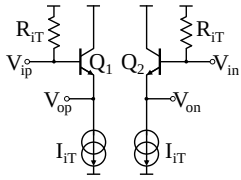

Figure 6.7: Input stage with 100 Ω differential termination.

Next is the CTLE, a similar schematic is used as for the driver in chapter 5, see Fig. 6.8. The differential pair Q_1-Q_2 only has resistive emitter-degeneration, while the pair Q_3-Q_4 has resistive and capacitive degeneration to introduce peaking. When V_{LEp} is high and V_{LEn} is low, only the resistive-degenerated pair contributes to the output signal. By decreasing V_{LEp} and increasing V_{LEn}, the capacitively degenerated pair contributes more to the output thus gradually more peaking can be introduced. This technique allows easy and accurately control over the peaking without needing a large (digitally) tunable capacitor C_C that introduces a lot of additional parasitics. The resistive emitter degeneration also helps to boost the linearity of this stage. The outputs are buffered and levelshifted down using the emitter followers Q_{13} and Q_{14} before being fed to the next stage.

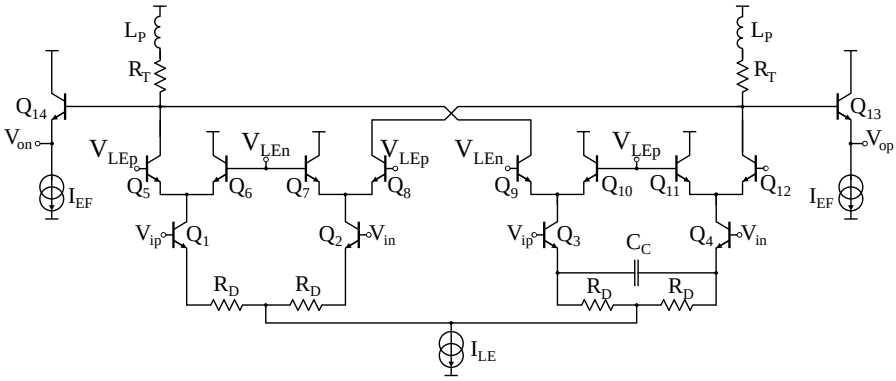

Figure 6.8: Schematic of the CTLE using a Gilbert-cell architecture.

In order to generate V_{LEp} and V_{LEn}, the circuit of Fig. 6.9 is used. A 7-bit current DAC generates the currents aI_B and $(1-a)I_B$, which are converted to voltages using Q_p and Q_n. Since a differential current is used, the common-mode voltage of V_{LEp} and V_{LEn} remains constant and the transistors Q_1 to Q_4 keep the same biasing point. Here, $(V_{LEp}+V_{LEn})/2$ is 2.1 V (for a=0.5), determined by I_B (which is 300 µA), Q_p, Q_n and M_1.

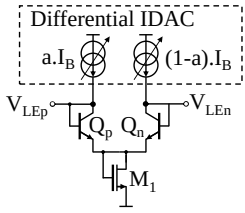

Figure 6.9: Conversion of a differential current to V_{LEp} and V_{LEn} for the CTLE.

In the circuit of Fig. 6.8, I_{LE} is 8 mA such that each differential pair has a 4 mA tail current. R_D and C_D are 50 Ω and 150 fF. The termination resistors R_T are 100 Ω and 50 pH of shunt peaking is added to enhance the bandwidth. The emitter followers are each biased with 2 mA. A simulation of the voltage transfer function from the input of the driver to the output of the CTLE is shown in Fig. 6.10. The DC-gain of this stage is only around 2.7 dB, most of the gain is situated in subsequent stages. The peaking of the CTLE can be varied between 0 and 7.7 dB.

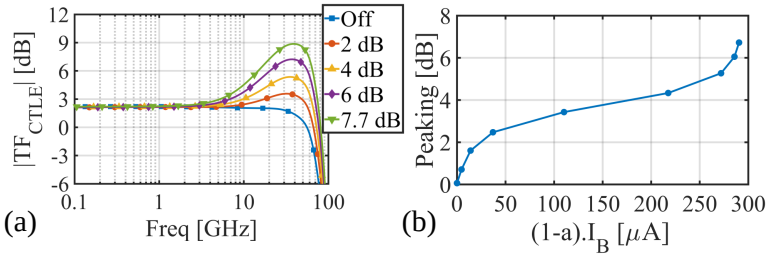

Figure 6.10: (a) Voltage transfer function from the input of the driver to the output of the CTLE for various peaking settings. (b) Peaking as a function of the current from the differential IDAC in Fig. 6.9.

6.3.2 Variable Gain Amplifier and Nonlinearity Compensation

The next stage serves as a variable gain amplifier (VGA) and nonlinearity compensation (NLC). For a given input voltage swing applied to the driver, the voltage swing incident on the output stage can be adjusted to optimize the performance. The NLC allows to symmetrically compress the inner levels of the PAM-4 signal to precompensate for compression in the output stage and by the modulator. The DCD circuit used to correct for offset voltage induced by mismatch or layout asymmetries is also included in this stage.

As shown in Fig. 6.11, the circuit consists of two differential pairs with cross-connected outputs. When the circuit is used as VGA, the current I_A is zero and only the differential pair Q_1-Q_2 is operational. By adjusting the resistive emitter degeneration R_{DT}, the gain of the stage can be varied: a higher R_{DT} causes more emitter degeneration and less gain. If the current I_A is non-zero, the NLC functionality starts to operate. The DC-response of two cross-connected differential pairs both with the same emitter degeneration is shown in Fig. 6.12. Here, I_T is 10 mA, R_E is 20 Ω, I_A is 0 mA when the NLC is off and 3 mA when it's on. The dashed line shows the differential output current (through Q_3-Q_4) when I_A is zero, so only Q_1-Q_2 contributes. We obtain the well-known $\tanh(\cdot)$ response. If I_A is 3 mA, the contribution of Q_5-Q_6 is subtracted from Q_1-Q_2. Since I_A is much smaller than I_T, the pair Q_5-Q_6 saturates much faster than Q_1-Q_2. Consequently, the DC-gain decreases at low input voltages, while remaining unaffected at higher input voltages (as Q_5-Q_6 is fully switched to one side and does not contribute anymore). This results in a distinct 'S'-shaped input-output characteristic as shown in Fig. 6.12.

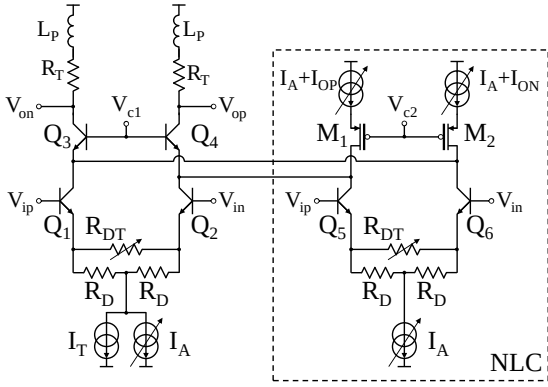

Figure 6.11: Circuit implementation of the VGA and NLC stage.

Subtracting the contribution of Q_5-Q_6 from Q_1-Q_2 decreases the full-swing output voltage. To compensate for this, the current I_A is added to to

the tail current of Q_1-Q_2 in order to preserve the full-swing output voltage. The common-mode output voltage of the stage decreases due to the additional tail currents. To avoid this, I_A is also added to each arm through the cascode transistors M_1 and M_2. Furthermore, the cascode transistors Q_3 and Q_4 help shielding the differential pairs from the output node to avoid bandwidth degradation due to both differential pairs being summed into a node.

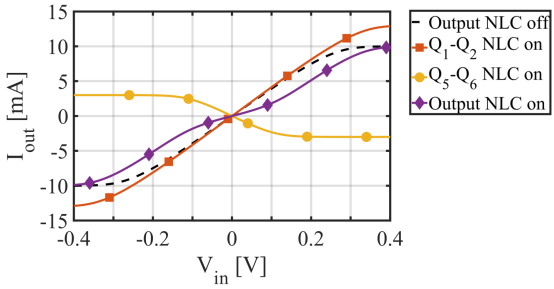

Figure 6.12: Differential output current without NLC (dashed line). Total output current and contributions of Q_1-Q_2 and Q_5-Q_6 when NLC is enabled.

The effect of the 'S'-shaped input-output response of Fig. 6.12 on the PAM-4 eye is illustrated in Fig. 6.13. When I_A is zero, the PAM-4 eye is unaffected, see Fig. 6.13(a). But if the NLC is enabled, the inner levels experience less gain such that they are compressed with respect to the outer levels, resulting in precompensation for symmetric compression, see Fig. 6.13(b). When not operated at full swing however, the swing of the PAM-4 signal is also affected. This can be compensated using the VGA functionality of the stage.

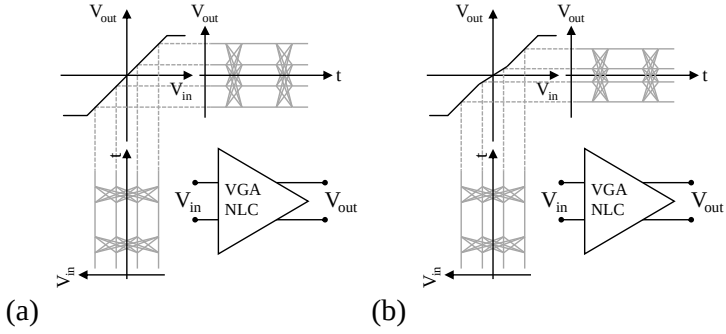

Figure 6.13: (a) Normal operation of the NLC stage. (b) Compressing of the inner PAM-4 levels using NLC.

The current sources I_{OP} and I_{ON} in the schematic, see Fig. 6.11 are used for the DCD. It operates exactly the same as for the previous driver (see p. 108). However, instead of using a single tunable current source and a differential pair to steer the current to the positive or negative signal line, two tunable current sources are used. The currents are tunable from 0 to 87.5 µA in steps of 12.5 µA which results in a DC offset voltage ranging from -100 mV to 100 mV at the output of the driver.

In the circuit of Fig. 6.11, I_T is 10 mA, I_A is configured between 0 and 3 mA in 200 µA steps, R_D is 28 Ω, R_T is 50 Ω and L_P is 50 pH. R_{DT} is implemented as a parallel circuit of MOS transistors in triode. In the off-state, R_{DT} is a few kΩ. While in the on-state, R_{DT} can be tuned between 20 Ω and 150 Ω. The voltage transfer function of the VGA (with I_A set to zero) is shown in Fig. 6.14(a). The gain is swept from the minimum to the maximum in steps of 1 dB. The parasitic capacitance causes some peaking at the lowest VGA-gain setting. The driver will typically be operated using a 300 mV_{pp} input signal, however, to demonstrate the effect of the VGA, a 200 mV_{pp} 64 Gbaud PAM-4 signal was applied to the driver channel. The eyes at the minimum and maximum gain setting are shown in Fig. 6.14(b) and (c). An eyeheight of around 500 mV_{pp} is ideal for the output stage. To verify the driver linearity, the level separation mismatch ratio (RLM) derived from the PAM4-eye is used [15]. For an ideal PAM4-eye, the RLM is 1. Compression in any of the four levels results in an decrease in RLM. We aim at an RLM higher than 0.9. Note however that preceding DSP, or our NLC can precompensate for driver or modulator compression. In Fig. 6.14(b) and (c), the RLM was respectively 0.96 and 0.91. For a 300 mV_{pp} 64 Gbaud PAM-4 signal, the simulated RLM at the output of the VGA (configured to 2 dB gain) is 0.90.

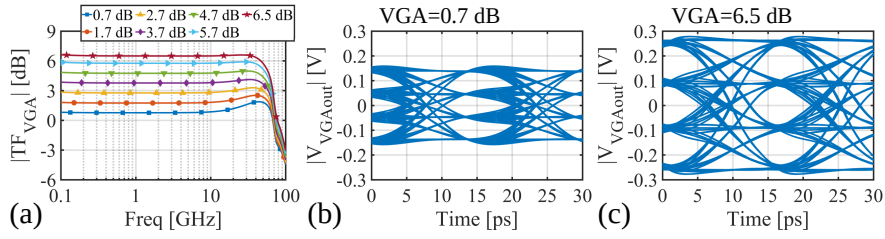

Figure 6.14: (a) Transfer function from the input to the output of the VGA stage for various gain settings. (b) and (c) transient simulations with a 200 mV_{pp} 64 Gbaud PAM-4 signal at the minimal and maximal gain setting.

The effect of the NLC circuit is demonstrated in Fig. 6.15. A 300 mV_{pp} 64 Gbaud PAM-4 was applied to the driver, the VGA was set to 2 dB, I_A is zero and the eye is captured at the output of the NLC, see Fig. 6.15(a).

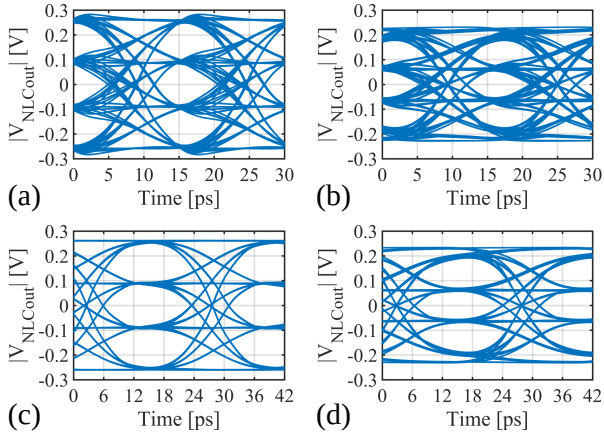

Figure 6.15: Signals at the output of the NLC with and without compensation. 64 Gbaud PAM-4 without (a) and with (b) compensation, 40 Gbaud PAM-4 without (c) and with (d) compensation.

Next, I_A was set to a rather extreme value of 1.5 mA, see Fig. 6.15(b). As the gain of the stage dropped due to the cross-coupled pair, the VGA-gain was increased with 3 dB. While it is clear that the inner levels are compressed, we also see a small decrease in signal swing and quite some additional intersymbol interference (ISI). The lower signal swing is expected, see also Fig. 6.13. For lower values of I_A, it's easier to compensate using the VGA. The additional ISI is unfortunately inherent to the system: the small current combined with the relative high swing on the NLC-differential pair Q_5-Q_6 causes one HBT to cut-off and become very slow at the outermost levels. The same simulation is repeated with 40 Gbaud in Fig. 6.15(c) and (d). The compression of the inner levels is more clear, just as the slow response of the HBT that switches off.

6.3.3 Output Stage

As the output stage has quite some gain to boost the signals up to their final swing, the associated linearity and bandwidth requirements provide an interesting challenge. In a first part, we will investigate how we can size the output stage to optimize the linearity while avoiding an excessive power consumption. To that end, we'll use the simplified schematic of Fig. 6.16. Simulations are conducted using 10 Gbaud PAM-4 signals to avoid bandwidth limiting effects that might distort our conclusions. To further simplify the simulation, the stage is driven with an ideal source with a differential impedance of 40 Ω, the resistors and current sources are ideal.

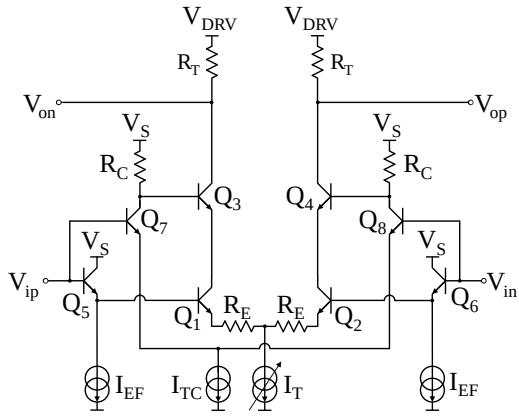

Figure 6.16: Simplified schematic used for linearity optimalization.

As already explained earlier, I_T is 60 mA, R_T is 50 Ω but since a 50 Ω load is connected to each side, the actual load seen by Q_3 and Q_4 is 25 Ω per side. The input common-mode voltage is determined by the preceding stage, in this case 2.2 V. Assuming a V_{BE} of around 0.9 V and a V_{CB} of 0.2 V, we find that V_{DRV} should be 3.35 V ($V_{cm,i} + 2V_{CB} + 0.5R_TI_T$), which can be rounded to 3.4 V. The output common-mode is then fixed at 2.6 V. The base of Q_3 and Q_4 should be at 2.4 V. As half of the swing is desired at that point, the easiest approach is to take I_{TC} half of I_T or 30 mA and R_C equal to the load of 25 Ω. This lead to V_S equal to approximately 2.8 V. I_{EF} is set to 5 mA and at this initial stage, we take R_E zero. All HBTs are sized such that they operate at their maximum f_T point. This leads to a power consumption of 315 mW, of which 111 mW is consumed by the auxiliary path and the emitter followers. A first step to decrease this power consumption is to decrease I_{TC} while increasing R_C. This keeps the swing at the base of Q_3 and Q_4 constant. I_{TC} was decreased from 30 mA to 3 mA while R_C was increased from 25 Ω to 250 Ω. This also affects the AC-performance, but since we use a 10 Gbaud signal, this influence is negligible. The signal swing was swept from 200 mV_{pp} to 400 mV_{pp} in steps of 50 mV. Fig. 6.17(a) shows the RLM as a function of output swing. It is clear that I_{TC} can be decreased quite a bit before the performance is deteriorated, see also the output eyes in Fig. 6.17(b) and (c). Therefore, we choose a new I_{TC} of 6 mA and the associated R_C of 125 Ohm. This helps decreasing the power consumption to 250 mW. At the same time, the maximum V_{CE} during transient simulation of Q_1-Q_2 and Q_3-Q_4 increases slightly, but still remains below 1.8 V up to 400 mV_{pp} input swing.

Next, we decrease R_C from 125 Ω to 15 Ω, while keeping I_{TC} constant at 6 mA. At the same time, we want the base of Q_3 and Q_4 to remain at 2.4 V, so

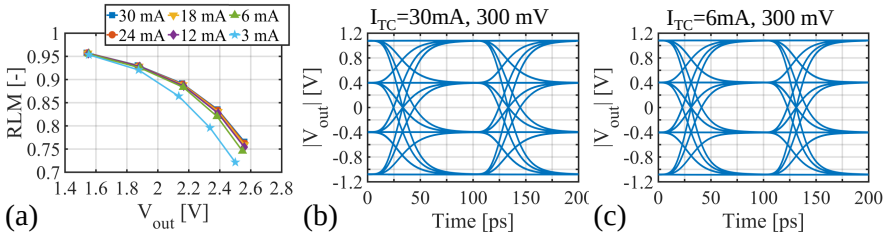

Figure 6.17: (a) RLM as a function of output voltage swing for various I_{TC}. Simulated using 10 Gbaud PAM-4 with a swing swept from 200 mV_{pp} to 400 mV_{pp}. 10 Gbaud PAM-4 eye at 300 mV_{pp} in, I_{TC} 30 mA (b) and 6 mA (c).

V_S should be lowered accordingly. The resulting RLM as a function of output voltage swing for various R_C values is shown in Fig. 6.18. Again, a 10 Gbaud PAM-4 signal was applied and its voltage swing was swept from 200 mV_{pp} to 400 mV_{pp} in steps of 50 mV. A clear increase in linearity is observed when lowering R_C from 125 Ω to 75 Ω. At 125 Ω, the swing at the base of Q_3 and Q_4 is so high that the V_{CE} drops below 0.7 V leading to a saturated cascode. By lowering R_C, the variation on $V_{CE,Q3}$ and $V_{CE,Q4}$ decreases, resulting in an improved cascode operation. At the same time, the variation on $V_{CE,Q1}$ and $V_{CE,Q2}$ increases. Up to 400 mV_{pp} input swing, all V_{CE}'s remain below 1.8 V. An R_C of 25 Ω is chosen, as this leads to a V_S of around 2.5 V. This allows to reuse the 2.5 V supply voltage of all previous stages.

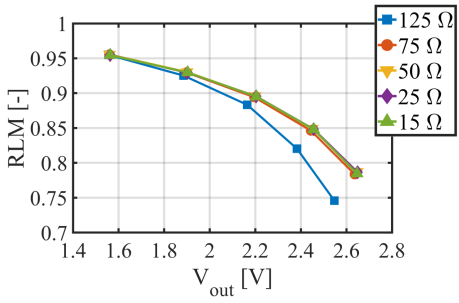

Figure 6.18: RLM as a function of output voltage swing for various I_{TC}. Simulated using 10 Gbaud PAM-4 with a swing swept from 200 mV_{pp} to 400 mV_{pp}.

The last trick to enhance the linearity is increasing the emitter degeneration of the main path through R_E. Simulations for R_E between 0 and 3 Ω are shown in Fig. 6.19. As this also leads to a decreased gain, the input swing is swept from 200 mV_{pp} to 600 mV_{pp}. An R_E between 1 and 2 Ω seems an optimal tradeoff between RLM and output swing. Therefore, we choose a R_E of 1.5 Ω.

Note that HBTs Q_1 and Q_2 have already some internal emitter degeneration, R_E is added on top of the existing degeneration. At 2 V_{pp}, we can now reach an RLM of around 0.94 with a power consumption of 245 mW. All V_{CE}'s remain below 1.8 V.

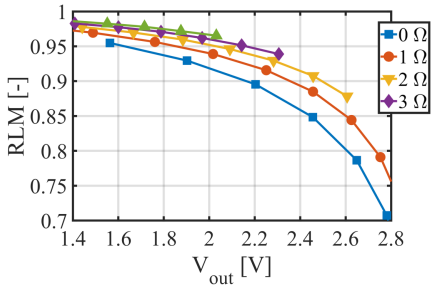

Figure 6.19: RLM as a function of output voltage swing for various R_E. Simulated using 10 Gbaud PAM-4 with a swing swept from 200 mV_{pp} to 600 mV_{pp}.

Now we can search for the optimal value of the capacitance C_C placed parallel over R_C to optimize the dynamic behavior, as explained in section 6.2. A simplified small-signal analysis already yields a system with four poles and two zeros. Due to the additional interaction between both paths, a full analysis is quite complex, let alone insightful [13]. Therefore, we add C_C to the idealized circuit from Fig. 6.16 and sweep its value to optimize the performance.

The voltage transfer function from input to output is shown in Fig. 6.20 for various C_C. Note that this is a highly idealized case: the resistors and capacitors are ideal, just like the current sources. When sweeping C_C from 0 to 1000 fF, a decrease in bandwidth is observed until 130 fF, after which the bandwidth increases slowly. Qualitatively, this can be understood by looking to Eq. (6.6): the system has two zeros and four poles, of which both zeros and one pole depend on C_C. By increasing C_C, the bandwidth starts to decrease due to the pole. At the same time, the dominant zero shifts closer to this pole resulting in pole-zero cancellation. At a certain specific capacitance, the zero is sufficiently close to cancel the effect of the pole and lead to a net increase in bandwidth. Additionally, increasing C_C leads to less peaking in the auxiliary path. At high frequencies, this peaking may cause high V_{CE} voltages in Q_1 to Q_4. Since the measures taken to increase the linearity already brought the V_{CE} well into the safe areas, this peaking is not a large problem. We select a relative large capacitance of 500 fF that can still be realized with a sufficiently high self resonance frequency (SRF).

The full schematic for the output stage is shown in Fig. 6.21. By switching from the ideal schematic to the full schematic, some values were optimized and

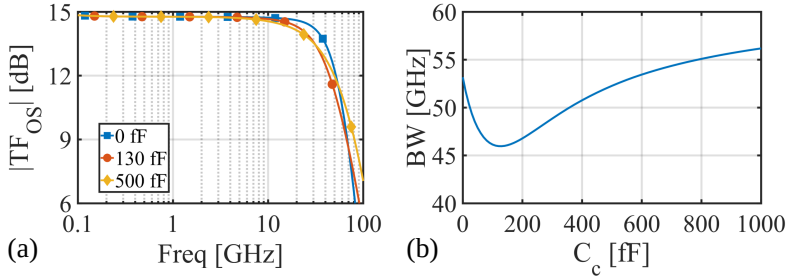

Figure 6.20: (a) Voltage transfer function from the input to the output of the output stage for the simplified schematic of Fig. 6.16 at various values for C_C. (b) Bandwidth of the output stage transfer function for a swept value of C_C.

shunt peaking was introduced through L_P. The tail currents (now implemented by real current mirrors) are unaltered: I_T is 60 mA, I_{TC} is 6 mA and I_{EF} is 5 mA. The supplies V_S and V_{DRV} are 2.5 V and 3.4 V respectively. R_T is 50 Ω, L_P is 100 pH, R_C is 23 Ω, C_C is 460 fF and R_E is 1.5 Ω.

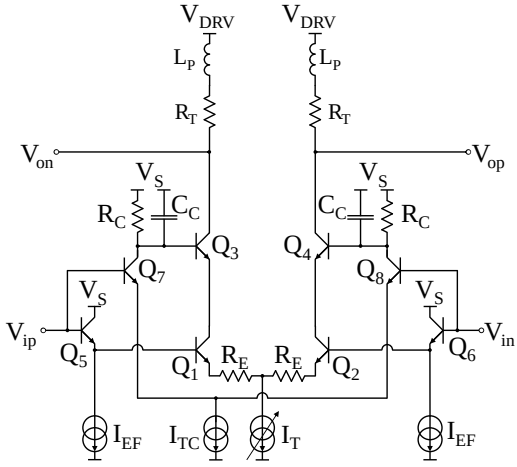

Figure 6.21: Full schematic of the output stage.

The simulated transfer function from the input of the output stage to the load, including the intermediate parasitics like ESD-cells, bondpads and a 200 pH bondwire is shown in Fig. 6.22(a). The stage has a DC-gain of 13.3 dB and a 3 dB bandwidth of 79 GHz. However, this is mainly due to the series peaking introduced by the parasitic bondwire. The transfer function drops to 10.8 dB around 50 GHz. Due to the preceding stages, this dip will drop further causing the system bandwidth to drop just below 50 GHz. The peak due to the

bondwire is sufficiently far to avoid deterioration of the 64 Gbaud eyes. By sweeping the input voltage between 200 and 400 mV_{pp} for various baudrates, the RLM as a function of output voltage swing is determined, see Fig. 6.22(b). At 10 Gbaud, a swing of 2 V_{pp} is obtained with an RLM of 0.93. The RLM drops to 0.91 at 2 V_{pp} for 40 Gbaud and it's only 0.84 at 64 Gbaud.

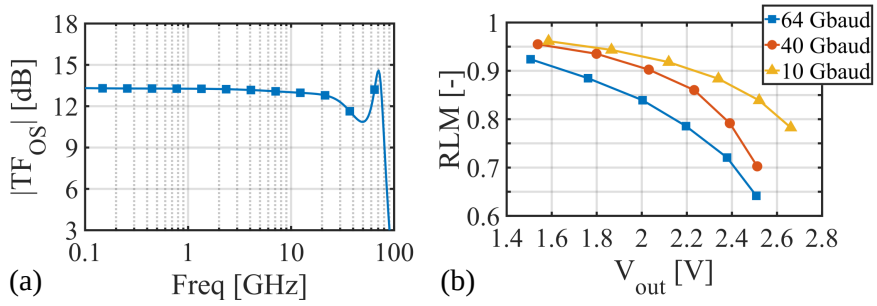

Figure 6.22: (a) Transfer function from output stage input to the load. (b) RLM as a function of output voltage swing for various baudrates.

The associated eyes which each with an output voltage swing of 2 V_{pp} are shown in Fig. 6.23. As can be observed, there's quite some additional ISI at higher baudrates, causing the outer levels to seemingly drop in amplitude. The PAM-4 levels when two consecutive symbols are identical do not show notable compression. It is expected that using some feedforward equalizer (FFE) equalization, the ISI can be improved resulting in a higher RLM.

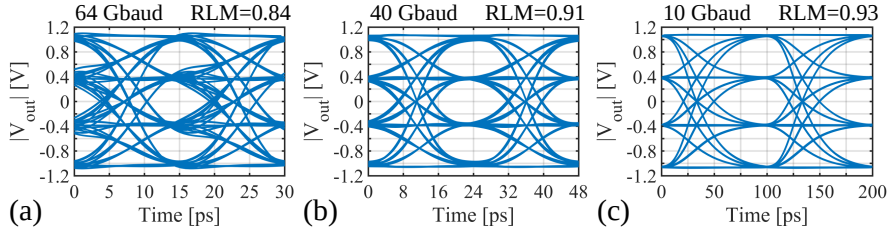

Figure 6.23: Transient simulations of a 64 Gbaud (a), 40 Gbaud (b) and 10 Gbaud (c) PAM-4 signal captured at the load.

In order to generate the large tail current I_T of 60 mA with a current source having a compliance voltage below 400 mV, a similar regulated cascode current source was used as in the previous driver, see page 114. Again, the protection MOS diodes were added in order to avoid any breakdown during startup.

6.3.4 Input and output network

Getting the high-speed signals on and off the chip poses some challenges at these high speeds. The bondwires, together with the capacitance associated with the bondpads and ESD-protection form an LC low-pass filter, as shown in Fig. 6.24(a). The bondpad capacitance C_{BP} is around 50 fF, while the ESD diodes to the supply and ground are each around 25 fF. Given a bondwire inductance of 200 pH, the circuit resonates at 35 GHz. The peaking and group delay associated with this resonance distort the PAM-4 eye resulting in a degraded performance.

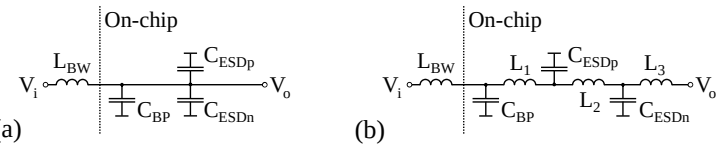

Figure 6.24: (a) Bondwire and internal parasitic capacitances at the bondpad. (b) Optimized input- and output network.

A solution is shown in Fig. 6.24(b): the capacitances are shielded from each other using various on-chip inductors. The circuit forms an artificial transmission line between the output signal and the inner circuit block (either the input or output stage) [16]. Using this approach, the initial values for the inductors L_1 to L_3 can be found. Further optimization was conducted together with the input and output stage.

6.3.5 Layout

The layout of a single channel is shown in Fig. 6.25. The bondpad pitch is 125 µm, with a GSSG bondpad configuration. As the outer ground-bondpads are shared between adjacent channels, the channel width becomes 375 µm. At the output, the shared bondpads are connected through the chip to an external bias voltage. The total length is 1080 µm. By unrolling some of the inductors in the input and output network, the gap between the input and output stage and their respective bondpads can be bridged. Without the input and output network, the data path is approximately 330 µm long and 240 µm wide. The output stage is 90 µm by 240 µm.

A micrograph of the die is given in Fig. 6.26. There are four channels placed next to each other. During layout, care has been taken to ensure all power planes are connected well in order to avoid IR-drop on the supply voltages. The outermost left and right side have been filled with decoupling capacitors and also serve as power distribution planes. The serial peripheral interface

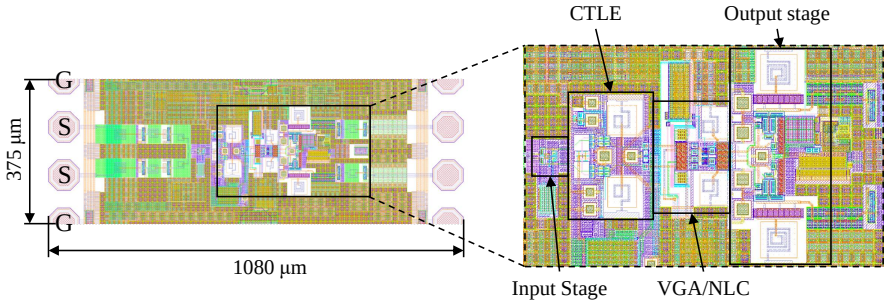

Figure 6.25: Layout of a single channel. Inset: zoomed version of the data path.

(SPI) registers that are used to control all settings in the channels is placed in the bottom right corner. The SPI block occupies 100 µm by 300 µm.

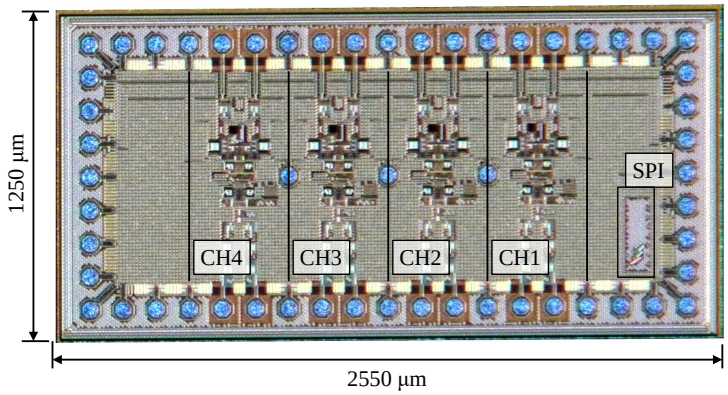

Figure 6.26: Annoted micrograph of the die.

6.4 Data path simulations

With the layouts, we can extract all parasitics and resimulate to confirm the post-layout performance. The result of an AC-simulation is shown in Fig. 6.27. At the input and output of the driver, the 200 pH bondwires are already taken into account. The performance of the input stage and CTLE are very similar, slightly less bandwidth due to some additional stray capacitances. For the VGA/NLC, it is clear that we underestimated the parasitics, as the bandwidth shows a clear decrease. Still, after extraction, the stage has a bandwidth of 57 GHz, the gain decreased by 0.6 dB, probably due to some additional contact resistance at the emitter. The performance of the output stage before and after extraction corresponds very well, a small drop in gain of 0.4 dB is observed.

The gain of the full cascade drops from 18.4 dB to 17.2 dB, due to the lower gain in the VGA/NLC and output stage. A small decrease in total bandwidth is observed: from 44.7 GHz to 39.8 GHz.

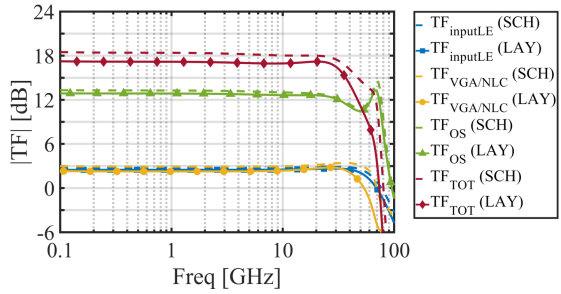

Figure 6.27: Transfer function of the input stage and CTLE, VGA/NLC, output stage and full channel before and after layout.

Transient simulations of a 64, 40 and 10 Gbaud PAM-4 signal with an input voltage swing swept between 200 and 400 mV_{pp} were used to determine the RLM as a function of output voltage swing for the extracted layouts, the results are shown in Fig. 6.28. The decreased gain is clearly visible, as the output swings have lowered. At 64 Gbaud, we see a decrease in RLM for the higher output swings, while the RLM seems unaffected for the 10 Gbaud case. The decrease in gain is likely caused by increased emitter resistances (due to e.g. contacting traces), which also slightly improves the linearity. However, due to additional group delay variations, the 40 Gbaud and 64 Gbaud case do not benefit from this.

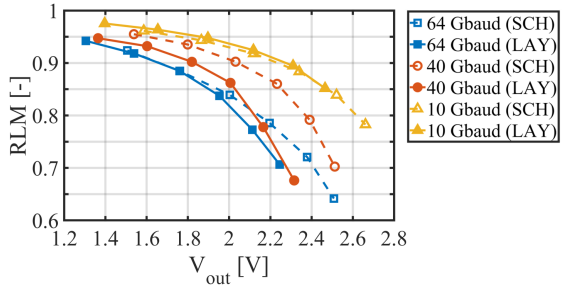

Figure 6.28: RLM as a function of output swing for various baudrates. Simulated before and after layout.

The eye diagrams observed at the output for the three baudrates, each for the same input voltage swing of 320 mV_{pp}, are illustrated in Fig. 6.29. It is indeed clear that there is quite some additional jitter visible in the 64 Gbaud

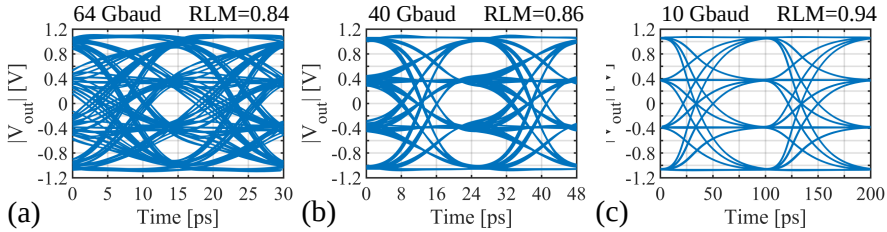

Figure 6.29: Transient simulations of a 64 Gbaud (a), 40 Gbaud (b) and 10 Gbaud (c) PAM-4 signal after layout.

case. This jitter and ISI result in a deteriorated RLM. It is expected that by using equalization, the RLM can be increased. In the 40 Gbaud case, we observe that the minimal-ISI-point of the outer and inner levels are shifted with respect to each other. Which again translates in a lower RLM. Since the 10 Gbaud eye is unaffected by the high-frequency behavior, a very clean eye is obtained, with an associated high RLM.

When transmitting NRZ signals, the driver linearity is not an issue anymore such that higher swings can be achieved. A 600 mV_{pp} 64 Gb/s NRZ signal was applied to the driver, the result is shown in Fig. 6.30. The continuous time line equalizer was set to introduce a small amount of peaking. The output swing is 2.8 $V_{pp,diff}$. Note that the tail current in the output stage can be controlled digitally, thus a higher swing is possible if the tail current is increased.

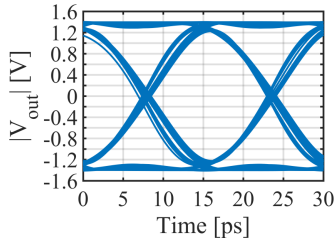

Figure 6.30: Post-layout transient simulations of a 64 Gb/s NRZ eye with 2.8 V_{pp} swing.

The power consumption is approximately 350 mW when all settings are nominal. Around 135 mW is supplied by the 2.5 V net, while the remaining 215 mW is supplied by the 3.4 V net. All four channels together use 1.4 W.

6.5 Conclusion

This chapter extends our work from NRZ towards PAM-4 drivers. The design of a four channel 64 Gbaud PAM-4 driver with 2 V_{pp} swing, and 2.8 V_{pp} swing for NRZ signals has been discussed. A breakdown voltage doubler architecture was selected for the output stage and optimized for linearity, bandwidth and power consumption. Moreover, the driver contains a VGA to ensure the output stage is operating at its optimal voltage swing. This same VGA is combined with a NLC which allows to compress the inner levels of the PAM-4 signal. As a result, precompensation of symmetric compression by the driver or the subsequent modulator is possible. Up to 6 dB of peaking can be introduced in the response using the CTLE.

The data path operates on a 2.5 V supply voltage, except for the output stage which operates on a 3.4 V supply. Additionally, the load is terminated to a separate supply, similar to the limiting driver in chapter 5. If required, the load can be connected to a different supply voltage than the output stage to further optimize the performance. The chip consumes 350 mW per channel at nominal operating settings. Consequently, the power efficiency is approximately 2.8 pJ/bit. Compared to other PAM-4 drivers, our driver achieves a low-power consumption for a moderate swing. For example [9] achieves 69 Gbaud DP16-QAM with an efficiency of 7.2 pJ/bit and 6 V_{pp} swing. However, this swing is only attained for the QPSK and SP-16QAM experiment, the DP-16QAM experiments only use a 2.4 V_{pp} swing for linearity reasons. The authors of [3] reach 6 pJ/bit with a 56 Gbaud PAM-4 signal and 3 V_{pp} swing. The four channel driver demonstrates 64 Gbaud DP-16QAM and DP-32QAM with a low power consumption of 2 pJ/bit, but only 1.5 V_{pp} swing. Furthermore, their driver introduces quite some peaking, which is undesired for intra-datacenter IM/DD links employing PAM-4.

It is important for future work to first focus on the demonstration of the driver in several use cases. Not only in a PAM-4 IM/DD link, but also in a (DP-)16QAM coherent transmitter. Given the various controls in the driver to optimize the performance, such experiments can give us hands-on experience in how the driver operates in such an environment and which controls are key to push the performance. Next generations of drivers can reuse this knowledge. Additionally, the focus on improving the linearity further while keeping the power consumption low will become key to keep up with higher modulation formats. This can be achieved by further optimizing the output stage, but also by improving the NLC stage to provide the precompensation up to 64 Gbaud while having less impact on the total signal swing. At last, an appealing path is the open-collector output stage, which would decrease the power consumption by 100 mW. Albeit at the cost of an increased sensitivity to interconnections and variations in the load impedance.

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7 Conclusion

7.1 Summary of the results

This dissertation has focused on optimizing optical transmitters for next-generation datacenter interconnects. To this end, we investigate both Mach-Zehnder modulators (MZMs) and the integrated driving circuits. The developed modulators aim to achieve both high-performance as well as seamless coupling to the driver integrated circuits (ICs).

In the first part of this dissertation, the high-speed electro-optic behavior of the Mach-Zehnder modulator was analyzed in depth. This allowed to identify the key performance tradeoffs and led to the design of a high-speed MZM on imec's iSiPP50G silicon photonics platform. Given the technology's PN-junction based phase modulator, an electrode structure was developed with optimized high-speed characteristics while allowing perfect integration with the driver IC. To circumvent the bandwidth-length tradeoff, the modulator was split in two shorter segments. The separate phase-shifting segments not only have a higher bandwidth than a single long segment, they also yield a 2-bit electro-optic digital-to-analog converter (DAC). While the measured bandwidth of the devices was lower than expected, the device characterization led to improved simulation models for future design iterations.

To keep up with increasing bandwidth demands on modulators, a novel technique was developed to embed finite impulse response (FIR) filters in slow-wave Mach-Zehnder modulators. This not only allows to extend the

bandwidth of the modulator, but allows to partially or fully shift equalization from the electrical domain inside the modulator. As the FIR filters are defined in the optical domain, a power and area-efficient way of equalization is obtained. A framework was developed for the modeling of these devices, modulators were fabricated and experiments were conducted showing the potential of the technique when employed in dispersion-limited links.

Both an NRZ and a PAM-4 driver IC for MZMs were designed in the second part of this dissertation. The four channel limiting driver, designed in a 55 nm SiGe BiCMOS technology, is capable of generating more than 50 Gb/s per channel at 2 V_{pp} swing. The limiting driver features a digitally tunable output swing and can introduce some overshoot in its response to help alleviate bandwidth limitations in the modulator. Two driver channels have been connected to the earlier developed segmented modulator in order to demonstrate 50 Gbaud PAM-4 generation. The experiments have shown the potential of such a 2-bit electro-optical DAC solution to reach high baudrates at a power consumption rivaling the state of the art in silicon photonic transmitters for intra-datacenter interconnects.

As datacenter interconnects scale to higher and higher line counts, an electro-optic DAC solution might not always be the best possibility in terms of footprint since two driver channels are required for one PAM-4 line. Therefore, a four channel 64 Gbaud 2 V_{pp} PAM-4 driver has been designed in a 130 nm SiGe BiCMOS technology. The same driver has a full swing of 2.8 V_{pp} for 64 Gb/s NRZ signals. In order to protect the output transistors, a breakdown voltage doubler architecture was adapted and optimized for a high linearity and bandwidth. Next to an adjustable output swing, the driver channels feature a continuous time linear equalizer (CTLE), a variable gain amplifier (VGA) and nonlinearity compensation (NLC) that allows to compensate for symmetric compression induced by the driver or the modulator.

7.2 Future work

Through measurements and experiments, the developed modulators and limiting driver were demonstrated. Both the design process and the experiments provide us with insights on what next steps we can undertake to continue improving the performance.

As already shown in the first part of this dissertation, the characterization of our Mach-Zehnder modulators are key to improve the simulation models. This was already covered partially by this work. However, more dedicated teststructures are required to fully grasp all effects. For example the effect of the substrate on the traveling-wave electrodes is not modeled well. As outlined in this manuscript, a redesign would benefit from a optimized termination

impedance to boost the bandwidth. For a PAM-4 optical transmitter, the insertion loss can be significantly decreased by omitting the unused child MZM and using edge couplers.

Embedding FIR filters inside modulators provides us with the possibility to shape the electro-optic frequency response to our needs. A major disadvantage is the flexibility of the solution since the filter is fixed in layout. Thus an important next step is to work out methods to reshape the response on the manufactured devices. One method would be to separate the bias voltage of segments belonging to different taps. An alternative way would be to replace the connections between segments by switchable elements allowing to select a direct connection, delay or crossing between two phase shifters. Main challenges in this approach are to make the elements sufficiently small, avoid excessive insertion loss and cross-talk, and ensure all switchable elements can be properly configured.

The electro-optic experiments with our four channel limiting driver and segmented MZM can be repeated using an improved MZM to show full compliance with the appropriate 53 Gbaud PAM-4 standard. Furthermore, the experiments can be extended to a coherent transmitter capable of 53 Gbaud 16QAM, by using an IQ modulator consisting of two segmented child MZMs. Second, automated calibration and biasing schemes for such a segmented modulator are required to ensure both segments are driven with the correct delay and swing. The driver already contains the capability to tune the output swing digitally, additional delay cells can be integrated with a relative low additional power consumption. To lower the power consumption of the driver further, an open-collector output stage might be considered. Nonetheless, utmost care should be taken to ensure that interconnection parasitics and load impedance pose no issues for the driver performance. Furthermore, this will decrease the flexibility of the driver as not all modulators will be suited.

The four channel PAM-4 driver's abilities are ideally tested further using elaborate PAM-4 experiments. Generation of a dual-polarization 16QAM constellation is certainly an important milestone. The linearity of the driver should be put to the test using higher-order constellation, albeit this will require more help from preceding (nonlinear) digital signal processing (DSP). Our proposed NLC circuit seems very promising, although it lacks high-speed performance. Measurements will be required to assess the advantage of this solution 'in the field'. Similar to the limiting driver, an open-collector output stage might provide a highly attractive boost in power efficiency at the costs outlined earlier.

7.3 Future prospects

The relentlessly increasing demand towards higher data rates is not expected to slow down in coming years. Innovations on both the drivers and modulators are crucial. Closer integration of the photonic integrated circuit (PIC) and electronic integrated circuit (EIC) will be key to limit the interconnection and footprint of the assembly. Flipchipping the EIC on top of the PIC, so called 3D integration, will likely be the to-go technique. This scenario also implies that the PIC will serve as an interposer for the EIC. For transceiver modules, it remains yet to be seen whether integrated lasers will find their place on this PIC. On one hand, integrating the laser on the same die yields additional gains in tight integration and low coupling losses. On the other hand, lasers are temperature sensitive and do not operate well at higher temperatures.

Improved integration further opens up the path towards co-packaged optics. By shortening the electrical channel between the core electronics and the transceiver module, the power consumption can be greatly reduced. By fully omitting the electrical channel and integrating the core electronics with the driver and PIC into one assembly, all additional electronics related to the interface can be omitted [1, 2].

While it is tempting to further integrate the drivers in deep submicron CMOS nodes, the analog performance of these nodes is not necessary better. Thus reaching higher bandwidths at these voltage high swings is hard. In contract, SiGe BiCMOS heterojunction bipolar transistors (HBTs) show promising results in obtaining a higher and higher f_T [3, 4]. It is thus very likely that SiGe BiCMOS will be the preferred technology. The main challenge will be how to keep up with higher data rates (either in baudrates as well as in spectral efficiency) or more parallel lanes, while keeping the power consumption low.

Just as important as pushing innovations in integration and high-speed electronics, is to push development on the optics. Silicon photonics allows very dense integration, high yield, high-volume production at low cost. But compared to for example III-V materials, the $V_\pi L_\pi$ is high. Furthermore, the bandwidth of silicon modulators based on reverse biased PN junctions is limited to about 90-100 GHz due to the carrier mobility [5]. Integrating III-V materials or lithium niobate on silicon can boost the performance of the modulators in terms of maximal achievable bandwidth and $V_\pi L_\pi$, at the cost of an increased complexity and loss of CMOS compatibility. However, techniques like micro-transfer printing may be key to integrate more exotic materials on silicon [6]. Moreover, transfer printing is not limited to photonics: small electrical ICs can be printed on PICs towards even tighter electro-optical heterogeneous integration.

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