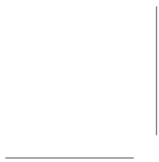
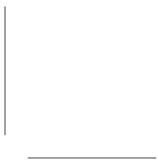
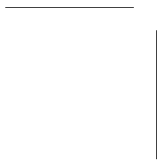
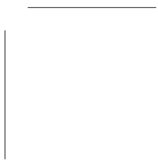

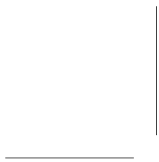
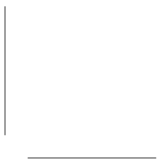
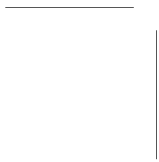
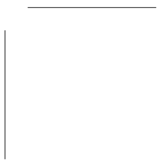

# Graphene-Silicon Photonic Integrated Devices for Optical Interconnects

## Fotonische geïntegreerde componenten op basis van grafeen en silicium voor optische interconnecties

Chiara Alessandri

Promotoren: prof. dr. ir. D. Van Thourhout, dr. M. Pantouvaki
Proefschrift ingediend tot het behalen van de graad van
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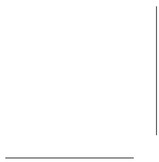
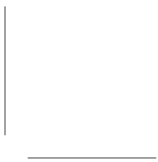
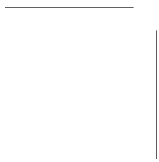
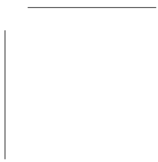

# Acknowledgments

It has been more than 5 years since I made the decision to move to Belgium to start a PhD. Despite having had an amazing time at imec during my master thesis, this choice was surrounded by doubts and fears. I didn't know if it was the right step. However, if I could go back in time, I would still make the same decision. Throughout the highs and lows, I have grown professionally, but even more so personally. By sharing my struggles and my successes, I have forged and deepened many friendships that I will always cherish. People close to me know that, even after six years it's still hard for me to accept many aspects of the Belgian lifestyle (early dinner, to name one!) and that I miss Italy very much. It's thanks to them that I have been able to call this place my home.

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This thesis is dedicated to my grandparents, my second parents. I was looking forward to showing it to you. I hope you would have been proud.

Now, before getting started, I want to share the lyrics of the photonics rap song I have written (and, of course, rapped) for the 'Epic Rap Battle of Science' during the 2018 imec PhD day.

**WHAT'S THE DIFFERENCE**

By Lil C

(Based on What's The Difference by Dr. Dre)

[Intro]
What's the difference between me and you?

[Verse 1]
We're living in a world of high speed data
Moving at a rate that we can't cater
Luckily for you there is photonics
It's here to achieve what electronics
Can't do, because it's too slow
Because its power consumption is a deathblow
Do you want to extend the Moore's law?
Then you're gonna have to turn to the photonics world
No current leakage, no heat dissipation
And you can use the same CMOS fabrication
Signal modulation, light amplification
Data transmission, photon emission
You ask, but what is it that you do?
Let me tell you, cuz it is so cool
We use total reflection to confine the light
Inside a structure that is called a waveguide
The core is made of silicon, the cladding is an oxide
The light can travel through it without ever going outside

Then you take graphene, a pure 2D material
You place it on a waveguide, and let it go serial
Its optical properties are so dope
So we wanna introduce 'em to the photonics globe

[Chorus]
What's the difference between me and you?
You sit the whole day on the chair like there was glue
Theoretical physics, and a lot of speculation
But it's all just a big useless cogitation

What's the difference between me and you?
You sit the whole day on the chair like there was glue
I try to solve the problems of telecommunications
So you and your ass can keep doing simulations

[Verse 2]
Enough with all the bashing, or you're gonna get depression
I'll show you some compassion, and teach y'all a lesson
Graphene has zero bandgap, it absorbs the light
Any wavelength of the spectrum, such a delight
If you take graphene and apply an electric field
You can tune the Fermi level to the energy you need
When the Fermi level is at the Dirac point
It absorbs any photon, it does not disappoint
Once the Fermi level starts moving high or low
Graphene's absorption sinks, and the modulation grow
You get the logic 0 where the min transmission is
Up to the 1 for a max transmission bliss
When you do this fast, you can easily transmit
A lot of data quick, for your favourite kitty pic
Now tell me more about how your TFETs work
You know what, just shut up, before I go berserk

[Chorus]
What's the difference between me and you?
You sit the whole day on the chair like there was glue
Theoretical physics, and a lot of speculation
But it's all just a big useless cogitation

What's the difference between me and you?
You sit the whole day on the chair like there was glue
I try to solve the problems of telecommunications
And leave you alone to deal with all of your frustrations

# Contents

**Acknowledgments** vii

**Contents** xi

**List of Figures** xv

**List of Tables** xxiii

**List of Acronyms** xxv

**List of Symbols** xxxi

**Samenvatting** xxxiii

**Summary** xxxvii

**1 Introduction** 1
- 1.1 Optical interconnects . . . . . . . . . . . . . . . . . . . . . . . . . 1
- 1.2 Silicon Photonics . . . . . . . . . . . . . . . . . . . . . . . . . . . 3
  - 1.2.1 Modulators . . . . . . . . . . . . . . . . . . . . . . . . 4
  - 1.2.2 Photodetectors . . . . . . . . . . . . . . . . . . . . . . 6
  - 1.2.3 Wavelength-division multiplexers . . . . . . . . . . . . . 7
- 1.3 Graphene . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 8
  - 1.3.1 Graphene properties . . . . . . . . . . . . . . . . . . . 9
  - 1.3.2 Graphene growth and transfer . . . . . . . . . . . . . . 16
- 1.4 Graphene characterisation techniques . . . . . . . . . . . . . . . 18
  - 1.4.1 Physical characterisation . . . . . . . . . . . . . . . . . 18
  - 1.4.2 Electrical characterisation: the transfer length method (TLM) . . . . . . . . . . . . . . . . . . . . . . . . . 20
- 1.5 Graphene photonic devices . . . . . . . . . . . . . . . . . . . . . 23
  - 1.5.1 Graphene modulators . . . . . . . . . . . . . . . . . . . 23
  - 1.5.2 Graphene photodetectors . . . . . . . . . . . . . . . . . 27
- 1.6 Characterisation of graphene photonic devices . . . . . . . . . . 30

1.6.1 Characterisation of graphene electro-absorption modulators . . . 32
1.6.2 Characterisation of graphene photodetectors . . . 34
1.7 Research objectives . . . 34
1.8 Thesis overview . . . 35

**2 Standard fabrication flow: process development and graphene electrical characterisation 39**
2.1 Introduction . . . 39
2.2 SOI substrate fabrication . . . 40
2.3 Graphene device fabrication: standard flow . . . 41
2.3.1 Alignment markers . . . 42
2.3.2 Graphene transfer . . . 44
2.3.3 Graphene shaping . . . 44
2.3.4 Graphene contacts . . . 48
2.3.5 Silicon contacts . . . 51
2.4 Characterisation of graphene TLM structures . . . 52
2.4.1 Sample design . . . 52
2.4.2 Electrical characterisation of TLM structures . . . 52
2.4.3 Raman characterisation . . . 58
2.5 Conclusions . . . 58

**3 Encapsulation of graphene devices 61**
3.1 Intrinsic doping and gate hysteresis in graphene devices . . . 61
3.2 Graphene device fabrication with a passivation layer . . . 64
3.2.1 Comparison of passivation methods . . . 64
3.2.2 Passivation-last process flow . . . 64
3.2.3 Passivation-first process flow . . . 65
3.3 Passivation-last on graphene FETs . . . 68
3.3.1 Sample design and characterisation technique . . . 68
3.3.2 Results . . . 68
3.3.3 Conclusions . . . 70
3.4 Passivation-first with seeding layer on graphene FETs . . . 71
3.4.1 Sample design and characterisation technique . . . 71
3.4.2 Results . . . 72
3.4.3 Conclusions . . . 73
3.5 Passivation-first on graphene EAMs . . . 73
3.5.1 Sample design and characterisation technique . . . 73
3.5.2 Results . . . 74
3.6 Conclusions . . . 74

**4 Single-layer graphene electro-absorption modulators 77**
4.1 Modeling of graphene EAMs . . . 77
4.1.1 Surface conductivity method . . . 78
4.1.2 Static electro-optical behaviour . . . 79

4.1.3 RC limited high-speed behaviour of the SLG EAM . . . 82
4.1.4 Device optimisation . . . . . . . . . . . . . . . . . . . . . 87
4.2 Characterisation of graphene EAMs . . . . . . . . . . . . . . . 89
4.2.1 Effect of Si waveguide doping on the performance of C-band TE SLG EAMs . . . . . . . . . . . . . . . . . . . . 89
4.2.2 Performance comparison of C-band TE and TM SLG EAMs 93
4.2.3 Performance of O-band TM SLG EAMs . . . . . . . . . 94
4.2.4 Large signal high speed performance . . . . . . . . . . . 95
4.3 Wavelength-division multiplexing (WDM) transmitters . . . . . 96
4.3.1 Design and fabrication . . . . . . . . . . . . . . . . . . . 97
4.3.2 Experimental results . . . . . . . . . . . . . . . . . . . . 98
4.4 Conclusions . . . . . . . . . . . . . . . . . . . . . . . . . . . . 103

**5 Double-layer graphene electro-absorption modulators 105**
5.1 Why double-layer graphene? . . . . . . . . . . . . . . . . . . . . 105
5.2 Modeling of double-layer graphene EAMs . . . . . . . . . . . . 106
5.2.1 Static performance: SLG vs DLG . . . . . . . . . . . . . 107
5.3 Experimental results . . . . . . . . . . . . . . . . . . . . . . . . 109
5.3.1 Design and fabrication . . . . . . . . . . . . . . . . . . . 109
5.3.2 $Al_2O_3$ spacer . . . . . . . . . . . . . . . . . . . . . . . . 110
5.3.3 $HfO_2$ spacer . . . . . . . . . . . . . . . . . . . . . . . . . 112
5.4 Optimisation of DLG EAMs and outlook . . . . . . . . . . . . 114
5.5 Conclusions . . . . . . . . . . . . . . . . . . . . . . . . . . . . 117

**6 Graphene photodetectors 119**
6.1 Introduction . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 119
6.2 Graphene photoresistor . . . . . . . . . . . . . . . . . . . . . . 121
6.2.1 Device concept . . . . . . . . . . . . . . . . . . . . . . . 121
6.2.2 Experimental results . . . . . . . . . . . . . . . . . . . . 121
6.2.3 Conclusions . . . . . . . . . . . . . . . . . . . . . . . . . 122
6.3 Photodetectors based on a graphene/Si Schottky junction . . . 123
6.3.1 Device concept . . . . . . . . . . . . . . . . . . . . . . . 123
6.3.2 Theoretical model . . . . . . . . . . . . . . . . . . . . . 124
6.3.3 TE graphene/Si Schottky photodetectors . . . . . . . . 127
6.3.4 Improving stability of the graphene/Si Schottky junction 130
6.3.5 TM graphene/Si Schottky photodetectors . . . . . . . . 132
6.4 Outlook . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 134

**7 Conclusions and Outlook 137**
7.1 Conclusions . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 137
7.2 Outlook . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 139

**Appendices 141**

**A Recipes used for devices fabrication 143**

A.1 Graphene field-effect transistors . . . . . . . . . . . . . . . . . . . 143
A.1.1 Standard flow . . . . . . . . . . . . . . . . . . . . . . . . . 143
A.1.2 Passivation-first flow . . . . . . . . . . . . . . . . . . . . . 145
A.2 Single-layer graphene electro-absorption modulators . . . . . . 146
A.2.1 Standard flow . . . . . . . . . . . . . . . . . . . . . . . . . 146
A.2.2 Passivation-first flow . . . . . . . . . . . . . . . . . . . . . 147
A.3 Double-layer graphene electro-absorption modulators . . . . . . 149
A.4 Graphene photoresistors . . . . . . . . . . . . . . . . . . . . . . . 151
A.5 Photodetectors based on a graphene/Si Schottky junction . . . 151

**References** **170**

**List of Publications** **171**

# List of Figures


1.1 Global data center IP traffic growth reported in Cisco Global Cloud Index: Forecast and Methodology report for 2016-2021 [1]. . . . . . 2
1.2 Schematic cross-section of imec's silicon photonics platform, with the basic passive and active devices. Taken from [2]. . . . . . . . . 3
1.3 Schematic representation of the working principle of a modulator. 4
1.4 Schematic representation of the working principle of a photodetector. 6
1.5 Schematic representation of a wavelength division multiplexing transceiver system. . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 7
1.6 Graphene is the building block for carbon-based materials of other dimensionalities. From left to right: graphene wrapped up into 0D buckyballs, rolled into 1D nanotubes or stacked into 3D graphite. Taken from [3]. . . . . . . . . . . . . . . . . . . . . . . . . . . 8
1.7 Atomic orbital diagram of a carbon atom: (a) ground state, (b) $sp^3$-hybridised as in diamond and (c) $sp^2$-hybridised as in graphite and graphene. [4] . . . . . . . . . . . . . . . . . . . . . . . . . . 10
1.8 (a) 2D hexagonal lattice of graphene in real space. $a_1$ and $a_2$ are the basis vectors and they define the unit cell, highlighted in grey. An armchair and a zigzag edge are highlighted in grey. (b) Reciprocal lattice (dashed), with reciprocal lattice vectors $b_1$ and $b_2$ defining the first Brillouin zone, marked in grey. $\Gamma$, $M$, $K$ and $K'$ are the high symmetry points. (c) Small views of the real (upper) and reciprocal (lower) lattice. Two sets of lattice planes with $d = 2.13$ Å and $d = 1.23$ Å are highlighted with dotted and full lines in the real space lattice. In the reciprocal lattice the corresponding diffraction spots are marked with a dotted and full hexagon, respectively. [4] . 11
1.9 Electronic dispersion in the honeycomb lattice. Right: zoom in of the energy bands close to one of the Dirac points, where the dispersion relation is linear. Image taken from [5]. . . . . . . . . . 12
1.10 Modulation of the resistivity of a graphene sample by the application of a gate voltage. The insets show its conical low-energy spectrum $E(k)$, indicating changes in the position of the Fermi energy $E_F$ with changing gate voltage $V_g$ [3]. . . . . . . . . . . . . . . . . . . . 13

1.11 (a) Absorption spectrum of n-doped graphene. It shows maximum absorption at THz frequencies, minimum absorption at mid-infrared frequencies and constant 2.3% absorption beyond the far-infrared. (b) Illustration of the various optical transition processes. At $\omega$ less than the thermal energy, transitions occur via intraband processes. At finite $\omega < 2\ \mu$, disorder plays an important role in imparting the momentum for the optical transition. A transition occurs around $\omega \approx 2\ \mu$, where direct interband processes lead to a universal 2.3% absorption. The absorption spectrum of p-doped graphene is analogous. Taken from [6]. . . . . . . . . . . . . . . . . . . . . . . . . . 14
1.12 Summary of the available technique to produce graphene, classified in terms of size, quality and price for any particular application. Taken from [7]. . . . . . . . . . . . . . . . . . . . . . . . . . . . . 16
1.13 (a) Optical microscope image of a shaped CVD graphene layer. Wrinkles and bilayer spots are visible. (b) Scanning electron microscope image of a shaped graphene layer on top of a waveguide. 19
1.14 Raman spectra of graphene. . . . . . . . . . . . . . . . . . . . . . . 19
1.16 (a) Cross section of a graphene FET used for measurement of TLM structures, with indications of how the voltage is applied. (b) Example of a typical $I_D - V_G$ curve for intrinsic graphene. . . . . . . 22
1.17 (a) Three-dimensional schematic illustration of the device. (b) Left, cross-section ofthe device, with an overlay ofthe optical mode plot. Right, a cross-section through the centre of the waveguide; the purple curve shows the magnitude of the electric field. Taken from [8]. 23
1.18 (a) A 3D schematic drawing of the SLG EAM built on a planarised SOI substrate. Taken from [9]. (b) 3D schematic image of the graphene-silicon microring resonator. Taken from [10]. . . . . . . . 24
1.19 (a) Optical micrograph of the MZI modulator. (b) Cross-section of the GPM through the dashed line A–A' of (a). Taken from [11]. . 24
1.20 Three-dimensional schematic illustration of two DLG EAMs. (a) is taken from [12] and (b) is taken from [13]. . . . . . . . . . . . . . . 25
1.21 (a) Schematic of the modulator consisting of a graphene/graphene capacitor integrated along a ring resonator. (b) Cross-section of the device, showing two layers of graphene separated by a 65 nm-thick $Al_2O_3$ dielectric layer. Taken from [14]. . . . . . . . . . . . . . . . 26
1.22 (a) Schematic of a device showing two layers of graphene separated by a 120 nm-thick $Al_2O_3$ dielectric layer to form a capacitor. (b) Finite element method calculation of the TM mode in the silicon waveguide. Taken from [15]. . . . . . . . . . . . . . . . . . . . . . . 26
1.23 Device geometries of the first demonstrated graphene photodetectors. (a) Taken from [16], (b) from [17] and (c) from [18]. . . . . . 28
1.24 (a) Silicon waveguide graphene photodetector with asymmetrical electrode geometry. Taken from [19]. (b) Metal-graphene-silicon photodetector based on a graphene/silicon Schottky junction. Taken from [20]. . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 29

1.25 (a) Graphene photodetector based on a slot-waveguide. Taken from [21]. (b) Graphene photodetector based a PhC defect waveguide. Taken from [22]. . . . . . . . . . . . . . . . . . . . . . . . . . . . . 29
1.26 (a) Plasmonically enhanced waveguide-integrated graphene photodetector. Taken from [23]. (b) SLG on SiN waveguide (brown) with split-gates, acting as plasmonic slot waveguide, to create a p-n junction in the channel. Taken from [24]. . . . . . . . . . . . . . . . . . 30
1.27 (a) Example of transmission spectra measured on waveguide with varying graphene coverage length. (b) Fitting of data of transmission as a function of length extracted from the measurement in (a). (c) Transmission spectra normalised to the reference waveguide. . . 31
1.28 (a) Example of transmission spectra measured on a graphene modulator with $L_{device}$ = 75 µm at varying DC bias. (b) Extracted transmission as a function of applied DC bias, obtained from the measurement in (a). . . . . . . . . . . . . . . . . . . . . . . . . . 33
1.29 (a) Schematics of the setup used to measure S-parameters. (b) Measured $S_{21}$-parameters on a 25 µm-long EAM at varying DC bias. 33
1.30 Schematics of the setup used for large signal characterisation. . . . 34

2.1 Schematic cross section of (a) a graphene FET device fabricated from a $SiO_2$/Si wafer substrate and (b) a single-layer graphene EAM fabricated from a SOI substrate. . . . . . . . . . . . . . . . . . . 41
2.2 Main steps of the final recipe used to fabricate SLG EAMs. . . . . 43
2.3 Si/$SiO_2$ substrate with delaminated graphene after immersion in OPD5262. . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 47
2.4 Comparison between different types of photoresist profiles: negative, positive or undercut. . . . . . . . . . . . . . . . . . . . . . . . . 48
2.5 Contact fabrication using a bi-layer process with LOR™ 1A and IX845 on a TLM structure. The lithography (left) and lift-off (right) steps were successful, but in some cases the contact pads delaminated when the sample was immersed in OPD5262 to strip the LOR™ 1A. . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 49
2.6 Top-down SEM image of a graphene EAM fabricated with support pads. The metal contact to Si is on the left side of the waveguide and is covered by a second metal contact, the support pad. On the right side of the waveguide, the metal contact to graphene has delaminated together with the portion of support pad covering it, leaving only a part of the support pad and paritally delaminated graphene on the substrate. . . . . . . . . . . . . . . . . . . . . . . 51
2.7 Cross section of graphene FETs used for TLM measurements with (a) 5 nm gate oxide and (b) 155 nm gate oxide. . . . . . . . . . . . 53
2.8 Example of $I_d$-$V_g$ measurements performed on a TLM structure with $t_{ox}$ = 5 nm and with (a) n-doped Si ($n = 2.4e18cm^{-3}$) and (b) p-doped Si ($p = 1.9e18cm^{-3}$). . . . . . . . . . . . . . . . . . . . . . 53

2.9 Values of graphene's contact resistance $R_{graC}$, mobility $\mu_c$ and neutrality point $V_{NP}$ (normalised to the gate oxide thickness $t_{ox}$) obtained from electrical measurements on TLM structures with different Si doping and gate oxide thickness. . . . . . . . . . . . . . . . . 54

2.10 Cumulative distribution function (CDF) plots showing the empirical cumulative distribution of graphene's contact resistance $R_{graC}$ and mobility $\mu_c$ for different Si doping levels, for p-typed and n-type Si doping. . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 55

2.11 Raman spectra measured on graphene on top of p-type Si with doping level $p = 1.2e18cm^{-3}$ (a) before device processing and (b) after device processing. . . . . . . . . . . . . . . . . . . . . . . . . . . 57

3.1 Schematic illustration of the charge-transfer process between the redox couple and graphene under different gate voltages. Taken from [25]. . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 62

3.2 Schematic cross section of a graphene FET passivated using the passivation-last approach. . . . . . . . . . . . . . . . . . . . . . . . 65

3.3 Steps to fabricate a graphene EAM with a passivation-first process flow. First, lithography for graphene shaping is performed, then the dielectric layer is deposited on the sample. For graphene contacts, a dry etching step is performed before evaporating the metal layer in order to open a via in the dielectric to contact the graphene. For silicon contacts, the dielectric is wet etched together with the thermal $SiO_2$. . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 66

3.4 (a) Cross-sectional SEM image of a graphene EAM fabricated with a passivation-first process flow. On the left side, the metal contact creates a side contact to graphene. However, the oxide below the metal is significantly over-etched, causing the metal to be lower than the graphene layer. On the right side, the metal contact to Si is visible. The metal was misaligned, which can be seen from the fact that the metal edge does not end where the high-doped Si region ends (dark orange). (b) Dektak step height measurement. The top surface of the graphene contact is $\sim$ 100 nm lower than expected. . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 67

3.5 Cumulative distribution function (CDF) plot showing the empirical cumulative distribution of the mobility $\mu_c$ and of the position of graphene's neutrality point $V_{NP}$ over time for samples passivated with the passivation-last approach using (a, b) HSQ, (c, d) SOG and (e, f) $Al_2O_3$. . . . . . . . . . . . . . . . . . . . . . . . . . . . 69

3.6 Raman spectrum of the CVD graphene used for the passivation-first experiment. . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 71

3.7 (a) Example of $I_D$-$V_G$ measurement on four devices with varying channel length, showing p-doped graphene and a small hysteresis of $\Delta V_{NP} = 4$ V. (b) Cumulative distribution function (CDF) plot showing the empirical cumulative distribution of the mobility $\mu_c$ for the sample passivated with $Al_2O_3$ using the passivation-first approach. 72

3.8 Comparison of transmission curves, measured with a double voltage sweep right after fabrication, between an unpassivated (a) and a passivated (b) 25 µm-long graphene EAMs. The same measurement is repeated on the passivated EAM after 2 months time (c). . . . . . 75

3.9 $S_{21}$ parameters measured on the passivated 25 µm-long SLG EAM at 0 V DC bias and 1560 nm wavelength. The two measurements are performed five months apart. . . . . . . . . . . . . . . . . . . . 76

4.1 Schematic cross section of a SLG EAM. The three doped silicon regions are either p- or n-doped: waveguide ($n_{wg}/p_{wg}$), slab ($n_{slab}/p_{slab}$) and contact ($n_{++}/p_{++}$). The graphene, oxide and silicon layers form a GOS capacitor. . . . . . . . . . . . . . . . . . . . . . . . . . 78

4.2 Real and imaginary part of (a) graphene surface conductivity $\sigma$ and (b) dielectric constant $\epsilon$ as a function of graphene chemical potential $\mu$ at 1560 nm wavelength, for scattering rate values of 0.5, 15 and 30 meV. . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 79

4.4 Equivalent electrical circuit of a single-layer graphene electro-absorption modulator. . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 82

4.16 (a) Top view microscope image showing the three WDM transmitters, each based on 5 graphene-Si EAMs and 5 second order MRRs. WDM1: $W_{wg}$ = 500 nm, $L_{device}$ = 100 µm; WDM2: $W_{wg}$ = 600 nm, $L_{device}$ = 100 µm; WDM3: $W_{wg}$ = 600 nm, $L_{device}$ = 150 µm. (b) Cross section of a graphene-Si EAM, passivated with Si (0.5nm)/$Al_2O_3$ (10nm). . . . . . . . . . . . . . . . . . . . . . . . 97

4.17 Transmission spectra, normalised to a reference waveguide, measured on a WDM filter without graphene, showing the insertion loss of the second order MRRs. . . . . . . . . . . . . . . . . . . . . . . 99

4.18 Left column: transmission spectra on (a) WDM1, (c) WDM2 and (e) WDM3 normalised to a reference waveguide without graphene. The voltage is varied from -4 V to 4 V on each graphene EAM, resulting in the tuning of the transmission on each channel. Right column: normalised transmission as a function of DC voltage bias, measured on (b) WDM1, (d) WDM2 and (f) WDM3. The transmission is extracted at the peak wavelength of each channel. . . . . 100

4.19 (a, b, c) Electro-optical $S_{21}$ (inset: $S_{11}$) frequency response measured at 0 V DC bias on WDM1, WDM2 and WDM3 respectively. The response is uniform across the 5 channels. (d) GOS capacitance and 3dB bandwidth of WDM1 as a function of DC bias. The GOS capacitance increases at forward bias, causing a drop in 3dB bandwidth. The ideal operating region is therefore at 0 V or low reverse bias. . . . . . 101

4.20 Eye diagrams measured at 25 Gbit/s on WDM2 at 2.5 $V_{pp}$ and -1.2 V DC bias. The performance is uniform across the 5 channels. The dynamic extinction ratio is limited by the low modal overlap with graphene when using TE-polarised light. . . . . . 102

4.21 SNR and dynamic ER as a function of bit rate. The SNR is higher than 3.0 up to 25 Gbit/s for all the WDM transmitters. The ER for WDM3 is higher than 1 dB up to 30 Gbit/s, due to the longer device length. . . . . . 102

4.22 Eye diagrams measured at 5 Gbit/s (a) and 30 Gbit/s (b) on CH2 of WDM3 at 2.5 $V_{pp}$ and -1.2 V DC bias. . . . . . 103

5.1 Schematic cross section of a DLG EAM. The two graphene layers, separated by a dielectric layer, form a graphene-oxide-graphene capacitor. . . . . . 106

6.1 Schematic cross section of (a) a graphene photoresistor and (b) a graphene/Si Schottky junction. . . . . . 120

6.2 (a) Dark current and (b) photocurrent ($I_{light} - I_{dark}$) as a function of $V_{bias}$ (as defined in Fig. 6.1a) for varying $V_{gate}$ measured on a graphene photoresistor with $L_{device} = 100$ µm at 12 dBm laser input power. . . . . . 123

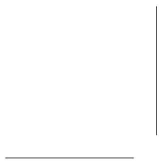
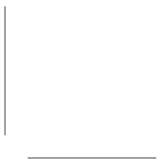
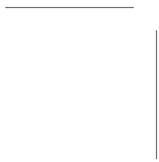
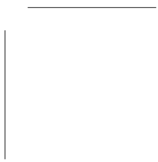
6.3 (a) Graphene band profile comparing the case with Pd-Pd contacts and Pd-Ti contacts. Adapted from [26]. (b) Graphene photodetector integrated on a silicon waveguide with asymmetric contact configuration. Taken from [19]. . . . . . 124

6.4 Energy band diagram for a graphene/Si Schottky junction with n-doped Si for (a) V = 0, (b) V > 0 and (c) V < 0. . . . . . 125

6.5 Schottky barrier height extracted from dark current measurements performed on Schottky photodetectors with (a) n-doped Si and (b) p-doped Si. . . . . . 128

6.6 Left column: graphene/n-Si; right column: graphene/p-Si. (a, b) Light current measurements (in logarithmic scale) performed on graphene Schottky photodetectors with $L_{device} = 150$ µm. (c, d) Extracted photocurrent as a function of the light power in the device. (e, f) Extracted responsivity as a function of the light power in the device. . . . . . 129

6.7 Measurements of the evolution of the dark current across a graphene/n-Si Schottky junction as a function of time for (a) a sample where transfer was performed in distilled water and (b) a sample where transfer was performed in diluted HF. . . . . . . . . . . . . . . . . . 131
6.8 Extraction of the Schottky barrier height of a graphene/n-Si Schottky junction (a) after sample annealing and (b) at varying temperature. . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 132
6.9 Left column: $L_{device} = 50$ µm; right column: $L_{device} = 100$ µm. (a, b) Light current measurements (in logarithmic scale) performed on graphene Schottky photodetectors with n-doped Si. (c, d) Extracted photocurrent (in logarithmic scale) as a function of the light power in the device. (e, f) Extracted responsivity as a function of the light power in the device. . . . . . . . . . . . . . . . . . . . . . . . . . . . 133
6.10 Schematic cross section of a graphene photodetector based on a $p - i - n$ junction in the Si waveguide and a Schottky junction between graphene and Si. . . . . . . . . . . . . . . . . . . . . . . . . . 134

# List of Tables


1.1 Summary of state-of-the-art modulators. . . . . . . . . . . . . . . . . 5

1.2 Summary of state-of-the-art graphene-based modulators. . . . . . . 37

1.3 Summary of state-of-the-art graphene-based waveguide photodetectors. . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 38

2.1 Equipment used for sample processing. . . . . . . . . . . . . . . . . . 43

2.2 Graphene delamination tests in OPD5262. . . . . . . . . . . . . . . . 46

2.3 Parameters extracted from Raman measurements performed on graphene devices after processing, with varying characteristics of the underlying Si doping. . . . . . . . . . . . . . . . . . . . . . . . . . 57

2.4 Comparison of parameters extracted from Raman spectra measured before and after graphene device processing. . . . . . . . . . . . . . 57

3.1 Summary of main passivation experiments published in literature. 63

3.2 Median values of mobility ($\mu_c$), contact resistance ($R_c$), position of graphene's neutrality point ($V_{NP}$) and hysteresis ($\Delta V_{NP}$) extracted from TLM measurements on the three samples passivated with passivation-last approach. . . . . . . . . . . . . . . . . . . . . 70

4.1 Summary of the level and type of Si doping used for the theoretical calculation shown in Fig. 4.9. . . . . . . . . . . . . . . . . . . . . . . 88

4.2 Summary of the level and type of Si doping on the three samples used for the experiment. . . . . . . . . . . . . . . . . . . . . . . . . . 90

4.3 Values of measured 3 dB frequency response ($f_{3dB}$) at 0 V DC bias on TE SLG EAMs for $L_{device}$ = 25, 40, 50 and 75 µm. The $f_{3dB}$ is higher for sample C (p-doped Si) and for smaller device lengths. . 92

4.4 Summary of the main figures of merit measured on the three types of SLG EAMs on sample C (p-doped Si). The values reported are for 75 µm-long devices. The FOM is calculated as ER/IL. The C-band TM SLG EAM offers the best trade-off. . . . . . . . . . . . . . . . 96

4.5 Waveguide width ($W_{wg}$) and device length ($L_{device}$) values used to fabricate the three WDM transmitters. Increasing $W_{wg}$ and $L_{device}$ is expected to increase the extinction ratio but also the device capacitance, and therefore to reduce the 3dB bandwidth. . . . . . . . 97
4.6 Insertion loss (IL) and extinction ratio (ER) at 8 $V_{pp}$. The values are averaged over 5 channels. WDM3 exhibits higher IL and ER due to the longer $L_{device}$. . . . . . . . . . . . . . . . . . . . . . . . 98
4.7 Total resistance ($R_{tot}$) and GOS capacitance ($C_{GOS}$) extracted from $S_{11}$ parameter fitting, simulated (from the fitted parameters in column 1 and 2) and measured $f_{3dB}$ at 0 V. The values are averaged over 5 channels. Due to the longer $L_{device}$, WDM3 exhibits higher RC constant, and therefore lower $f_{3dB}$. . . . . . . . . . . . . . . . . . 101

5.1 Summary of the main figures of merit measured on the three types of DLG EAMs fabricated with $Al_2O_3$. The FOM is calculated as ME/IL. The C-band TM DLG EAM offers the best trade-off. . . . 110
5.2 Summary of optimised $W_{DLG}$ and $d_{contact}$ values obtained for different light polarisations and operating wavelengths. . . . . . . . . 117

6.1 Light-induced resistance modulation for varying input laser power (set on laser) at fixed $V_{bias}$ = -1.5 V and $V_{gate}$ = 3 V. . . . . . . . 122
6.2 Values of ideality factor and Schottky barrier height at 0 V extracted from dark current measurements on Schottky photodetectors with n-doped and p-doped Si. . . . . . . . . . . . . . . . . . . . . . . . . 128
6.3 Summary of the main figures of merit measured on the different types of graphene photodetectors presented in this chapter. . . . . 134

# List of Acronyms

**1D** One-dimensional

**2D** Two-dimensional

**3D** Three-dimensional

## A

**AOC** Active optical cables

**ALD** Atomic layer deposition

## C

**CDF** Cumulative distribution function

**CMOS** Complementary metal-oxide-semiconductor

**CMP** Chemical mechanical planarisation

**CVD** Chemical vapour deposition

## D

**DBM** Difference between the medians

**DLG** Double-layer graphene

## E

**EAM** Electro-absorption modulator

**ER** Extinction ratio

## F

**FET** Field effect transistor

**FKE** Franz-Keldysch effect

**FOM** Figure of merit

**FSR** Free spectral range

**FWHM** Full width at half maximum

## F

**GOG** Graphene-oxide-graphene

**GOS** Graphene-oxide-silicon

## H

**hBN** Hexagonal boron nitride

**HSQ** Hydrogen silsesquioxane

## I

**I/O** Input Output

**IC** Integrated circuit

**ICP** Inductively coupled plasma

**IL** Insertion loss

**IPA** Isopropyl alcohol

## M

**MDM** Mode-division multiplexing

**ME** Modulation efficiency

**MGM** Metal-graphene-metal

**MGS** Metal-graphene-silicon

**MRR** Micro-ring resonators

**MZI** Mach-Zender interferometer

## O

**OVS** Overall visible spread

## P

**PB** Photo-bolometric

**PD** Photodetector

**PDM** Polarisation-division multiplexing

**PIC** Photonics integrated circuit

**PMMA** Poly methyl methacrylate

**PRBS** Pseudorandom binary sequence

**PTE** Photo-thermoelectric

**PV** Photovoltaic

## R

**RC** Resistance capacitance

**RF** Radio frequency

**RIE** Reactive ion etching

## S

**SDM** Space-division multiplexing

**SEM** Scanning electron microscopy

**SLG** Single-layer graphene

**SOG** Spin-on glass

**SOI** Silicon-on-insulator

## T

**TCAD** Technology computer aided design

**TE** Transverse electric

**TLM** Transfer length measurement/method

**TM** Transverse magnetic

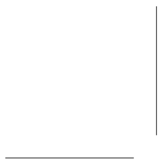
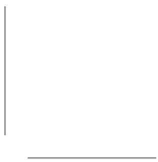
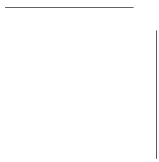
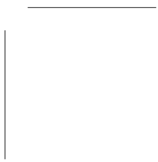
## V

**V**$_{pp}$ Voltage peak-to-peak

## W

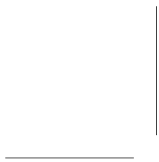
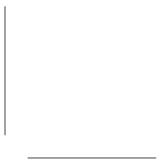
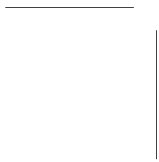
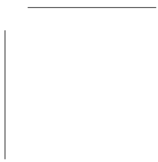
**WDM** Wavelength-division multiplexing

**WG** Waveguide

# List of Symbols

| | | |
|---|---|---|
| $\mu$ | Graphene Fermi level | eV |
| $\mu_C$ | Graphene carrier mobility | $cm^2Vs^{-1}$ |
| $v_F$ | Fermi velocity | m/s |
| $\hbar$ | Reduced Planck constant | Js |
| $I_D$ | Drain current | A |
| $V_D$ | Drain voltage | V |
| $V_G$ | Gate voltage | V |
| $V_{NP}$ | Graphene Neutrality Point | V |
| $n_0$ | Fixed number of charged carriers in graphene | $cm^{-2}$ |
| $n_s$ | Accumulated number of charged carriers in graphene | $cm^{-2}$ |
| $n^*$ | Graphene's impurity carrier density | $cm^{-2}$ |
| $\epsilon_0$ | Vacuum permittivity | $F/cm^2$ |
| $\epsilon$ | Dielectric constant | - |
| $q$ | Elementary charge | C |
| $t_{ox}$ | Oxide thickness | nm |
| $R_C$ | Contact resistance | Ω µm |
| $R_{graC}$ | Graphene contact resistance | Ω µm |
| $R_{SiC}$ | Silicon contact resistance | Ω µm |
| $R_{gra}$ | Graphene sheet resistance | $\Omega/\square$ |
| $R_{Si}$ | Silicon sheet resistance | $\Omega/\square$ |
| $f_{3dB}$ | 3 dB bandwidth | GHz |

# Samenvatting

In een tijdspanne van één minuut melden zich één miljoen personen aan op Facebook, wisselen mensen 41.6 miljoen berichten uit op WhatsApp of Messenger, behandelt Google ruim 3.8 miljoen zoekopdrachten, terwijl 694.444 uren worden bekeken op Netflix [27]. Deze cijfers stijgen elke jaar en er wordt voorspeld dat het verkeer in datacenters tegen 2021 meer dan 20.6 ZB/jaar (1 ZB = 1,000,000,000,000 GB) zal bereiken, een verdrievoudiging in vergelijking met 2016 [1]. Bij deze cijfers stellen zich twee vragen. Hoe kunnen we deze hoeveelheid aan data verzenden en bewerken en tegelijkertijd het energieverbruik laag houden? En hoe gaan we de datasnelheid verhogen?

Het antwoord is het gebruik van optische interconnecties op alle hiërarchische communicatieniveaus. Optische interconnecties hebben een revolutie teweeggebracht in het telecommunicatieveld: ze laten toe te voldoen aan de eisen van datanetwerken met hoge snelheid en hoge bandbreedte en ze worden reeds ingezet voor datatransmissie over lange afstand en communicatie tussen machines in datacenters. De logische volgende stap om de datasnelheid te blijven verhogen is de schaling van optische interconnecties om elektrische interconnecties te vervangen voor communicatie binnen een chip of tussen verschillende chips. Het doel van deze transceivers is om de elektrische data te converteren in optische data voor transmissie of om optische data te ontvangen en te converteren in elektrische data voor verwerking of opslag binnenin de chip. Een transceiver omvat een optische lichtbron, modulatoren om het signaal van elektrisch naar optisch om te zetten voor uitvoer, fotodetectoren om het ingangssignaal van optisch naar elektrisch om te zetten en de elektronische drivers voor deze fotonische componenten. Deze fotonische IC's zijn al gedemonstreerd op platforms op basis van verschillende materialen, zoals III-V-materialen, siliciumnitride (SiN) of silicium-op-isolator (SOI) [28–32]. Onlangs is grafeen naar voren getreden als een interessant nieuw materiaal voor toepassingen in de fotonica en is het onderwerp geweest van een groot aantal theoretische en experimentele studies. Grafeen is een tweedimensionaal materiaal met een hoge absorptie in de telecommunicatiebanden. Het vertoont een hoge treksterkte, flexibiliteit, transparantie, hoge geleidbaarheid en snelle dragerdynamiek. In deze thesis wordt grafeenintegratie in de fotonica bestudeerd, meer specifiek in modulatoren en fotodetectoren.

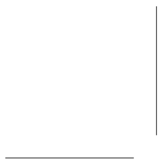
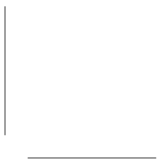
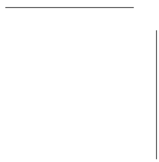
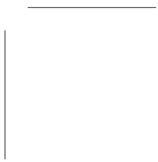
Optische componenten uit grafeen zijn gebaseerd op een grafeenlaag die bovenop een golfgeleider is getransfereerd. Grafeen is het actieve absorberende materiaal, terwijl de golfgeleider, in dit geval bestaande uit Si, het licht leidt. De fabricage van dergelijke componenten is op zichzelf een uitdaging vanwege het bidimensionale karakter van grafeen. Het eerste doel van deze thesis was om een 'standaard' fabricagerecept te ontwikkelen om op grafeen gebaseerde componenten te produceren. Verschillende uitdagingen, zoals grafeendelaminatie, moesten worden overwonnen om een succesvol recept uit te werken. Dit recept werd gebruikt om testcomponenten te vervaardigen met verschillende soorten en niveaus van Si-doping. Uit vergelijkend onderzoek van elektrische metingen, uitgevoerd op transmissielijnstructuren, blijkt dat het type en niveau van Si-doping geen detecteerbaar effect heeft op de elektrische eigenschappen van grafeen. Deze conclusie werd bevestigd door Raman spectroscopie. Daarna werd gefocust op de ontwikkeling van een proces met een encapsulerend materiaal om grafeen te beschermen tegen externe factoren, zoals polymeerresten of omgevingslucht, en om hysteretisch gedrag in grafeen componenten te verminderen. Ten eerste werd een 'passivation-last' benadering toegepast, waarbij het 'standaard' fabricagerecept werd gebruikt om grafeen componenten te fabriceren en het encapsulerend materiaal aan te brengen op het einde van de proces. Verschillende passiverende materialen, zoals waterstofsilsesquioxaan (HSQ), spin-on glas (SOG) en aluminiumoxide ($Al_2O_3$), werden getest door middel van elektrische metingen op gepassiveerde grafeen veldeffecttransistoren (FET's) op drie verschillende momenten. $Al_2O_3$ werd geïdentificeerd als het beste materiaal om het hysteretisch gedrag te verminderen en de p-doping in grafeen te behouden. Het behoud van de p-doping is belangrijk vanwege het uiteindelijke doel om gepassiveerde enkellaags grafeen (SLG) elektroabsorptiemodulatoren (EAM's) te fabriceren. Zoals wordt aangegeven in de volgende paragraaf, is p-gedopeerd grafeen ideaal om een hoge snelheid met lage DC-bias te bereiken op SLG EAM's. Later werd een passivation-first' benadering ontwikkeld, waarbij het encapsulerend materiaal aan het begin van de proces op het monster werd afgezet om grafeen tijdens de fabricage te beschermen tegen externe besmetting. Een Si-kiemlaag werd gebruikt als nucleatielaag om de afzetting van $Al_2O_3$ te bevorderen. Met deze benadering werd een betere uniformiteit van de prestaties bekomen. Om deze reden werd hetzelfde recept gebruikt om $Al_2O_3$-gepassiveerde SLG EAM's te fabriceren. In vergelijking met niet-gepassiveerde SLG EAM's werd naast een uitstekende stabiliteit in de statische en hogesnelheidsprestaties over een tijdsperiode van twee maanden ook een verminderde hysterese waargenomen.

Na het aanpakken van fabricage-uitdagingen, werd de focus verlegd naar de optimalisatie van grafeen-gebaseerde modulatoren. Een theoretisch model werd ontwikkeld om het statische en hogesnelheidsgedrag van SLG EAM's te beschrijven op basis van een grafeen-oxide-silicium structuur. Het theoretische model toonde aan dat p-gedoteerd grafeen in combinatie met p-gedoteerd silicium een hoge modulatiebandbreedte bij lage DC-bias mogelijk maakt. Met deze configuratie hebben we 75 µm-lange TM EAM's gedemonstreerd die in de

O-band en in de C-band werken. De O-band EAM vertoonde een extinctieratio van 3,1 dB en een 3 dB bandbreedte van 16,0 GHz bij 1 V DC bias. De C-band EAM vertoonde 6,5 dB extinctieratio en 14,2 GHz 3 dB bandbreedte bij 0 V DC bias. Daarnaast werden open oogdiagrammen gemeten tot 50 Gbit/s met 2,5 $V_{pp}$ en -0,5 V DC bias bij een golflengte van 1560 nm. Vervolgens werden SLG EAM's geintegreerd met n-gedopeerde Si golfgeleiders in drie vijfkanaals golflengtemultiplexing (WDM)-zenders. Deze vertoonden uniforme prestaties over vijftien SLG EAM's. Daarnaast werden er open oogdiagrammen gemeten tot 25 Gbit/s in de C-band op elk kanaal. Dit demonstreerd potentieel voor gegevensoverdracht bij 5 x 25 Gbit/s.

Vervolgens werden dubbellaagse grafeen (DLG) EAM's bestudeerd als alternatief voor SLG EAM's. Na het uitvoeren van een theoretische analyse werden de statische prestaties van de twee componenttypes vergeleken. Er werd ontdekt dat DLG EAM's meer dan het dubbele van de extinctieratio bereiken in vergelijking met SLG EAM's, maar dat deze lijden aan insertieverlies. Met $Al_2O_3$ als dielectricum tussen de twee grafeenlagen, werd een extinctieratio van 26 dB en een bandbreedte van 2,2 GHz bereikt voor DLG EAM's. Slechte componentstabiliteit en aanzienlijk hysteretisch gedrag gaven echter aan dat een verdere optimalisatie van de proces nog steeds nodig is. Er werden manieren voorgesteld om de fabricageopbrengst te verhogen door specifieke verwerkingsstappen te optimaliseren en de prestaties te verbeteren door de geometrie van het component te optimaliseren.

Ten slotte werd er gefocust op grafeen-gebaseerde fotodetectoren. Verschillende soorten fotodetectoren werden bestudeerd, waarbij de beste resultaten werden behaald met behulp van een grafeen-Si Schottky-diodeconfiguratie. Er werd een fotoresponsiviteit van 12,8 mA/W bereikt bij een DC-bias van -2 V met TM-gepolariseerd licht en een 100 µm-lang component.

# Summary

In the time span of one minute, one million people log in on Facebook, people exchange 41.6 million messages on WhatsApp or Messenger, Google handles 3.8 million search queries, while 694,444 hours are watched on Netflix [27]. These numbers are increasing every year and it is forecast that traffic in data centers will reach 20.6 ZB/year (1 ZB = 1,000,000,000,000 GB) by 2021, three times the amount of 2016 [1]. These numbers should raise two questions. How are we going to transmit and process this massive amount of data while keeping the power consumption low? And how are we going to keep increasing the data transfer speed?

The answers lie in the adoption of optical interconnects at all hierarchical communication levels. Optical interconnects have revolutionised the telecommunications field: they allowed to meet the requirements of high-speed and high-bandwidth data networks and they are currently deployed for long-distance data transmission and communication between machines inside data centers. Scaling down optical interconnects to substitute electrical interconnects for communication within a chip or between different chips is the natural next step to keep increasing the transfer speed. The vision of optical interconnects includes the implementation of opto-electronic transceivers at the input and output of a chip. The goal of these transceivers is to convert the electrical data into optical for transmission or to receive optical data and convert it into electrical data for processing or storage in the chip. A transceiver includes an optical light source, modulators to convert the signal from electrical to optical for output, photodetectors to convert the input signal from optical to electrical, and the electronic drivers for these photonic components. Photonics ICs have been demonstrated on platforms based on different materials, such as III-V materials, silicon nitride (SiN) or silicon-on-insulator (SOI) [28–32]. Recently, graphene has emerged as an interesting new material for applications in photonics and has been the subject of a vast number of theoretical, as well as experimental studies. Graphene is a bidimensional material with high absorption in the telecommunication bands. It shows high tensile strength, flexibility, transparency, high conductivity and fast carrier dynamics. In this thesis, graphene integration in photonics integrated devices is studied, namely in modulators and photodetectors.

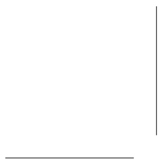
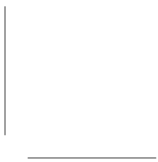
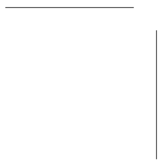
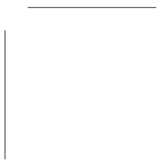
Graphene photonics devices are based on a graphene layer transferred on top of a waveguide. Graphene is the active absorbing material, while the waveguide, in our case made in Si, simply guides the light. The fabrication of such devices is a challenge on its own due to graphene's bidimensional nature. The first effort of this thesis was to develop a 'standard' fabrication recipe to process graphene-based devices. Various challenges, such as graphene delamination, had to be overcome to achieve a final recipe, which was used to fabricate samples with different types and levels of Si doping. Results of electrical measurements performed on backgated linear transfer length measurement (TLM) structures were compared and it was seen that the type and level of Si doping have no detectable effect on graphene's electrical properties. These results were confirmed with Raman spectroscopy. Afterwards, we focused on the development of a fabrication flow using an encapsulating material to protect graphene from external factors, such as polymer residues or ambient air, and to reduce hysteretic behaviour in graphene devices. First, a passivation-last approach was employed, were the 'standard' process flow was used to fabricate graphene devices and the encapsulating material was deposited or spin-coated at the end of the process flow. Different passivating materials, such as hydrogen silsesquioxane (HSQ), spin-on glass (SOG) and aluminum oxide ($Al_2O_3$), were tested by means of electrical measurements performed on passivated graphene field effect transistors (FETs) at different moments in time. $Al_2O_3$ was identified as the material that allows to reduce hysteretic behaviour, while preserving p-doping in graphene. The latter is important due to the ultimate goal of fabricating passivated single-layer graphene (SLG) electro-absorption modulators (EAMs). As explained in the next paragraph, p-doped graphene is ideal for high-speed operation at low DC bias of SLG EAMs. Later, a passivation-first approach was developed, where the passivating material was deposited on the sample at the beginning of the process flow in order to protect graphene from external contamination during fabrication. A Si seeding layer was used as nucleation layer to aid the deposition of $Al_2O_3$. A better uniformity of performance was measured across the sample fabricated with this approach. We therefore used the same recipe to fabricate $Al_2O_3$-passivated SLG EAMs, obtaining excellent stability in the device DC and high-speed performance over a time span of two months and significantly reduced hysteresis compared to unpassivated SLG EAMs.

After tackling fabrication challenges, the focus was moved to the optimisation of graphene-based modulators. A theoretical model was developed to describe the static and high-speed behaviour of SLG EAMs based on a graphene-oxide-silicon structure. The theoretical model allowed to identify that p-doped graphene combined with p-doped silicon enables high-speed operation at low DC bias. Using this configuration, we demonstrated 75 µm-long TM EAMs operating in the O-band and in the C-band. The O-band EAM exhibited 3.1 dB extinction ratio and 16.0 GHz 3 dB bandwidth at 1 V DC bias, while with the C-band EAM we achieved 6.5 dB extinction ratio and 14.2 GHz 3 dB bandwidth at 0 V DC bias. In addition, we measured open eye diagrams up to 50

Gbit/s using 2.5 $V_{pp}$ and -0.5 V DC bias at a wavelength of 1560 nm. We then integrated SLG EAMs with n-doped Si waveguides into three five-channel wavelength division multiplexing (WDM) transmitters and we demonstrated uniform device performance across fifteen SLG EAMs. We measured open eye diagrams up to 25 Gbit/s in the C-band on each channel, thus showing potential for data transmission at 5 x 25 Gbit/s.

Next, we studied double-layer graphene (DLG) EAMs as an alternative to SLG EAMs. After performing a theoretical analysis, we compared the static performance of the two device types. We found that DLG EAMs allow to achieve more than double the extinction ratio compared to SLG EAMs, but suffer in insertion loss. Using $Al_2O_3$ as spacer between the two graphene layers, we reached an extinction ratio of 26 dB and a 3 dB frequency response of 2.2 GHz for DLG EAMs. However, poor device stability and significant hysteretic behaviour indicated that a further improvement in the fabrication flow was still necessary. We suggested ways to increase the fabrication yield by optimising specific processing steps and to improve the performance by optimising the device geometry.

Last, we focused on graphene-based photodetectors. Different types of photodetectors were studied, achieving the best results using a graphene-Si Schottky diode configuration. Using TM-polarised light and a 100 µm-long device, we reached a photoresponsivity of 12.8 mA/W at a DC bias of -2 V.

# Chapter 1

# Introduction

## 1.1 Optical interconnects

In the sixty years since the introduction of the first electronic integrated circuit (IC), there can be no doubt that it has revolutionised our lives. Electronic circuits permeate every part of our existence: they can be found in schools, homes, universities, industries, hospitals, phones, means of transport etc. As the 21st century is well on its way, new technologies are emerging to complement, and in some cases replace, the electronic interconnects and circuits we have come to know. The exponential growth of social networking, cloud computing and big data applications in recent years demands an increase in traffic speed and bandwidth that electronics alone cannot match [33]. In the time span of one minute, one million people log in on Facebook, people exchange 41.6 million messages on WhatsApp or Messenger, Google handles 3.8 million search queries, while 694,444 hours are watched on Netflix [27]. These numbers are increasing every year and it is forecast that traffic in data centers will reach 20.6 ZB/year (1 ZB = 1,000,000,000,000 GB) by 2021, three times the amount of 2016 (Fig. 1.1) [1]. An additional challenge is posed by the need to keep the power consumption low while handling such massive amount of data. Data centers in the world have dramatically increased in number in the past 10 to 15 years. In 2016 their energy consumption amounted to about 3% of the global electricity supply, more than the UK's total consumption, and accounted for about 2% of total greenhouse emissions, equal to the airline industry [34]. The need to transfer, store and process this data at high speed, while keeping the power consumption low ($< 1$ pJ/bit), has been the driver for the development and implementation of optical interconnects as replacement for electrical ones [35, 36].

Different hierarchical communication levels exist in data centers: intra-

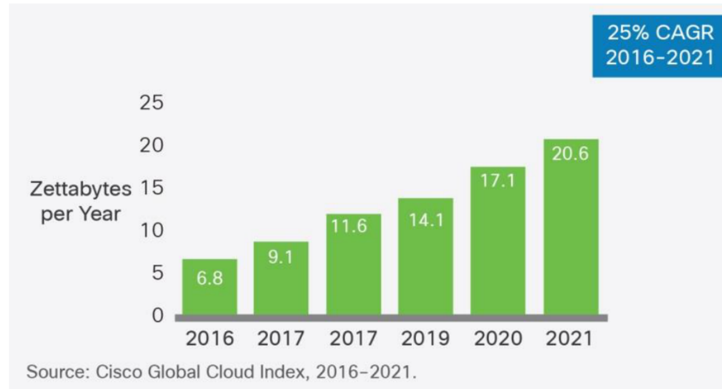



**Figure 1.1:** Global data center IP traffic growth reported in Cisco Global Cloud Index: Forecast and Methodology report for 2016-2021 [1].

chip, chip-to-chip (on a board), board-to-board (in a cabinet), backplane-to-backplane (in a machine) and rack-to-rack (machine-to-machine). Optical technology is already employed in optical connection cables called Active Optical Cables (AOC) for rack-to-rack and backplane-to-backplane communication. Rack-to-rack interconnections have to cover a few meters distance for close proximity servers up to kilometer-range distance in big data centers for remote high-bandwidth interconnection between different rooms. The advancing of AOC technology meets a bottleneck at chip-to-chip and intra-chip interconnections, where data is still handled by electrical interconnect wires that cannot match the speed of optical interconnects [37]. For instance, transferring data from a computer's central processor to its memory is a well-known bottleneck, where the electrical wires cannot move the data fast enough to keep the processor busy.

The main issue affecting electrical interconnects is signal attenuation, caused by the resistance of the wires and by dielectric losses. In addition, losses in electrical wires are frequency-dependent, therefore higher frequency components experience higher attenuation compared to lower frequency ones, leading to signal distortion. The simplest solution to increase the information capacity of a given wire is to increase its cross-sectional size, which reduces the resistance (R) but also increases the cost. However, the greater wire cross-section becomes a problem inside data centers because, due to limited space, the density of wiring is limited. If the cross-section is decreased, the resistance increases while the capacitance (C) remains constant, since it depends on the shape of the cross-section. This leads to a higher RC constant, which limits the speed of RC-limited lines. Finally, interconnects are also affected by cross-talk between densely-packed wires, which affects signal quality [37, 38].

These problems can be solved with the adoption of optical interconnects at all hierarchy communication levels, allowing to increase the transfer speed of

more than 50 times compared to copper connections by using less power. In addition, losses in optical media are independent of the modulation speed and the cross-talk between adjacent optical fibers is negligible.

## 1.2 Silicon Photonics

The vision of optical interconnects for on-board connections includes the implementation of opto-electronic transceivers at the chip inputs/outputs (I/Os). The goal of these transceivers is to convert the electrical data into optical for transmission or to receive optical data and convert it into electrical data for processing or storage in the chip. A typical transceiver includes an optical light source, modulators to convert the signal from electrical to optical for output, photodetectors to convert the input signal from optical to electrical, and the electronic drivers for these photonic components. Alternatively to modulators, direct modulation of lasers is a viable option, being cheaper and simpler than external modulation. However, direct modulation suffers from non-linear effects, bit-rate limitations caused by the turn-on delay and chirp effects. In addition, modulation is generally slower than in external modulators, as the highest possible modulation frequency is limited by the resonance frequency of the laser. Photonics ICs have been demonstrated on platforms based on different materials, such as III-V materials, silicon nitride (SiN) for passive components or silicon-on-insulator (SOI) [28–32]. Each platform has different advantages and disadvantages, but the SOI platform has attracted particular interest. Silicon photonics refers to the approach of designing optical devices employing silicon as an optical medium that photons can use to transfer enormous data at high speed. The wide use of silicon in electronics leads to low cost fabrication of silicon photonics circuits, as they can be fabricated using the already mature CMOS technology. In addition, silicon is a high refractive index material thus offering high index contrast with its surrounding (silicon dioxide

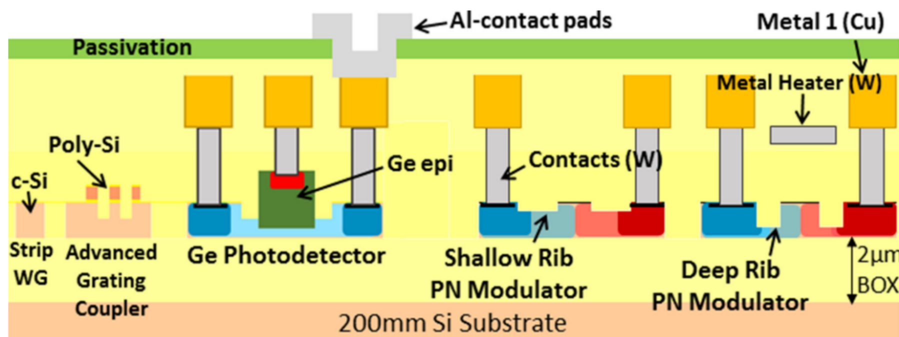



**Figure 1.2:** Schematic cross-section of imec's silicon photonics platform, with the basic passive and active devices. Taken from [2].

or air), allowing to highly confine light in a silicon waveguide and therefore to downscale the device dimensions. Silicon photonics technology for optical communications is developed to operate at the standard telecommunication wavelength bands centered around 1.55 µm (C-band) or 1.33 µm (O-band).

The silicon photonics platform in imec uses SOI wafers with a diameter of 200 mm or 300 mm [2, 32]. The tools and technological processes developed for fabrication of CMOS electronic chips are exploited for silicon photonics chips as well. On each SOI wafer, the top crystalline silicon layer is 220 nm-thick and the buried oxide (BOX) has a thickness of 2 µm. The waveguides are patterned using standard CMOS-compatible 193 nm lithography. The 300 mm platform offers the additional advantage of 193 nm immersion lithography. The top silicon layer of the SOI is used to form passive and active components such as waveguides, multiplexers/de-multiplexers, fiber grating couplers and silicon-based modulators. Three different silicon waveguide patterning steps are employed to allow maximum processing flexibility, with etch depths of 220 nm, 150 nm and 70 nm. The silicon can be n-doped or p-doped and three implantation steps are available to optimise the doping level to the type of device. After silicon patterning, the waveguides are usually planarised using an oxide cladding. If Ge-based devices are fabricated, Ge is epitaxially grown to enable photodetectors in the Si photonics platform. Typical CMOS contact and metallisation processing is used to contact the active devices. Fig. 1.2 shows the schematic cross-section of imec's Si photonics platform, with the basic passive and active devices [2].

In the next two sections, we will review the state-of-the-art modulators and photodetectors based on the silicon photonics platform.

### 1.2.1 Modulators

Modulators are devices used to manipulate a property of light and are used to convert an electrical signal into an optical one. Depending on the properties of the material used to modulate the light beam, modulators are divided into

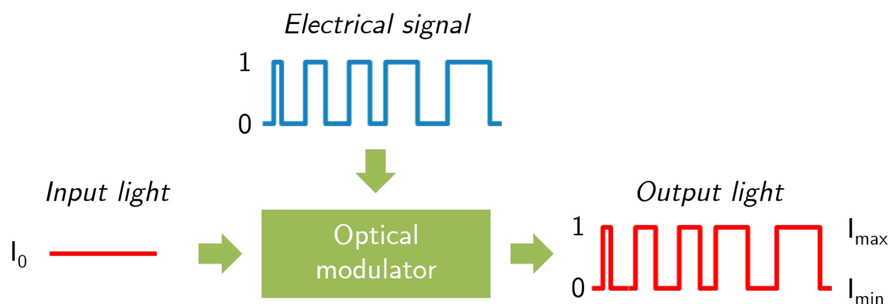



**Figure 1.3:** Schematic representation of the working principle of a modulator.

**Table 1.1:** Summary of state-of-the-art modulators.

| Modulator type | Ref. | Footprint (µm$^2$) | Optical BW (nm) | IL (dB) | Static ER (dB) | Dynamic power (fJ/bit) | 3dB BW (GHz) | Bit Rate (Gb/s) |
|---|---|---|---|---|---|---|---|---|
| Si MRR | [39] | 5×5 | <1 nm | 1 | 9 | 0.9 | 20 | 44 |
| Si MRR | [40] | 10×10 | <1 nm | 3.8 | 4.4 | - | 42 | 60 |
| Si MRR | [41] | 10×10 | <1 nm | 1.2 | - | 600* | 50 | 112 |
| Si MZI | [42] | 750×500 | - | 6.5 | 30 | - | 28 | 60 |
| Si MZI | [2] | 2000×500 | 80 | 5.6 | 2.3 | 720 | 27 | 56 |
| Si MZI | [43] | - | - | - | - | - | - | 50 |
| GeSi EAM | [44] | 80×10 | 10 | 4.4 | 4 | - | $> 50$ | 100 |
| Ge EAM | [45] | 40×10 | 22.5 | 4.9 | 4.6 | 12.8 | $> 50$ | 56 |

* Includes power consumption of CMOS drivers

two groups: absorptive modulators and refractive modulators. In absorptive modulators the absorption coefficient of the material is changed, in refractive modulators the refractive index of the material is changed. Fig. 1.3 shows the operating principle of an electro-absorption modulator. The intensity of the incoming laser beam is modulated via an electric voltage by causing a change in the absorption spectrum of the active material. Two of the most important figures of merit of a modulator are the insertion loss and the extinction ratio. The insertion loss (IL) is the minimum loss that results from the insertion of a device in a transmission line and should be as small as possible. It is the ratio between the power of the input optical signal ($I_0$) and the maximum power ($I_{max}$) of the output optical signal. The extinction ratio (ER) is the ratio between maximum ($I_{max}$) and minimum ($I_{min}$) power of the output optical signal. The greater the ER, the easier it becomes to distinguish between the 1's and 0's of the output signal. Other important figures of merit for modulators are operation speed (3 dB bandwidth), bit rate, drive voltage, power consumption, optical bandwidth and temperature stability.

The first demonstration of a silicon photonics modulator with gigaherts bandwidth in the early 2000s represented a turning point in the development of silicon photonics technologies [46]. Since then, many approaches have been considered to realise silicon-based modulators and to continuously improve modulation efficiency, bandwidth and insertion loss. In silicon, modulation of the refractive index is achieved via the free carrier plasma dispersion effect. A metal-oxide-silicon (MOS) capacitor phase shifter, a p-n diode or a p-i-n diode are employed to modulate the charge density in silicon [2, 46]. This effect has been exploited to build high-speed silicon modulators based on micro-ring resonators (MRRs) [39–41, 47] and Mach-Zender interferometers

**Figure 1.4:** Schematic representation of the working principle of a photodetector.

(MZIs) [42, 43, 48, 49]. MRR modulators offer small device footprint and low power consumption, but they suffer from very narrow optical bandwidth due to their resonant nature. In addition, due the thermo-optic effect in Si, they are very sensitive to process and thermal variations, often requiring thermal stabilisation through heaters, increasing the overall power consumption. MZI modulators exhibit high-speed operation and wider optical bandwidth than MRR modulators. However, they are affected by high power consumption and large footprint. In order to overcome these limitations, other materials have also been studied to complement silicon, such as GeSi and Ge. GeSi modulators have been shown to operate at 100 Gbit/s [44]. They have wider optical bandwidth than MRR modulators and, at the same time, smaller footprint and lower power consumption than MZI modulators. Ge modulators, based on the Franz-Keldysch effect (FKE), have also been demonstrated up to 56 Gbit/s [45]. They are compact and high-speed, but they are wavelength-dependent and offer an optical bandwidth of ∼20 nm. Table 1.1 reports a summary of state-of-the-art high-speed modulators.

### 1.2.2 Photodetectors

Photodetectors are devices used for the detection of light. Photodetectors deliver an electrical output signal, such as a voltage or an electric current, which is proportional to the input optical power (Fig. 1.4). Many types of photodetectors exist, such as photodiodes, metal-semiconductor-metal (MSM) photodetectors, phototransistors etc. A very important figure of merit for photodetectors is the responsivity, which measures the electrical output per optical input. Another important parameter is the dark current, or the current which flows in the device when there is no optical input. This quantity should be minimised to improve the sensitivity of the detector. Other important figures of merit are operation speed (3 dB bandwidth), bit rate and operating bias.

Photon energies at telecom wavelengths ($\lambda$ = 1.3-1.6 µm) are not sufficient for direct (band-to-band) photodetection in silicon, therefore the integration of other materials is necessary to build photodetectors. In silicon photonics, they are typically realised using Ge [50] or III-V materials, such as InGaAs [51, 52]. The development of Ge photodetectors experienced a dramatic change when the use of single-crystal bulk Ge was replaced with epitaxially-grown Ge on Si. The use of Si as a substrate reduced the fabrication costs and allowed the

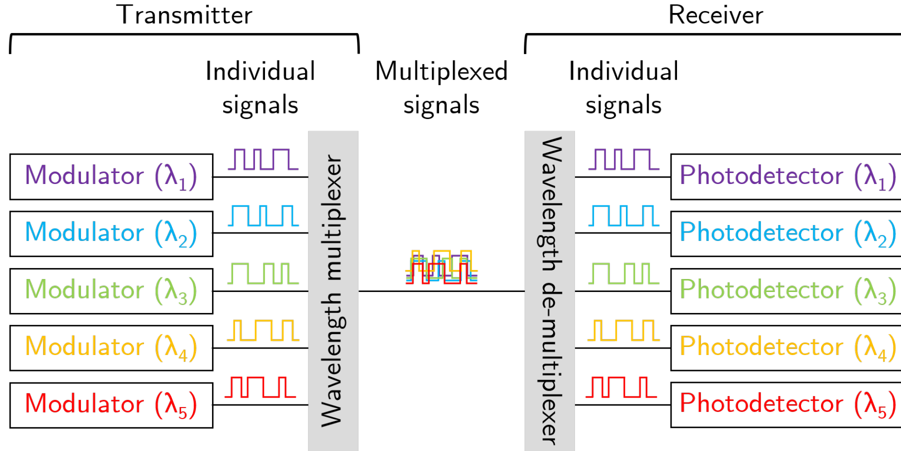



**Figure 1.5:** Schematic representation of a wavelength division multiplexing transceiver system.

introduction of this material into the optical communications field. On-chip integrated Ge photodetectors [53–59] are now part of the standard library of components in silicon photonics foundries [32, 60]. However, the integration of Ge on Si is complex. The main challenge to obtain good quality Ge on Si is the 4.2% lattice mismatch between the two elements [50]. Responsivities have been demonstrated up to 6.54 A/W [59] and 3 dB bandwidths have been measured up to 67 GHz [55–57] or up to 100 GHz when combined with plasmonics [58].

### 1.2.3 Wavelength-division multiplexers

To meet the demand set by the exponential growth of global data center traffic, as seen at the beginning of this chapter, the Ethernet Alliance estimated that data center operators will have to upgrade their network to 1.6 Tb/s by 2022 [61]. This is certainly a challenging task which is not easy to achieve only with the development of single devices. An effective solution is represented by advanced multiplexing technologies, where multiple signals are combined into one signal over a shared medium. For example, several telephone calls may be carried using only one wire. Multiplexing originated in telegraphy in the 1870s, and is now widely applied in telecommunications. Different multiplexing solutions exist, such as wavelength-division multiplexing (WDM), space-division multiplexing (SDM), mode-division multiplexing (MDM) and polarisation-division multiplexing (PDM) [62, 63].

Wavelength-division multiplexing uses different channels to carry signals at different wavelengths in a single optical fiber or waveguide simultaneously (Fig. 1.5) [64, 65]. Space-division multiplexing [66] is based on multi-core waveguides, mode-division multiplexing [67] on multiple guided modes, and

polarisation-division multiplexing uses two orthogonal polarisations together. These approaches have independent degrees of freedom and can be combined to form hybrid multiplexing systems with capacity up to Pbit/s [63]. Among these, wavelength-division multiplexing (WDM) links, enabled by low loss, broadband and low power consumption modulators, have been one of the most successful technologies. WDM allows to exploit the full bandwidth of existing optical fibers, leading to a reduced construction cost. In addition, it is simple to implement as channels can be flexibly added or removed, and the active optical equipment is shared by the different channels. Important figures of merit of WDM transmitters are the grid spacing, which is the spacing in optical frequency (or wavelength) between adjacent channels, the crosstalk between adjacent channels, the insertion loss and the extinction ratio of each channel.

## 1.3 Graphene

Graphene, a novel bidimensional material, has been studied in recent years for applications in photonics. Graphene photonics has the potential to be a low-cost, compact technology and graphene can potentially enable devices with extremely wide optical bandwidth and high-speed operation [68]. In the next sections we will dig deeper into the wonders of this 2D material and review its integration in photonics to build modulators and photodetectors.

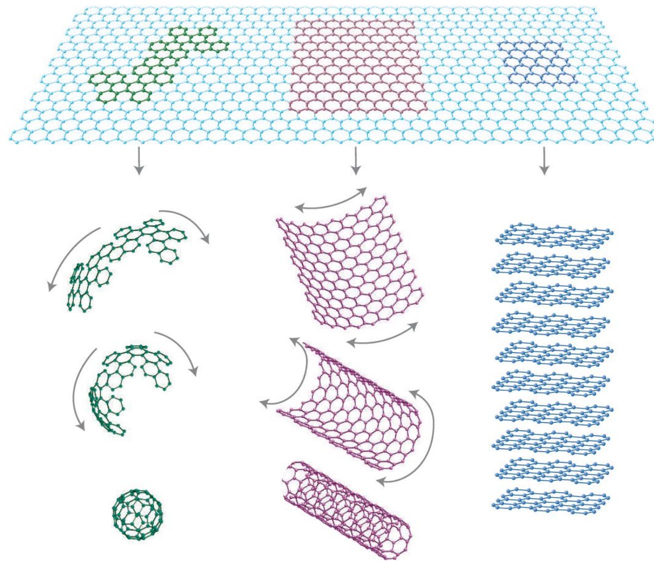


**Figure 1.6:** Graphene is the building block for carbon-based materials of other dimensionalities. From left to right: graphene wrapped up into 0D buckyballs, rolled into 1D nanotubes or stacked into 3D graphite. Taken from [3].

Called a “supermaterial”, graphene is being studied all over the world by researchers trying to better understand it and find its best application [7]. The easiest way to describe graphene is as a single layer of graphite, the material we all know because it makes up the core of pencils we use every day to write. Graphite is made of several layers, graphene layers, stacked on top of each other. In the very same act of writing, we remove some layers from the graphite core of our pencils and transfer them on a piece of paper. If we are lucky, it can happen that we produce a single layer of graphene. Isolating graphene from a piece of graphite is, however, not so trivial. In 2004, Andre Geim together with his then PhD student Konstantin Novoselov managed to isolate a single layer of graphene for the first time in a controlled way, using a mechanical exfoliation method [69]. When graphene is isolated from graphite it takes on some phenomenal properties. It shows high tensile strength, flexibility, transparency, high conductivity and impermeability to most gases and liquids.

In the next few subsections, we will detail graphene properties and methods to grow and transfer it.

### 1.3.1 Graphene properties

Graphene is a monolayer of carbon atoms tightly packed into a two dimensional honeycomb lattice. It is the basic building block for graphitic materials of all other dimensionalities: it can be wrapped up into 0D fullerenes, rolled into 1D nanotubes or stacked into 3D graphite, where graphene layers are held together by van der Waals interactions (Fig. 1.6) [3].

In order to understand the *atomic structure* of graphene, it is useful to first gain an understanding of the structure of elemental carbon. Carbon electrons (Z = 6) occupy the $1s^2$, $2s^2$, $2p_x$ and $2p_y$ atomic orbitals (Fig. 1.7a). When forming bonds with other atoms, one of the $2s$ electrons is promoted into the empty $2p_z$ orbital, resulting in the formation of hybrid orbitals. In diamond, the $2s$ energy level hybridises with the three $2p$ levels to form four energetically equivalent $sp^3$-orbitals, that are occupied with one electron each (Fig. 1.7b). In graphite, only two of the three $2p$-orbitals take part to the hybridisation, forming three $sp^2$-orbitals (Fig. 1.7c). The $sp^2$-orbitals form in-plane $\sigma$-bonds, that are 1.42 Å-long, hence they lie symmetrically in the $xy$ plane at 120° angles. The remaining $2p$-orbital forms interplane $\pi$-bonds with the other $2p$-orbitals from the other graphene layers that compose the graphite. The in-plane $\sigma$-bonds are stronger than the interplane $\pi$-bonds, therefore graphite is characterised by an easy shearing along the layer plane.

Graphene is made out of carbon atoms arranged in a hexagonal structure, but this structure can also be seen as a triangular lattice with a basis of two atoms per unit cell (Fig. 1.8a). The unit cell of graphene is a rhombus with a basis of two nonequivalent carbon atoms, A and B (black and white in the figure). In cartesian coordinates the real space basis vectors of the unit cell $a_1$ and $a_2$ are written as

$$a_1 = \frac{a}{2}\left(3, \sqrt{3}\right) \text{ and } a_2 = \frac{a}{2}\left(3, -\sqrt{3}\right) \tag{1.1}$$

with $a \approx 1.42$ Å. The corresponding reciprocal lattice and the first Brillouin zone are displayed in Fig. 1.8b. The high symmetry points $\Gamma$, $M$, $K$ and $K'$ are also indicated in Fig. 1.8b. In graphene, the two points $K$ and $K'$ are of particular importance and are known as Dirac points. Their coordinates in reciprocal space are written as [5]

$$K = \left(\frac{2\pi}{3a}, \frac{2\pi}{3\sqrt{3}a}\right) \text{ and } K' = \left(\frac{2\pi}{3a}, -\frac{2\pi}{3\sqrt{3}a}\right) \tag{1.2}$$

The scientific and technological interest in graphene has mainly been driven by its interesting *electronic properties* [5]. Graphene is a semi-metal, or zero-gap semiconductor. Its conduction and valence bands meet at the Dirac points (Eq. 1.2), which are the six points at the corners of its Brillouin zone [70]. As explained, each carbon atom in the graphene lattice is connected to its three nearest neighbours by strong in-plane covalent $\sigma$-bonds. The $2p_z$-orbital, occupied by the fourth valence electron, is oriented perpendicular to the plane of the graphene sheet and does not interact with the in-plane $\sigma$-electrons. The $2p_z$-orbitals from neighbouring atoms overlap, resulting in delocalised $\pi$ (occupied or valence) and $\pi^*$ (unoccupied or conduction) bands. Most of the electronic properties of graphene can be understood in terms of these $\pi$-bands [4].

The band structure of graphene can be modeled by a simple tight-binding model with nearest-neighbour hopping only and considering a single $\pi$ electron per atom [5]. The resulting dispersion relation can be written as

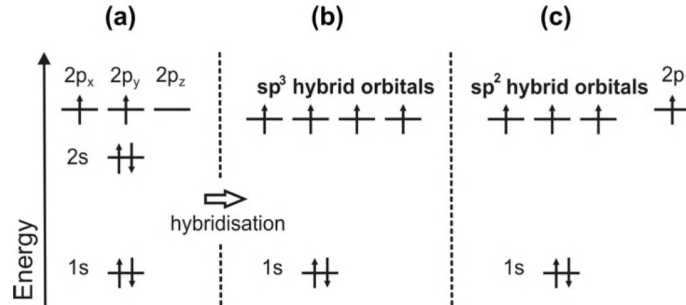



**Figure 1.7:** Atomic orbital diagram of a carbon atom: (a) ground state, (b) $sp^3$-hybridised as in diamond and (c) $sp^2$-hybridised as in graphite and graphene. [4]

$$E^{\pm}(k_x, k_y) = \pm\gamma_0 \sqrt{1 + 4\cos\frac{\sqrt{3}k_x a}{2}\cos\frac{k_y a}{2} + 4\cos^2\frac{k_y a}{2}} \qquad (1.3)$$

where $a = \sqrt{3}a_{C-C}$, and $\gamma_0$ is the nearest-neighbour overlap integral, which assumes values between 2.5 and 3 eV. The calculated band structure is shown in Fig. 1.9 for $\gamma_0 = 2.7$ eV.

In intrinsic graphene, each carbon atom contributes with one electron completely filling the valence band and leaving the conduction band empty. As a consequence, the Fermi level $\mu$ is situated precisely at the energy where the conduction and valence bands meet, i.e. in correspondence of the Dirac points. Graphene is therefore a zero-gap semiconductor. Expanding Eq. 1.3 close to one of the Dirac points results in a linear dispersion relation between energy $E(\mathbf{k})$ and momentum $\mathbf{k}$:

$$E^{\pm}(\mathbf{k}) = \hbar v_F |\mathbf{k} - K| \qquad (1.4)$$

where $\mathbf{k} = (k_x, k_y)$ is the reciprocal vector and $v_F = \sqrt{3}\gamma_0 a/2\hbar$ is the Fermi velocity. This equation is valid only within $\pm 1$ eV from the Dirac point and is

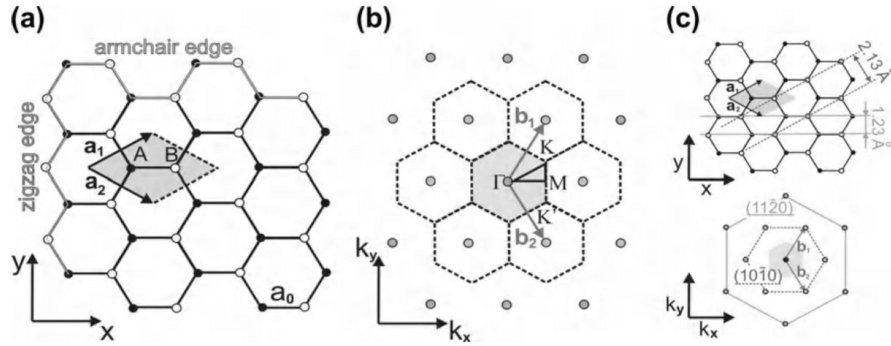



**Figure 1.8:** (a) 2D hexagonal lattice of graphene in real space. $a_1$ and $a_2$ are the basis vectors and they define the unit cell, highlighted in grey. An armchair and a zigzag edge are highlighted in grey. (b) Reciprocal lattice (dashed), with reciprocal lattice vectors $b_1$ and $b_2$ defining the first Brillouin zone, marked in grey. $\Gamma$, $M$, $K$ and $K'$ are the high symmetry points. (c) Small views of the real (upper) and reciprocal (lower) lattice. Two sets of lattice planes with $d = 2.13$ Å and $d = 1.23$ Å are highlighted with dotted and full lines in the real space lattice. In the reciprocal lattice the corresponding diffraction spots are marked with a dotted and full hexagon, respectively. [4]

plotted in the right part of Fig. 1.9. The energy dispersion (Eq. 1.4) resembles the energy of ultrarelativistic particles, which in quantum mechanics are described by the massless Dirac equation. Theoretical and analytical calculations provide an estimation for the Fermi velocity as $v_F = 10^6$ m/s, meaning that electrons in graphene move at relativistic speed and therefore behave like massless particles [71]. The density of states per unit cell can be derived from the tight-binding Hamiltonian. Close to the Dirac point, the dispersion can be approximated using Eq. 1.4 and the density of states per unit cells is given by

$$\rho(E) = \frac{2A_c}{\pi}\frac{|E|}{v_F^2} \tag{1.5}$$

where $A_c$ is the unit cell area given by $A_c = 3\sqrt{3}a^2/2$. The density of states per unit cell is therefore linear with the energy [5].

Graphene is characterised by a high *carrier mobility*, with values up to 300,000 $\mathrm{cm^2V^{-1}s^{-1}}$ measured on graphene encapsulated with hexagonal boron nitride (hBN) [72]. From the Drude model it is known that the conductivity $\sigma$ can be defined in terms of two important material properties, carrier density $n$ and mobility $\mu_C$:

$$\rho^{-1} = \sigma = ne\mu_C \tag{1.6}$$

Graphene's Fermi level can be tuned either by doping [73] or electrostatically by use of the electric field effect [69, 74], allowing to modulate its conductivity. In field effect measurements, a gate voltage is applied and the field effect mobility can be extracted from the gate voltage dependency of the conductivity:

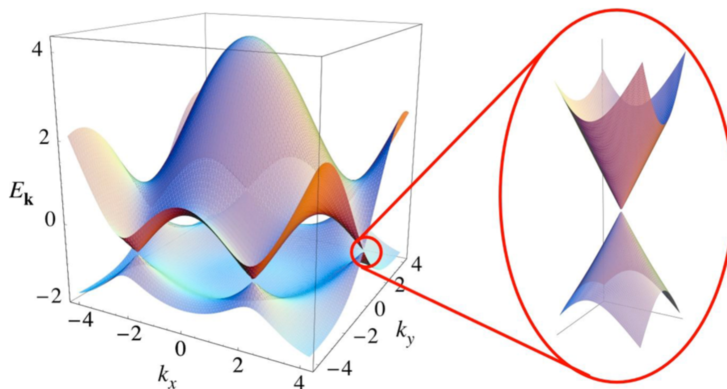



**Figure 1.9:** Electronic dispersion in the honeycomb lattice. Right: zoom in of the energy bands close to one of the Dirac points, where the dispersion relation is linear. Image taken from [5].

$$\mu_C = \frac{d\sigma}{dV_g}\frac{1}{C_{ox}} \tag{1.7}$$

where $C_{ox}$ the gate capacitance. Fig. 1.10 shows the modulation of the resistivity $\rho$ with the applied voltage in a field effect experiment. Although theoretically the density of charge carriers should go to zero at the Dirac point, experimentally it has been observed that there remains a finite conductivity of the order of $4e^2/\hbar$ [71]. Conductivity and mobility values depend on graphene's quality and on the material and roughness of the substrate used for growth and for device fabrication [75–79]. It is still an open question whether there is an intrinsic explanation for a minimum conductivity in graphene [3]. More details about electrical characterisation of graphene will be given in Section 1.4.2.

Another exceptional property of graphene is its *tensile strength*. Defect-free, monolayer graphene is considered to be the strongest material ever tested, with an intrinsic strength of 130 GPa. The assembling of wrinkled graphene can lead to the preparation of a membrane with tensile strength of over 12 GPa [80].

The unique electronic structure of graphene leads to several distinctive *optical properties*, which have attracted interest for high-speed optoelectronic devices [68]. The light-matter interactions in graphene are surprisingly strong and it was indeed the strong optical absorption of single-layer graphene that allowed the initial discovery of exfoliated graphene monolayers by visual inspection under an optical microscope [69]. The fraction of absorbed light in graphene can be calculated using Fermi's golden rule. The central quantity to be computed is the transition rate of electrons excited from the valence band to the conduction band when light is incident on the graphene layer. To obtain

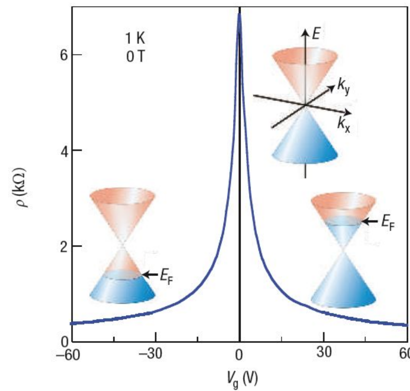



**Figure 1.10:** Modulation of the resistivity of a graphene sample by the application of a gate voltage. The insets show its conical low-energy spectrum $E(k)$, indicating changes in the position of the Fermi energy $E_F$ with changing gate voltage $V_g$ [3].

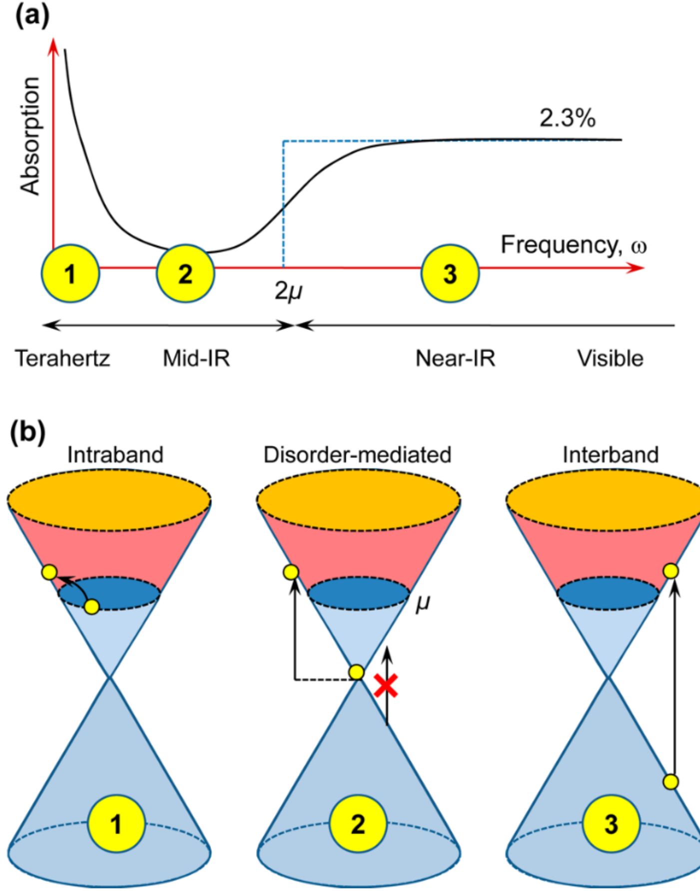



**Figure 1.11:** (a) Absorption spectrum of n-doped graphene. It shows maximum absorption at THz frequencies, minimum absorption at mid-infrared frequencies and constant 2.3% absorption beyond the far-infrared. (b) Illustration of the various optical transition processes. At $\omega$ less than the thermal energy, transitions occur via intraband processes. At finite $\omega < 2\ \mu$, disorder plays an important role in imparting the momentum for the optical transition. A transition occurs around $\omega \approx 2\ \mu$, where direct interband processes lead to a universal 2.3% absorption. The absorption spectrum of p-doped graphene is analogous. Taken from [6].

the contributions from all the states, it is then necessary to integrate over the momentum and multiply the result by four (two for spin, two for valley). The result for the total transition rate per unit area $\tau$ is [81]

$$\frac{1}{\tau} = e^2 A_0^2 \frac{\omega}{8\hbar^2} \tag{1.8}$$

where $\omega$ is the frequency of the incident light and $A_0$ is the unit area of graphene. If light of frequency $\omega$ is shining upon a unit area $A_0$ of graphene, the amount of absorbed power per unit area is $W_a = \hbar\omega/\tau$. The energy flux impinging on graphene is given by $W_i = c\epsilon_0 E_0^2/2$. Therefore, the fraction of transmitted light $T$ is [81]

$$T = 1 - \frac{W_a}{W_i} = 1 - \pi\alpha \simeq 0.977 \tag{1.9}$$

where $\alpha = e^2/4\pi\epsilon_0\hbar c$ is the fine structure constant. The absorption of light $A$ is therefore independent of frequency and it is given only by universal constants:

$$A = \frac{W_a}{W_i} = \pi\alpha \simeq 0.023 \tag{1.10}$$

At finite doping, the transmission can be written as

$$T = 1 - \frac{W_a}{W_i} = (1 - \pi\alpha)\theta(\omega - 2E_F) \tag{1.11}$$

where the Heaviside step function $\theta(\omega - 2E_F)$ takes into account that absorption can only occur for frequencies larger than twice the Fermi energy, due to Pauli's principle. The reason why the transmission is controlled by the fine structure constant originates in the chiral nature of the electrons in graphene [81]. The results written so far are valid in the region where the energy-momentum dispersion relation is linear (energies smaller than 1 eV). If the intensity of light impinging on graphene is large, then nonlinear corrections to Eq. 1.9 start to play a role, which is expected to lead to a decrease in the transmittance.

Being a zero-bandgap material, graphene can absorb light at any wavelength from visible to infrared. In the infrared region, the absorption is mainly attributed to interband transitions, i.e. direct optical transitions between the valence and conduction bands (Fig. 1.11). Graphene absorbs 2.3% of the perpendicularly incident light (Eq. 1.10), which can be enhanced further by integrating graphene on a photonics waveguide to increase the interaction length between light and graphene. Because absorption in graphene is related to its fine structure constant, stacking two layers of graphene on top of each other causes the absorption to double [82]. Graphene's absorption can be easily tuned through capacitive charging by applying an electric field [83], and has therefore the potential to enable active optoelectronic functionality onto passive optical waveguides, such as Si and low-loss SiN waveguides [84]. Finally, its high mobility makes graphene a candidate for applications in high-speed optoelectronic devices, such as photodetectors and modulators.

### 1.3.2 Graphene growth and transfer

As introduced earlier, *mechanical exfoliation* of graphite was the first successful method to isolate single-layer graphene [69]. This top-down method delivers very high quality graphene flakes, that are very useful to study fundamental properties and for prototyping new devices. However, it is impractical for large-scale applications and only devices with small area can be fabricated using flakes. The industrial use of graphene requires large scale and cost-effective production methods, while providing a balance between ease of fabrication and final material quality (Fig. 1.12) [85]. Graphene can be synthesised using large-scale cost-effective bottom-up techniques, such as *chemical vapour deposition* (CVD). This technique is used for the production of all the graphene used throughout this thesis. CVD refers to the decomposition of a carbon gas on a catalyst surface, usually a metal such as nickel (Ni), copper (Cu) or platinum (Pt) [86–88]. The temperature and pressure conditions are very important and, if well controlled and optimised, CVD growth can deliver large-area single-layer graphene. The dimension of graphene grains is only limited by the crystal size of the underlying growth substrate. CVD growth is being extensively researched, therefore the material quality is improving continuously. Researchers still have to face some challenges, such as developing growth recipes at lower temperature

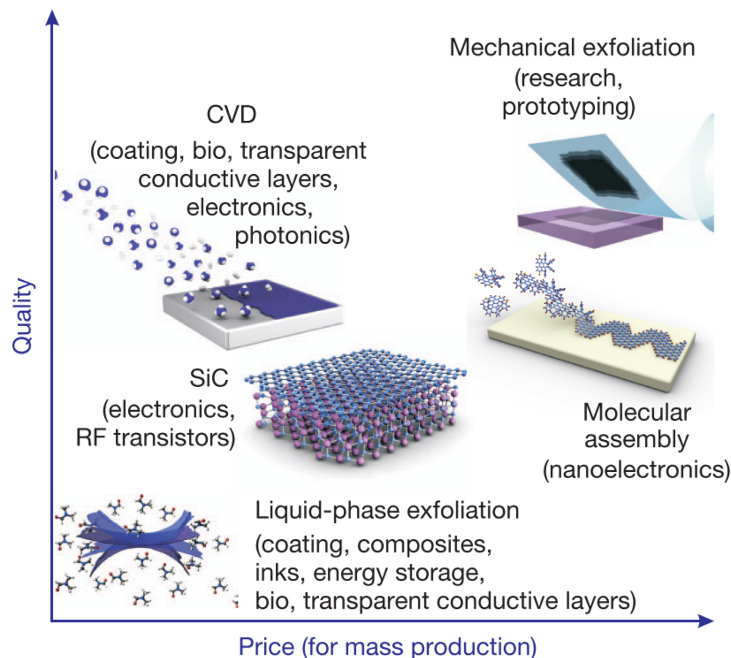



**Figure 1.12:** Summary of the available technique to produce graphene, classified in terms of size, quality and price for any particular application. Taken from [7].

without compromising the quality of the growth material, in order to respect requirements for FAB integration. In addition, challenging tasks include increasing the grain size and developing recyclable growth substrates to reduce production costs and waste.

Next to mechanical exfoliation and CVD growth, other graphene deposition techniques are:

- *Chemical exfoliation*, a top-down technique, where graphene layers are exfoliated from a piece of graphite by the intercalation of molecules between the graphene sheets. This method is scalable and low-cost, but results in low yield and low graphene quality.
- *Reduction of graphene oxide* (GO), where graphite is first oxidised, then the GO is exfoliated by sonication in water. GO is not conductive, but its conductivity can be restored by thermal annealing or chemical treatment. This method is scalable and low-cost, but the final graphene sheets show low purity and high defect density.
- *Thermal decomposition of SiC*, where a wafer of SiC is exposed to temperatures as high as 1400°C, causing the evaporation of Si and the formation of a graphene monolayer. This method yields high-quality graphene and is scalable, but it is very costly, it requires a high thermal budget and expensive substrates.

In many cases, such as for all the devices under study for this thesis, the growth substrate is not the target substrate needed to fabricate these devices. For example, silicon photonics devices are based on a SOI substrate, but CVD graphene needs a metal substrate to be successfully grown. In addition, the temperature used to grow graphene is still too high and not CMOS-compatible, therefore it would be harmful for the target substrate (such as the SOI substrate) to grow graphene directly on-site [86]. These issues lead to the need to transfer the graphene layer from its growth template to the target substrate. Transfer is the delamination of graphene from the growth substrate, followed by the lamination on the target substrate. Transfer is a very challenging and critical step. It can contaminate and introduce defects in the graphene layer, such as tears or ripples, reducing its quality. As it will be further discussed in Chapter 2, an additional challenge is the adhesion of graphene to the target substrate, which is low especially for good quality graphene, resulting in delamination during device fabrication. Many transfer processes have been studied, and they can be divided in three categories [89]:

1. *Etch-based delamination.* This is the main method used in literature. A polymer layer is first spin-coated on top of graphene as support layer. Afterwards, the growth substrate is separated from the graphene layer by etching. Metallic residues from the substrate or from the etchant are often observed on the graphene layer after transfer.

2. *Ion intercalation-based delamination.* This method, often called 'bubble transfer', is based on intercalation of ions between graphene and the growth substrate. For a Pt substrate, the delamination takes place in a NaOH solution, where $H_2$ bubbles, formed at the graphene/Pt interface by applying a constant current, cause the delamination of the graphene/PMMA stack from the growth substrate.
3. *Dry peeling-based delamination.* In this method, graphene is protected by a polyvinyl alcohol (PVA) solution. The PVA/graphene stack is mechanically debonded from the substrate. The actual mechanism behind this transfer method is not fully understood.

A comprehensive overview of the main techniques to grow and transfer graphene, along with a detailed roadmap for graphene in technology, can be found in [85] and [86].

## 1.4 Graphene characterisation techniques

### 1.4.1 Physical characterisation

*Optical microscopy* is a well-established technique that can be used in first place to analyse large area graphene thanks to its simplicity. In fact, optical microscopy allows for a quick thickness and quality inspection before using more precise methods such as Raman spectroscopy, scanning electron microscopy (SEM) or atomic force microscopy (AFM). Graphene visibility using optical microscopy is explained by the change of the interference colour of reflected light from graphene with respect to the empty substrate. The kind of substrate used to support graphene and the light wavelength play a very important role. By using monochromatic light graphene can be isolated for any $SiO_2$ thickness, although 300 nm and 90 nm are the most appropriate for visual detection when using a white light source and naked eye [90]. An example of a graphene layer observed under scanning electron microscopy is shown in Fig. 1.13a.

*Scanning electron microscopy* (SEM) is of prime importance for the characterisation of microstructures on a scale down to 10 Å. A focused electron beam, with primary energy of 2-10 keV, is scanned over the surface under study and, simultaneously, it detects the electrons emitted from the surface. The intensity of this emitted signal determines the brightness of that particular spot on the screen. The formation of a topographical image is due to local variations of the electron emissivity of the surface. This technique provides a combination of high magnification, large depth of focus, high resolution and ease of applicability. It is of particular importance for those cases in which graphene is not visible with the optical microscope, such as graphene on SOI substrates. An example of a graphene layer observed under scanning electron microscopy is shown in Fig. 1.13b.

*Raman spectroscopy* is a non-destructive spectroscopic technique where the inelastic scattering of monochromatic light, typically from a laser source, in-

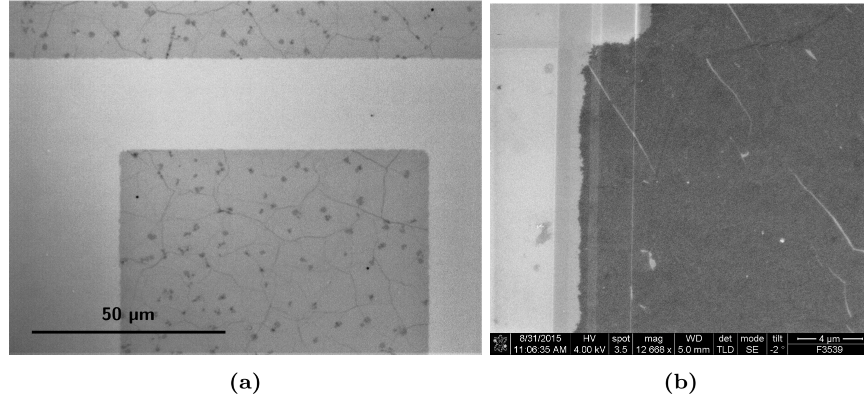



**Figure 1.13:** (a) Optical microscope image of a shaped CVD graphene layer. Wrinkles and bilayer spots are visible. (b) Scanning electron microscope image of a shaped graphene layer on top of a waveguide.

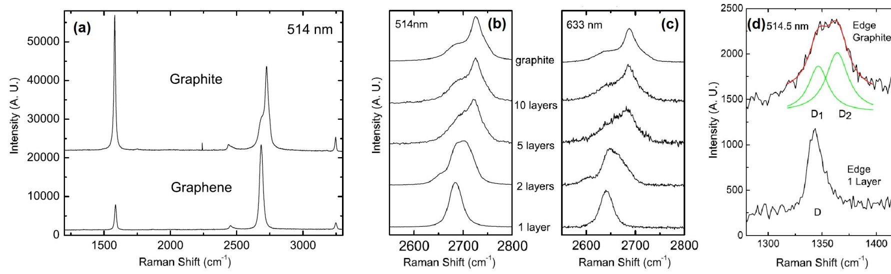



**Figure 1.14:** (a) Comparison of Raman spectra at 514 nm for bulk graphite and graphene. They are scaled to have similar height of the $2D$-peak at $\sim$ 2700 cm$^{-1}$. (b) Evolution of the spectra at 514 nm with the number of layers. (c) Evolution of the spectra at 633 nm with the number of layers. (d) Comparison of the $D$-band at 514.5 nm at the edge of bulk graphite and single layer graphene, with the fit of the $D_1$ and $D_2$ components of the $D$-band of bulk graphite. [93]

teracts with a sample [91, 92]. The scattered light coming from the irradiated sample is gathered with a system of lenses and sent through a spectrophotometer to obtain a Raman spectrum. In a typical Raman spectrum the intensity of the scattered light (in a.u.) is plotted as a function of the energy difference between the incident and the scattered light, called Raman shift (in cm$^{-1}$). Raman spectroscopy represents a unique way to capture the electronic structure of graphene and to identify graphene layers. Fig. 1.14 compares Raman spectra of graphene and bulk graphite. The two most intense features are the $G$-peak at $\sim$ 1580 cm$^{-1}$ and the $2D$-peak at $\sim$ 2700 cm$^{-1}$. The $G$-peak is a first order Raman band, i.e. scattering involving one phonon, corresponding to an in-plane vibration of the neighbouring sp$^2$ carbon atoms of the graphene

lattice. This peak is therefore present also in carbon materials of other dimensions, such as carbon nanotubes or graphite. Its intensity changes as the number of graphene layers increases (Fig. 1.14a). The $2D$-peak, also known as $G'$-peak, is a second order Raman band, i.e. the scattering involves two phonons, corresponding to an in-plane breathing mode of the carbon rings. In the Raman spectrum of single-layer graphene, the $2D$-peak is the most intense feature and it can be fitted with one lorentzian curve. As the number of layers increases, the intensity of the $2D$-peak decreases, its position shifts and the peak broadens (Fig. 1.14b). Since zone-boundary phonons do not satisfy the Raman fundamental selection rule, they are not seen in first order Raman spectra of defect-free graphite, but they give rise to a peak at $\sim 1350$ cm$^{-1}$ in defected graphite. This peak is called $D$-peak and it corresponds to an in-plane breathing mode of the carbon rings. The intensity of this peak depends on the amount of defects present in the sample. The intensity of the $D$-peak may also increase closer to the edges of the sample compared to the centre (Fig. 1.14d). The quality of the Raman spectrum of single-layer graphene is judged by looking at the sharpness of the $2D$-peak and by calculating the ratios $I_D/I_G$ and $I_{2D}/I_G$ [93–102]. A good quality spectrum is characterised by $I_D/I_G < 0.2$ and $I_{2D}/I_G > 1.2$. The Raman spectrum of graphene is also sensitive to the presence of doping [97, 100, 103, 104], which causes the width and the position of the $G$-peak and $2D$-peak to change, and to the presence of external strain, which induces a splitting of the $G$-peak [105].

### 1.4.2 Electrical characterisation: the transfer length method (TLM)

The transfer length measurement (TLM) is the primary method used for the extraction of the metal/graphene contact resistance and graphene's sheet resistance from electrical measurements of graphene field effect transistors (FETs). In addition, the mobility can also be extracted from this measurement.

The TLM method is depicted in Fig. 1.15. Metal-graphene contacts are placed at different distance between each other along a stripe of graphene. Probes are placed on each pair of contacts, and the resistance between them is obtained by applying a voltage ($V$) and measuring the resulting current ($I$). The measured total resistance ($R_{tot} = V/I$) between two contacts has two main contributions, namely the contact resistance and the channel (sheet) resistance, and is given by

$$R_{tot} = 2R_C + R_{channel} = 2R_C + R_S\frac{L}{W} \tag{1.12}$$

where $L$ is the channel length (distance between two contacts), $W$ is the channel width, $R_C$ is the contact resistance and $R_S$ is the sheet resistance. The TLM method assumes therefore a linear dependence between $R_{tot}$ and $L$. The measured $R_{tot}$ for each device is plotted as a function of channel length $L$ and a linear fit of all the data points is performed (as shown in Fig. 1.15). If the

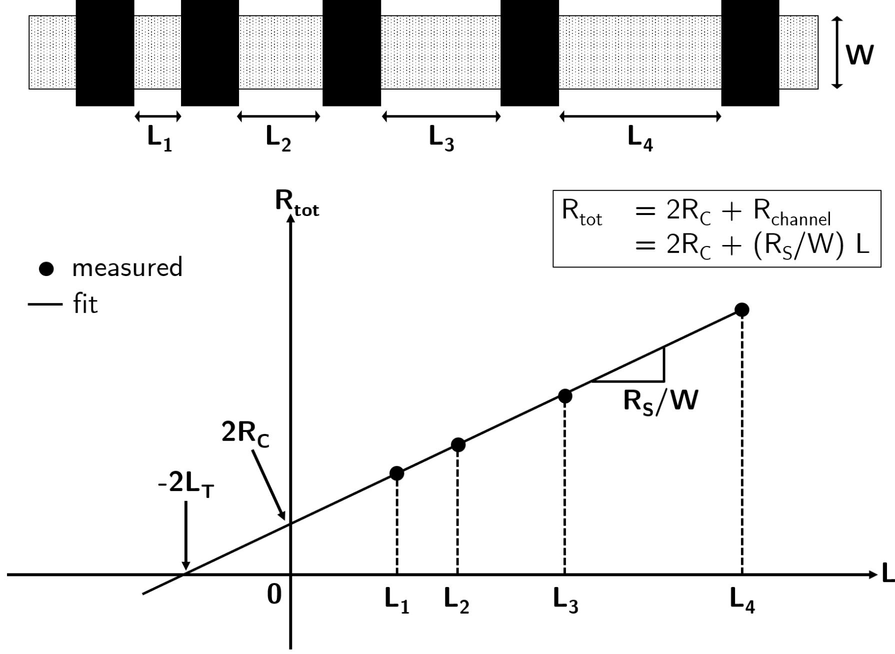



**Figure 1.15:** Description of the TLM method.

linear fit is given by the equation $y = a + bx$, the contact resistance $R_C$ is extracted from the intercept $a$, while the sheet resistance $R_S$ is extracted from the slope $b$, as follows

$$R_C = \frac{a}{2}, \qquad R_S = bW \tag{1.13}$$

Both are normally multiplied by $W$ to obtain a value independent from the dimension of the contact. In this way the sheet resistance has units of $\Omega/\square$ and the contact resistance has units of $\Omega$ μm.

Characterisation of graphene TLM structures is performed by measuring the total resistance of each graphene FET varying the backgate voltage $V_G$, but keeping the drain voltage $V_D$ fixed (Fig. 1.16a). The characteristic V-shaped $I_D - V_G$ curve of graphene electrical response is obtained (Fig. 1.16b). The minimum of this curve corresponds to graphene's neutrality point ($V_{NP}$). The contact and sheet resistance values can be extracted via the TLM method at any given $V_G$. Because the position of the charge neutrality point depends on graphene's doping and varies from sample to sample, the contact and sheet resistance are typically extracted at $V = V_{NP}$, so that a comparison between different samples is possible.

After plotting the $I_D - V_G$ curve, $R_{tot} = I_D V_D$ is calculated and plotted as a function of gate voltage ($R_{tot} - V_G$). The maximum resistance for each

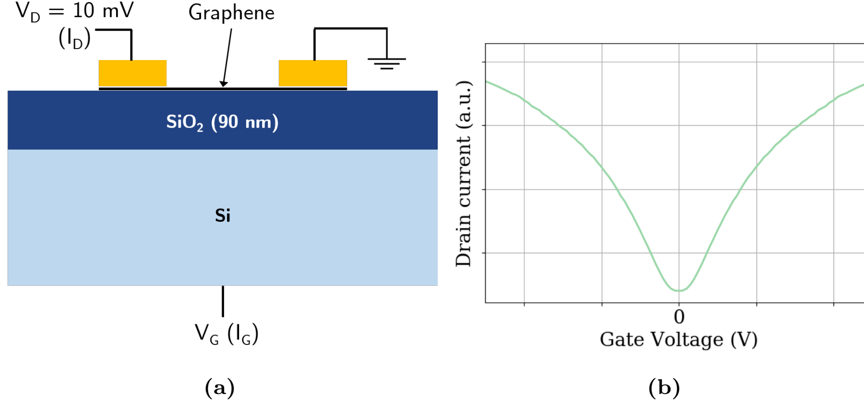



**Figure 1.16:** (a) Cross section of a graphene FET used for measurement of TLM structures, with indications of how the voltage is applied. (b) Example of a typical $I_D - V_G$ curve for intrinsic graphene.

channel length is extracted together with the position of the charge neutrality point. The curves are then all aligned at the neutrality point, therefore the total resistance is plotted as a function of $(V_G - V_{NP})$. Once the data is aligned, the contact resistance $R_C$ and the sheet resistance $R_S$ are extracted for each value of $(V_G - V_{NP})$ according to Eq. 1.13. From the sheet resistance the sheet conductivity can be calculated as $G_S = 1/R_S$. Graphene's mobility can be estimated based on the gate-modulated sheet conductivity. The relation between the current density $\boldsymbol{J}$ and an applied electric field $\boldsymbol{E}$ can be written according to Drude's model as

$$\mathbf{J} = G_S\mathbf{E} = \frac{nq^2\tau}{m}\mathbf{E} = nq\mathbf{v}_D \tag{1.14}$$

where $G_S$ is the sheet conductivity and $\mathbf{v}_D$ the drift velocity. The mobility $\mu_C$ is an indication of how fast carriers can move through a material and is defined as the ratio of the field $\mathbf{E}$ and the drift velocity $\mathbf{v}_D$:

$$\mathbf{v}_D = \mu_C\mathbf{E} \tag{1.15}$$

Combining Eq. 1.14 and Eq. 1.15, we obtain

$$G_S = nq\mu_C \tag{1.16}$$

For a back-gated graphene FET, the number of carriers in graphene $n$ is given by

$$n = \frac{\epsilon_0\epsilon}{qt_{ox}}V_G = \frac{C_{ox}}{q}V_G \tag{1.17}$$

where $\epsilon_0$ is the vacuum permittivity, $\epsilon$ is the dielectric constant of the gate oxide, $q$ is the elementary charge, $t_{ox}$ the gate oxide thickness and $C_{ox}$ the capacitance of the gate oxide. Combining Eq. 1.16 and Eq. 1.17, we obtain

$$G_S = nq\mu_C = \mu_C C_{ox} V_G \tag{1.18}$$

By differentiating both sides of the equation, and solving for $\mu_C$ we can write the formula to extract the mobility from the sheet conductivity:

$$\mu_c = \frac{1}{C_{ox}} \frac{\Delta G_S}{\Delta V_G} \tag{1.19}$$

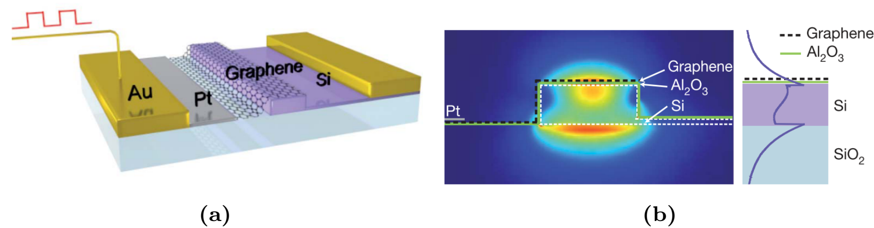
## 1.5 Graphene photonic devices

Thanks to its remarkable optical properties, graphene is the perfect material for optoelectronic applications [68, 106, 107]. In the next two subsections, we will describe state-of-the-art graphene modulators and photodetectors, underlining different geometries and explaining advantages and disadvantages.

### 1.5.1 Graphene modulators

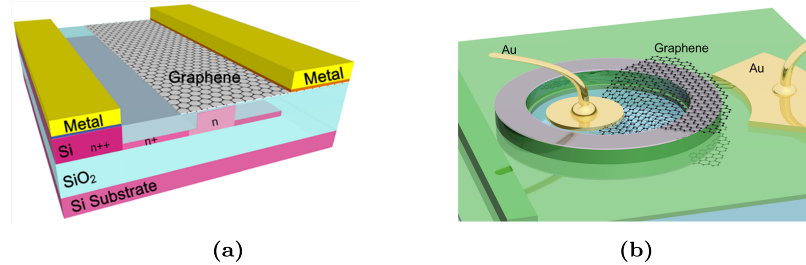
High-speed graphene modulators have been reported in literature in single-layer graphene (SLG) [8–11, 108–110] or double-layer graphene (DLG) [12–15, 111] configuration on top of the waveguide. DLG modulators are based on a graphene-oxide-graphene capacitor, while SLG modulators are based on a graphene-oxide-silicon capacitor. Due to the presence of two graphene layers, DLG modulators offer potential for higher extinction ratio than SLG modulators, but they suffer from higher insertion loss. In addition, SLG modulators have a simpler fabrication process compared to DLG modulators, requiring the transfer of only one graphene layer.

The very first *single-layer graphene* EAM was demonstrated by *Liu et al.* in 2011 [8]. A 50 nm-thick Si layer was used to connect the 250-nm-thick Si



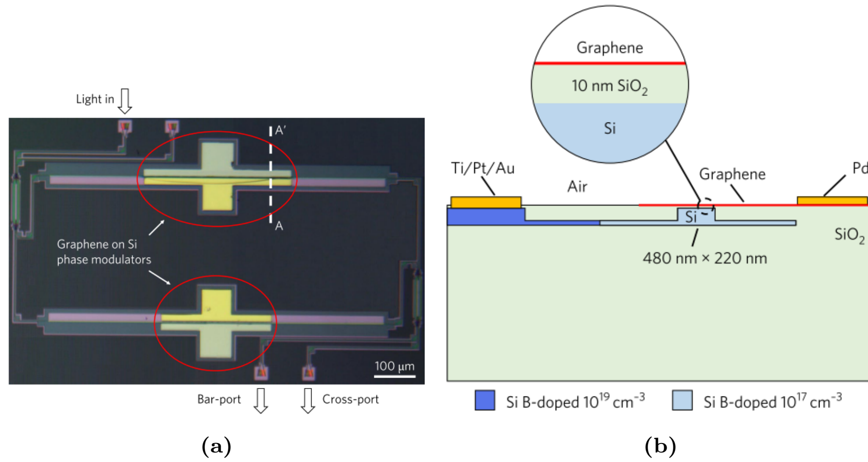

(a) (b)

**Figure 1.17:** (a) Three-dimensional schematic illustration of the device. (b) Left, cross-section ofthe device, with an overlay ofthe optical mode plot. Right, a cross-section through the centre of the waveguide; the purple curve shows the magnitude of the electric field. Taken from [8].




(a) (b)

**Figure 1.18:** (a) A 3D schematic drawing of the SLG EAM built on a planarised SOI substrate. Taken from [9]. (b) 3D schematic image of the graphene-silicon microring resonator. Taken from [10].




(a) (b)

**Figure 1.19:** (a) Optical micrograph of the MZI modulator. (b) Cross-section of the GPM through the dashed line A–A' of (a). Taken from [11].

bus waveguide to the metal contact. Both the Si layer and the waveguide were shallowly doped with boron (B) to reduce the sheet resistance. A layer of $Al_2O_3$ was deposited on the waveguide and a CVD-grown graphene sheet was then transferred on top (Fig. 1.17). By electrically tuning the Fermi level of the graphene sheet, they demonstrated a 3 dB bandwidth of 1.2 GHz at a DC bias of -3.5 V and an extinction ratio of 4 dB at 4 $V_{pp}$. They also showed a broad operation spectrum that ranges from 1.35 to 1.6 µm under ambient conditions, surpassing the optical bandwidth of Ge modulators, with an active area of only 25 $\mu m^2$. *Hu et al.* presented a SLG EAM with improved performance in 2014 [108] and later published it in 2016 [9]. The design was based on the one from [8], with the difference that the SOI substrate was fabricated in a silicon photonics platform and the n-doped waveguide was planarised with $SiO_2$ to simplify graphene transfer on top (Fig. 1.18a). The device exhibited

a 3 dB frequency response of 5.9 GHz and open eye diagrams at 10 Gbit/s using 2.5 $V_{pp}$ at 1.75 V DC bias in the wavelength range between 1530 nm and 1565 nm. The first ring-based SLG modulator was demonstrated in 2015 by *Ding et al.* [10] (Fig. 1.18b). They demonstrated a high extinction ratio of 12.5 dB at 8.8 $V_{pp}$ and on-off electro-optical switching with an extinction ratio of 3.8 dB by applying a square-waveform with 4 $V_{pp}$. In 2018 *Sorianello et al.* demonstrated the first graphene phase modulator based on a Mach-Zender interferometer [11]. The modulator showed a record 35 dB extinction ratio and 5 GHz 3dB bandwidth. Open eye diagrams were demonstrated up to 10 Gbit/s with 2 $V_{pp}$ in a push–pull configuration for binary transmission of a non-return-to-zero data stream over 50 km of single-mode fibre.

The first *double-layer graphene* EAM was demonstrated in 2012 by *Liu et al.* [12]. The modulator was fabricated by transferring two layers of graphene on top of a Si waveguide with $Al_2O_3$ as spacer between them (Fig. 1.20a). It operated at 1 GHz with a modulation depth of 0.16 dB/µm at a drive voltage of 5 V. In 2014 *Mohsin et al.* demonstrated a DLG EAM using HSQ to planarise the waveguide and $Al_2O_3$ as spacer between the two graphene layers (Fig. 1.20b) [13]. The modulator showed an improved extinction ratio of 16 dB thanks to the longer graphene covering the waveguide, with an insertion loss of only 3.3 dB. The measured 3 dB bandwidth was 670 MHz. The first ring-based graphene modulator was demonstrated in 2015 by *Phare et al.* [14]. A 3 dB frequency response of 30 GHz and open eye diagrams at 22 Gbit/s were demonstrated by reducing the capacitance of the device using a 65 nm-thick $Al_2O_3$ as spacer between the two graphene layers (Fig. 1.21). However, employing a thick $Al_2O_3$ came at the expense of the high drive voltage (7.5 $V_{pp}$) and high DC bias (-30 V) necessary to operate the device. The resonant nature of the ring modulator limits the device optical bandwidth. In 2016, *Dalir et al.* demonstrated a new DLG EAM with a different geometry [15].

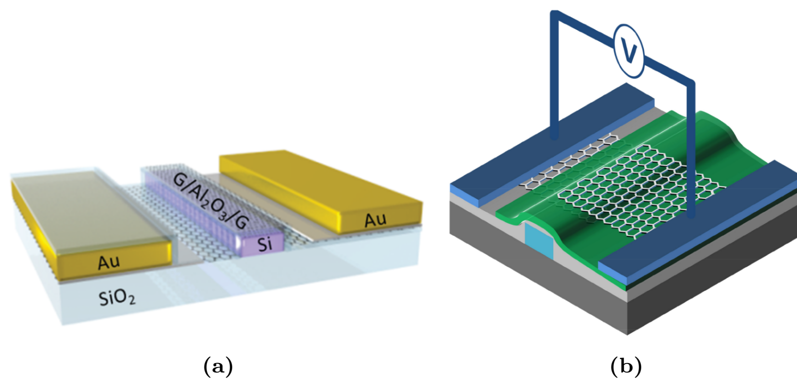
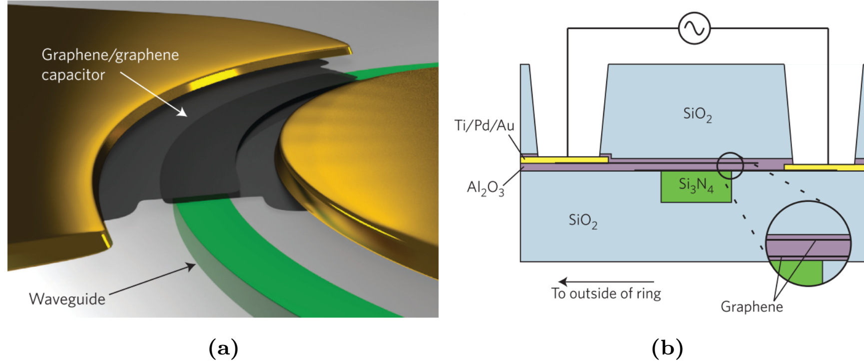
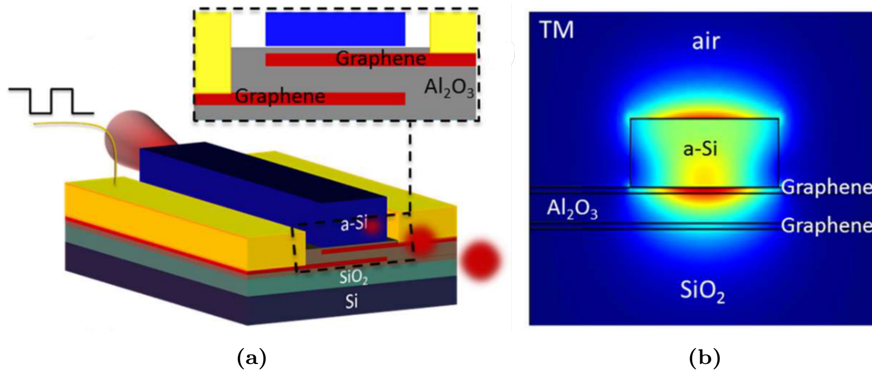



**Figure 1.20:** Three-dimensional schematic illustration of two DLG EAMs. (a) is taken from [12] and (b) is taken from [13].




**(a)** **(b)**

**Figure 1.21:** (a) Schematic of the modulator consisting of a graphene/graphene capacitor integrated along a ring resonator. (b) Cross-section of the device, showing two layers of graphene separated by a 65 nm-thick $Al_2O_3$ dielectric layer. Taken from [14].




**(a)** **(b)**

**Figure 1.22:** (a) Schematic of a device showing two layers of graphene separated by a 120 nm-thick $Al_2O_3$ dielectric layer to form a capacitor. (b) Finite element method calculation of the TM mode in the silicon waveguide. Taken from [15].

The double-layer graphene structure was fabricated below an amorphous silicon waveguide, in order to maximise the light interaction with the graphene layers (Fig. 1.22). The device exhibited 0.9 dB insertion loss, 2 dB extinction ratio and an improved 3 dB frequency response of 35 GHz across a broad wavelength range (1500 nm - 1640 nm). However, due to the 120 nm-thick $Al_2O_3$ used as spacer between the two graphene layers, a high operating DC bias of 25 V was necessary to achieve such speed. Finally, in 2019 *Giambra et al.* reported a 120 µm-long DLG EAM, built on top of a silicon waveguide with a 20 nm-thick SiN spacer between the two graphene layers, exhibiting 20 dB IL and 3 dB ER for 9 $V_{pp}$ [111]. The device showed 29 GHz 3 dB frequency response and open eye diagrams at 50 Gbit/s using 3.5 $V_{pp}$, at a high DC bias of 8 V. This

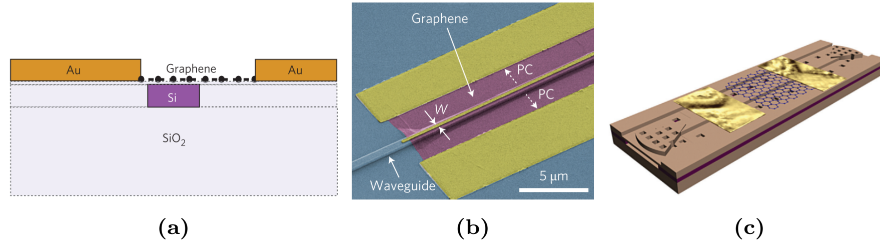
performance was achieved thanks to very high quality CVD graphene and an improved transfer method.

Table 1.2 (at the end of this chapter) summarises the important parameters of state-of-the-art graphene modulators. While ring modulators clearly allow to achieve higher extinction ratio, EAMs offer many more advantages, such as smaller device footprint, greater optical bandwidth, higher temperature stability and lower insertion loss.

### 1.5.2 Graphene photodetectors

With its zero-bandgap and high carrier mobility, graphene-based photodetectors are promising for broadband photodetection at high speed. Early on, graphene photodetectors were mainly demonstrated based on field effect transistors (FETs) structures [112], where different mechanisms play a role in the photodetection process [113]. The dominating photodetection effect depends on the type of device configuration and is chosen based on the application. For telecom, where high-speed operation is a key requirement, three effects are typically considered, namely the photovoltaic effect, the photo-thermoelectric effect and the bolometric effect, because they allow to exploit the ultra-fast carrier dynamics in graphene ($\sim$ fs-ps) [114]. Photocurrent generation through the photovoltaic (PV) effect is based on the separation of photogenerated electron-hole ($e^-$-$h^+$) pairs by a built-in electric field at the junctions between positively (p-type) and negatively (n-type) doped regions of graphene [115, 116]. Because of the built-in field, the device can work in bias-free condition. The same effect can also be achieved by applying an external bias voltage, but this leads to the generation of large dark current, being graphene a semi-metal. In the photo-thermoelectric effect (PTE), the photocurrent is generated between two graphene regions with different doping, which have different thermoelectric power (Seebeck coefficient). The photocurrent is proportional to the difference in thermoelectric power between the two regions and, following the second law of thermodynamics, the photogenerated hot electrons diffuse from areas with lower density of states to areas with higher density of states [117]. The photo-bolometric (PB) effect is associated with the change in the transport conductance of the device as a consequence of the heating produced by the incident photons. The change in conductance is attributed to the variation in carrier mobility of graphene by temperature change. This mechanism requires an external bias to detect the photocurrent and can operate on homogeneous graphene (without a p–n junction) [113, 118, 119].

Because the aim of this thesis is to study graphene applications in integrated photonics with waveguide-based devices, the literature review of graphene photodetectors will focus only on demonstrated waveguide graphene photodetectors. As mentioned earlier, integrating graphene on a waveguide represents an advantage because it allows to increase the interaction between light and graphene.




**(a)** **(b)** **(c)**

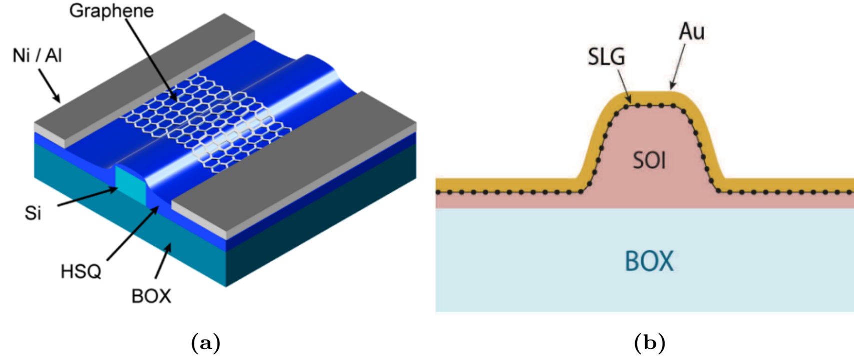
**Figure 1.23:** Device geometries of the first demonstrated graphene photodetectors. (a) Taken from [16], (b) from [17] and (c) from [18].

Early demonstration of graphene photodetectors was predominantly based on PV and devices were fabricated with graphene flakes [16–18]. *Gan et al.* [16] demonstrated a metal-graphene-metal (MGM) structure with an asymmetrical electrode design (Fig. 1.23a). One of the two metal contacts overlapped with the waveguide mode to form the built-in electrical field that separated the photogenerated electron-hole pairs. The device showed a responsivity of 0.1 A/W and a 3 dB bandwidth of 20 GHz. *Pospischil et al.* [17] fabricated a graphene-metal junction on top of a SOI waveguide to create the built-in electrical field to separate photocarriers (Fig. 1.23b). A flat photoresponse of 0.05 A/W was reported from the O-band to the U-band (1310 nm to 1675 nm), well beyond the wavelength range of Ge photodetectors, and a 3 dB bandwidth of 18 GHz was achieved. *Wang et al.* [18] built a graphene/silicon heterostructure on a silicon waveguide (Fig. 1.23c). This junction helps reducing the dark current and achieving a high on/off ratio. The device showed a photoresponse of 0.13 A/W.

The first graphene photodetector using CVD-grown graphene was demonstrated in 2014 by *Schall et al.* [19]. Graphene was integrated on a silicon waveguide planarised with HSQ and a lateral asymmetrical electrode geometry was used (Fig. 1.24a). The device showed a photoresponse of 0.016 A/W, a 3 dB bandwidth of 41 GHz and detection at 50 Gbit/s (and beyond). The performance was optimised by the same group later in 2017 [120] reaching a 3 dB bandwidth of 75 GHz. In addition to a record high-speed response, the device was fabricated on a 6" wafer using an up-scalable fabrication process. This result was further improved one year later [121] with the demonstration of a 3 dB bandwidth of 128 GHz and a photoresponse of 0.032 A/W (15 V/W).

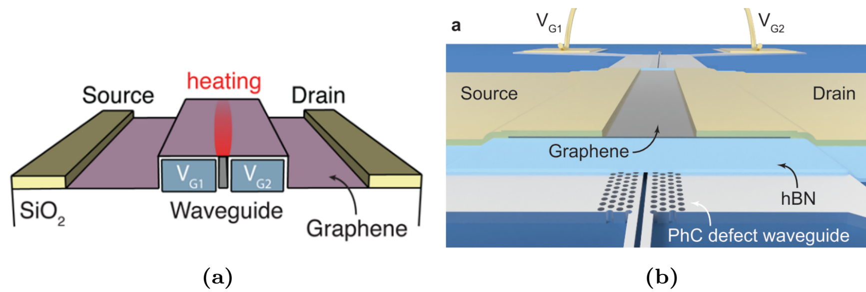
An improvement in photoresponse up to 0.37 A/W was achieved in 2015 by *Goykhman et al.* [20] using a metal-graphene-silicon (MGS) photodetector based on a graphene/silicon Schottky junction (Fig. 1.24b). The metal contact was fabricated directly on top of the silicon waveguide, thus providing plasmonic enhancement.

Next to pushing the high-speed performance, different waveguide and device geometries were also investigated. In 2015, *Shiue et al.* [122] demonstrated a graphene photodetector with asymmetrical electrode design, where graphene




**(a)** **(b)**

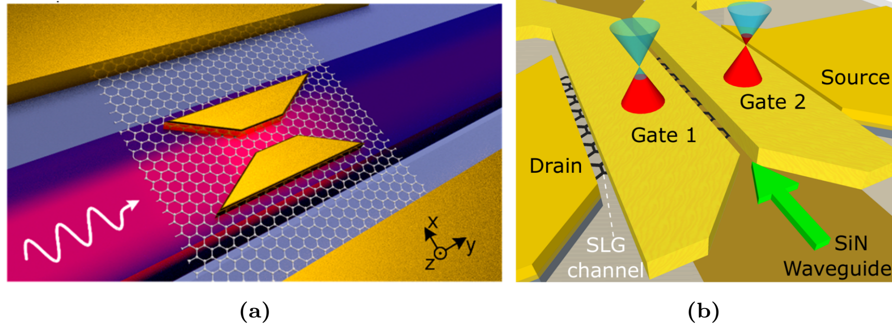
**Figure 1.24:** (a) Silicon waveguide graphene photodetector with asymmetrical electrode geometry. Taken from [19]. (b) Metal-graphene-silicon photodetector based on a graphene/silicon Schottky junction. Taken from [20].




**(a)** **(b)**

**Figure 1.25:** (a) Graphene photodetector based on a slot-waveguide. Taken from [21]. (b) Graphene photodetector based a PhC defect waveguide. Taken from [22].

was encapsulated between two layers of hBN. A responsivity of 0.36 A/W and a 3 dB bandwidth of 42 GHz were achieved. *Wang et al.* [123] demonstrated in 2016 a graphene photodetector based on a silicon slot waveguide using TE-polarised light. A responsivity of 0.27 A/W was achieved at 1550 nm. In the same year, *Schuler et al.* [21] also fabricated a slot waveguide graphene photodetector, where the two rib waveguides were used as dual back-gates, creating a p-n junction in the region where the optical absorption takes place (Fig. 1.25a). The device showed a responsivity of 0.08 A/W and a 3dB bandwidth of 65 GHz. In 2015, *Wang et al.* [124] demonstrated a broadband graphene photodetector based on a SiN waveguide using an asymmetrical electrode design. An internal photoresponsivity of 0.13 A/W was achieved at 1550nm. Later in 2018, *Gao et al.* [125] also used a SiN waveguide to demonstrate a responsivity of 2.36 A/W and a 3 dB bandwidth of 33 GHz. *Schuler et al.* [22] used a silicon photonics crystal defect waveguide to confine light in a narrow region and increase light-matter interaction (Fig. 1.25b). Responsivities of 4.7




(a) (b)

**Figure 1.26:** (a) Plasmonically enhanced waveguide-integrated graphene photodetector. Taken from [23]. (b) SLG on SiN waveguide (brown) with split-gates, acting as plasmonic slot waveguide, to create a p-n junction in the channel. Taken from [24].

V/W and 0.17 A/W were shown, together with a >18 GHz 3dB bandwidth. In 2019 different types of plasmonically enhanced graphene photodetectors were demonstrated [23, 24, 126]. *Ma et al.* [23] fabricated field-enhancing nanosized metallic structures on top of a silicon waveguide covered with graphene (Fig. 1.26a). The device exhibited 0.5 A/W responsivity, >110 GHz 3dB bandwidth and data reception at 100 Gbit/s. *Muench et al.* [24] used Au split double-gates to create a p-n junction and to stimulate a surface plasmon polariton gap-mode (Fig. 1.26b). A responsivity of 12.2 V/W and a 3 dB bandwidth of 42 GHz were demonstrated.

Table 1.3 reports the important parameters of state-of-the-art graphene-based waveguide photodetectors. Devices based on the PTE effect show good responsivity and high-speed performance, they can be operated without applying a voltage bias and they offer low dark current. Devices where the geometry was optimised for better carrier collection [20, 22, 125] or where plasmonic enhancement was used [23, 24] show higher responsivity.

## 1.6 Characterisation of graphene photonic devices

In this section, the main characterisation methods used to evaluate the performance of graphene-based electro-absorption modulators and photodetectors are explained.

**Loss measurements.** The goal of this measurement is to extract the absorption loss of the graphene sheet in 'standard conditions', i.e. at ambient conditions when no voltage is applied to the device. It is performed on both modulators and photodetectors. When the laser is turned on, the input light signal travels through the optical fiber and is then coupled into the waveguide through a fiber grating coupler. When the light travels through the waveguide, it interacts with the graphene layer shaped over it. At the end of the waveguide,

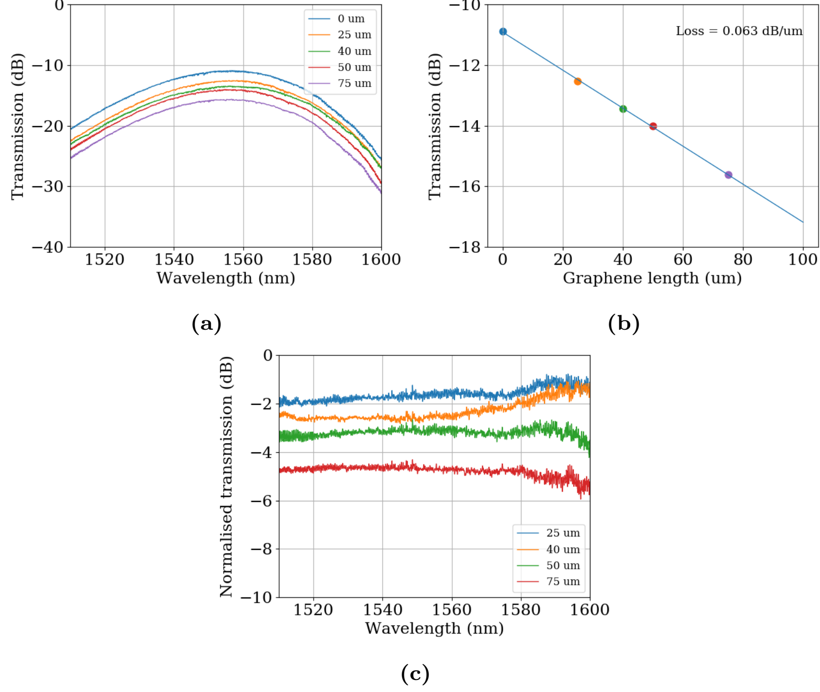



**Figure 1.27:** (a) Example of transmission spectra measured on waveguide with varying graphene coverage length. (b) Fitting of data of transmission as a function of length extracted from the measurement in (a). (c) Transmission spectra normalised to the reference waveguide.

a second grating coupler couples the light into an optical fiber and the output signal is measured by a power meter. The loss in dB is given by

$$L = 10 \log_{10} \left( \frac{P_{in}}{P_{out}} \right) \tag{1.20}$$

where $P_{in}$ (in W) is the power of the input optical signal and $P_{out}$ (in W) is the power of the output one. The measurement setup is calibrated to eliminate losses due to optical fibers and fiber connectors. Therefore, the measured transmission includes grating coupler losses, waveguide losses and losses due to graphene absorption. To normalise the measurements and eliminate the grating coupler losses, a waveguide without graphene is measured and used as reference. Waveguides with different graphene coverage length are measured at wavelengths ranging from 1510 nm to 1600 nm for the C-band and from 1260 nm to 1360 nm for the O-band. The different transmission spectra are first plotted together (Fig. 1.27a). The peak transmission value of each device length

is extracted, plotted as a function of graphene coverage length and a linear fit is performed (Fig. 1.27b). Graphene's absorption (in dB/µm) is extracted as the slope of this linear fit. The transmission normalised to the reference waveguide is also plotted to verify the flat absorption spectrum of graphene (Fig. 1.27c). In pristine graphene and without any voltage applied, the Fermi level is close to the Dirac point. As a consequence, graphene's absorption is at its maximum and the transmission is close to its minimum. In reality, graphene in ambient shows p-doping behaviour. Graphene's Fermi level is located in the valence band, causing the absorption to decrease and the transmission to increase. Therefore, graphene's doping affects the value of maximum transmission in the transmission spectra. This value is also affected by light scattering and absorption due to defects on CVD-grown graphene layers, such as wrinkles and grain boundaries. Furthermore, polymer residues and contaminants from processing can also cause increased absorption. To minimise the impact of these effects, it is important to extract the absorption loss from the fitting of transmission measurements of waveguides with varying graphene coverage length.

### 1.6.1 Characterisation of graphene electro-absorption modulators

**Electro-optical DC measurements.** After measuring the optical behaviour of the modulators in 'standard conditions', the same transmission measurement is performed while applying a DC bias across the device. The applied voltage sweep depends on the thickness of the oxide of the device being measured. For a device with 5 nm-thick $SiO_2$, the voltage is swept between -4 V and 4 V. For each device length, the transmission spectra at varying DC bias are plotted together (Fig. 1.28a). The maximum transmission of each spectrum is extracted and plotted as a function of DC bias to obtain the modulation curve (Fig. 1.28b). The extinction ratio of the device is calculated from the minimum and maximum of this curve as $ER = |T_{max} - T_{min}|$. The modulation efficiency is obtained by dividing the extinction ratio by the device length ($ME = ER/L_{device}$).

**Small signal high speed performance.** The high-speed performance of the graphene modulator is first characterised by performing small signal S-parameter measurements. The bandwidth of the modulator is measured using a 50 GHz lightwave component analyzer (LCA) (Fig. 1.29a). Before measurement, the system is calibrated with the response of the probe, cable and bias tee. The characteristic impedance of the transmission lines used for this measurement is 50 Ω. The frequency response of the modulator is measured between 100 MHz and 30 GHz at varying DC bias, using -8 dBm RF power and 12 dBm laser power. The choice of DC bias sweep is dictated by the experiment being carried out, but it is usually in the range between -3 V and 3 V for a modulator with 5 nm-thick $SiO_2$. From the normalised $S_{21}$-parameters

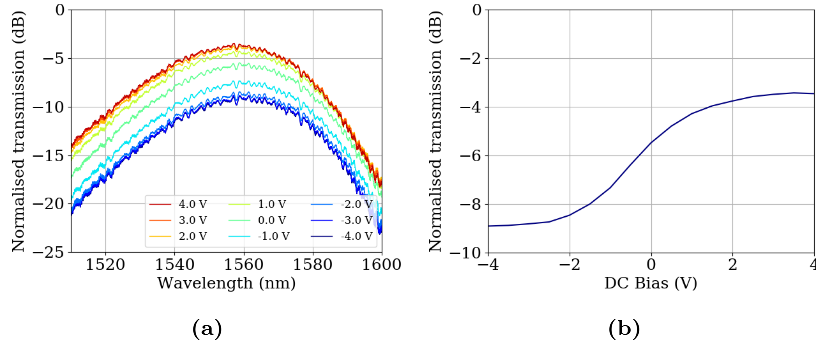



**Figure 1.28:** (a) Example of transmission spectra measured on a graphene modulator with $L_{device}$ = 75 µm at varying DC bias. (b) Extracted transmission as a function of applied DC bias, obtained from the measurement in (a).

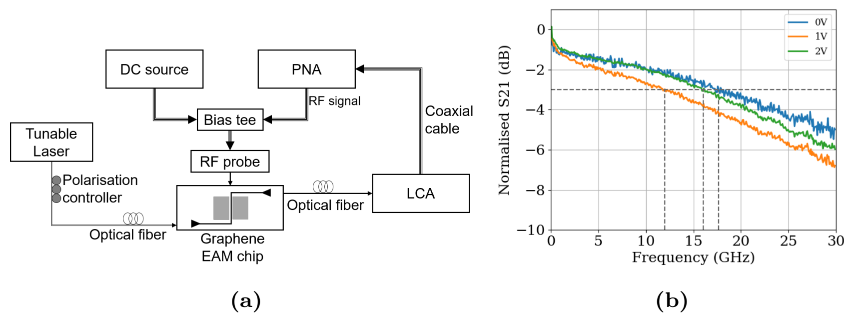



**Figure 1.29:** (a) Schematics of the setup used to measure S-parameters. (b) Measured $S_{21}$-parameters on a 25 µm-long EAM at varying DC bias.

measurement, plotted as a function of frequency, the 3dB bandwidth of the modulator is extracted (Fig. 1.29b).

**Large signal high speed performance.** The large signal modulation is measured with a pseudorandom binary sequence (PRBS) signal. The pattern length of this signal can vary between $2^7$-1 to $2^{23}$-1. The output signal from the modulator is amplified using an erbium-doped fiber amplifier (EDFA) and filtered using an optical tunable filter before reaching the oscilloscope (Fig. 1.30). The measurement is performed with a peak-to-peak voltage swing of 2.5 $V_{pp}$. The DC bias is chosen at a voltage value where the extinction ratio (at the selected $V_{pp}$) and the 3 dB frequency response are maximised. Starting from 5 Gbit/s, the data rate is increased until the measured eye diagram is not open anymore. For each eye diagram, the signal-to-noise ratio (SNR) and the dynamic extinction ratio are measured.

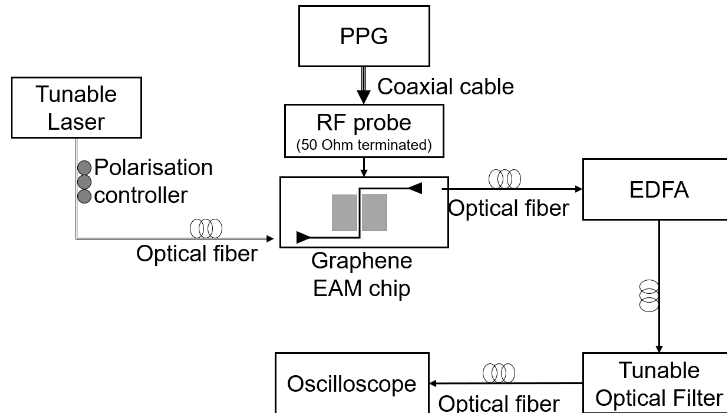



**Figure 1.30:** Schematics of the setup used for large signal characterisation.

### 1.6.2 Characterisation of graphene photodetectors

Characterisation methods of graphene photodetectors can vary depending on the type of photodetector being measured. For this reason, a detailed description of the measurements that were carried out in this thesis is given in Chapter 6, where the experimental work on photodetectors is explained.

## 1.7 Research objectives

With global data traffic continuously on the rise, there is strong demand for a technology that can meet the telecommunications industry requirements in terms of bandwidth, footprint, insertion loss and power consumption. As discussed in the course of this chapter, graphene has potential for photonics thanks to its remarkable optical properties (such as broadband absorption) and to its fast carrier dynamics. In addition, graphene is promising also when it comes to its integration in the silicon photonics platform. Graphene processing is compatible with complemental metal oxide semiconductor (CMOS) processing, which is currently used in silicon photonics. Graphene can be fabricated purely by post-processing on passive waveguide structures, therefore it can be integrated in the back-end-of-line (BEOL) and doesn't need full integration into the silicon photonics, or silicon nitride, platforms. This thesis entitled "Graphene-silicon photonic integrated devices for optical interconnects" aims to evaluate the potential of graphene-based photonics devices for use in future datacom applications. In particular, the following are some of the questions that this thesis aims to tackle:

- Can graphene devices be fabricated in a repeatable and reliable way?
- Can long-term performance stability be achieved in graphene devices?

- What are the performance limitations of graphene electro-absorption modulators?
- How can the performance of graphene electro-absorption modulators be improved?
- Is the performance of high-speed graphene electro-absorption modulators repeatable or can it only be achieved on a few champion devices?
- Can graphene modulators be demonstrated in both the C-band and the O-band, as expected from graphene's broadband absorption?
- What are possible device geometries for graphene photodetectors and what is their limitation?

To provide an answer to these questions, three goals have been identified. The first goal is the optimisation of the process flow used to fabricate graphene-based devices, such as graphene electro-absorption modulators, photodetectors and field-effect transistors. Graphene devices with and without passivation layer are fabricated and characterised. The second goal is to build a model to describe the working mechanism of single-layer graphene electro-absorption modulators. This model is used to optimise the high-speed performance of these devices without sacrificing other figures of merit. Several electro-absorption modulators are fabricated and characterised to corroborate the theoretical analysis. Wavelength division multiplexing transmitters based on single-layer graphene modulators are also designed and experimentally demonstrated. In addition, electro-absorption modulators based on a double-layer graphene structure are fabricated and analysed, theoretically and experimentally. The third and final objective is the fabrication and characterisation of graphene-based photodetectors. The performance of devices with different geometries is tested and conclusions are drawn based on these results and on literature reports.

The entirety of this work was performec in imec, Leuven. The graphene used for our work was provided by *Graphenea* (www.graphenea.com) or grown in-house in imec. The SOI and Si/$SiO_2$ wafers used for fabrication of graphene devices were fabricated in imec's 200 mm pilot line.

## 1.8 Thesis overview

Chapter 1 contains an introduction to optical interconnects, silicon photonics and graphene. We review state-of-the-art modulators and photodetectors, graphene properties and graphene-based photonic devices.

Chapter 2 explains the standard process flow used for fabrication of graphene-based devices, such as graphene electro-absorption modulators, photodetectors and field-effect transistors. A statistical analysis of results of TLM measurements performed on graphene FETs fabricated with this process flow is presented.

In Chapter 3, we introduce the process flow to fabricate passivated graphene devices. Using this flow, we fabricate graphene FETs with different passivation layers to test the quality of the encapsulation material. In the end, we fabricate and characterise passivated graphene electro-absorption modulators.

In Chapter 4, a theoretical model for single-layer graphene electro-absorption modulators is presented. Several modulators are fabricated and characterised to corroborate the theoretical analysis.

In Chapter 5, double-layer graphene electro-absorption modulators are studied as an alternative to single-layer modulators. A theoretical model is used to predict their static behaviour and experiments are carried out to test different types of oxide spacer between the two graphene layers. An analysis of performance optimisation is then presented.

Chapter 6 introduces graphene-based photodetectors. Different types of single-layer graphene photodetectors are studied, theoretically and experimentally.

**Table 1.2:** Summary of state-of-the-art graphene-based modulators.

| Modulator type | Ref. | Footprint (µm$^2$) | Wavelength (nm) | Optical BW (nm) | Pol. | Max T (°C) | IL (dB) | Static ER (dB) | Static power (mW) | Dynamic power (fJ/bit) | 3dB BW (GHz) | Max. Bit Rate (Gb/s) | $V_{pp}$ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SLG EAM | [9] | ~**500** | 1550 | **80** | TM | **175** | **3.8** | 2.5 | $<1\times10^{-10}$ | 350 | 2.6-5.9 | 10 | 2.5 |
| SLG EAM | [110] | ~**500** | 1550 | 70 | TM | - | 6 | 4.4 | $<1\times10^{-8}$ | **110** | **15.7** | **20** | 2.5 |
| SLG Ring | [10] | ~2500 | 1550 | <1 | TE | - | >15 | **12.5** | - | - | - | - | 8.8 |
| SLG MZI | [11] | ~20,000 | 1550 | - | TE | - | ~9 | 35 | $<1\times10^{-10}$ | 1000 | 5 | 10 | **2** |
| DLG EAM | [15] | ~**60** | 1550 | **140** | TM | **145** | **0.9** | 2 | - | - | **35** | - | - |
| DLG EAM | [111] | ~ 1200 | 1550 | - | TE | - | 20 | 3 | - | - | 29 | **50** | **3.5** |
| DLG Ring | [14] | ~10,000 | 1550 | <1 | TE | - | ~12 | **15** | - | 800 | 30 | 22 | 7.5 |

**Table 1.3:** Summary of state-of-the-art graphene-based waveguide photodetectors.

| Photodetector type | Effect | Ref. | Responsivity (A/W) | Responsivity (V/W) | Dark current (µA) | 3 dB BW (nm) | DC Bias (V) | Bit rate (Gbit/s) |
|---|---|---|---|---|---|---|---|---|
| Asymmetric contacts (Si wg) | PV | [19] | 0.016 | - | - | 45 | No | 50 |
| Asymmetric contacts (Si wg) | PV | [121] | 0.032 | 15 | - | 128 | 0.5 | - |
| Asymmetric contacts (SiN wg) | PB | [124] | 0.013 | - | - | - | 8 | - |
| Interdigitated contacts (SiN wg) | PV-PTE | [125] | 2.36 | - | 20 | 33 | 1 | - |
| Gra/Si Schottky junction | PV | [20] | 0.37 | - | $\sim$3 | - | 3 | - |
| Double-gated slot wg | PTE | [21] | 0.08 | 3.5 | - | 65 | 0.3 | - |
| Double-gated PhC wg | PTE | [22] | 0.17 | 4.7 | - | 18 | 0.4 | - |
| Double-gated plasmonic wg | PTE | [24] | - | 12.2 | 0 | 42 | 0 | - |
| Plasmonic wg | PB | [23] | 0.5 | - | -2mA | 110 | -0.4 | 110 |

Chapter 2

# Standard fabrication flow: process development and graphene electrical characterisation

The first goal of this PhD thesis is to improve and optimise the process flow used to fabricate graphene-based devices, such as graphene electro-absorption modulators and field-effect transistors. In the first part of this chapter, we explain and discuss the development of the standard process flow and we address the main fabrication challenges encountered. This flow will be used to realise the graphene-based devices presented later in the thesis. In the second part, we present electrical measurements performed on graphene TLM structures with different doping of the underlying silicon and different gate oxide thickness. We compare the results to assess whether these parameters influence graphene's properties, and we support our conclusions analysing measurements of graphene's Raman spectrum on the same samples. Some of the experiments in this chapter were carried out with advice from, or together with, Inge Asselberghs and Xiangyu Wu.

## 2.1 Introduction

Two different techniques were employed for the fabrication of the samples under study: optical lithography (photolithography), and electron-beam (e-beam) lithography. Both techniques have been employed for many years for the fabrication of microelectronic devices [127–129] and are based on lithography, one of the key drivers for the semiconductor industry. Lithographic patterning re-

lies on the transfer of a pattern to a photosensitive layer (photoresist). The solubility of this layer is changed by exposure to light, so that the pattern is revealed upon resist development. The patterned resist is used to transfer the design to the substrate or material below by etching or by deposition of an additional layer, e.g. a metal.

Both photolithography and e-beam lithography offer advantages and disadvantages. E-beam lithography has higher resolution than photolithography based on glass masks (10 nm versus 1 µm), allowing to fabricate devices with smaller dimensions. In addition, it offers great design flexibility, as the imprinted patterns can be changed every time a new exposure is performed. On the other hand, photolithography is a much faster method because all the patterns are imprinted on the photoresist simultaneously. E-beam lithography relies on sequential writing of the devices and is therefore a slow process. Photolithography was our preferred technique to fabricate the vast majority of our samples due to its faster nature. For this reason, we will refer from now on to photolithography, unless otherwise specified. E-beam lithography was eventually never used in the context of this thesis, but we consider it to be the next logical step to fabricate devices with smaller critical dimensions.

Different types of devices are employed for our experiments. Graphene field-effect transistors (FET) are used to study the electrical properties of graphene by means of the TLM technique explained in chapter 1. These devices are based on a simple $SiO_2$/Si wafer substrate, with a 90 nm-thick $SiO_2$ (Fig. 2.1a). The ultimate goal, however, is the fabrication of graphene photonics devices, such as graphene-silicon electro-absorption modulators (EAM) and photodetectors (PD). These devices are based on a silicon-on-insulator (SOI) substrate that undergoes multiple fabrication steps before being used for processing of graphene devices (Fig. 2.1b).

## 2.2 SOI substrate fabrication

The graphene photonics devices studied in this thesis are based on a 220 nm-thick silicon (Si) waveguide (Fig. 2.1b), fabricated on a silicon-on-insulator (SOI) wafer with 2 µm buried oxide in imec's 200 mm or 300 mm Si photonics platform [32]. The Si waveguide is partially etched on one side, creating a rib structure that allows to contact the waveguide through the 70 nm-thick Si slab layer. The waveguide is embedded in $SiO_2$ to ensure a planar surface, which is very important to obtain a good graphene transfer later on. Three phosphorus or boron implantation steps are carried out to minimise the Si contact and sheet resistance, without significantly increasing the waveguide loss. This leads to three regions with different doping concentrations, as shown in Fig. 2.1b: $n_{++}$ (or $p_{++}$) for the contact region, $n_{slab}$ (or $p_{slab}$) for the slab region and $n_{wg}$ (or $p_{wg}$) for the waveguide region. After Si waveguide patterning, a chemical-mechanical planarisation (CMP) step is performed to planarise the waveguides. To isolate graphene, that will be later transferred on these devices, from the

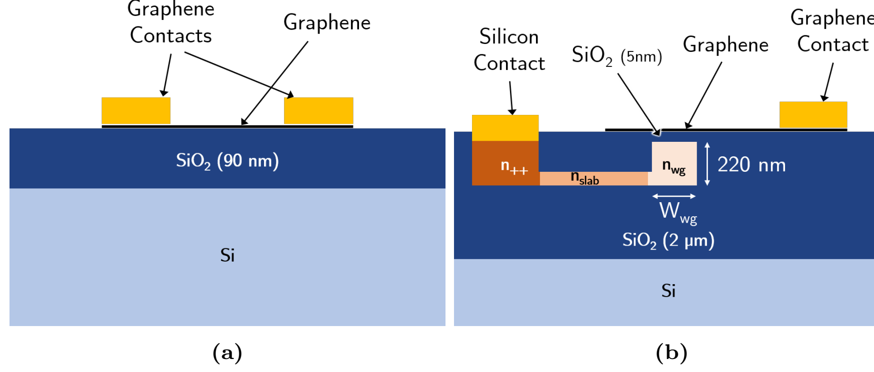



**Figure 2.1:** Schematic cross section of (a) a graphene FET device fabricated from a $SiO_2$/Si wafer substrate and (b) a single-layer graphene EAM fabricated from a SOI substrate.

Si waveguide, a layer of thermal oxide (most often 5 nm) is grown on top. As a last step, the wafer is mechanically diced. The dicing step is necessary for further processing of these devices, as graphene transfer can't yet be performed on wafer scale [86].

## 2.3 Graphene device fabrication: standard flow

Fabricating graphene devices is a challenging task. Graphene, as a 2D material, is easily affected by the way samples are handled during the fabrication process. Something as simple as grabbing the sample with tweezers too close to the area of interest, can negatively impact the final outcome. Therefore, extreme care is put in handling the samples always in the same way, so that results can be compared and reproduced as much as possible. However, the hardest challenges are the ones linked with the type of processing materials or recipes used. Because of the experimental nature of device fabrication, it is easy to identify a problem when a fabrication step fails, but difficult to recognise the cause. When a new issue arises, a set of experiments is usually carried out to isolate the source and find a solution.

The journey through graphene device fabrication is very similar for any type of starting substrate. The main steps that compose the fabrication flow are the following:

1. *Alignment markers.* Metal alignment markers are processed on the substrate to allow good alignment of the mask with the sample. This step is performed only for the $SiO_2$/Si substrate, because markers for the SOI substrate are already processed during the substrate fabrication explained in section 2.2.

2. *Graphene transfer.* A single layer of graphene is transferred from the original growth template to the target substrate.
3. *Graphene shaping.* Graphene is shaped in order to remove it from the areas on the substrate where it is not needed.
4. *Graphene contacts.* Metal contact pads are formed on the graphene layer.
5. *Silicon contacts.* Metal contact pads are formed on Si. This step is not needed for graphene FETs fabricated starting from $SiO_2$/Si substrate.

Each of these steps is carried out by following a detailed step-by-step recipe. These recipes are detailed in the upcoming sections. In some cases, such as for graphene shaping and graphene contact formation, we start from describing the initial recipe used. We explain the main issues encountered with this recipe and present the experiments performed to solve them. We then present the final fabrication recipe that we developed as a result of this optimisation process.

All the fabrication steps are performed in a cleanroom environment to minimise dust particles that can settle on the sample or on the optical mask and cause defects. Great importance is given to the cleanliness of the sample and of the graphene layer. Some general rules, which apply to all the fabrication steps, are followed rigorously. Before photoresist spinning, any dust particle that may have deposited on the sample is removed with compressed air. This procedure is repeated right before photoresist exposure, to avoid transferring unwanted shapes on the substrate. After exposure, the dissolution of photoresist, which is performed in acetone, is facilitated by heating up the solvent up to 45°C. This is followed by an overnight treatment in cold acetone to help eliminating additional residues and by IPA rinsing. In addition, every time a new sample is processed, the glass mask is properly cleaned following a strict cleaning procedure. These precautions are extremely important to ensure process repeatability.

Throughout this thesis, we follow the approach of always shaping graphene first and applying metal contacts afterwards. Following this rule, the number and the order of these steps can be modified, depending on the type of device fabricated and experiment performed. For example, to fabricate double-layer graphene (DLG) EAMs, an oxide deposition step followed by a second graphene transfer step are added after step 3, and step 5 is replaced by a second graphene metallisation step. Fig. 2.2 depicts the main steps of the final recipe used to fabricate SLG EAMs. Details about the step-by-step fabrication process followed for each experiment and type of device, together with the parameters used for the different recipes, are provided in appendix A. A list of the main tools used for sample processing is provided in Table 2.1.

### 2.3.1 Alignment markers

Metal alignment markers are processed on the $SiO_2$/Si blanket samples to be used in later steps to align the graphene shapes with the metal contacts. A

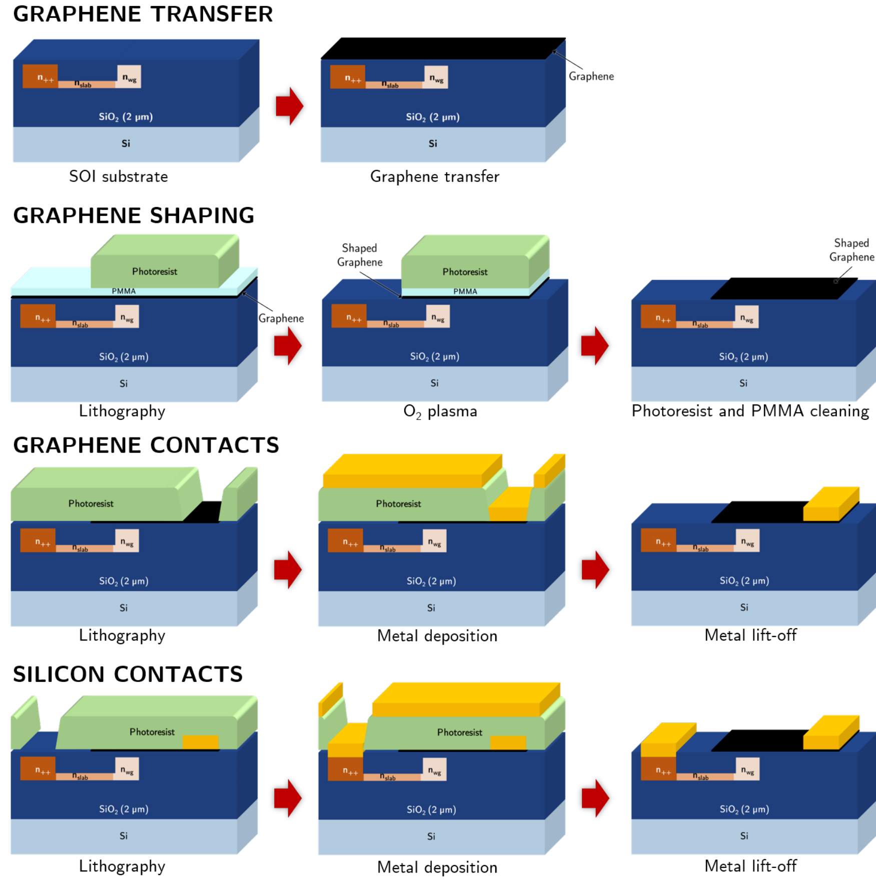



**Figure 2.2:** Main steps of the final recipe used to fabricate SLG EAMs.

**Table 2.1:** Equipment used for sample processing.

| Process | Tool | Details |
|---|---|---|
| Photolithography | Karl Suss MA6/MA8 | UV400, $\lambda \approx 405$ nm, contact mode, res. $\geqslant 1$ µm |
| E-beam lithography | Advantest F7000 | Res. $\geqslant 10$ nm |
| Metallisation | Alcatel SCM600 | Evaporation (thermal), $10^{-6}$ mbar |
| | Pfeiffer PLS 580 | Electron beam evaporation, 10 kV, $10^{-6}$ mbar |
| Seeding layer | Pfeiffer PLS 580 | Electron beam evaporation, $4\times10^{-6}$ mbar |
| Passivation layer | ASM Polygon 8200 | Atomic layer deposition (ALD) |
| Dielectric etching | Lam Versys® M | $BCl_3$-based reactive ion etching (RIE) |

positive resist and a lift-off process are used. The standard metal stack used for alignment markers is Ti (2nm)/Pd (50 nm).

The step-by-step recipe used for alignment markers is the following:

1. Pre-cleaning: acetone at 45°C for 5 min + IPA rinse at RT
2. Drying bake: hotplate at 120°C for 5 min
3. Spin coating: IX845 at 4000 rpm for 30 sec (3 sec ramp)
4. Curing: hotplate at 120°C for 1 min
5. Exposure: hard contact for 8 sec
6. Development: OPD5262 for 90 sec + DIW rinse
7. Metal deposition: Ti (2nm)/Pd (50 nm) by e-gun evaporation
8. Lift-off: acetone at 45°C for 3 hrs* + IPA rinse at RT

### 2.3.2 Graphene transfer

Graphene used for our experiments is grown by chemical vapour deposition (CVD) at wafer scale, typically on a copper (Cu) or platinum (Pt) substrate. The main techniques used for growth and transfer of synthetic graphene have been explained in chapter 1. The development of such techniques is outside the scope of this work and therefore it will not be explained in details [86]. The single-layer graphene used for our experiments was grown and transferred in-house [87, 88] or by the commercial vendor *Graphenea* (www.graphenea.com). The target substrate is generally diced to a size of about 2 by 2 cm$^2$ and graphene is subsequently transferred onto the target dies. Because of the topography of the SOI substrates in the proximity of the waveguides, which vary between 0 and 20 nm across the wafer, graphene on these samples usually exhibits more wrinkles and defects compared to simple $SiO_2$/Si substrates.

### 2.3.3 Graphene shaping

#### Initial graphene shaping recipe

To obtain graphene coverage only on selected areas of the substrate, a graphene shaping step is performed by photolithography and dry etching. The first fabrication recipe we tested to shape graphene included the use of a single layer of photoresist. The sample is first cleaned in acetone and IPA and then baked at 120°C to remove moisture. The sample is then spin coated with a layer of positive photoresist, IX845. The expected photoresist thickness is $\sim$ 1 µm. After resist baking, the graphene pattern is transferred from the optical mask to the photoresist by exposing it to UV light at a wavelength of 405 nm. The exposure time is a very critical parameter, where a variation as small as 0.2 s leads to different results. An underexposed resist will fail to develop, while an overexposed resist will lead to smaller-than-desired graphene

shapes. Similarly, the development time of the photoresist is also an important parameter. In this case, a variation of $\sim$ 2 s makes a difference in the final outcome. If the development time is too long, the non-exposed regions of the photoresist will start dissolving. If too short, the exposed photoresist will not be removed completely. After development, the quality of the photoresist is checked under a green light optical microscope. Alignment marks are the most important feature to check to make sure graphene is properly aligned. This is particularly crucial when dealing with a SOI substrate, because a small alignment error can lead to partial or no graphene waveguide coverage. The resolution of photolithography is $\sim$ 1 µm, therefore we always foresee an error margin of $\sim$ 1 µm when preparing the designs. Within the limits of the optical microscope, it is also important to check whether the photoresist seems well developed. If the results are not satisfying, the exposure and development steps are repeated after cleaning the photoresist from the sample in acetone and isopropyl alcohol (IPA). If the photoresist is successfully developed, an oxygen plasma treatment is performed for 2 minutes to etch graphene where it is not covered by photoresist. After etching, the photoresist is completely removed from the sample in acetone at 45°C overnight, followed by a cleaning step in IPA at room temperature (RT). The detailed initial step-by-step recipe we used is the following:

1. Pre-cleaning: acetone at 45°C for 5 min + IPA rinse at room temperature
2. Drying bake: hotplate at 120°C for 5 min
3. Spin coating: IX845 at 4000 rpm for 30 sec with 3 sec ramp (photoresist thickness = $\sim$ 1 µm)
4. Curing: hotplate at 120°C for 1 min
5. Exposure: hard contact for 8 sec
6. Development: OPD5262 for 90 sec
7. Graphene etching: $O_2$ plasma for 2 min at 100 W
8. Sample cleaning: acetone at 45°C overnight + IPA rinse at RT

**Graphene delamination**

During the development step in OPD5262, initially we observed severe graphene delamination caused by intercalation of the TMAH-based chemical under the graphene layer. For graphene patterning, a large part of the photoresist covering the sample is developed and only a few separate rectangles are imprinted on the remaining photoresist. These shapes are attacked by the intercalated developer on all sides, causing the drifting or stripping of the areas that should remain covered by the resist.

One possible root cause of this problem is the presence of moisture between graphene and the substrate, which causes low adhesion and can lead to a higher

**Table 2.2:** Graphene delamination tests in OPD5262.

| Set | Hotplate | | $N_2$ oven | | Vacuum oven | | Delamination time |
|---|---|---|---|---|---|---|---|
| | T | Time | T | Time | T | Time | |
| # 1 | - | - | - | - | - | - | $< 1s$ |
| # 2 | 120°C | 10m | - | - | - | - | $< 1s$ |
| | 120°C | 20m | - | - | - | - | $\sim 15s$ |
| | 120°C | 30m | - | - | - | - | $< 1s$ |
| # 3 | - | - | 120°C | 2h | - | - | $\sim 4m$ |
| | - | - | 120°C | 3h | - | - | $\sim 2s$ |
| | - | - | 165°C | 3h | - | - | $\sim 2s$ |
| | - | - | 200°C | 4h | - | - | $\sim 2s$ |
| # 4 | - | - | - | - | RT | 64h | $\sim 4s$ |
| | - | - | - | - | 150°C | 58h | $\sim 4s$ |
| | - | - | - | - | 400°C | 40h | $\sim 3s$ |
| # 5 | 120°C | 10m | 120°C | 1h45m | - | - | $\sim 15s$ |
| | 120°C | 20m | 120°C | 1h45m | - | - | $\sim 15s$ |
| | 120°C | 30m | 120°C | 1h45m | - | - | $\sim 15s$ |
| # 6 | 120°C | 5m | - | - | 100°C | 58h | $\sim 40s$ |
| | 120°C | 10m | - | - | 100°C | 58h | $\sim 1m30s$ |
| | 120°C | 15m | - | - | 100°C | 58h | $\sim 1m30s$ |

chance of delamination. Therefore, we carried out sets of experiments on unprocessed Si/$SiO_2$/graphene samples with the goal of reducing the moisture before processing and avoiding graphene delamination. Each experiment was based on two steps. First the samples were baked, then they were immersed in a beaker with a developer to test the adhesion of graphene with the substrate. Using a chronometer, we timed how long it took for graphene to visually start delaminating from each sample. We tested different baking treatments, i.e. hotplate, $N_2$ oven and vacuum oven. Each treatment was tested at different temperatures or different baking times, and was employed stand alone or in combination with other treatments. The delamination tests were carried out in OPD5262. Table 2.2 reports a summary of the sets of experiments performed with details of the baking temperatures and times and of the recorded delamination times. We found no clear correlation between the type of treatment or the baking time and the time it took for graphene to delaminate. Regardless of the treatment and of the type and concentration of the developer, graphene kept delaminating when immersed in OPD5262 (Fig. 2.3), even if the delamination time was sometimes longer compared to a sample without baking treatment. Not even increasing the baking time to as long as 64 h helped im-

proving the delamination time to more than 90 seconds. Considering that the development time used in our recipe is 90 seconds, none of these experiments can be considered a success in order to prevent graphene delamination.

To conclude the experiment, we performed further delamination tests in different developers. We used diluted OPD5262 (OPD5262:$H_2O$ 1:10 and 1:4), Microposit™ 351 and Microstrip® 2001. In all cases, graphene delaminated in less than 2 minutes, indicating the necessity to undertake a different route to solve the issue.

### Final graphene shaping recipe

In order to prevent delamination due to the exposure of graphene to the developer, we introduced a PMMA protective layer in the recipe, to be spin-coated before the photoresist. During lithography, the photoresist is exposed and developed as before, but the PMMA layer keeps covering the whole sample and protects the graphene layer. When the sample undergoes $O_2$ plasma etching, the PMMA is etched away together with graphene, creating the desired shapes. The remaining PMMA that covers the graphene shapes is dissolved in acetone together with the photoresist during the last cleaning step in the recipe. The addition of the PMMA layer proved to be successful to prevent graphene delamination and was therefore integrated in the final recipe. The resulting fabrication flow is the following, where the differences with the initial graphene recipe on page 45 are emphasised in bold:

1. Pre-cleaning: acetone at 45°C for 5 min + IPA rinse at RT
2. Drying bake: hotplate at 120°C for 5 min

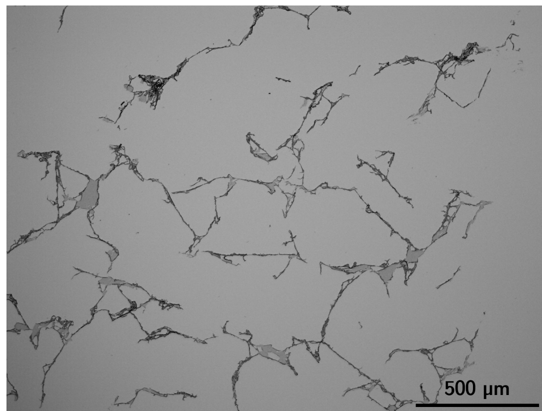



**Figure 2.3:** Si/$SiO_2$ substrate with delaminated graphene after immersion in OPD5262.

3. **Spin coating 1: Chlorobenzene PMMA 3% at 6000 rpm for 60 sec (3 sec ramp)**
4. **Curing 1: hotplate at 120°C for 3 min**
5. Spin coating 2: IX845 at 4000 rpm for 30 sec with 3 sec ramp (photoresist thickness = ∼ 1 µm)
6. Curing 2: hotplate at 120°C for 1 min
7. Exposure: hard contact for 8 sec
8. **Development: Microposit™ 351 for 60 sec + DIW rinse**
9. Graphene etching: $O_2$ plasma for 12 min at 100 W
10. Sample cleaning: acetone at 45°C overnight + IPA rinse at RT

### 2.3.4 Graphene contacts

The procedure to fabricate metal contacts to graphene is based on a lift-off procedure. After exposure and development, the photoresist covers the whole sample except the areas were the metal contacts have to be fabricated. Once again, the quality of the developed photoresist and of the alignment is assessed under a green light optical microscope. After metal evaporation, the lift-off process is carried out by placing the sample in acetone at 45°C. To achieve low graphene contact resistance, we use 50 nm-thick palladium (Pd) to contact graphene [130]. The photoresist dissolves, lifting off the metal layer deposited on top, and only the desired metal shapes which are in contact with the substrate remain imprinted. After lift-off, the sample is once again cleaned in IPA at room temperature. The exposure and development times in this step are even more critical than in the shaping step. Any residue of photoresist on the contact area caused by a non-optimal photolithography can lead to delamination of the metal contacts and therefore to lift-off failure.

In this case, the photoresist is protecting most of the sample area (dark-field mask), with only a few openings exposing graphene to the developer. The small contact area is enough to avoid delamination of graphene during resist development, therefore the PMMA layer is not needed in this step of the process.

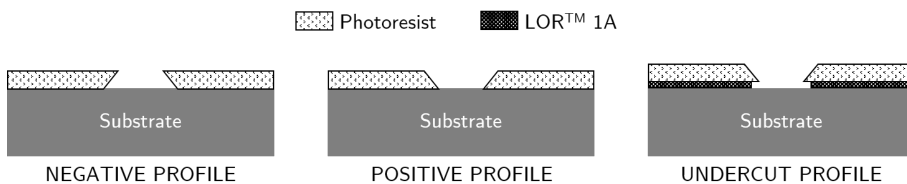



**Figure 2.4:** Comparison between different types of photoresist profiles: negative, positive or undercut.

The cleanest way to fabricate good quality metal contacts is through lithography with a photoresist with a negative profile (Fig. 2.4). A negative profile allows to achieve a clean cut between the metal that should adhere to the substrate to form the contacts and the one that needs to be removed via lift-off. This profile is achieved by means of an image reversal photoresist. The resist is first exposed using an inverted mask. At this point the resist behaves like an exposed positive resist with positive side-walls. The sample then goes through a reversal bake to cross-link the exposed area, while the unexposed area remains photo-active. Finally, a flood exposure (without mask) is performed to make the resist, which was not exposed in the first step, soluble in the developer.

After unsuccessfully trying to develop an in-house recipe for processing with a negative photoresist, we tested bi-layer processing as an alternative solution which would allow to obtain a similar result. Bi-layer processing consists in using two layers of photoresist. The first layer, LOR™ 1A, is coated and pre-baked before the photoresist. When the sample is exposed, both LOR™ and resist layers will become soluble in the developer. LOR™ resists develop isotropically, creating a bi-layer re-entrant profile (Fig. 2.4) which ensures discontinuous metal deposition on top. The contact fabrication recipe we adopted initially is the following:

1. Pre-cleaning: acetone at 45°C for 5 min + IPA rinse at room temperature
2. Drying bake: hotplate at 120°C for 5 min
3. Spin coating 1: LOR™ 1A at 4500 rpm for 45 sec (thickness = 0.1 µm)
4. Curing 1: hotplate at 190°C for 5 min

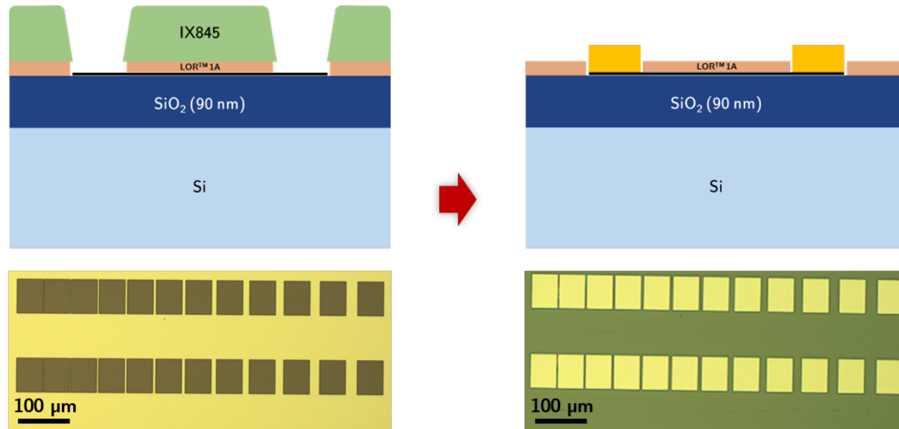



**Figure 2.5:** Contact fabrication using a bi-layer process with LOR™ 1A and IX845 on a TLM structure. The lithography (left) and lift-off (right) steps were successful, but in some cases the contact pads delaminated when the sample was immersed in OPD5262 to strip the LOR™ 1A.

5. Spin coating 2: IX845 at 4000 rpm for 30 sec
6. Curing 2: hotplate at 120°C for 1 min
7. Exposure: low vacuum for 7.6 s
8. Development: OPD5262 for 52 s
9. Metal deposition
10. Lift-off: cold acetone overnight
11. Sample cleaning: OPD5262 for 10sec + DIW rinse

This recipe turned out to be successful all the way until the second-to-last step (Fig. 2.5, right). The lift-off in acetone allows to strip the IX845 photoresist, but not LOR™ 1A. The last cleaning step in OPD5262 is therefore necessary to remove the LOR™ layer from the sample. However, after LOR™ is dissolved and completely removed from the sample, the graphene patches come directly in contact with the developer, causing immediate delamination of graphene and the metal layer on top.

Another issue introduced by this recipe is that LOR™ 1A is only 0.1 µm thick, therefore only a very thin metal layer can be deposited on the sample, or the lift-off would not be successful. A way to overcome this is by adding an extra metallisation step to process thicker support contact pads on top. This complicates the fabrication by adding an extra lithography step. The metal we mostly used to contact graphene in our devices is palladium (Pd), due to its low contact resistance with graphene [130]. Palladium has weak adhesion with the substrate, showing poor resistance to the fabrication of an additional metal layer on top, as visible from the delaminated graphene contact pad in Fig. 2.6.

Eventually, we developed a recipe for metal contacts using IX845 and a positive resist profile. Even though using a positive profile is not the cleanest solution, the thickness of our metal contacts is only $\sim$ 50 nm, which is very thin compared to the 1 µm-thick IX845. Therefore, a successful lift-off can be obtained if the process is assisted with a pipette to blow off the metal layer, while the sample is in a beaker of clean hot acetone. The strong flow of acetone helps the metal that has to lift-off to detach from the metal shapes that form the contact pads.

The final step-by-step recipe used for graphene contacts is the following :

1. Pre-cleaning: acetone at 45°C for 5 min + IPA rinse at RT
2. Drying bake: hotplate at 120°C for 5 min
3. Spin coating: IX845 at 4000 rpm for 30 sec (3 sec ramp)
4. Curing: hotplate at 120°C for 1 min
5. Exposure: hard contact for 8 sec
6. Development: OPD5262 for 90 sec + DIW rinse

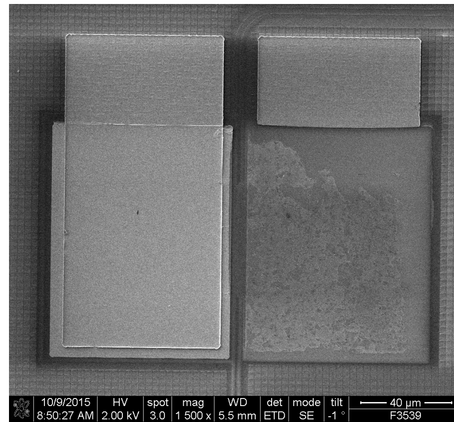



**Figure 2.6:** Top-down SEM image of a graphene EAM fabricated with support pads. The metal contact to Si is on the left side of the waveguide and is covered by a second metal contact, the support pad. On the right side of the waveguide, the metal contact to graphene has delaminated together with the portion of support pad covering it, leaving only a part of the support pad and paritally delaminated graphene on the substrate.

7. Metal deposition: Pd (50 nm) by e-gun evaporation
8. Lift-off: acetone at 45°C for 3 hrs* + IPA rinse at RT

* Put 3 pipettes of hot acetone in a new small beaker. Move the sample in the small beaker very quickly and blow acetone very hard on the sample with the pipette, staying as close as possible to the sample.

### 2.3.5 Silicon contacts

The fabrication of Si contacts is in every way similar to the one of graphene contacts, with only one difference. After exposure and development, and before evaporating the metal layer, the sample undergoes a wet etching process in buffered hydrofluoric acid (BHF) to remove the thermal oxide layer from the contact area. The oxide growth rate in air at room temperature after BHF etching has a logarithmic behaviour and is 0.2 nm/decade [131]. To avoid excessive oxide re-growth, it is important to evaporate the metal for contacts right after the etching step is complete. For Si contacts we use a metal stack made of titanium (Ti), platinum (Pt) and gold (Au). We first deposit 20 nm of Ti by thermal evaporation. Without removing the sample from the chamber, we evaporate 20 nm of Pt to act as protection layer against oxidation of Ti. To end, we transfer the sample to another tool where we deposit 30 nm of Au by e-gun evaporation. The Au layer allows to achieve good contact with the probes used for measurements.

The step-by-step recipe used for Si contacts is the same as for graphene contacts on page 50 up until step 6. The remaining steps are as follows:

7. $SiO_2$ etching: BHF for 1 min (right before loading the sample in the metal evaporation tool)
8. Metal deposition: Ti (20 nm)/Pt (20 nm) by thermal evaporation; Au (30 nm) by e-gun evaporation
9. Lift-off: acetone at 45°C for 3 hrs* + IPA rinse at RT

* Put 3 pipettes of hot acetone in a new small beaker. Move the sample in the small beaker very quickly and blow acetone very hard on the sample with the pipette, staying as close as possible to the sample.

## 2.4 Characterisation of graphene TLM structures

### 2.4.1 Sample design

In chapter 1 (section 1.4.2), the TLM method was introduced as the tool of choice to extract graphene's contact and sheet resistance from its electrical response. For this reason, the mask design used to fabricate graphene photonics devices, such as SLG EAMs, always includes a design area with different flavours of TLM structures to allow electrical testing of graphene properties. The flow used to fabricate these TLM structures is the standard flow of SLG EAMs described in appendix A, section A.2.1. Throughout this PhD work, many samples based on SOI substrates were fabricated with different characteristics, such as different type and level of Si doping and gate oxide thickness. As a consequence, a variety of TLM structures were measured to test the influence of these parameters on the electrical characteristics of graphene. The availability of such big number of samples allows to perform a large scale study of graphene's properties.

The TLM structures used in this thesis are designed to have channel lengths of 2, 3, 5, 6, 8, 10, 15, 20, 25, 30 and 35 µm, while the channel width is 50 µm. Fig. 2.7 shows the cross section of two types of graphene FETs that are fabricated on SOI substrates and that form the TLM structures. In one case, the gate oxide is only the grown thermal oxide, which is 5 nm-thick (Fig. 2.7a). In the second case, an extra oxide thickness of 150 nm is fabricated under the TLM structures and, together with the thermal oxide, it forms a 155 nm-thick gate oxide layer (Fig. 2.7b). Graphene used for the samples presented in this section was grown by the commercial vendor *Graphenea*.

### 2.4.2 Electrical characterisation of TLM structures

The graphene FETs that form the TLM structures are measured in a backgated configuration. The backgate voltage sweep was adapted according to

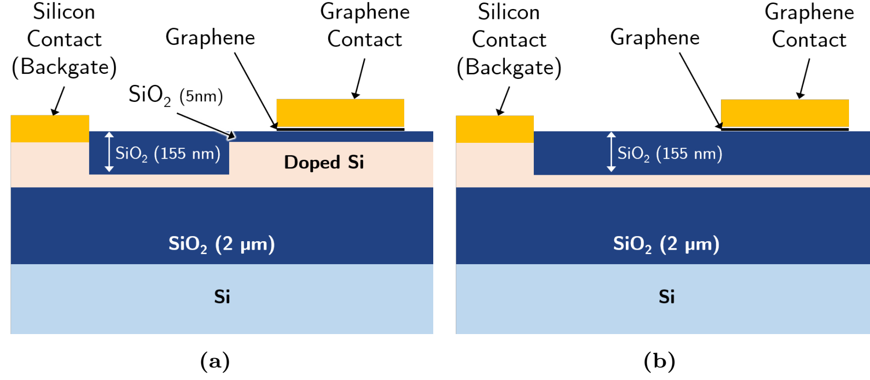



**Figure 2.7:** Cross section of graphene FETs used for TLM measurements with (a) 5 nm gate oxide and (b) 155 nm gate oxide.

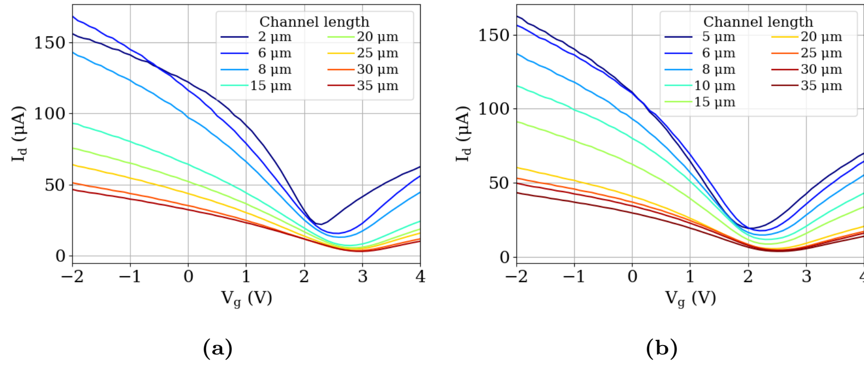



**Figure 2.8:** Example of $I_d$-$V_g$ measurements performed on a TLM structure with $t_{ox}$ = 5 nm and with (a) n-doped Si ($n = 2.4e18cm^{-3}$) and (b) p-doped Si ($p = 1.9e18cm^{-3}$).

the thickness of the gate oxide, following the rule of never applying more than 2 V per 1 nm of oxide thickness to avoid oxide breakdown. As a result, the graphene FETs with 5 nm-thick gate oxide were typically measured with a maximum voltage sweep of -3 V to 8 V, while the ones with 155 nm-thick gate oxide of -30 V to 90 V. The choice of the latter is dictated by the tool limitations, which allows to apply maximum 100 V. The lower limit was chosen to be lower (in absolute value) than the upper limit due to graphene's charge neutrality point usually being located at positive voltage in these structures because of p-doping in graphene. Examples of $I_d$-$V_g$ measurements performed on TLM structures with n-doped and p-doped Si are shown in Fig. 2.8.

The box and whisker plots in Fig. 2.9 show a summary of extracted values of graphene's contact resistance $R_{graC}$, mobility $\mu_c$ and neutrality point $V_{NP}$

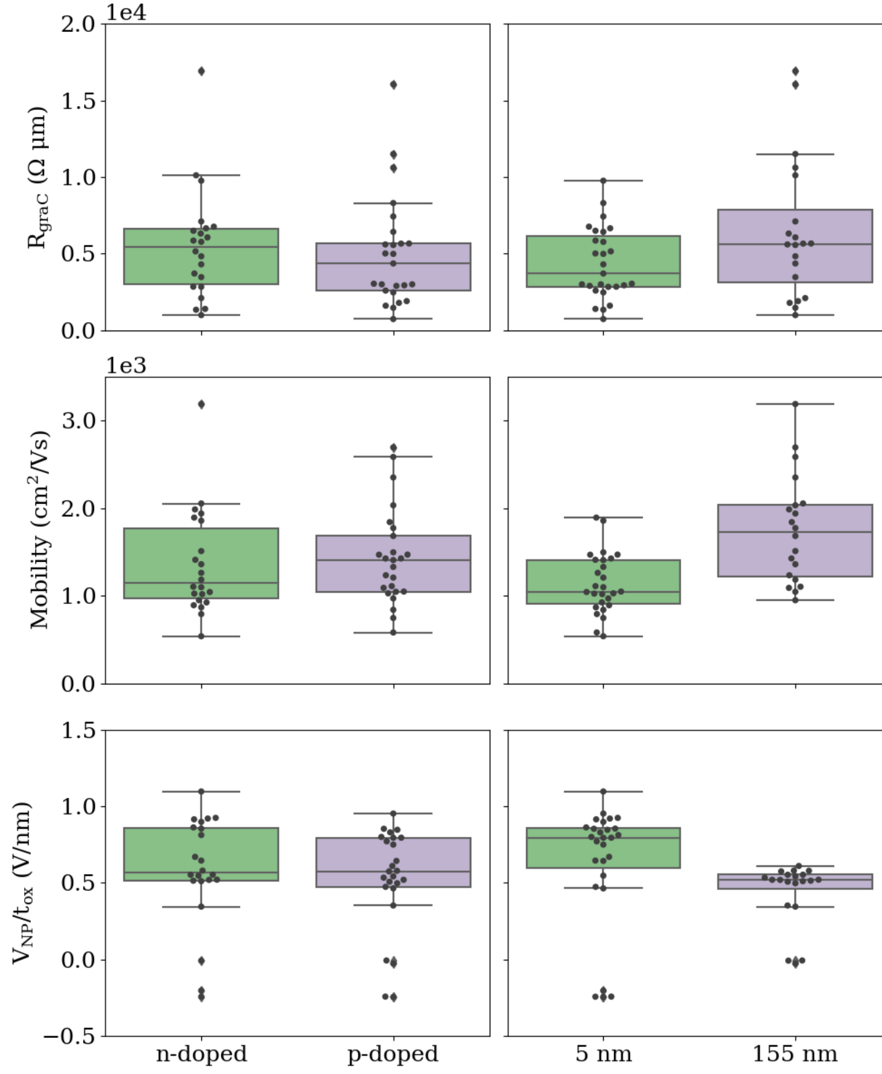



**Figure 2.9:** Values of graphene's contact resistance $R_{graC}$, mobility $\mu_c$ and neutrality point $V_{NP}$ (normalised to the gate oxide thickness $t_{ox}$) obtained from electrical measurements on TLM structures with different Si doping and gate oxide thickness.

from various samples used in this thesis. The contact resistance is extracted at the neutrality point, while the mobility is extracted at $n_s = 8.6e12$ cm$^{-2}$. The values of $V_{NP}$ are normalised to the gate oxide thickness $t_{ox}$, so that a comparison between structures with different $t_{ox}$ is possible. It is important to notice that a significant sample-to-sample variation is present and is demonstrated by

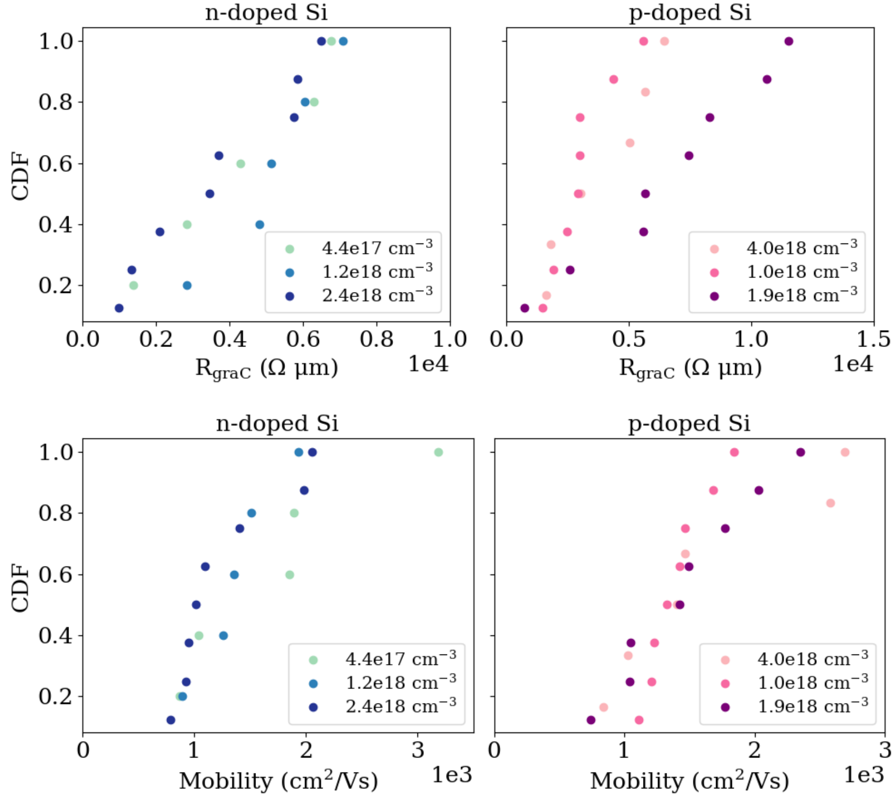



**Figure 2.10:** Cumulative distribution function (CDF) plots showing the empirical cumulative distribution of graphene's contact resistance $R_{graC}$ and mobility $\mu_c$ for different Si doping levels, for p-typed and n-type Si doping.

the wide distribution range of the data sets. This indicates a variability in graphene's quality, especially for the samples used in this analysis where graphene is exposed to air, due to the invasive fabrication process steps. It is therefore important to establish a method to conclude with reasonable certainty whether one data set is significantly different from another and if the differences are due to variability in graphene's properties. A simple quantitative comparison between two different box plots can be performed by calculating the difference between the medians (DBM) of the two data sets and dividing it by the overall visible spread (OVS), which is the difference between the greatest of the two upper quartiles and the smallest of the two lower quartiles [132]. When we divide the BDM by the OVS and multiply by 100, we obtain a percentage which

helps quantifying the inference of the two data sets:

$$\frac{BDM}{OVS} \times 100 \tag{2.1}$$

For a number of samples of 30 or less, which is the case here, the two groups are statistically different if this percentage is over 33% [132]. The box and whisker plots on the left column of Fig. 2.9 compare values obtained from TLM structures fabricated with underlying p-doped or n-doped Si. For these data sets, we obtain overlapping percentages of 27.4%, 32.8% and 2.1% for $R_{graC}$, $\mu_c$ and $V_{NP}/t_{ox}$ respectively. This result indicates that the type of Si doping does not affect graphene's properties. The box plots on the right column of Fig. 2.9 show a comparison between the two different gate oxide thicknesses, 5 nm and 155 nm. For $R_{graC}$ we obtain an overlapping percentage of 38.4%, which is slightly higher than the cut-off limit of 33%. Most importantly, we obtain percentages of 60.2% and 69.3% for $\mu_c$ and $V_{NP}/t_{ox}$, indicating a statistical difference between the two data sets. Therefore, we can conclude that the TLM structures with thicker gate oxide exhibit higher mobility and lower graphene doping.

To conclude the analysis of the electrical measurements, we perform a final comparison between values of $R_{graC}$ and $\mu_c$ obtained from TLM structures with different levels of Si doping using cumulative distribution function (CDF) plots. The CDF is the probability that the variable takes a value less than or equal to x. That is

$$F_X(x) = P(X \leq x) \tag{2.2}$$

In a CDF plot, the horizontal axis is the allowable domain for the given probability function. Because the vertical axis is a probability, it must fall between zero and one and it increases from zero to one as we go from left to right on the horizontal axis. CDF plots are generated for each level of Si doping, separately for n-doped and p-type doped Si, and are shown in Fig. 2.10. No clear correlation is visible between the values of $R_{graC}$ and $\mu_c$ and the level of doping in Si, therefore we can conclude that the latter does not affect graphene's properties.

As pointed out before, a variability in graphene's quality causes the data to be spread in a wide range. For example, the values of graphene's mobility for p-doped Si with carrier concentration of $p$ = 1.9e18 cm$^{-3}$ range from 750 to 2350 cm$^2$/Vs, while the contact resistance ranges from 730 to 11500 Ω µm. This variation is linked with the processing used to fabricate these devices. Polymers and solvents come directly in contact with the graphene layer, leaving residues that increase the scattering rate in graphene and reduce its conductivity. Similarly, also wrinkles and non-uniformities from graphene transfer are present on the graphene layer and affect its electrical behaviour. Not enough data is available to perform a thorough study of the graphene quality variability within a single sample. However, where available, it indicates that even within the same sample graphene is not always uniform.

**Table 2.3:** Parameters extracted from Raman measurements performed on graphene devices after processing, with varying characteristics of the underlying Si doping.

| Doping type | Doping conc. (cm$^{-3}$) | $I_D/I_G$ | $I_{2D}/I_G$ | $FWHM_{2D}$ |
|---|---|---|---|---|
| n-doped | 4.4e17 | 0 | 1.2 | 110 |
| n-doped | 1.2e18 | 0.2 | 3.3 | 53 |
| n-doped | 1.6e18 | 0.3 | 2.9 | 101 |
| p-doped | 1.2e18 | 0.5 | 2.3 | 100 |
| p-doped | 1.9e18 | 0.2 | 1.2 | 108 |

**Table 2.4:** Comparison of parameters extracted from Raman spectra measured before and after graphene device processing.

| | Doping type | Doping conc. (cm$^{-3}$) | $I_D/I_G$ | $I_{2D}/I_G$ | $FWHM_{2D}$ |
|---|---|---|---|---|---|
| Before processing | n-doped | 1.6e18 | 0.07 | 2.9 | 29 |
| | p-doped | 1.2e18 | 0.06 | 3.0 | 25 |
| After processing | n-doped | 1.6e18 | 0.34 | 2.9 | 101 |
| | p-doped | 1.2e18 | 0.5 | 2.3 | 100 |

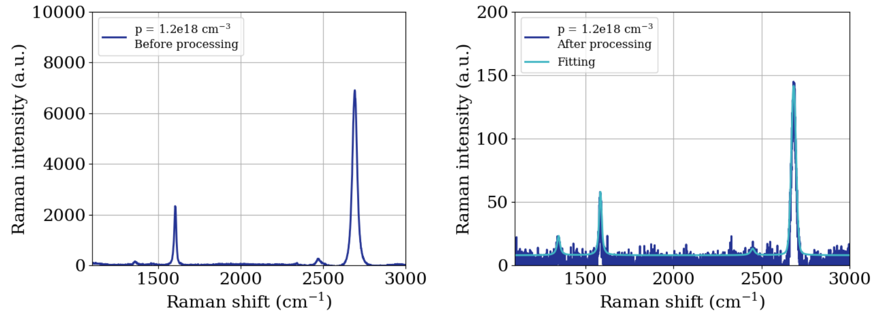



**Figure 2.11:** Raman spectra measured on graphene on top of p-type Si with doping level $p = 1.2e18cm^{-3}$ (a) before device processing and (b) after device processing.

Values of contact resistance between Pd and graphene have been shown in literature to vary between $\sim$ 80 [133] and $\sim$ 6000 Ω µm [134]. The values measured on our samples mostly fall within that range (Fig. 2.9). The presence of samples showing higher values indicates that an optimisation of the contact resistance is necessary. For instance, patterning the graphene contact area [135] or engineering the contact via ion bombardment [133, 136] have been proven to be effective methods towards reducing the metal-graphene contact resistance.

### 2.4.3 Raman characterisation

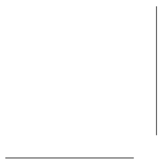
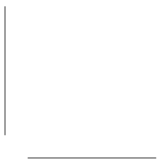
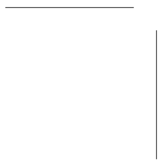
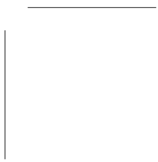
In addition to electrical measurements, we measured Raman spectra to compare graphene's quality after processing among samples with different type and level of doping of the underlying Si. For this purpose we compare the intensity ratio of the D- and G-peaks ($I_D/I_G$) to identify the presence of defects. We then compare the intensity ratio of the 2D- and G-peaks ($I_{2D}/I_G$) and the full width half maximum of the 2D-peak ($FWHM_{2D}$) to confirm the presence of a sharp, high and symmetric 2D-peak characteristic of high-quality, defect-free graphene. The most important parameters extracted from the spectra are reported in Table 2.3. Fluctuations in the intensity of the D-peak are observed, indicating that the presence of defects is subject to sample-to-sample variability. Similarly, the intensity of the 2D-peak shows fluctuations that do not correlate with the level or the type of Si doping used. The values of the full width at half maximum of the 2D-peak ($FWHM_{2D}$) are consistent on almost all the samples. In two cases, measurements of Raman spectra were performed before and after device processing on the same sample to check the influence of the fabrication flow on the quality of the graphene layer. Table 2.4 reports a comparison of parameters extracted from Raman spectra measured on graphene on Si with n-type doping ($n = 1.6e18cm^{-3}$) and p-type doping ($p = 1.2e18cm^{-3}$). Raman spectra measured on the sample with p-type Si doping ($p = 1.2e18cm^{-3}$) are plotted in Fig. 2.11. In both cases, a distinct increase in the intensity of the D-peak and in the value of $FWHM_{2D}$ after processing is observed. This indicates an increased number of defects on the sample following device fabrication, most likely due to polymers and solvent residues.

## 2.5 Conclusions

In this chapter, we presented the standard processing flow and steps required to fabricate graphene-based devices. This flow was used to process most of the graphene-based devices during the time frame of this thesis. We then described the main fabrication challenges we encountered, which are an indication of the difficulty of handling samples with a 2D material such as graphene. Graphene delamination during the graphene shaping step was solved by introducing an intermediate PMMA protective layer between graphene and the photoresist. Contacts fabrication proved difficult, because the techniques usually employed for this step caused graphene or metal contact delamination. In the end, a simple process involving a positive photoresist was developed.

Finally, we showed the results of electrical measurements performed on linear transfer length measurement (TLM) structures, used to extract graphene's electrical properties. We analysed values of graphene's contact resistance $R_{graC}$, mobility $\mu_c$ and neutrality point $V_{NP}$ extracted from TLM measurements performed on a large number of devices with different Si doping and different gate oxide thickness. We concluded that the type and level of Si

doping have no detectable effect on graphene's electrical properties, and confirmed this result with Raman measurements. The gate oxide thickness seems to affect graphene's mobility and position of the neutrality point, where the TLM structures with thicker oxide exhibited higher graphene's $\mu_c$ and smaller $V_{NP}$.

Chapter 3

# Encapsulation of graphene devices

In chapter 2, we explained the standard process flow used to fabricate graphene-based devices and we presented results of electrical measurements performed on graphene TLM structures. In this chapter, we explain the reasons why graphene devices are sensitive to external factors, such as ambient air and roughness of the underlying substrate, and how an encapsulation layer helps protecting the graphene layer. Afterwards, we detail the steps of the process flow used to fabricate graphene devices with an encapsulating material. We present electrical data extracted from TLM measurements on passivated graphene field-effect transistors (FET) in order to identify the optimal material and process flow to use for passivation. In the end, we use $Al_2O_3$ to passivate graphene electro-absorption modulators (EAM). We show results from DC and high-speed measurements obtained on these devices and compare them with results on unpassivated EAMs. Some of the experiments in this chapter were carried out with advice from, or together with, Inge Asselberghs and Xiangyu Wu.

Part of the results contained in this chapter have been presented and published as abstract in Alessandri et al. *Graphene Week* (2019) [137].

## 3.1 Intrinsic doping and gate hysteresis in graphene devices

Graphene-based devices show high sensitivity to environmental factors (e.g. ambient air), to organic solvents and lithography resists used for fabrication and to the surface chemistry and roughness of the underlying $SiO_2$. Adsorbates

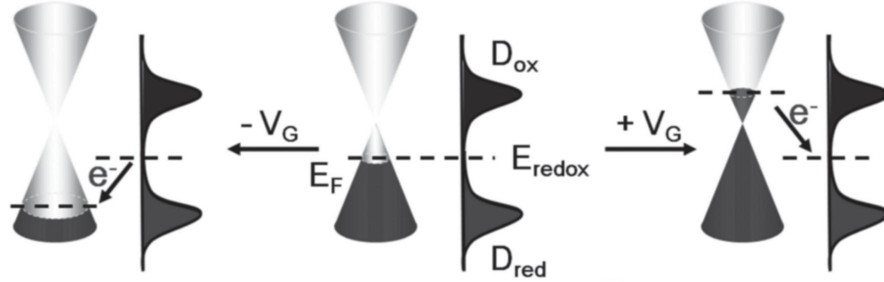
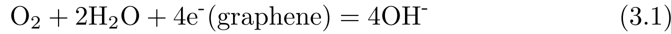



**Figure 3.1:** Schematic illustration of the charge-transfer process between the redox couple and graphene under different gate voltages. Taken from [25].

on the graphene surface cause unintentional p-type doping, while adsorbates at the graphene/$SiO_2$ interface affect the mobility and the performance of graphene devices [78, 138–140]. In particular, $H_2O$ and $O_2$ molecules at the interface between graphene and $SiO_2$ introduce trap states that cause hysteretic behaviour. Electrons are transferred spontaneously from graphene to $H_2O/O_2$ redox couples through the following electrochemical redox reaction [25]:



$$O_2 + 2H_2O + 4e^{-}(\text{graphene}) = 4OH^{-} \tag{3.1}$$

The electrochemical potential of the redox couple in atmospheric conditions is -5.3 eV. The Fermi level of graphene, which is -4.6 eV, lies therefore above the electrochemical potential of the $H_2O/O_2$ redox couple, providing a potential difference that allows transfer of electrons from the Fermi level of graphene to the unoccupied states of the redox couple, as illustrated in Fig. 3.1.

A way to improve the stability of graphene devices is the encapsulation of graphene using a protective layer. A high-k dielectric medium is expected to screen the charged impurities located at the graphene/$SiO_2$ interface [141, 142] and, if deposited at the beginning of the fabrication flow, it can protect graphene from contacting organic solvents and lithography resists during processing. Different experimental studies on the effect of a passivation layer on graphene field-effect-transistors (FETs) have been reported and are summarised in Table 3.1. The work presented in [143] is of particular interest because it compares hysteresis, graphene mobility and graphene doping on graphene FETs fabricated without passivation, passivated with aluminum oxide ($Al_2O_3$) directly grown on graphene and passivated with $Al_2O_3$ grown on an Al seeding layer. In all cases, the $Al_2O_3$ is grown by atomic layer deposition (ALD). Devices fabricated without passivation layer show heavy p-type doping and hysteresis, attributed to molecular doping from $O_2/H_2O$ redox couples at the graphene/$SiO_2$ interface and to photoresist. When the graphene FETs are passivated with $Al_2O_3$ directly grown on graphene, the p-type doping on graphene is reduced, but a large hysteresis is still present due to trap states at the inter-

**Table 3.1:** Summary of main passivation experiments published in literature.

| Ref. | Seeding layer | Dielectric | Thickness (nm) | Mobility ($cm^2/Vs$) | Hysteresis | Graphene doping |
|---|---|---|---|---|---|---|
| [143] | - | - | - | 1400 | Yes | *p* |
| [143] | - | $Al_2O_3$ | 90 | 1500 | Yes | Slightly *p* |
| [143] | Al | $Al_2O_3$ | 90 | 1000-2700 | No | Neutral |
| [144] | - | $SiO_2$ | 10 | 2000 | - | *n* |
| [144] | - | SiN | 10 | 4000 | - | *n* |
| [145] | Al | $Al_2O_3$ | 20 | - | - | - |
| [146] | Al | $Al_2O_3$ | 15 | 8000 | - | Neutral |
| [147] | Ti | $Al_2O_3$ | 0.6 | 10000 | - | - |
| [147] | Al | $Al_2O_3$ | 1.2 | - | - | - |

face with the top dielectric. When $Al_2O_3$ is directly grown on graphene at the end of the process flow, photoresist residues, grain boundaries, wrinkles and defects on the graphene layer act as nucleation centers, however there is no control over their density or uniformity, as they are unintentional. As a consequence, the passivation layer does not grow uniformly and the results cannot be reproduced from sample to sample. This issue can be solved by assisting the $Al_2O_3$ growth with an aluminum seeding layer before the ALD process. The Al seeding layer oxidises quickly when exposed to ambient after deposition and acts as a uniform nucleation layer for $Al_2O_3$. Graphene FETs passivated with the aid of the Al seeding layer show no hysteresis and no graphene doping, indicating high quality of the passivation layer.

Following the example set by the existing literature work, in the remainder of this chapter we show experiments aimed at studying the effect of different fabrication flows and different passivation layers on the performance of graphene FETs. In particular, there are two main areas where passivation can help. First, protection during the fabrication flow, to avoid exposure to solvents and polymers. Second, long-term protection from ambient to achieve stability over time. This chapter mainly focuses on the first area, while already demonstrating short-term stability ($\sim$ 2 months) in device performance. In Section 3.2, we explain the two fabrication flows used to process passivated graphene devices. Following the passivation-last flow, we fabricate samples with three different encapsulating materials: hydrogen silsesquioxane (HSQ), spin-on glass (SOG) and $Al_2O_3$. The goal is to identify a passivation layer that allows to preserve p-doping in graphene, which is important for SLG EAMs, as explained later in chapter 4. In addition, we look at stability over time of graphene's characteristics, such as carrier mobility, position of neutrality point and device hysteresis. After identifying in Section 3.3 $Al_2O_3$ as the best passivation layer among the three, we proceed in Section 3.4 with the fabrication of a sample

with a passivation-first flow where the $Al_2O_3$ is deposited with the assistance of a Si seeding layer. Finally, in Section 3.5, we test the passivation-first approach on single-layer graphene-Si electro-absorption modulators (EAM), using a (Si)/$Al_2O_3$ encapsulation layer.

## 3.2 Graphene device fabrication with a passivation layer

### 3.2.1 Comparison of passivation methods

If not protected, graphene-based devices come in contact with different organic solvents and lithography resists during the fabrication process, in addition to constantly being exposed to ambient conditions. As explained in the previous section, adsorbates on the graphene surface and ambient exposure may affect the device performance. Even though extreme importance is given to keeping the samples clean from any form of contamination, as pointed out in chapter 2, retaining graphene pristine till the end of the processing flow and for the period of time needed for measurements is a challenge.

One solution to this problem is given by the deposition of a dielectric material on top of graphene to passivate and stabilise the device. Two approaches can be used to passivate graphene: passivation-last and passivation-first. As the name suggests, the passivation-last approach consists on depositing a dielectric material on the sample as last processing step, after the fabrication of the graphene devices is completed. This allows to encapsulate graphene and protect it from degradation caused by exposure to the environment over time. However, with this solution, graphene still comes in contact with polymers and solvents during the fabrication process. These contaminants are hard to remove completely, as a consequence they remain trapped between the graphene layer and the dielectric. The second approach consists of covering graphene with a dielectric at the beginning of the fabrication flow. The advantage of this method is that graphene is protected from early on in the fabrication process, reducing the amount of residues and therefore obtaining a cleaner interface between graphene and the dielectric. The disadvantage is a more complex process flow, which is more difficult to optimise successfully due to additional fabrication steps.

### 3.2.2 Passivation-last process flow

In the passivation-last approach, samples are fabricated following the standard flow explained in chapter 2 and, at the very end of the flow, the passivation layer is deposited or spin-coated on top of the samples. Fig. 3.2 shows the schematic cross section of a graphene FET at the end of such processing. The device is entirely covered by the passivation layer and, in order to perform measurements, the probes have to scratch through this layer to come in contact with the metal.

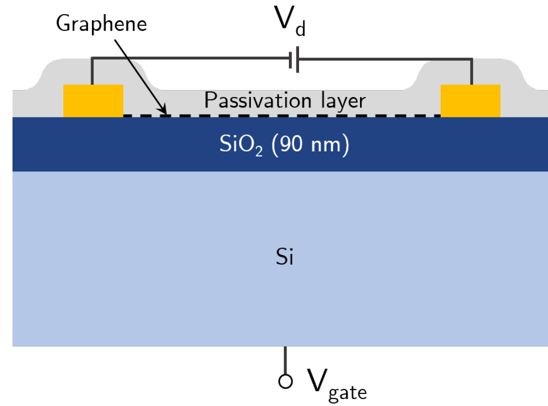



**Figure 3.2:** Schematic cross section of a graphene FET passivated using the passivation-last approach.

### 3.2.3 Passivation-first process flow

The passivation-first process flow is structured as follows:

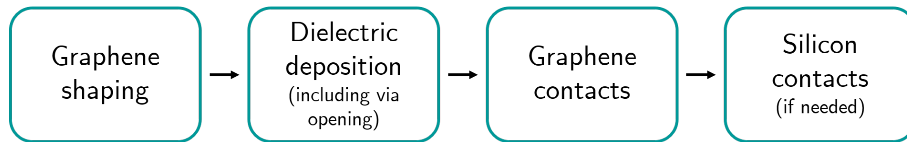



Fig. 3.3 shows as an example the steps to fabricate a SLG EAM with a passivation-first process flow. The dielectric of choice, selected based on the type and purpose of the experiment, is deposited on the sample right after the graphene shaping step. There are two reasons behind the choice of depositing the dielectric after, and not before, the graphene shaping step. First, it removes the need to etch the dielectric to shape the graphene underneath. Second, the dielectric coverage is extended to the whole sample and not only to the graphene shapes. This helps preventing intercalation of solvents at the interface between graphene and $SiO_2$ during processing. The disadvantage is that graphene is still exposed to solvents during the shaping step.

When working with a passivation layer, the first challenge is to achieve a homogeneous growth of high-$\kappa$ dielectrics directly on graphene by atomic layer deposition (ALD), as discussed in Section 3.1. To address this challenge, a growth recipe was developed that foresees the deposition of a thin Si seeding layer on the sample before ALD growth to provide intentional nucleation sites. The 0.5 nm-thick Si layer is evaporated on the sample and afterwards kept in air for 10 min to ensure oxidation. Afterwards, a layer of dielectric is deposited by ALD. $Al_2O_3$ is deposited from trimethyl aluminum (TMA) and water (H2O),

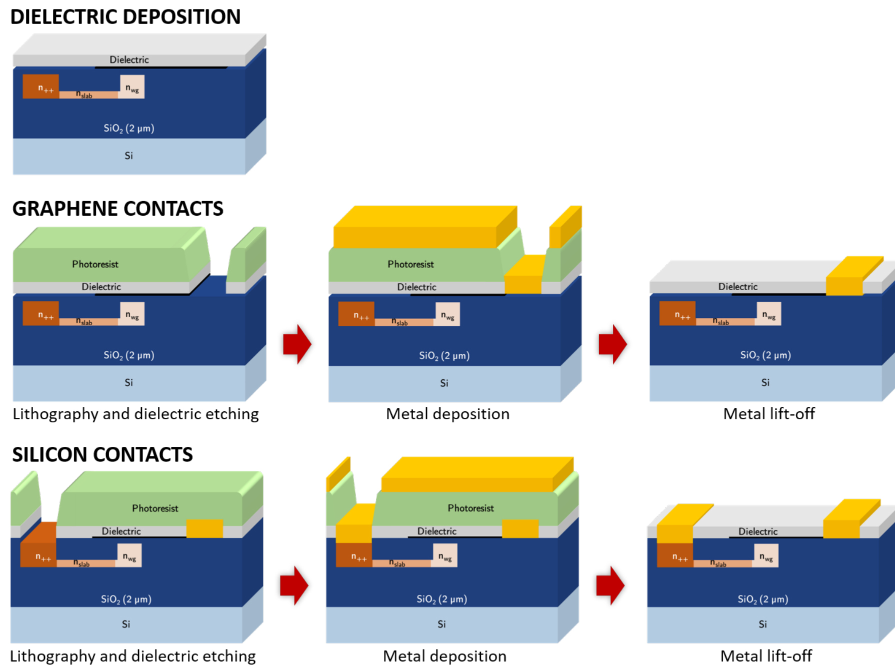
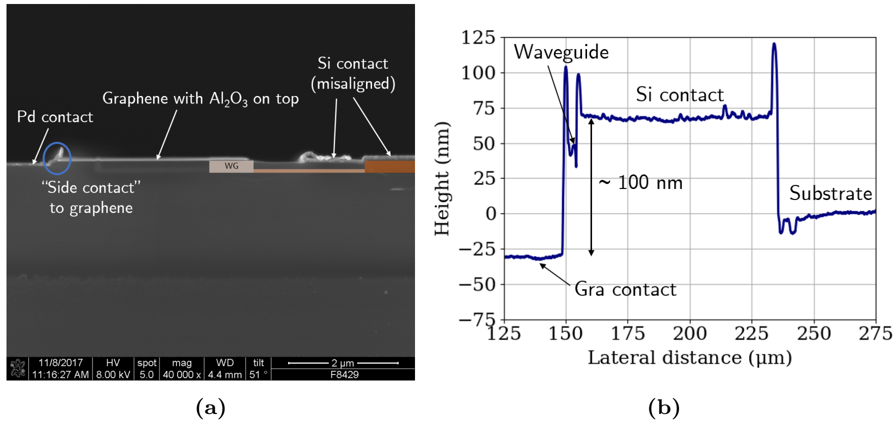



**Figure 3.3:** Steps to fabricate a graphene EAM with a passivation-first process flow. First, lithography for graphene shaping is performed, then the dielectric layer is deposited on the sample. For graphene contacts, a dry etching step is performed before evaporating the metal layer in order to open a via in the dielectric to contact the graphene. For silicon contacts, the dielectric is wet etched together with the thermal $SiO_2$.

using nitrogen (N2) as carrier gas. In the case of $HfO_2$, TMA is substituted with hafnium chloride ($HfCl_4$).

After dielectric deposition, metal contacts to graphene are fabricated. When the lithography for graphene contacts is done, before the metal is evaporated on the sample, the dielectric material needs to be etched in order to open a via that allows to contact graphene. In case the material chosen for the passivation layer is an oxide, such as $Al_2O_3$ or $HfO_2$, the vias are opened through a dry etching process. During the etching step, graphene is also removed from the contact area, therefore an edge contact between graphene and the metal is created. In case of an edge contact, the graphene side is exposed and the metal comes in contact with the edge instead of the top surface of graphene. In an edge contact, graphene's $\sigma$ orbitals contribute to the bond with the metal, unlike in a top contact where the bond is created only with graphene's $\pi$ orbitals [148]. The choice of dry etching is dictated by the need to use a selective recipe that removes only the dielectric used for passivation without attacking the $SiO_2$ right




**(a)** **(b)**

**Figure 3.4:** (a) Cross-sectional SEM image of a graphene EAM fabricated with a passivation-first process flow. On the left side, the metal contact creates a side contact to graphene. However, the oxide below the metal is significantly over-etched, causing the metal to be lower than the graphene layer. On the right side, the metal contact to Si is visible. The metal was misaligned, which can be seen from the fact that the metal edge does not end where the high-doped Si region ends (dark orange). (b) Dektak step height measurement. The top surface of the graphene contact is ∼ 100 nm lower than expected.

below it. The use of a wet etchant such as BHF would not allow to precisely control the etching process, resulting in an unwanted removal of $SiO_2$. If the dry etching step is not successful and part of the $SiO_2$ is also removed [149], the metal will be at a lower height than intended and have no contact with graphene. This is clearly visible in the cross-sectional SEM image in Fig. 3.4a. On the left side, the metal is supposed to create a side contact to graphene. However, the oxide layer below the Pd contact is over-etched, causing the metal pad to be ∼ 100 nm lower than expected (Fig. 3.4b). Another reason to use dry etching is to avoid in-plane etching. A sideways over-etching of graphene would result in no contact with the metal, since the same resist pattern is used for etching and for metal lithography. The recipe we used is based on reactive ion etching (RIE). In RIE, reactant gases are excited to ions, which hit the substrate of the surface perpendiculary when a strong electric field and low pressure are applied. To etch $Al_2O_3$ we used a pressure of 5 mT, 450 W inductively coupled plasma (ICP) power, 100 V bias and a gas mix of 50% $BCl_3$ and 50% He. The recipe we used to etch $HfO_2$ is also $BCl_3$-based. These recipes allowed to successfully fabricate the devices used for the experiments described later in Sections 3.4 and 3.5. However, they did not always deliver successful results, as shown in Fig. 3.4a, therefore a more precise control of the etch rate and etch depth is necessary in the future if this fabrication flow is to be used to process more samples.

The silicon contacts step does not undergo any major change compared to

the standard flow described in chapter 2, as a wet etching step with BHF was already included to remove the thermal $SiO_2$ on top of the Si. BHF can also be used to etch $Al_2O_3$ or $HfO_2$ and the etching time is simply increased to remove the extra dielectric thickness.

## 3.3 Passivation-last on graphene FETs

### 3.3.1 Sample design and characterisation technique

Using the passivation-last approach, we fabricated three samples to test the effect of different passivation layers on graphene's properties. The samples used for this experiment are based on a Si/$SiO_2$ substrate (Fig. 3.2). The flow used to fabricate them is described in appendix A, section A.1.1. The graphene layer was grown and transferred in-house. These samples are designed to fit as many TLM structures as possible in order to gather statistics and are measured with automatic probing. We tested three different materials: HSQ, SOG and $Al_2O_3$. After performing a mild annealing at 150°C in $N_2$, HSQ and SOG are spin-coated on the samples, while $Al_2O_3$ is grown by ALD without the aid of a seeding layer. The graphene FETs were back-gated through the 90 nm $SiO_2$. We performed a double sweep measurement, where the voltage is first swept from -35 V to 35 V and then back to -35 V. This is done to study the hysteretic behaviour of the device caused by charged traps. The relevant quantities, such as $\mu_c$, $R_{graC}$ and $V_{NP}$, were extracted using the methods explained in chapter 1. To quantify the device hysteresis, we calculate the variation of the position of graphene's charge neutrality point between the backward and forward sweeps as $\Delta V_{NP} = V_{NP,bwd} - V_{NP,fwd}$. Three measurements were performed on each sample. The first one was carried out right after the deposition of the passivation layer. The same measurement was then repeated in two later moments in time. This approach allows to monitor the aging of the sample and whether graphene's properties, such as mobility and doping, are stable over time.

### 3.3.2 Results

Cumulative distribution function (CDF) plots are generated for each type of passivation layer in order to visualize the distribution of $\mu_c$ and $V_{NP}$ values from up to 36 TLM structures across each sample (Fig. 3.5). Table 3.2 reports the median values of $\mu_c$, $R_c$, $V_{NP}$ and $\Delta V_{NP}$ for the three samples measured over a period up to four weeks. The mobility was extracted at $n_s = 8.6e12\ \mathrm{cm}^{-2}$, while the contact resistance was extracted at the neutrality point. No significant difference in mobility values across the three samples is present within the standard deviation (± 500 cm$^2$/Vs). In addition, $\mu_c$ remains stable over time for all three samples, indicating no apparent degradation of graphene quality. The $Al_2O_3$ sample shows an average mobility of 2790 cm$^2$/Vs at t=0, almost double the value reported in literature for a graphene FET fabricated with an equivalent passivation-last process flow [143]. However, if we look at the CDF

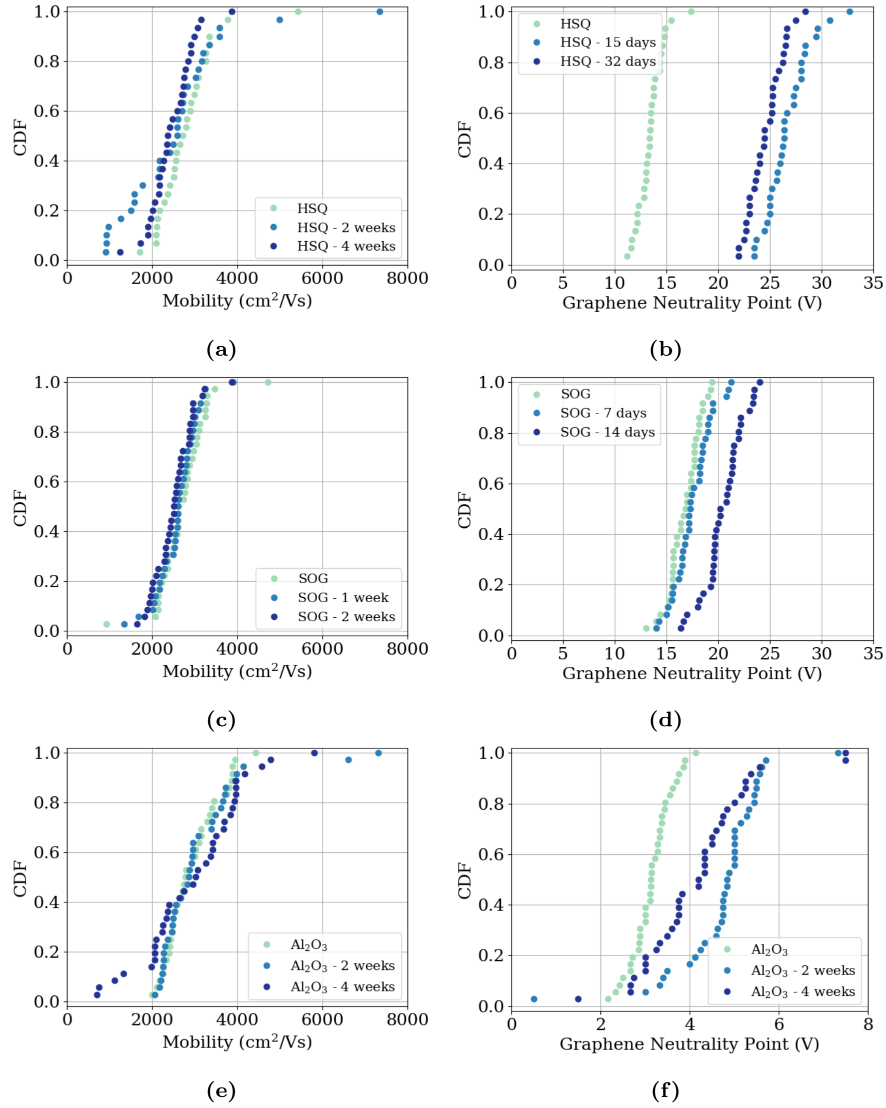



**Figure 3.5:** Cumulative distribution function (CDF) plot showing the empirical cumulative distribution of the mobility $\mu_c$ and of the position of graphene's neutrality point $V_{NP}$ over time for samples passivated with the passivation-last approach using (a, b) HSQ, (c, d) SOG and (e, f) $Al_2O_3$.

plots (left column of Fig. 3.5), we can see that the mobility is characterised by a significant spread across the measured devices. The $Al_2O_3$ sample shows the biggest spread among the three samples, with a difference of 1600 $cm^2/Vs$ between 10 and 90 percentiles for the measurement at t = 0. HSQ shows a

**Table 3.2:** Median values of mobility ($\mu_c$), contact resistance ($R_c$), position of graphene's neutrality point ($V_{NP}$) and hysteresis ($\Delta V_{NP}$) extracted from TLM measurements on the three samples passivated with passivation-last approach.

| | **HSQ** | | | **SOG** | | | **$Al_2O_3$** | | |
|---|---|---|---|---|---|---|---|---|---|
| | t = 0 | t = 2 weeks | t = 4 weeks | t = 0 | t = 1 week | t = 2 weeks | t = 0 | t = 2 weeks | t = 4 weeks |
| $\mu_c$ ($cm^2$/Vs) | 2760 | 2590 | 2390 | 2680 | 2620 | 2520 | 2790 | 2860 | 3050 |
| $R_c$ (Ω µm) | 320 | 350 | 400 | 290 | 330 | 290 | 360 | 270 | 260 |
| $V_{NP}$ (V) | 13.4 | 26.4 | 24.5 | 16.9 | 17.3 | 20.4 | 3.1 | 4.9 | 4.3 |
| $\Delta V_{NP}$ (V) | 7.6 | 4.5 | 4.5 | 9.9 | 9.1 | 8.0 | 3.0 | 6.7 | 8.8 |

smaller spread, with 1260 $cm^2$/Vs, and SOG exhibits the smallest spread of 1120 $cm^2$/Vs. This variation across the sample can be attributed to a lack of uniformity in the deposited passivation layer, especially for $Al_2O_3$. Similarly to the mobility, also graphene's contact resistance is stable over time within the standard deviation (± 90 Ω µm). The first signs of ambient effects can be noticed analysing the variation in position of graphene's neutrality point. $V_{NP}$ shifts of ∼ 11 V in only two weeks time on the HSQ sample. The SOG sample is more stable, with a shift of ∼ 4 V after two weeks, but the best result is achieved with $Al_2O_3$, with a shift of only ∼ 1 V after four weeks. This can also be visualised in the CDF plots in the right column of Fig. 3.5. The $Al_2O_3$ sample shows the maximum hysteresis degradation, with a difference of almost 6 V between the first and the last measurement after 4 weeks, followed by the HSQ sample with a hysteresis degradation of ∼ 3 V, and the SOG sample with ∼ 2 V.

### 3.3.3 Conclusions

In conclusion, all three materials show advantages and disadvantages. The sample passivated with $Al_2O_3$ draws more interest in the context of finding a solution which can be used in the future for wafer-scale fabrication. $Al_2O_3$ shows stable mobility and contact resistance and a small shift of the position of graphene's neutrality point over four-weeks time. However, improvements in the quality and uniformity of the encapsulation layer are necessary to achieve a smaller mobility spread across the sample and to reduce the hysteresis degradation over time. Fabricating passivated graphene devices with the passivation-first approach assisting the deposition of $Al_2O_3$ with a seeding layer is expected to help in this regard.

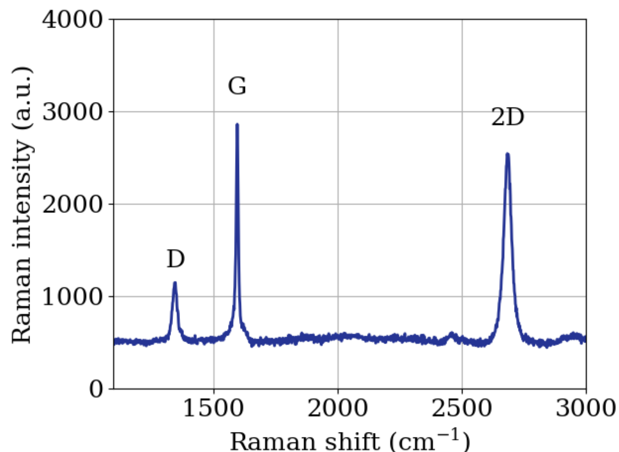



**Figure 3.6:** Raman spectrum of the CVD graphene used for the passivation-first experiment.

## 3.4 Passivation-first with seeding layer on graphene FETs

### 3.4.1 Sample design and characterisation technique

In order to obtain a higher quality passivation layer, we proceeded with the fabrication of a sample using the passivation-first approach introduced in Section 3.2. The sample is based on a Si/$SiO_2$ substrate and, as before, it is designed to fit a large number of TLM structures. The graphene layer was grown and transferred in-house. For the deposition of the passivation layer, we first evaporate 0.5 nm of Si as seeding layer by e-gun evaporation, and then deposit 10 nm of $Al_2O_3$ as capping layer by atomic layer deposition (ALD). As explained at the beginning of this chapter, the deposition of a thin seeding layer on top of graphene before $Al_2O_3$ deposition helps achieving better dielectric uniformity and therefore better encapsulation. Because the passivation layer is deposited at the beginning of the fabrication flow, it also protects graphene from contacting organic solvents and lithography resists during processing. In addition, depositing the dielectric after, and not before, graphene patterning allows to obtain full sample coverage and reduce intercalation of solvents between graphene and $SiO_2$ during processing. The flow used to fabricate these samples is described in detail in appendix A, section A.1.2.

Graphene's quality was assessed by Raman spectroscopy. The sample was then characterised by back-gating the graphene FETs through the 90 nm-thick $SiO_2$. We performed a double sweep measurement, where the voltage is first swept from -35 V to 35 V and then back to -35 V. This is done to study the hysteretic behaviour of the device caused by charged traps. The relevant

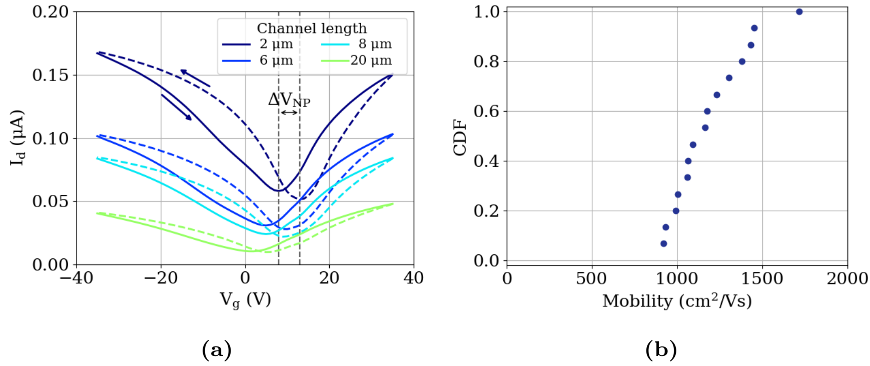



**Figure 3.7:** (a) Example of $I_D$-$V_G$ measurement on four devices with varying channel length, showing p-doped graphene and a small hysteresis of $\Delta V_{NP} = 4$ V. (b) Cumulative distribution function (CDF) plot showing the empirical cumulative distribution of the mobility $\mu_c$ for the sample passivated with $Al_2O_3$ using the passivation-first approach.

quantities, such as $\mu_c$, $R_{graC}$ and $V_{NP}$, were extracted using the methods explained in chapter 1. To quantify the device hysteresis, we calculate the variation of the position of graphene's charge neutrality point between the backward and forward sweeps as $\Delta V_{NP} = V_{NP,bwd} - V_{NP,fwd}$.

### 3.4.2 Results

The Raman spectrum of the CVD graphene on this sample after procressing is shown in Fig. 3.6. The appearance of the D-peak denotes the presence of defects in the carbon lattice. The 2D-peak is a clear sharp peak characteristic of monolayer graphene, with full width at half maximum ($FWHM_{2D}$) of 29.7 $cm^{-1}$ and positioned at 2683 $cm^{-1}$ [93]. The $I_D/I_G$ ratio is 0.4 and the $I_{2D}/I_G$ ratio is 1.0, indicating low layer quality.

Fig. 3.7a shows the measured $I_d - V_g$ curve on four devices with channel lengths ranging from 2 to 20 µm. Graphene's p-doping is preserved on this sample ($V_{NP} = 5$ V) and only a small hysteresis ($\Delta V_{NP} = 4$ V) is present. The contact resistance extracted from the $I_d - V_g$ measurements is 250 Ω µm, comparable with the one obtained with the passivation-last approach. The mobility values show more uniformity compared to the $Al_2O_3$ samples fabricated with the passivation-last approach (Fig. 3.7b). The difference between the 10 and 90 percentiles is reduced to 490 $cm^2/Vs$, indicating a better uniformity of the deposited dielectric. The median value of mobility is, however, only 1165 $cm^2/Vs$, confirming the low layer quality detected through Raman spectroscopy. This value of mobility is also lower than those reported in literature for graphene passivated with $Al/Al_2O_3$, which range between 1500 $cm^2/Vs$ [143] and 8000 $cm^2/Vs$ [146].

### 3.4.3 Conclusions

Due to the nature of passivation-first processing, results (such as the mobility) cannot be compared with the ones extracted by measuring the same sample before dielectric deposition. It is therefore difficult to conclude whether the low value of mobility is caused by the type of deposition used for the passivation layer or it is intrinsic to the graphene layer transferred on this specific sample. In either case, it would be beneficial in the future to perform a set of experiments to assess how different deposition parameters affect graphene's properties. A comparison of the effect on graphene's properties of different seeding layers would also be interesting to carry out. In addition, it is important to have good control over the interface between graphene and the passivation layer. For this purpose, different cleaning recipes should be investigated, such as forming gas (FOG) annealing or $H_2$ plasma cleaning [150–153].

In conclusion, the results of this experiment indicate that passivation-first does not yet yield better results compared to the passivation-last approach. However, our primary purpose is to develop and use a passivation approach which is up-scalable and could be transferred to a fab environment. In such case, graphene would be covered by an oxide layer right after graphene shaping and a passivation-last approach would not be possible. For this reason, we choose to continue working with the passivation-first process flow and to test it on graphene electro-absorption modulators.

## 3.5 Passivation-first on graphene EAMs

### 3.5.1 Sample design and characterisation technique

Similarly to graphene FETs, single-layer graphene electro-absorption modulators (SLG EAMs) also show hysteresis effects. To test whether a passivation layer helps reducing hysteretic behaviour and improving stability over time, we fabricated and compared unpassivated and passivated SLG EAMs. For this experiment, we used a n-doped Si with waveguide doping $n_{wg}$ = 2.3e18 cm$^{-3}$ and slab doping $n_{slab}$ = 2.7e19 cm$^{-3}$. The passivated SLG EAMs were fabricated using passivation-first processing with 0.5 nm Si seeding layer and 10 nm $Al_2O_3$. The details of the flow used to fabricate these samples are described in appendix A, section A.2.2. The graphene layer was grown and transferred by the commercial vendor *Graphenea*.

First, we performed double sweep electro-optical measurements at 1560 nm wavelength on an unpassivated 25 µm-long SLG EAM, sweeping the voltage bias from -4 V to 4 V, and then from 4 V back to -4 V. We then performed the same measurement on a 25 µm-long SLG EAM fabricated on the passivated sample. The same measurement was repeated after two months to assess the stability of the encapsulation layer over time. The focus of the comparison is placed on graphene's doping and on the hysteretic effect. The latter is quantified by calculating the difference in transmission between backward and

forward sweep at 0 V. We completed the comparison by measuring the electro-optical $S_{21}$ frequency response of the same 25 µm-long passivated SLG EAM between 100 MHz and 30 GHz at DC bias ranging from -1 V to 1 V with a vector network analyser, using -8 dBm RF power and a 50 Ω-load resistor. Two measurements were performed with a time distance of five months between each other.

### 3.5.2 Results

The double-sweep electro-optical measurement performed on the unpassivated SLG EAM is shown in Fig. 3.8a. The hysteretic behaviour is very pronounced, with a difference in transmission at 0 V between the forward and backward voltage sweep of $\Delta T = 0.35$ dB. This behaviour is not present on the passivated EAM, where $\Delta T$ is only 0.02 dB (Fig. 3.8b). The same measurement repeated on the passivated EAM after two-months time shows no significant degradation in the response of the device, with $\Delta T = 0.16$ dB (Fig. 3.8c). These results show that the $Al_2O_3$ passivation layer suppresses the hysteretic electro-optical response, while at the same time preserving the p-doping characteristic of unpassivated graphene.

The $S_{21}$ frequency response of the passivated SLG EAM is shown in Fig. 3.9 at 0 V DC bias and 1560 nm wavelength. The two measurements, performed five months apart from each other, show good agreement. The extracted 3 dB bandwidths, i.e. the frequency at which the signal amplitude reduces by 3 dB, are $9.4 \pm 0.3$ GHz and $8.9 \pm 0.3$ GHz for $t = 0$ and $t = 5$ months, respectively, demonstrating excellent performance stability over time. The extra noise in the measurement performed at $t = 5$ months is due to a slightly worse calibration of the setup.

Two parameters could be optimised to further improve stability over time. The first is the thickness of the $Al_2O_3$, as it has been shown to affect the performance stability of graphene field-effect devices [143]. A thick $SiO_2$ layer ($\sim$ 1 µm) could be deposited on top of the $Al_2O_3$ to further increase the thickness of the dielectric stack. The second parameter is the type of seeding layer used for $Al_2O_3$ deposition, because it has a significant impact on the dielectric constant ($\kappa$) and morphology of ALD $Al_2O_3$ [147]. A higher $\kappa$ would also allow to achieve a better mobility retention in graphene [144], leading to lower graphene resistance and to higher ER.

## 3.6 Conclusions

In this chapter, we presented and compared two process flows used to fabricate graphene devices with a protective passivation layer. The first, the passivation-last flow, relies on the fabrication steps of the standard flow explained in chapter 2, with the addition of the deposition of a dielectric layer at the end. The second, the passivation-first flow, is used to process devices where graphene

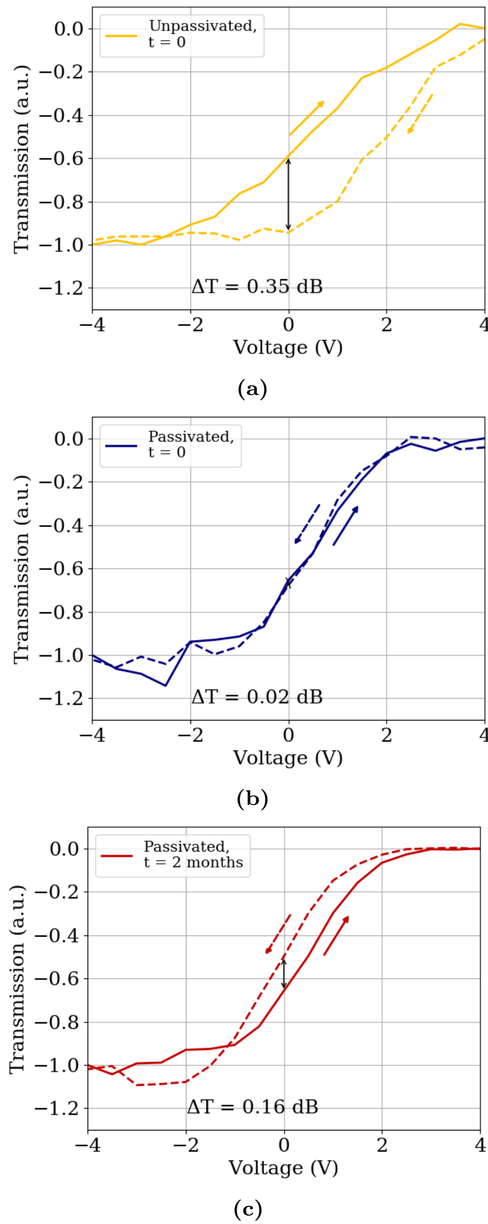



**Figure 3.8:** Comparison of transmission curves, measured with a double voltage sweep right after fabrication, between an unpassivated (a) and a passivated (b) 25 µm-long graphene EAMs. The same measurement is repeated on the passivated EAM after 2 months time (c).

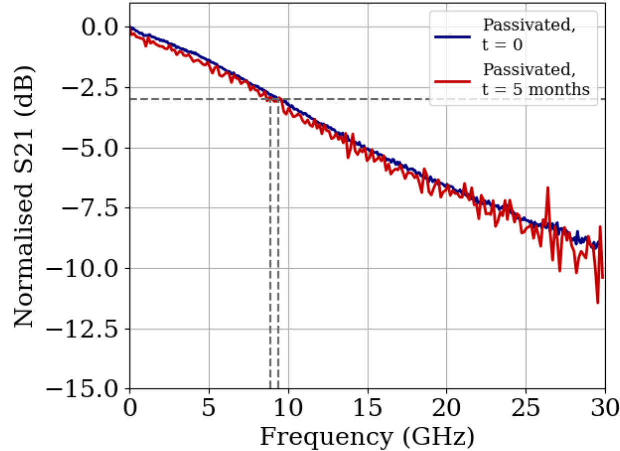



**Figure 3.9:** $S_{21}$ parameters measured on the passivated 25 µm-long SLG EAM at 0 V DC bias and 1560 nm wavelength. The two measurements are performed five months apart.

is protected from early on in the fabrication process by a passivation layer. This flow allows to reduce the amount of residues on graphene, which affect the performance of these devices. The passivation-first process flow presented some difficulties, related to the deposition of a uniform dielectric layer on top of graphene and the etching of such dielectric to fabricate graphene contacts. The former was addressed with the aid of a Si seeding layer to act as nucleation layer, and the latter by using a dry etching recipe which allows to etch the passivating dielectric without removing the $SiO_2$ below.

In the second part of the chapter, we compared electrical data extracted from TLM measurements on graphene FETs fabricated with the passivation-last approach. We identified $Al_2O_3$ as the passivating material that allows to reduce hysteretic behaviour, while also preserving graphene's p-doping. Motivated by the need to obtain more uniform performance across the sample, we tested the passivation-first approach using a Si seeding layer and 10 nm $Al_2O_3$ on graphene FETs. Even though in terms of electrical performance the passivation-first approach did not yield better results compared to passivation-last, we decided to proceed with the fabrication of SLG EAMs using this process flow. Passivation-first is the only passivation method compatible with processing in a fab environment and therefore it meets our goal to work with up-scalable fabrication flows. On SLG EAMs fabricated with the passivation-first approach we obtained improved stability in the device DC and high-speed performance over time and reduced hysteresis compared to unpassivated SLG EAMs.

# Chapter 4

# Single-layer graphene electro-absorption modulators

In this chapter, we dig deeper into graphene-based electro-absorption modulators (EAM). We present a theoretical model that describes the working mechanisms of single-layer graphene (SLG) EAMs, and we use this model to identify the optimal characteristics to maximise DC and high-speed performance. These theoretical findings are compared with extensive experimental results, measured on samples with different design and processing characteristics. Finally, we incorporate the SLG EAMs into wavelength-division multiplexer (WDM) transmitters to demonstrate up-scalability of graphene processing and the integration of graphene devices with functional silicon photonics circuits.

Part of the text and results contained in this chapter have been published in Alessandri et al. *Jpn. J. Appl. Phys.* **59**(5) 052008 (2020) [154] and in Alessandri et al. *Appl. Opt.* **59**(4) 1156-1162 (2020) [155].

Part of the results have also been presented and published as conference proceedings or abstract in Alessandri et al. *SSDM* **(invited)** (2020) [156], Alessandri et al. *OFC* Th2A.7 (2019) [157], Alessandri et al. *ECOC* We4C.2 (2018) [110], Alessandri et al. *CLEO Pac. Rim* Th4G.3 (2018) [109] and Alessandri et al. *Graphene Week* (2017) [158].

## 4.1 Modeling of graphene EAMs

What sets graphene apart from other optical materials is its bidimensional nature. The interaction between the light traveling through a waveguide and a graphene layer is modelled using a numerical simulation of the electromagnetic

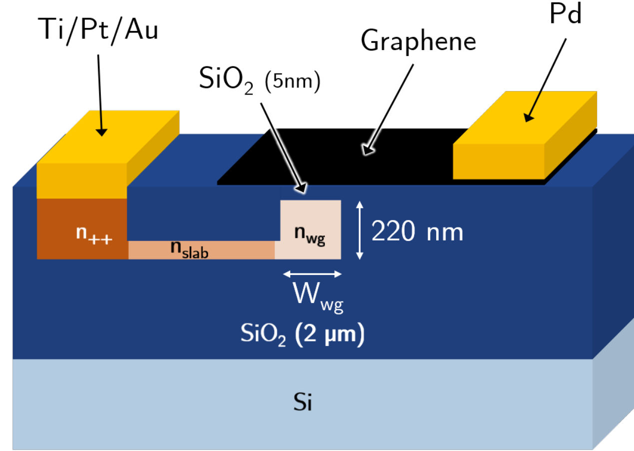



**Figure 4.1:** Schematic cross section of a SLG EAM. The three doped silicon regions are either p- or n-doped: waveguide ($n_{wg}/p_{wg}$), slab ($n_{slab}/p_{slab}$) and contact ($n_{++}/p_{++}$). The graphene, oxide and silicon layers form a GOS capacitor.

field. In the case of graphene, only the in-plane components of the electromagnetic field play a role. Because graphene's thickness is as small as one atom, it is usually characterised with a surface conductivity model rather than a bulk permittivity one. To perform simulations of optical modes in waveguides with graphene we have used Lumerical MODE solutions, which includes the surface conductivity model in the material database.

Fig. 4.1 shows the cross section of a single-layer graphene electro-absorption modulator. The silicon-oxide-graphene configuration will be used throughout the chapter for simulations and experiments.

### 4.1.1 Surface conductivity method

The 2D complex optical conductivity is calculated using the Kubo formula [83], which takes into account interband (from conduction band to the valence band or viceversa) and intraband (to an upperstate in the same band as the original state) transitions, and is given by

$$\sigma(\omega, \Gamma, \mu, T) = \sigma_{intra}(\omega, \Gamma, \mu, T) + \sigma_{inter}(\omega, \Gamma, \mu, T) \tag{4.1}$$

where $\omega$ is the angular frequency, $\hbar\Gamma$ is graphene's charged particle scattering rate, $T$ is the temperature and $\mu$ is graphene's Fermi level. The intraband term $\sigma_{intra}(\omega, \Gamma, \mu, T)$ and the interband term $\sigma_{inter}(\omega, \Gamma, \mu, T)$ are given by

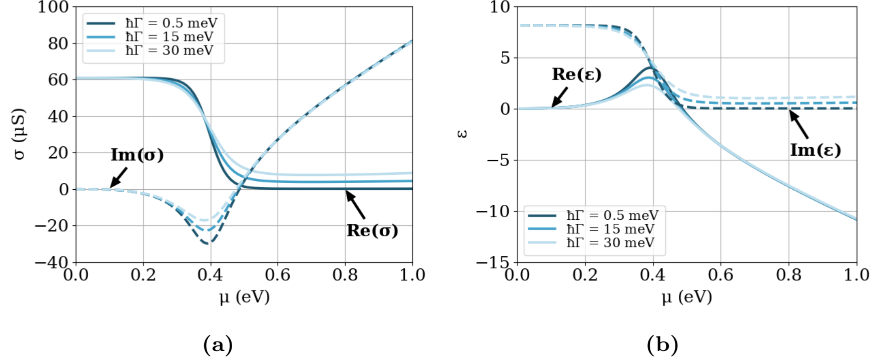



**Figure 4.2:** Real and imaginary part of (a) graphene surface conductivity $\sigma$ and (b) dielectric constant $\epsilon$ as a function of graphene chemical potential $\mu$ at 1560 nm wavelength, for scattering rate values of 0.5, 15 and 30 meV.

$$\sigma_{intra}(\omega, \Gamma, \mu, T) = \frac{iq^2}{\pi\hbar^2(\omega + i2\Gamma)} \int_0^\infty \xi \left( \frac{\partial f_d(\xi)}{\partial \xi} - \frac{\partial f_d(-\xi)}{\partial \xi} \right) \mathrm{d}\xi \tag{4.2}$$

$$\sigma_{inter}(\omega, \Gamma, \mu, T) = \frac{iq^2(\omega + i2\Gamma)}{\pi\hbar^2} \int_0^\infty \frac{f_d(-\xi) - f_d(\xi)}{(\omega + i2\Gamma)^2 - 4(\xi/\hbar)^2} \mathrm{d}\xi \tag{4.3}$$

where $q$ is the elementary charge, $\hbar$ is the reduced Planck constant and $k_B$ is Boltzmann constant, and

$$f_d(\xi) \equiv \frac{1}{\exp[(\xi - \mu)/(k_B T)] + 1} \tag{4.4}$$

is the Fermi-Dirac distribution.

Fig. 4.2a and 4.2b show the real and imaginary part of graphene's surface conductivity and dielectric constant respectively at 1560 nm wavelength, for scattering rates of 0.5, 15 and 30 meV, generated using the surface conductivity model integrated in Lumerical MODE. Graphene changes character from metallic to dielectric at $\mu = 0.515$ eV. In the range $\mu > 0.515$ eV different scattering rates lead to different values of conductivity and dielectric constant. As it will be better explained in the next section, imperfections in the graphene layer induce density inhomogeneities, causing variations in the optical conductivity.

### 4.1.2 Static electro-optical behaviour

The static electro-optical behaviour of a single-layer graphene electro-absorption modulator (SLG EAM) is defined by the relation between the absorption and graphene's Fermi level $\mu$. Graphene's absorption is derived from the 2D complex optical conductivity $\sigma(\omega, \Gamma, \mu, T)$ (Eq. 4.1). Graphene's Fermi level $\mu$ can

be shifted by sweeping the voltage $V_g$ across the graphene-oxide-silicon (GOS) capacitor [83], according to

$$V_g = \frac{q\,(n_0 + n_s)}{C_{GOS}} = \frac{q}{\pi\,(\hbar v_F)^2}\frac{\mu^2}{C_{GOS}} \tag{4.5}$$

where $v_F$ is the Fermi velocity of carriers in graphene and $C_{GOS}$ is the capacitance of the GOS capacitor. The Fermi level $\mu$ is described by the sum of two contributions:

$$\mu = \mu_0 + \Delta\mu \tag{4.6}$$

$\mu_0$ is the initial Fermi level position due to the fixed number of charges $n_0$ (graphene's intrinsic doping), and $\Delta\mu$ is the Fermi level shift caused by the number of charges $n_s$ accumulated on the graphene layer when we apply $V_g$ across the capacitor.

The static electro-optical behaviour of the SLG EAM as a function of applied voltage is mainly affected by two parameters: graphene's intrinsic doping ($n_0$) and scattering rate ($\hbar\Gamma$). The intrinsic doping $n_0$ is the unintentional doping present on the graphene layer in ambient conditions and it affects the position of minimum transmission as a function of applied voltage. Fig. 4.3a shows the simulation of the optical transmission as a function of gate voltage of a SLG EAM for TE-polarised light at 1560 nm. The $SiO_2$ thickness and waveguide width used for the simulation are 5 nm and the 500 nm respectively. Two scenarios of graphene doping are considered, $n_0 = 0$ cm$^{-2}$ (neutral graphene) and $n_0 = 12e12$ cm$^{-2}$ (p-doped graphene), and graphene's scattering rate is $\hbar\Gamma = 15$ meV. For neutral graphene, the minimum is at 0 $V$, therefore switching between high transmission (on-state) and low transmission (off-state) requires $\sim$ 3.5 V or $\sim$ -4 V DC bias. For p-doped graphene, the minimum transmission point is shifted to negative bias. In this case, switching occurs between -2 $V$ and 2 $V$, which is preferable in order to minimise the DC bias at operation. The scattering rate $\hbar\Gamma$, inversely proportional to the mobility $\mu_c$ [76], affects the extinction ratio of the modulator. As shown in Fig. 4.3b, a lower scattering rate, implying higher graphene quality, results in higher extinction ratio for a given $V_{pp}$ because graphene can reach full transparency. For example, a 75 µm-long SLG EAM would show 0.5 dB higher extinction ratio for $\hbar\Gamma$ = 0.43 meV compared to $\hbar\Gamma = 30$ meV ($\mu \sim 1000$ cm$^2$V$^{-1}$s$^{-1}$ [76]). In real applications, the scattering rate of CVD-grown graphene is often more than 10 meV [76, 159], resulting in a reduced extinction ratio and increased insertion loss.

If we repeat the same simulation assuming TM-polarised light, we immediately see that the device exhibits almost twice the absorption, due to the bigger overlap between the TM optical mode and the graphene layer compared to TE (Fig. 4.3c). For TE polarisation, the absorption is $\leqslant$ 0.05 dB/µm, while for TM polarisation it reaches almost 0.15 dB/µm.

For a more accurate estimation of the electro-optical behaviour of the SLG EAM, the effect of the charges on the refractive index of Si should also be

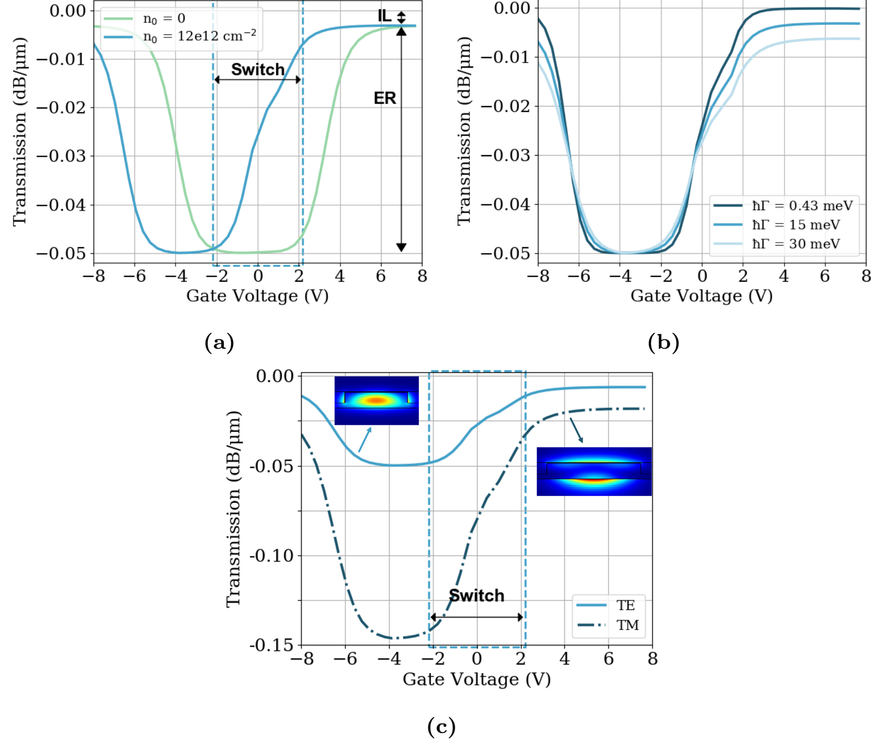



**Figure 4.3:** (a) Simulated transmission as a function of gate voltage at $\lambda = 1560$ nm of a TE ($W_{wg} = 500$ nm) SLG EAM with 5 nm oxide and $p_{wg} = 1.0e18$ cm$^{-3}$ for neutral ($n_0 = 0$ cm$^{-2}$) and p-doped ($n_0 = 12e12$ cm$^{-2}$) graphene, with graphene's scattering rate $\hbar\Gamma = 15$ meV. (b) Same as (a), but for p-doped graphene ($n_0 = 12e12$ cm$^{-2}$) and scattering rates $\hbar\Gamma = 0.43$, 15, 30 meV. (c) Comparison of transmission between a TE ($W_{wg} = 500$ nm) and TM ($W_{wg} = 750$ nm) SLG EAMs for $n_0 = 12e12$ cm$^{-2}$ and $\hbar\Gamma = 30$ meV.

taken into account. This effect dominates the device insertion loss especially when graphene is of high quality. When a voltage is applied across the GOS capacitor, charges accumulate also at the interface between the Si waveguide and the oxide and they affect the propagation constant of the optical mode through the waveguide. The effect of free carriers can be modeled through Soref's formula at $\lambda = 1550$ nm [160, 161]:

$$\begin{aligned}\Delta n\,(\lambda = 1550) &= -5.4 \cdot 10^{-22} \Delta N^{1.011} - 1.53 \cdot 10^{-18} \Delta P^{0.838} \\ \Delta\alpha\,(\lambda = 1550) &= 8.88 \cdot 10^{-21} \Delta N^{1.167} + 5.84 \cdot 10^{-20} \Delta P^{1.109}\end{aligned} \tag{4.7}$$

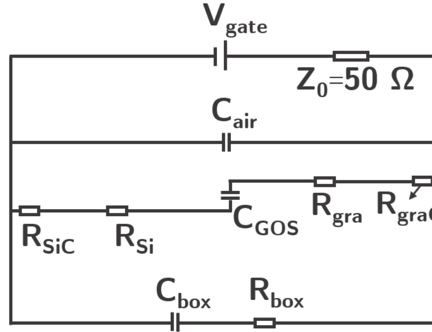



**Figure 4.4:** Equivalent electrical circuit of a single-layer graphene electro-absorption modulator.

### 4.1.3 RC limited high-speed behaviour of the SLG EAM

The 3 dB frequency response of a SLG EAM is limited by the RC constant of the device and can be simulated using the equivalent electrical circuit in Fig.4.4. The most important contributions to the total device RC are the total device resistance and the graphene-oxide-silicon (GOS) capacitance, which will be analysed separately.

#### Resistance

The device total resistance ($R_{tot}$) is the sum of graphene's contact and sheet resistance ($R_{graC}$ and $R_{gra}$) and the Si contact and sheet resistance ($R_{SiC}$ and $R_{Si}$). Graphene's resistance is affected by the scattering rate $\hbar\Gamma$. The latter is proportional to the impurity density $n^*$, caused by local potential fluctuations and electron/hole puddles on the graphene layer [78, 112]. The higher the impurity density, the higher scattering rate, which corresponds to lower mobility and therefore higher resistance. When the mobility is higher (lower $\hbar\Gamma$ and $n^*$), the peak in graphene's resistance corresponding to the neutrality point is higher. As a consequence, the resistance experiences a more abrupt change when the gate voltage is increased or decreased to move away from the neutrality point [76]. The values of $R_{graC}$ and $R_{gra}$ at a fixed DC voltage bias are also affected by graphene's intrinsic doping $n_0$. For $n_0 = 0$, graphene's resistance reaches its peak value at 0 V voltage bias, and decreases for increasing (or decreasing) voltage bias. When a voltage $V_{gate}$ is applied on the device, as indicated in Fig. 4.1, p-doped (n-doped) graphene shows a peak value at negative (positive) voltage bias due to the shift of graphene's charge neutrality point (Fig. 4.5a). The resistance then decreases as the voltage increases (decreases). In case of p-doped graphene, there is therefore a low resistance region for voltage values around or greater than 0 V. The Si contribution to $R_{tot}$ depends on the doping level of the three Si regions: contact, slab and waveguide

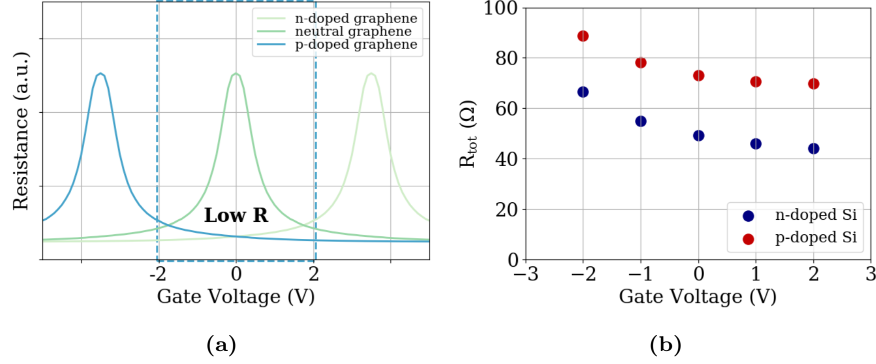



**Figure 4.5:** (a) Graphene resistance as a function of gate voltage for n-doped, pristine and p-doped graphene. For p-doped graphene there is a low resistance region for voltage values around or greater than 0 V. The plotted data is illustrative and adapted from measurements. (b) Simulated total resistance as a function of gate voltage of a 75 µm-long SLG EAM with p-doped graphene, for p-doped ($p_{wg} = 1.9e18$ cm$^{-3}$, $p_{slab} = 3.2e19$ cm$^{-3}$) and n-doped silicon ($n_{wg} = 2.3e18$ cm$^{-3}$, $n_{slab} = 2.7e19$ cm$^{-3}$). P-doped silicon exhibits higher sheet resistance than n-doped silicon. The voltage-dependent behaviour is caused by $R_{graC}$ and $R_{gra}$.

areas. To properly estimate how the silicon doping impacts the resistance, we perform a process simulation using Sentaurus TCAD, which accurately emulates the real processing performed in the fab. Afterwards we extract the values of silicon resistance ($R_{Si}$ and $R_{SiC}$) for the three doped regions together by performing a transient device simulation at different voltage values. Fig. 4.5b shows an example of the values of $R_{tot}$ as a function of gate voltage for a 75 $\mu$m-long device with p-doped graphene (mobility $\mu_c$ = 800 cm$^2$/Vs; $R_{graC}$ = 880 Ω µm and $R_{gra}$ = 340 Ω/□ at 0 V) and a waveguide width of 500 nm, for p-doped ($p_{wg} = 1.9e18$ cm$^{-3}$, $p_{slab} = 3.2e19$ cm$^{-3}$) and n-doped ($n_{wg} = 2.3e18$ cm$^{-3}$, $n_{slab} = 2.7e19$ cm$^{-3}$) Si. P-doped silicon exhibits higher sheet resistance than n-doped silicon, due to the lower mobility of holes compared to electrons and due to the slightly lower doping concentration. The variation of $R_{tot}$ with gate voltage is influenced by the voltage-dependent behaviour of $R_{graC}(V)$ and $R_{gra}(V)$ only.

### GOS capacitance

The total GOS capacitance $C_{GOS}$ is given by the series of graphene's quantum capacitance $C_q$, the oxide capacitance $C_{ox}$ and the Si depletion capacitance $C_{Si}$:

$$\frac{1}{C_{GOS}} = \frac{1}{C_q} + \frac{1}{C_{ox}} + \frac{1}{C_{Si}} \tag{4.8}$$

The quantum capacitance is possessed by all materials and is related to the

density of states of the capacitor plates. However, it is usually a large positive quantity and therefore irrelevant for most materials except for low-density-of-states systems, such as graphene. Graphene's quantum capacitance is given by the following equation [103, 162]:

$$C_q = \frac{2q^2}{\hbar v_F \sqrt{\pi}} \sqrt{|n_s + n_0|} = \frac{2q^2}{\hbar^2 v_F^2 \pi} |\mu| \tag{4.9}$$

where $\mu$ is graphene's Fermi level as defined in Eq. 4.6. The quantum capacitance is characterised by a minimum when $\mu = 0$ ($\Delta\mu = -\mu_0$, according to Eq. 4.6) and it increases linearly for $|\mu| > 0$ (Fig. 4.6a). For intrinsic (undoped) graphene, the Fermi level is at the Dirac point, $\mu_0 = 0$ and therefore $C_q = 0$ for $\Delta\mu = 0$ (Fig. 4.6b). In p-doped (n-doped) graphene, $\mu_0 < 0$ ($\mu_0 > 0$) and, as a consequence, the minimum of $C_q$ is located at $\Delta\mu = -\mu_0$ (Fig. 4.6b). When graphene is not pristine, the additional impurity carrier density $n^*$ should be included in the calculation. The quantum capacitance becomes [112]

$$C_q = \frac{2q^2}{\hbar v_F \sqrt{\pi}} \sqrt{|n_s + n_0| + |n^*|} \tag{4.10}$$

If we compare $C_q$ with $C_{ox}$ calculated for 5 nm of $SiO_2$ (Fig. 4.6), we see that the latter is significantly smaller for each value of $\mu$ far from the neutrality point. When $n* > 0$, the minimum of the quantum capacitance increases and $C_q$ becomes significantly higher than $C_{ox}$ for any value of chemical potential, as shown by the dotted lines in Fig. 4.6. For this reason, when placed in series with $C_{ox}$, the contribution of $C_q$ is minor.

The analytical model used to calculate $C_{GOS}$ as a function of applied voltage $V_g$ is based on the one for the MOS capacitor [163], with the difference that for the GOS capacitor graphene's quantum capacitance $C_q$ is included in the calculation. The voltage is applied on the graphene contact, while the silicon contact is grounded. In accumulation ($V_g < V_{FB} < 0$ for p-doped Si and $V_g > V_{FB} > 0$ for n-doped Si, with $V_{FB}$ being the commonly known flatband voltage of a MOS capacitor [163]), the silicon layer is not yet depleted, so the quantities that play a role are $C_q$ and $C_{ox}$. To calculate the amount of charges $n_s$ accumulated on the graphene layer for each $V_g < V_{FB}$, we need to solve the following system

$$\begin{cases} V_g - V_{FB} = Q_{acc}\left(\frac{1}{C_{ox}} + \frac{1}{C_q}\right) = n_s\left(\frac{1}{C_{ox}} + \frac{1}{C_q}\right) \\ C_q = \frac{2q^2}{\hbar v_F \sqrt{\pi}} \sqrt{|n_s + n_0| + |n^*|} \qquad \text{(Eq. 4.10)} \end{cases} \tag{4.11}$$

where $Q_{acc}$ is the accumulation charge. The resulting equation for $n_s$ is

$$\frac{q}{C_{ox}} n_s + \left(\frac{\hbar v_F{}^2 \sqrt{\pi}}{2q}\right) \frac{n_s}{\sqrt{|n_s + n_0| + |n^*|}} + (V_{FB} - V_g) = 0 \tag{4.12}$$

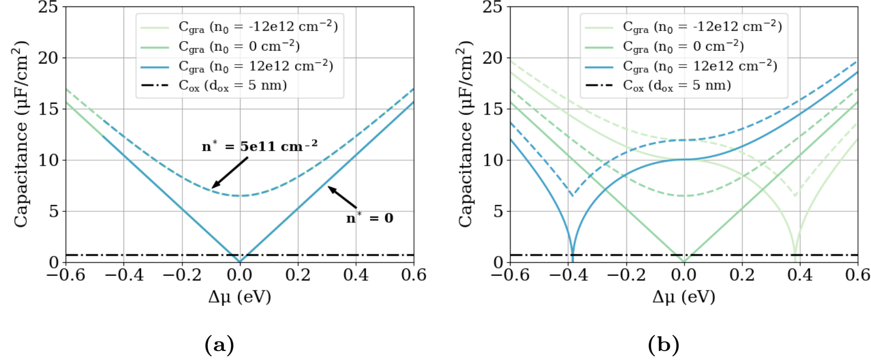



**Figure 4.6:** (a) Calculated graphene quantum capacitance as a function of graphene's Fermi level $\mu$, for n-doped ($n_0 = -12e12$ cm$^{-2}$), neutral ($n_0 = 0$ cm$^{-2}$) and p-doped ($n_0 = 12e12$ cm$^{-2}$) graphene, compared with the capacitance of 5 nm-thick $SiO_2$. The full lines are calculated for $n^* = 0$ and the dotted lines for $n^* = 5e11$ cm$^{-2}$. (b) Same as (a), but the capacitance is plotted as a function of Fermi level shift ($\Delta\mu = \mu - \mu_0$).

Once the value of $n_s$ for each $V_g$ is known, we can calculate $C_q$ through Eq. 4.9 and therefore the total accumulation capacitance

$$C_{GOS,acc} = \left(\frac{1}{C_{ox}} + \frac{1}{C_q}\right)^{-1} \tag{4.13}$$

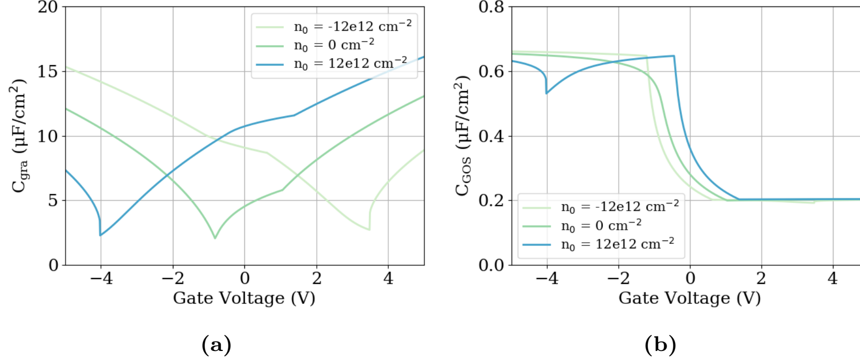
Graphene's natural doping $n_0$ is considered in the calculation as an initial condition and it will automatically affect the position of graphene's charge neutrality point in the final result. In fact, $n_s$ and $n_0$ in Eq. 4.9 are summed up before applying the absolute value, which is necessary to make a distinction between n-doped ($n_0 < 0$) and p-doped graphene ($n_0 > 0$). In inversion ($V_g > V_T > 0$ for p-doped Si and $V_g < V_T < 0$ for n-doped Si, where $V_T$ is threshold voltage [163]) the silicon layer has reached maximum depletion and the quantities to be considered are $C_q$, $C_{ox}$ and $C_{Si,max}$. Eq. 4.12 becomes

$$\frac{q}{C_{ox}} n_s + \left(\frac{\hbar v_F{}^2 \sqrt{\pi}}{2q}\right) \frac{n_s}{\sqrt{|n_s + n_0| + |n^*|}} + (V_g - V_{FB} - 2\phi_F) = 0 \tag{4.14}$$

where the bulk potential $\phi_F$ takes into account the voltage drop due to $C_{Si,max}$. The total inversion capacitance can be calculated as

$$C_{GOS,inv} = \left(\frac{1}{C_{ox}} + \frac{1}{C_q} + \frac{W_{dep,max}}{\varepsilon_0 \varepsilon_{Si}}\right)^{-1} \tag{4.15}$$

where $W_{dep,max}$ is the maximum width of the depletion region in the silicon layer.




**(a)** **(b)**

**Figure 4.7:** (a) Graphene quantum capacitance as a function of gate voltage for n-doped ($n_0 = -12e12$ cm$^{-2}$), neutral ($n_0 = 0$ cm$^{-2}$) and p-doped ($n_0 = 12e12$ cm$^{-2}$) graphene ($n^* = 5e11$ cm$^{-2}$). The minimum of $C_q$ shifts depending on the graphene doping. (b) Theoretical GOS capacitance as a function of gate voltage with fixed p-type silicon waveguide doping ($p_{wg} = 1.0e18$ cm$^{-3}$), for n-doped ($n_0 = -12e12$ cm$^{-2}$), neutral ($n_0 = 0$ cm$^{-2}$) and p-doped ($n_0 = 12e12$ cm$^{-2}$) graphene ($n^* = 5e11$ cm$^{-2}$). $C_q$ affects $C_{GOS}$ only in proximity of its minimum.

To calculate the total capacitance $C_{GOS,dep}$ in depletion ($V_{FB} < V_g < V_T$ for p-doped Si and $V_{FB} > V_g > V_T$ for n-doped Si), a different approach is necessary. The width of the depletion region in silicon $W_{dep}$ has to be calculated for values of the surface potential $\phi_s$ ranging from 0 to $2\phi_F$. From $W_{dep}$, the depletion charge $Q_{dep}$ and therefore the number of charges on graphene $n_s$ can be calculated. The total GOS capacitance in depletion is given by

$$C_{GOS,dep} = \left( \frac{1}{C_{ox}} + \frac{1}{C_q} + \frac{W_{dep}}{\varepsilon_0 \varepsilon_{Si}} \right)^{-1} \tag{4.16}$$

All the quantities that have been calculated as a function of $\phi_s$ can then be expressed as a function of the applied voltage through

$$V_g = V_{FB} + \phi_s - Q_{dep} \left( \frac{1}{C_{ox}} + \frac{1}{C_q} \right) \tag{4.17}$$

Throughout the calculation of $C_{GOS}$, the values of $V_g(n_s)$, and therefore $V_g(\mu)$, are extracted step by step, and are used to obtain graphene's absorption (and therefore transmission) as a function of the applied voltage $V_g$ through Eq. 4.5, as shown in Fig. 4.3.

The results of the calculation of $C_{GOS}$ for a GOS capacitor with p-doped silicon ($p_{wg} = 1.0e18$ cm$^{-3}$) and for n-doped ($n_0 = -12e12$ cm$^{-2}$), neutral ($n_0 = 0$ cm$^{-2}$) or p-doped ($n_0 = 12e12$ cm$^{-2}$) graphene are shown in Fig. 4.7b. As expected, graphene's quantum capacitance affects $C_{GOS}$ only where $C_q$ reaches its minimum (Fig. 4.7a). This effect is clearly visible only when

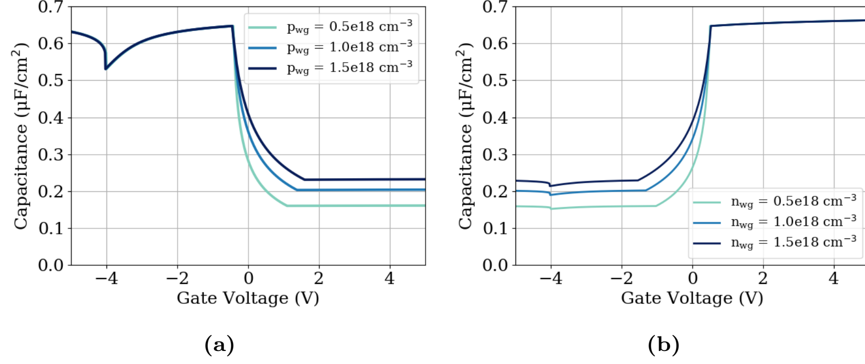



**Figure 4.8:** Calculated GOS capacitance with p-doped graphene ($n_0 = 12e12\,\text{cm}^{-2}$), for varying p-type (a) and n-type (b) Si waveguide doping levels. The capacitance in depletion decreases for lower doping level.

the GOS capacitor is in accumulation mode, and therefore $C_{GOS}$ is higher. As a consequence, reducing $C_q$ by reducing the impurity density $n^*$ would only have a small effect on $C_{GOS}$ as a whole. In order to decrease $C_{ox}$, we could use an oxide with a lower permittivity or increase the oxide thickness. However, both solutions would increase the field necessary to accumulate charges on the capacitor plates to operate the device. In other words, the lower capacitance would allow to obtain a higher 3 dB frequency response, but the extinction ratio for the same voltage range would be significantly reduced. The device capacitance can therefore be optimised by focusing on how $C_{Si}$ changes when varying the type and level of doping, and on how this affects $C_{GOS}$. Fig. 4.8 shows the calculation of $C_{GOS}$ performed for p-doped graphene ($n_0 = 12e12$ cm$^{-2}$) for different levels of p-type and n-type silicon doping. The capacitance in accumulation is not affected by the variation in silicon doping level. A reduction in depletion capacitance is achieved for lower silicon doping, as expected due to the lower silicon depletion capacitance $C_{Si}$ when the silicon doping is decreased. Due to this characteristic MOS behaviour, it is preferable to operate the device in depletion in order to obtain lower capacitance. It should be noted that, while a lower capacitance is beneficial to achieve a higher 3 dB frequency response, it also leads to a higher driving voltage and by consequence a larger power consumption. If graphene used to fabricated SLG EAMs approaches its ideal condition (high mobility and low scattering rate), the switch between on- and off-states will be very sharp (Fig. 4.3b) that the $V_{pp}$ used for measurements won't be an issue even at low capacitance.

### 4.1.4 Device optimisation

To optimise the SLG EAM for high-speed operation, the 3 dB frequency response of the device has to be maximised. This figure of merit is limited by

**Table 4.1:** Summary of the level and type of Si doping used for the theoretical calculation shown in Fig. 4.9.

| Doping type | Slab doping ($cm^{-3}$) | Wg doping ($cm^{-3}$) |
|---|---|---|
| n-doped | 2.7e19 | 2.3e18 |
| p-doped | 3.2e19 | 1.9e18 |

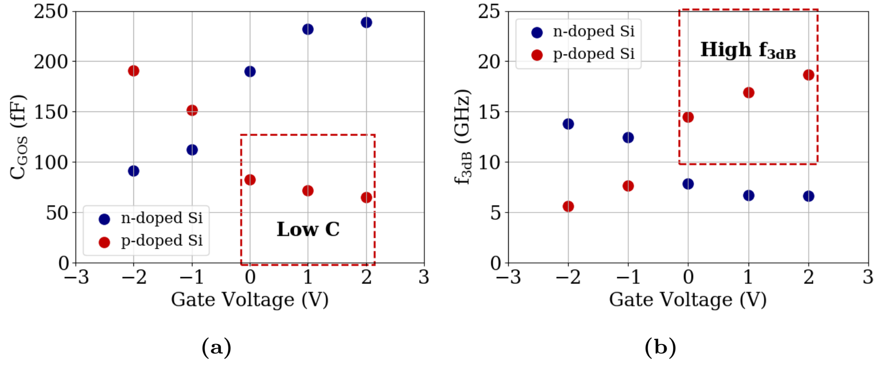



**Figure 4.9:** Calculated GOS capacitance (a) and simulated 3 dB frequency response (b) as a function of gate voltage of a 75 µm-long SLG EAM, for p-doped ($p_{wg} = 1.9e18$ cm$^{-3}$, $p_{slab} = 3.2e19$ cm$^{-3}$) and n-doped silicon ($n_{wg} = 2.3e18$ cm$^{-3}$, $n_{slab} = 2.7e19$ cm$^{-3}$). P-doped Si allows to operate the SLG EAM in depletion in the operating region of interest (0-2 V), thus achieving more than double $f_{3dB}$ compared to n-doped Si.

the device RC constant, therefore the total resistance and capacitance of the device have to be minimised in the desired operating region in order to obtain the lowest possible RC. In fabricated devices, graphene is most often p-doped, due to dangling oxygen bonds in the $SiO_2$ below and also due to environmental and polymer contamination during processing [164, 165]. In terms of static electro-optical performance, as seen in section 4.1.2, this means that the switching between on and off states takes place in the region between -2 V and 2 V voltage bias. This region corresponds to the low resistance region in case of p-doped graphene, as shown in Fig. 4.5. In order to have low capacitance in the same voltage range, p-doped Si is preferable because it allows to operate the device in depletion for voltage bias higher than 0 V. As a result, when p-doped graphene is combined with p-doped silicon, the total RC is reduced in the region between 0 V and 2 V. Likewise, in case of n-doped graphene, the situation would be reversed and the best choice would be a device with n-doped silicon operating at low reverse bias. This is better visualised in the example in Fig. 4.9. Fig. 4.9a shows the values of $C_{GOS}$ as a function of gate voltage for a 75 $\mu$m-long device with p-doped graphene ($n_0 = 12e12$ cm$^{-2}$) and

a waveguide width of 500 nm, for p-doped and n-doped Si (doping values in Table 4.1). Using these values of $C_{GOS}$ and values of $R_{tot}$ from Fig. 4.5b, the 3 dB frequency response is then extracted by simulating the electrical equivalent circuit in Fig. 4.4. Even though p-doped silicon exhibits higher sheet resistance than n-doped silicon, the considerably lower GOS capacitance of the EAM with p-doped silicon in the 0 V - 2 V region allows to achieve a two-fold improvement in 3 dB frequency response at 0 V (Fig. 4.9b).

Patterning graphene under the contact area, e.g. with holes, to increase the edge contact perimeter between graphene and the metal can lead to a significant reduction in graphene's contact resistance [166]. For example, improved values of graphene contact and sheet resistance ($R_{graC}$ = 100 Ω µm and $R_{gra}$ = 60 Ω/□) would allow to achieve a 3 dB frequency response of 17 GHz (18% improvement) at 0 V DC bias for a 75 µm-long EAM and 25 GHz for a 25 µm-long EAM. With reduced doping in the waveguide ($p_{wg} = 4e17$ cm$^{-3}$) this values could be further improved up to 23 GHz and 31 GHz for $L_{device}$ of 75 µm and 25 µm respectively.

## 4.2 Characterisation of graphene EAMs

In the first part of this experimental section, we compare the performance of four C-band SLG EAMs on TE waveguides between three samples, fabricated with different type and level of doping in Si. In section 4.2.2, we select the sample with p-type Si doping and we compare the performance of C-band SLG EAMs on TE and TM waveguides, showing the benefit of using TM waveguides. In section 4.2.3, on the same sample with p-type Si and using TM waveguides, we show uniform performance of SLG EAMs in the O-band, thus demonstrating broadband operation. In section 4.2.4, we conclude that the best performance is given by SLG EAMs on TM waveguides in the C-band, and we measure open eye diagrams up to 50 Gbit/s. All the measurements performed in this chapter were carried out with 6 dBm laser power (measured at the laser output), except for S-parameters and eye diagrams measurements which were performed with 12 dBm laser power. If a different laser power was used, we specify it in the text. All the devices presented in this chapter were fabricated using graphene grown and transferred by the commercial vendor *Graphenea*.

### 4.2.1 Effect of Si waveguide doping on the performance of C-band TE SLG EAMs

We fabricated three samples with different type and level of doping in Si (summary in Table 4.2). Sample A was fabricated with n-doped Si, with average carrier concentrations of $n_{slab} = 2.5e18$ cm$^{-3}$ and $n_{wg} = 1.2e18$ cm$^{-3}$ for the slab and the waveguide regions respectively. Sample B was fabricated using higher n-doping in the Si slab and waveguide regions than sample A ($n_{slab} = 2.7e19$ cm$^{-3}$ and $n_{wg} = 2.3e18$ cm$^{-3}$), with the purpose of reducing the total para-

**Table 4.2:** Summary of the level and type of Si doping on the three samples used for the experiment.

| | Doping type | Slab doping ($cm^{-3}$) | Wg doping ($cm^{-3}$) |
|---|---|---|---|
| **Sample A** | n-doped | 2.5e18 | 1.2e18 |
| **Sample B** | n-doped | 2.7e19 | 2.3e18 |
| **Sample C** | p-doped | 3.2e19 | 1.9e18 |

sitic resistance without significantly impacting the GOS capacitance. Sample C was fabricated using p-doped Si ($p_{slab}$ = 3.2$e$19 $cm^{-3}$ and $p_{wg}$ = 1.9$e$18 $cm^{-3}$). The full flow used to fabricate these samples is described in appendix A, section A.2.1.

The three samples were first characterised by performing unbiased fiber-to-fiber transmission measurements on SLG EAMs with waveguides optimised for TE mode propagation (TE waveguides, $W_{wg}$ = 500 nm) and with four different device lengths ($L_{device}$ = 25, 40, 50 and 75 µm). The transmission scales linearly with the device length, and the extracted average and standard deviation values of absorption are 0.08 ± 0.01 dB/µm, 0.08 ± 0.01 dB/µm and 0.05 ± 0.01 dB/µm for samples A, B and C respectively.

We then performed biased fiber-to-fiber transmission measurements on the same EAMs, by sweeping the wavelength from 1510 nm to 1600 nm, while applying a DC bias ranging from -4 V to 4 V. Fig. 4.10a shows the extracted extinction ratio (ER) versus device length ($L_{device}$) for the three samples at

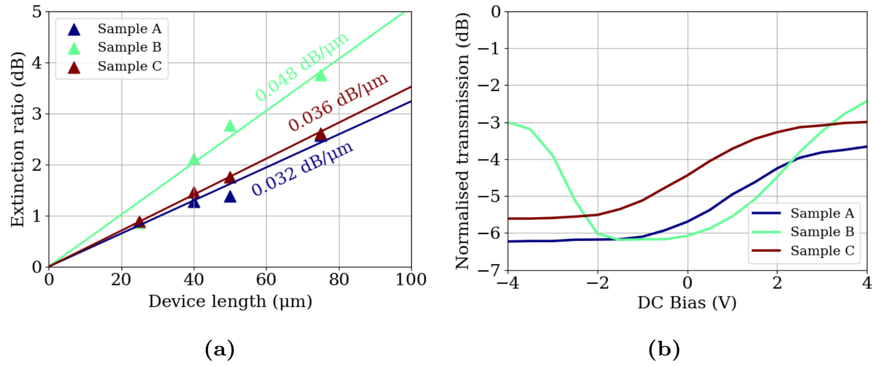



**Figure 4.10:** (a) Extinction ratio as a function of device length of TE SLG EAMs, obtained by measuring the transmission at 1560 nm from -4 V to 4 V DC bias on three samples with different type and level of Si doping. The ER scales linearly with device length. (b) Transmission, normalised to the reference waveguide, as a function of applied DC bias, measured on TE SLG EAMs with $L_{device}$ = 75 µm. Graphene is p-doped on all the samples.

the peak transmission wavelength of 1560 nm. The values of ER scale linearly with the device length, reaching up to 2.6 dB for Samples A and C and 3.8 dB for sample B for $L_{device}$ = 75 µm. An example of the extracted transmission as a function of DC bias at 1560 nm for $L_{device}$ = 75 µm is reported in Fig. 4.10b. All three samples show minimum transmission of the modulation curve located at reverse bias which indicates p-type doping in graphene. Sample B exhibits lower p-type graphene doping than the other two samples, which translates into the minimum transmission being shifted towards lower reverse bias. As a consequence, when the reverse bias on sample B is increased, graphene approaches again transparency, resulting in a more symmetrical transmission curve compared to the other two samples. The average and standard deviation values of modulation efficiency ($ME = ER/L_{device}$) across the four devices at 1560 nm are 0.03 ± 0.01 dB/µm, 0.05 ± 0.01 dB/µm and 0.04 ± 0.01 dB/µm for samples A, B and C respectively. The higher modulation in sample B is attributed to higher mobility in graphene compared to the other two samples. This is confirmed by the values of graphene's mobility extracted from transfer length measurements (TLM) of graphene's electrical test structures fabricated on the same sample (1610 $cm^2V^{-1}s^{-1}$ for sample B and 1490 $cm^2V^{-1}s^{-1}$ for sample C). The lower p-type graphene doping and the higher graphene mobility in sample B are attributed to sample-to-sample variations of graphene's properties, caused by uncontrolled variations in processing conditions.

The electro-optical $S_{21}$ frequency response of the modulators was measured between 100 MHz and 30 GHz at DC bias ranging from 0 V to 2 V with a vector network analyser, using -8 dBm RF power and 12 dBm laser power. Fig. 4.11a compares the extracted 3 dB frequency response ($f_{3dB}$) of the three samples as a function of DC bias for $L_{device}$ = 75 µm. Fig. 4.11b and 4.11c compare the extracted $R_{tot}$ and $C_{GOS}$ from the fitting of the $S_{11}$ frequency response measured on the three samples, performed using the equivalent electrical circuit shown in Fig. 4.4. Among the n-doped samples, sample B exhibits the highest 3 dB frequency response at any forward voltage bias, with a maximum value of 8.9 GHz at 0 V DC bias for $L_{device}$ = 75 µm. The decrease in $R_{tot}$ (20% at 0 V DC bias) achieved in sample B with the higher doping in the slab and waveguide regions, counteracts the slight increase in $C_{GOS}$ caused by the higher waveguide doping (13% at 0 V DC bias). The higher graphene mobility in sample B might also contribute to the lower $R_{tot}$. This allows to improve the $f_{3dB}$ from sample A to sample B at any forward voltage bias, e.g. with a gain of 2 GHz (29%) at 0 V DC bias (Table 4.3). As expected from the theoretical analysis, the sample fabricated using p-doped Si (sample C) shows a substantial increase in 3 dB frequency response compared to sample B, with values up to 22.8, 21.6, 14.2 and 16.1 GHz at 0 V DC bias for $L_{device}$ = 25, 40, 50 and 75 µm respectively (Table 4.3). Even though the total device resistance is higher, the lower $C_{GOS}$ obtained by operating the device in depletion mode instead of accumulation mode allows to significantly reduce the total RC constant, and thus enhance the 3 dB frequency response at any forward voltage bias. The values of $f_{3dB}$ decrease with the device length, due to the increase in the total

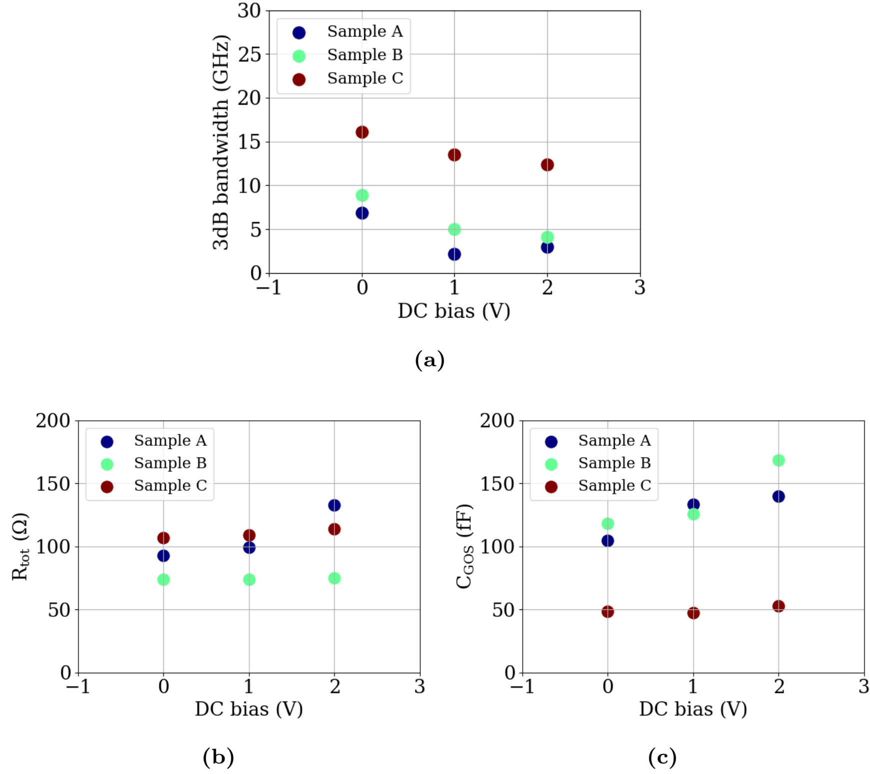



**Figure 4.11:** (a) 3 dB frequency response, (b) total resistance $R_{tot}$ and (c) GOS capacitance $C_{GOS}$ as a function of DC bias of TE SLG EAMs with $L_{device}$ = 75 µm on the three samples. The values of $R_{tot}$ and $C_{GOS}$ were extracted from $S_{11}$ parameters fitting. Sample C exhibits higher $f_{3dB}$ due to the lower $C_{GOS}$.

**Table 4.3:** Values of measured 3 dB frequency response ($f_{3dB}$) at 0 V DC bias on TE SLG EAMs for $L_{device}$ = 25, 40, 50 and 75 µm. The $f_{3dB}$ is higher for sample C (p-doped Si) and for smaller device lengths.

| | **Measured $f_{3dB}$ (GHz)** | | | |
|---|---|---|---|---|
| | **L = 25 µm** | **L = 40 µm** | **L = 50 µm** | **L = 75 µm** |
| **Sample A** | 10.9 | 7.7 | 8.2 | 6.9 |
| **Sample B** | 12.9 | 10.6 | 9.6 | 8.9 |
| **Sample C** | 22.8 | 21.6 | 14.2 | 16.1 |

RC constant of the circuit (Table 4.3).

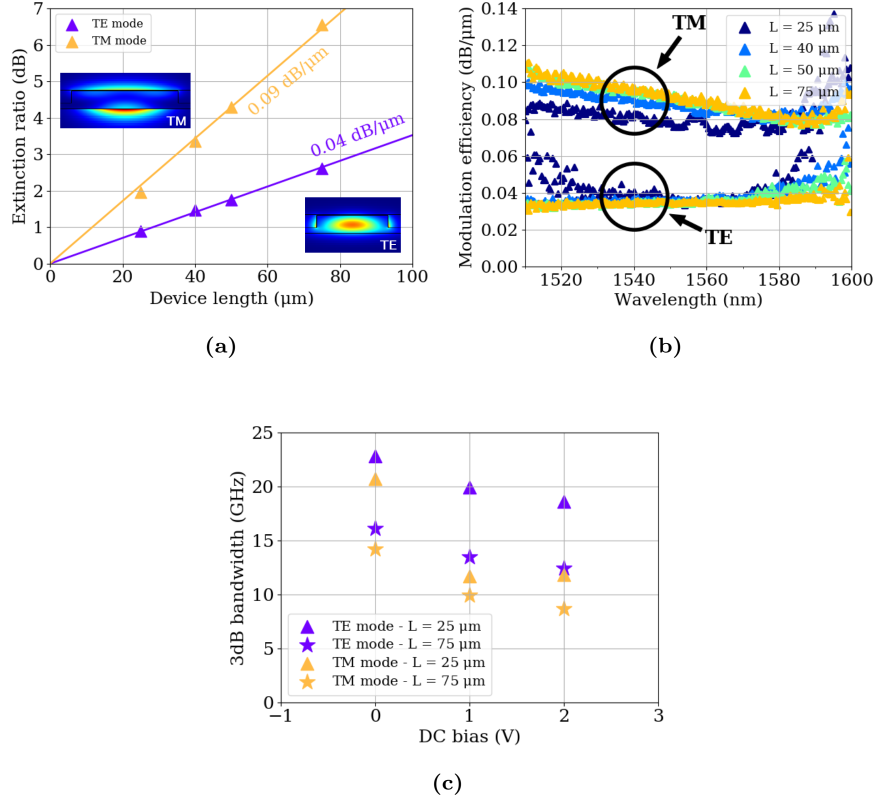
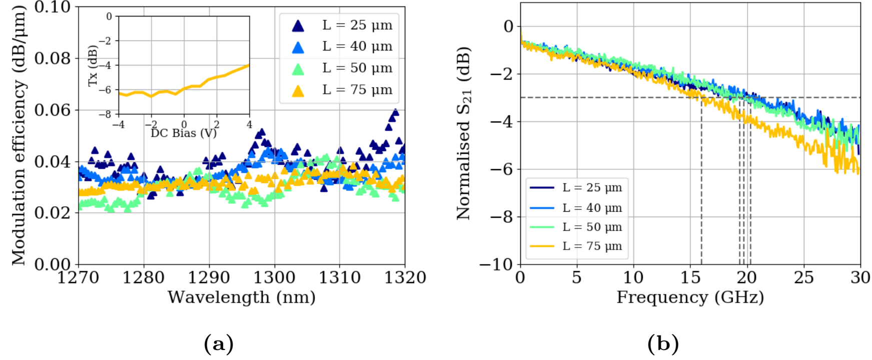



**Figure 4.12:** (a) Comparison of measured extinction ratio on sample C between TE mode and TM mode SLG EAMs. TM EAMs exhibit higher ER due to the bigger mode overlap with the graphene layer. (b) Modulation efficiency as a function of wavelength of the four TE and four TM C-band SLG EAMs on sample C. All the devices are broadband and the ME is consistent across the C-band spectrum. (c) Comparison of 3 dB frequency response between TE and TM SLG EAMs measured on sample C as a function of applied DC bias for different device lengths. TM SLG EAMs have lower $f_{3dB}$ than TE SLG EAMs.

### 4.2.2 Performance comparison of C-band TE and TM SLG EAMs

Despite the high 3 dB frequency response achieved with the sample with p-doped Si (sample C), the ER of the SLG EAMs remains limited when using TE-polarised light, with values ranging from 0.9 dB for $L_{device}$ = 25 µm to 2.6 dB for $L_{device}$ = 75 µm. Using waveguides optimised for TM mode propagation (TM waveguides) can increase the ER for a given device length, due to the bigger overlap between the TM optical mode and the graphene layer compared to TE (see inset of Fig. 4.12a). To maximise the overlap with graphene and keep




(a) (b)

**Figure 4.13:** (a) Modulation efficiency as a function of wavelength of the four TM O-band SLG EAMs. The devices are broadband and the ME is consistent across the O-band spectrum. Inset: normalised transmission as a function of applied DC bias measured on the 75 µm-long EAM. (b) $S_{21}$ parameters measured on the four TM O-band SLG EAMs at 1 V DC bias.

propagation losses not too high, but still ensure single-mode confinement in the waveguide, we use a waveguide width of 750 nm [9]. Unbiased transmission measurements performed on sample C (p-doped Si) from 1510 nm to 1600 nm on SLG EAMs with TM waveguides, equivalent to the ones performed on TE waveguides, showed that graphene's absorption is 0.09 ± 0.01 dB/µm, which is 2.3 times higher than the 0.04 ± 0.01 dB/µm measured on TE waveguides, in agreement with the value of 2.2 extracted from Lumerical MODE simulations. The ME of the four SLG EAMs is consistent across the measured C-band spectrum for both TE and TM devices (Fig. 4.12b). The drawback in using TM waveguides comes from the wider waveguide width, which leads to higher sheet resistance and GOS capacitance, resulting in a 1.1 $\sim$ 1.5 times lower 3 dB frequency response compared to TE waveguides (Fig. 4.12c). Nevertheless, due to the low $C_{GOS}$ at forward bias on the SLG EAMs with p-doped Si, TM waveguides exhibit 3 dB frequency response at 0 V DC bias of 20.7, 18.0, 15.7 and 14.2 GHz for $L_{device}$ = 25, 40, 50 and 75 µm respectively.

### 4.2.3 Performance of O-band TM SLG EAMs

To demonstrate the broadband operation of graphene devices, we measured TM graphene-Si EAMs fabricated on sample C with exactly the same processing steps and cross section, but with grating couplers and waveguide width designed to operate in the O-band. We characterised four devices, with same lengths as the TM C-band devices demonstrated earlier ($L_{device}$ = 25, 40, 50 and 75 µm) and waveguide width of 380 nm. Fiber-to-fiber transmission measurements from 1260 nm to 1330 nm, resulted in an average absorption across the four devices of 0.10 ± 0.01 dB/µm. The biased transmission measurements were

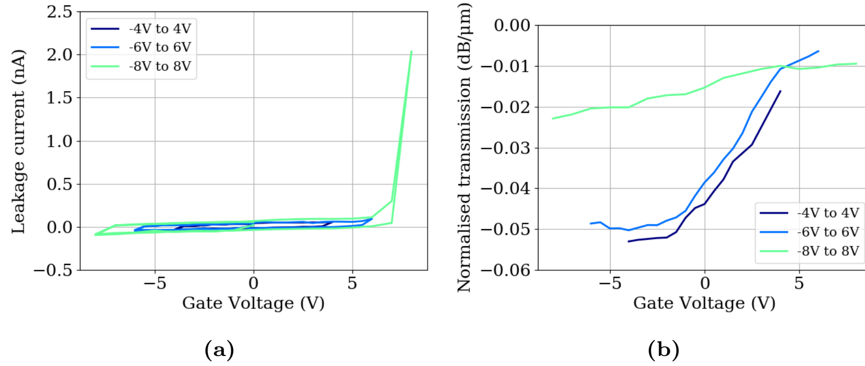



**Figure 4.14:** Breakdown test performed on a 75 µm-long O-band SLG EAM. (a) I-V measurement and (b) transmission as a function of voltage at increasing sweeping bias range from ±4 V to ±8 V.

performed sweeping the DC bias from -4 V to 4 V and the wavelength from 1270 nm to 1320 nm. The average and standard deviation values of ME at the peak of the fiber grating couplers (1300 nm) across the four devices are 0.041 ± 0.005 dB/µm. The extracted ME of the four TM O-band SLG EAMs is consistent across the O-band spectrum, as shown in Fig. 4.13a. The lower modulation efficiency compared to C-band TM devices is due to the higher energy of the photons in the O-band. As a consequence, it is necessary to apply a higher voltage in order to achieve full transparency in graphene, which results in oxide breakdown. We performed a breakdown test on the 75 µm-long SLG EAM by slowly increasing the DC bias sweeping range from ±4 V to ±10 V. The ME increases up to 0.045 dB/µm at ±6 V and then it decreases down to 0.03 dB/µm at ±7 V and to 0.005 dB/µm at ±10 V, due to the increased leakage current. Examples of *I-V* and transmission versus voltage measurements at ±4 V, ±6 V and ±8 V are plotted in Fig. 4.14. The 3 dB frequency response of the O-band SLG EAMs, extracted from electro-optical $S_{21}$-parameters measurements at 1300 nm wavelength, reaches values of 19.7, 20.3, 19.3 and 16.0 GHz at 1 V DC bias for $L_{device}$ = 25, 40, 50 and 75 µm respectively (Fig. 4.13b).

### 4.2.4 Large signal high speed performance

A summary of the performance of the C-band TE, C-band TM and O-band TM SLG EAMs on sample C is reported in Table 4.4 for $L_{device}$ = 75 µm. The FOM is defined as ER/IL and should therefore be as high as possible. The C-band TM EAM represents the best compromise between IL and ER, as shown by the high value of FOM, while also exhibiting a 3 dB frequency response of 14 GHz. Eye diagrams were measured on the C-band SLG EAM with p-doped Si (sample C), TM waveguide and $L_{device}$ = 75 µm at 1560 nm

**Table 4.4:** Summary of the main figures of merit measured on the three types of SLG EAMs on sample C (p-doped Si). The values reported are for 75 µm-long devices. The FOM is calculated as ER/IL. The C-band TM SLG EAM offers the best trade-off.

| | IL (dB) | ER (dB) | FOM | $f_{3dB}$ (GHz) | $\lambda$ (nm) |
|---|---|---|---|---|---|
| **C-band TE** | 3.0 | 2.6 | 0.9 | 16.1 | 1510 - 1600 |
| **C-band TM** | 4.2 | 6.5 | 1.5 | 14.2 | 1510 - 1600 |
| **O-band TM** | 4.0 | 3.1 | 0.8 | 16.0 | 1270 - 1320 |

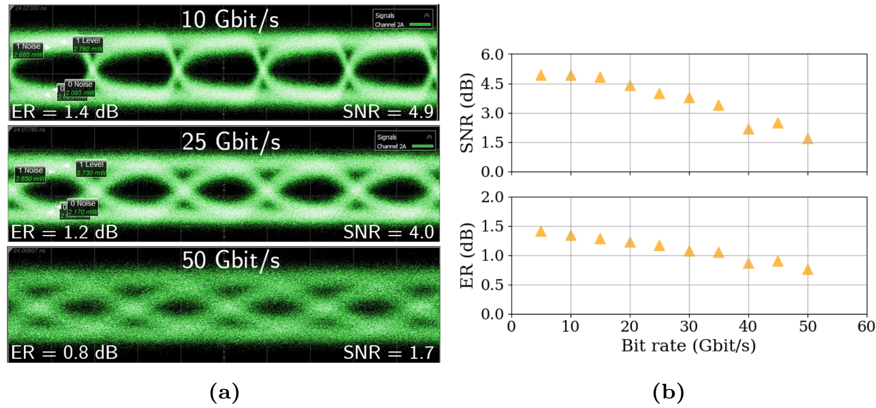



**Figure 4.15:** (a) Eye diagrams measured at 10, 25 and 50 Gbit/s on the SLG EAM with p-doped Si, TM waveguide and $L_{device}$ = 75 µm (sample C). (b) SNR and large-signal extinction ratio plotted as a function of the bit rate for the same device. The SNR and the ER remain higher than 3.0 and 1.0 dB respectively up to 35 Gbit/s.

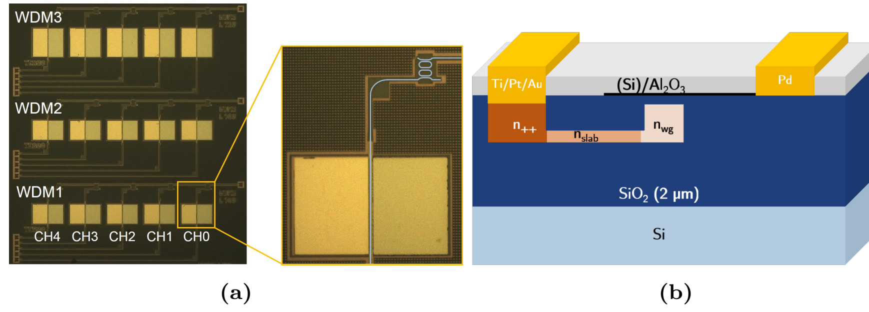
using $2^{23}$-1 PRBS, 2.5 $V_{pp}$ and a 50 Ω terminated probe. Open eye diagrams were generated from 5 Gb/s up to 50 Gbit/s, thus demonstrating potential for high speed data transmission using graphene technology. Examples at 10 Gbit/s, 25 Gbit/s and 50 Gbit/s are shown in Fig. 4.15a. The large-signal ER and the signal-to-noise ratio (SNR) are reported in Fig. 4.15b as a function of bit rate. The dynamic energy consumption ($E_{bit} = CV^2/4$) of the SLG EAM is calculated to be $\sim$ 112 fJ, while the static power consumption is $< 10^{-8}$ mW, due to the low leakage current flowing through the GOS capacitor ($<$ 10 pA).

## 4.3 Wavelength-division multiplexing (WDM) transmitters

Graphene-based modulators can be implemented in WDM systems to modulate the signal on the different channels. However, experimental work on

**Table 4.5:** Waveguide width ($W_{wg}$) and device length ($L_{device}$) values used to fabricate the three WDM transmitters. Increasing $W_{wg}$ and $L_{device}$ is expected to increase the extinction ratio but also the device capacitance, and therefore to reduce the 3dB bandwidth.

| | WDM1 | WDM2 | WDM3 |
|---|---|---|---|
| **$W_{wg}$ (nm)** | 500 | 600 | 600 |
| **$L_{device}$ (µm)** | 100 | 100 | 150 |




(a) (b)

**Figure 4.16:** (a) Top view microscope image showing the three WDM transmitters, each based on 5 graphene-Si EAMs and 5 second order MRRs. WDM1: $W_{wg}$ = 500 nm, $L_{device}$ = 100 µm; WDM2: $W_{wg}$ = 600 nm, $L_{device}$ = 100 µm; WDM3: $W_{wg}$ = 600 nm, $L_{device}$ = 150 µm. (b) Cross section of a graphene-Si EAM, passivated with Si (0.5nm)/$Al_2O_3$ (10nm).

graphene-based modulators has mainly been focused on the development of individual components, due to challenges in processing, transfer and integration of high quality graphene at large scale [86]. In this section, we experimentally demonstrate for the first time the integration of multiple graphene EAMs with functional silicon photonics circuits.

### 4.3.1 Design and fabrication

We fabricated three WDM transmitters consisting of 5 SLG EAMs and 5 second order MRRs each, as shown in Fig.4.16a. The SLG EAMs used for this experiment have same doping as Sample B, which was presented in the previous section ($n_{slab}$ = 2.7$e$19 cm$^{-3}$ and $n_{wg}$ = 2.3$e$18 cm$^{-3}$). The full flow used to fabricate this sample is described in appendix A, section A.2.2. Each transmitted wavelength goes through the SLG EAMs before being added to the bus waveguide of the MRRs. The channel spacing of the MRRs, acting as multiplexer, is designed to fit a grid spacing of 300 GHz (2.4 nm) and a free-spectral range (FSR) of 12 nm. The rings have a racetrack shape and are implemented with 450 nm-wide waveguides, 9 µm coupling length, 5 µm radius and 190 nm bus-ring gap [64]. To reduce fabrication complexity and power

consumption, no temperature control was used, therefore variations in IL, resonant wavelength and cross-talk are expected due to local non-uniformities, as shown in [64]. The first transmitter (WDM1) is made of five identical graphene EAMs with 500 nm-wide waveguides and 100 µm-long graphene. The second (WDM2) and third (WDM3) transmitters are made of graphene EAMs with 600 nm-wide waveguides and 100 µm- and 150 µm-long graphene respectively. The MRRs are connected to the EAMs using tapers.

The device fabrication was carried out following the passivation-first approach (see chapter 3). $Al_2O_3$ was chosen as encapsulating material because it allows to obtain hysteresis-free electro-optical response, it preserves the p-doping characteristic of unpassivated graphene and it's stable over time [143]. To ensure a uniform passivation layer, we first evaporated 0.5 nm of Si as seeding layer by e-gun evaporation, and then deposited 10 nm of $Al_2O_3$ as capping layer by atomic layer deposition (ALD). Due to the passivation-first approach, graphene is removed from the contact area, and a side contact between graphene and Pd is created.

### 4.3.2 Experimental results

We first performed unbiased fiber-to-fiber transmission measurements of the three WDM transmitters, each composed of 5 channels. The insertion loss (IL) of each channel was calculated as the peak transmission of the channel, normalised to the transmission of a reference waveguide without graphene at the same wavelength. The extracted average and standard deviation values of IL over the 5 channels are 3.8 ± 1.0 dB, 2.9 ± 0.7 dB and 4.0 ± 0.5 dB for WDM1, WDM2 and WDM3 respectively (Table 4.6). To determine the main source of insertion loss, we performed transmission measurements on a WDM filter without graphene, with same design as WDM2, located on a different die. These measurements, normalised to a reference waveguide, show that the IL due to the second order MRRs is ∼2 dB for CH1 and less than 1 dB for all other channels (Fig. 4.17). Therefore, we conclude that the loss of the WDM transmitters is dominated by the IL of the graphene modulators.

The electro-optical response of the graphene EAMs was characterised by sweeping the wavelength from 1510 nm to 1600 nm on each channel, while applying voltage bias ranging from -4 V to 4 V. The optical power was mea-

**Table 4.6:** Insertion loss (IL) and extinction ratio (ER) at 8 $V_{pp}$. The values are averaged over 5 channels. WDM3 exhibits higher IL and ER due to the longer $L_{device}$.

| | $L_{device}$ (µm) | IL (dB) | ER (dB) |
|---|---|---|---|
| **WDM1** | 100 | 3.8 ± 1.0 | 5.5 ± 0.1 |
| **WDM2** | 100 | 2.9 ± 0.7 | 5.6 ± 0.1 |
| **WDM3** | 150 | 4.0 ± 0.5 | 8.1 ± 0.7 |

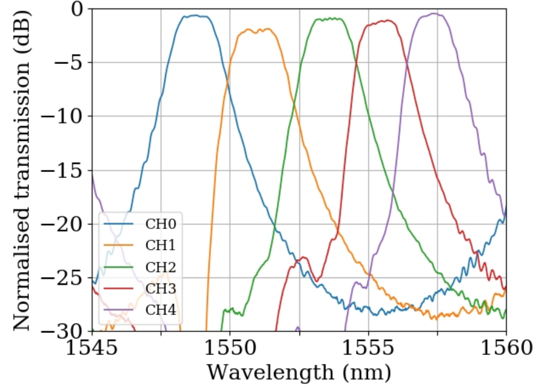



**Figure 4.17:** Transmission spectra, normalised to a reference waveguide, measured on a WDM filter without graphene, showing the insertion loss of the second order MRRs.

sured at the output of the transmitters (bus waveguide). These measurements performed on WDM1, WDM2 and WDM3 are shown in Fig. 4.18a, 4.18c and 4.18e respectively, with reduced wavelength range from 1552.5 nm to 1562.5 nm for clarity. The extinction ratio (ER) at 8 $V_{pp}$ was obtained by extracting the transmission as a function of the voltage at the peak transmission wavelength of each channel (Fig. 4.18b, 4.18d and 4.18f for WDM1, WDM2 and WDM3 respectively). The ER is consistent across all the channels, with average values of $5.5 \pm 0.1$ dB for WDM1, $5.6 \pm 0.1$ dB for WDM2 and $8.1 \pm 0.7$ dB for WDM3 (Table 4.6). The higher ER in WDM3 is due to the longer device length, which ensures a longer interaction between the graphene layer and the evanescent field of the light travelling through the waveguide. The electro-optical switching in transmission occurs around 0 V, because of p-doping in graphene. The carrier mobility of graphene is estimated to be $\sim$ 800 $cm^2/(Vs)$ from measurements performed on electrical test structures fabricated on the same sample. The static power consumption at -1 V is calculated to be $< 2 \times 10^{-8}$ mW, due to the $<$ 20 pA measured leakage current.

The electro-optical $S_{21}$ frequency response was measured between 100 MHz and 30 GHz on the three WDM transmitters at DC bias ranging from -2 V to 2 V with a vector network analyser, using -8 dBm RF power. Fig. 4.19a, 4.19b and 4.19c show the $S_{21}$ and $S_{11}$ frequency response at 0 V DC bias of WDM1, WDM2 and WDM3 respectively. The trend of the 3dB bandwidth as a function of DC bias is shown in Fig.4.19d for WDM1. The highest 3dB bandwidth is measured at -1 V and 0 V, where the total RC constant of the device reaches the minimum. This behaviour is expected for SLG EAMs with n-doped Si, as shown at the beginning of this chapter (Fig. 4.9). At reverse bias graphene's neutrality point is approached, therefore the total resistance of graphene increases, and

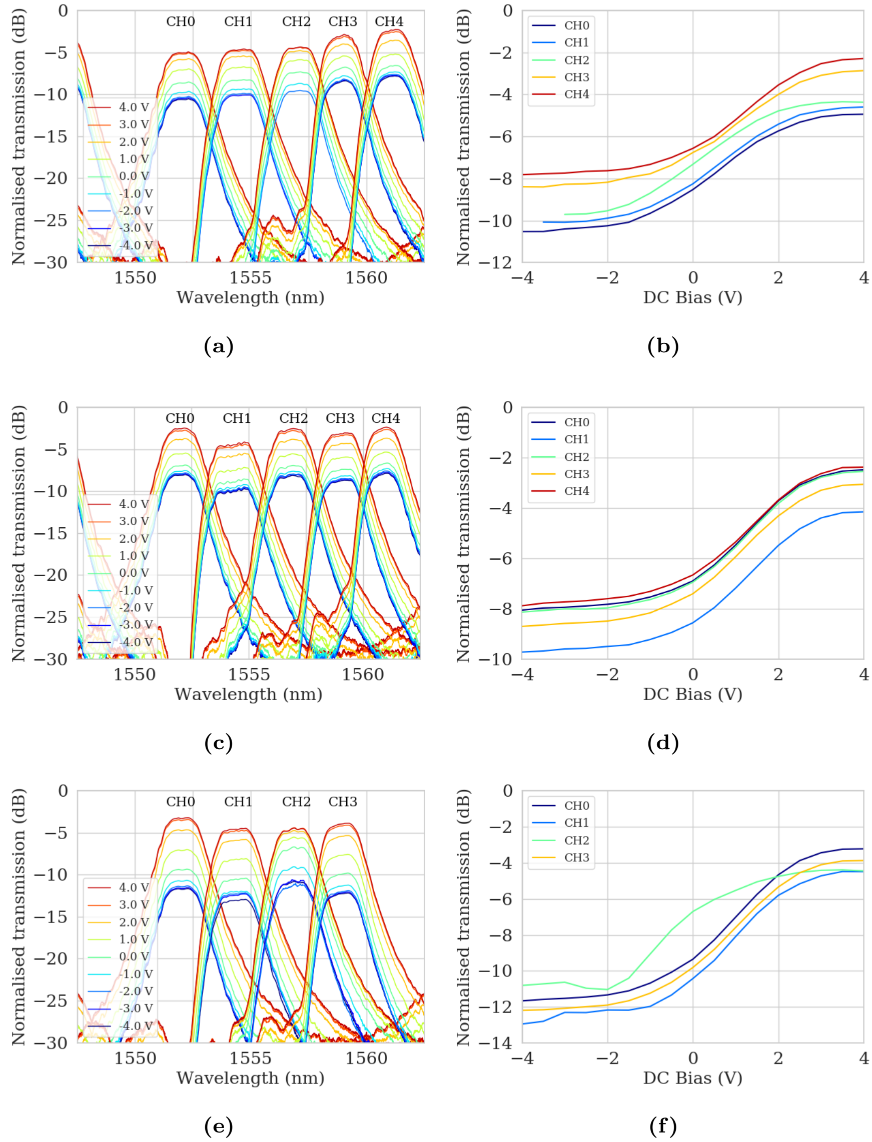



**Figure 4.18:** Left column: transmission spectra on (a) WDM1, (c) WDM2 and (e) WDM3 normalised to a reference waveguide without graphene. The voltage is varied from -4 V to 4 V on each graphene EAM, resulting in the tuning of the transmission on each channel. Right column: normalised transmission as a function of DC voltage bias, measured on (b) WDM1, (d) WDM2 and (f) WDM3. The transmission is extracted at the peak wavelength of each channel.

**Table 4.7:** Total resistance ($R_{tot}$) and GOS capacitance ($C_{GOS}$) extracted from $S_{11}$ parameter fitting, simulated (from the fitted parameters in column 1 and 2) and measured $f_{3dB}$ at 0 V. The values are averaged over 5 channels. Due to the longer $L_{device}$, WDM3 exhibits higher RC constant, and therefore lower $f_{3dB}$.

| | $L_{device}$ (μm) | $R_{tot}$ (Ω) | $C_{GOS}$ (fF) | $f_{3dB}$ (GHz) at 0 V | |
|---|---|---|---|---|---|
| | | | | Simulated | Measured |
| **WDM1** | 100 | 78 ± 5 | 112.6 ± 0.5 | 10.1 ± 0.5 | 9.5 ± 0.7 |
| **WDM2** | 100 | 65 ± 5 | 134.7 ± 0.5 | 9.5 ± 0.5 | 9.3 ± 0.1 |
| **WDM3** | 150 | 49 ± 5 | 206.6 ± 0.5 | 7.0 ± 0.5 | 7.1 ± 0.3 |

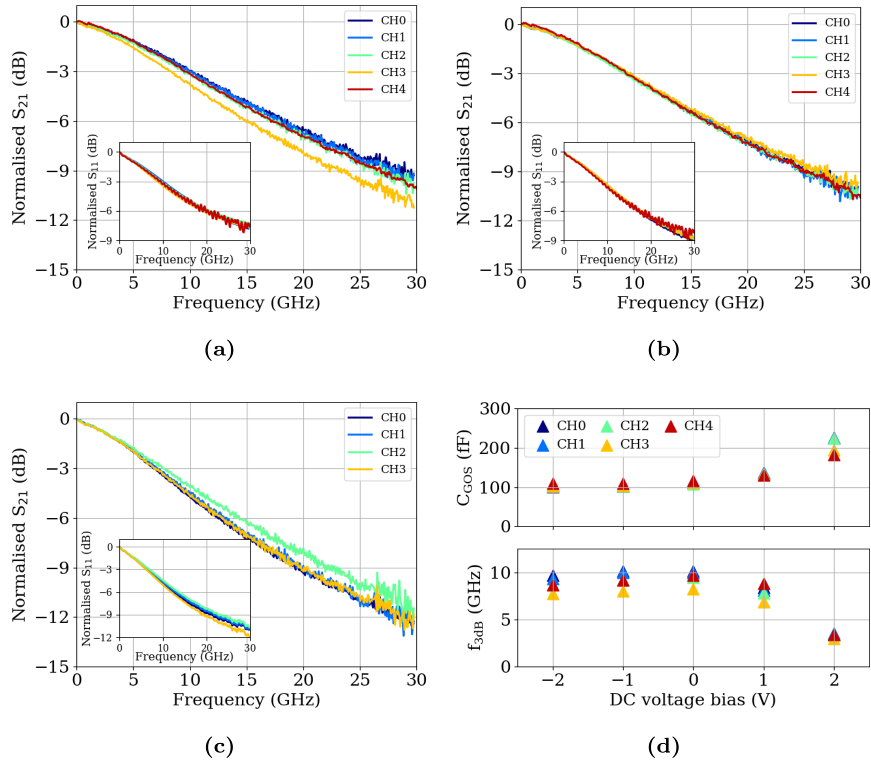



**Figure 4.19:** (a, b, c) Electro-optical $S_{21}$ (inset: $S_{11}$) frequency response measured at 0 V DC bias on WDM1, WDM2 and WDM3 respectively. The response is uniform across the 5 channels. (d) GOS capacitance and 3dB bandwidth of WDM1 as a function of DC bias. The GOS capacitance increases at forward bias, causing a drop in 3dB bandwidth. The ideal operating region is therefore at 0 V or low reverse bias.

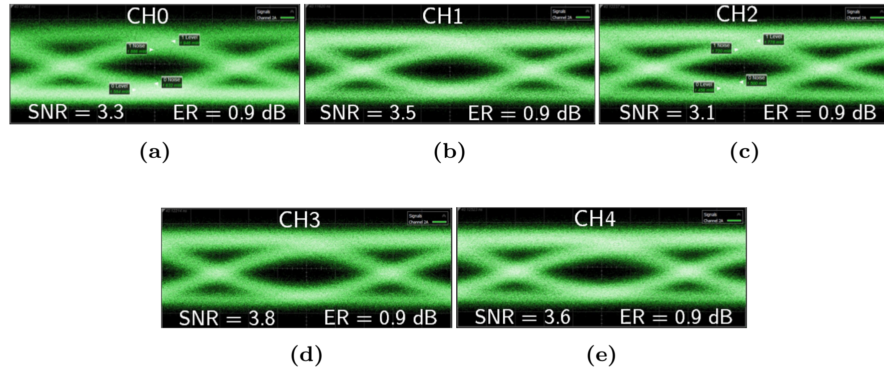



**Figure 4.20:** Eye diagrams measured at 25 Gbit/s on WDM2 at 2.5 $V_{pp}$ and -1.2 V DC bias. The performance is uniform across the 5 channels. The dynamic extinction ratio is limited by the low modal overlap with graphene when using TE-polarised light.

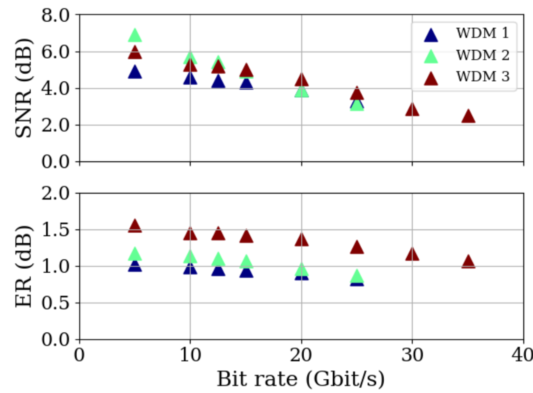
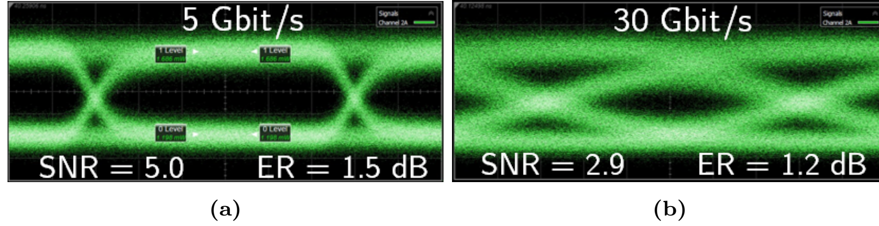



**Figure 4.21:** SNR and dynamic ER as a function of bit rate. The SNR is higher than 3.0 up to 25 Gbit/s for all the WDM transmitters. The ER for WDM3 is higher than 1 dB up to 30 Gbit/s, due to the longer device length.

the 3dB bandwidth decreases slightly. At forward bias the GOS capacitor with n-doped Si enters the accumulation region, characterised by a drastic increase in the capacitance (Fig. 4.19d), causing a drop in the 3dB bandwidth. Average 3dB bandwidths of 9.5 ± 0.7 GHz, 9.3 ± 0.1 GHz and 7.1 ± 0.3 GHz were recorded respectively for WDM1, WDM2 and WDM3 at 0 V DC bias. The response decreases as the waveguide width and the graphene length increase, due to the higher RC constant (Table 4.7).

Eye diagrams were measured at the peak wavelength of each channel using $2^7$-1 PRBS at 2.5 $V_{pp}$ with a 50 Ω terminated probe. The applied DC bias is different for each channel because of small variations in graphene doping,




(a) (b)

**Figure 4.22:** Eye diagrams measured at 5 Gbit/s (a) and 30 Gbit/s (b) on CH2 of WDM3 at 2.5 $V_{pp}$ and -1.2 V DC bias.

with an average value of -1.2 ± 0.2 V. Open and symmetrical eye diagrams were generated from 5 Gb/s to 25 Gb/s for all the channels, thus allowing to transmit data up to 5 x 25 Gb/s on each WDM transmitter. Eye diagrams measured on the 5 channels of WDM2 are shown in Fig. 4.20. The dynamic ER and signal-to-noise ratio (SNR) of the 5 channels on each WDM transmitter are reported in Fig. 4.21 as a function of bit rate. The SNR is higher than 3.0 up to 25 Gbit/s for all the WDM transmitters. WDM3 exhibits a 45% higher ER, due to the longer graphene waveguide coverage, thus allowing to obtain open eye diagrams up to 30 Gb/s with an SNR of 2.9 and a dynamic ER of 1.2 dB (Fig. 4.22b). This shows that the primary limiting factor of these devices is the extinction ratio, followed by the frequency response. The dynamic energy consumption ($E_{bit} = CV^2/4$) of a single graphene EAM at -1 V is estimated to be ∼163 fJ for WDM1, ∼195 fJ for WDM2 and ∼308 fJ for WDM3. These values are, to the best of our knowledge, the lowest reported for graphene-based modulators.

As discussed in section 4.2, to further improve the high-speed performance of these devices, p-type Si doping can be employed. A two-fold improvement in ER can be achieved by designing graphene-based WDM transmitters for TM- instead of TE-polarised light. Furthermore, an improvement of the graphene quality, and therefore of the carrier mobility of graphene, will allow to increase the ER for fixed $V_{pp}$, reduce the graphene resistance, and reduce the IL of the graphene EAMs.

## 4.4 Conclusions

In this chapter, we analysed the DC and high-speed performance of SLG EAMs. We compared results obtained on three samples, fabricated with p-doped graphene and Si waveguides with different type and level of Si doping. By means of a theoretical model, we discussed the influence of the waveguide doping on the total parasitic resistance and capacitance of SLG EAMs and we compared it to experimental results obtained from the three samples. In addition, we compared results obtained with TE-polarised light and TM-polarised light, and we demonstrated high-speed operation in the C-band and in the O-band, for

a total wavelength range of 140 nm. The best static and high speed performance was obtained using p-doped Si waveguides in combination with p-doped graphene. We obtained open eye diagrams up to 50 Gbit/s on a 75 µm-long C-band TM SLG EAM, which is to date the fastest demonstrated single-layer graphene modulator.

Furthermore, we integrated SLG EAMs with n-doped Si waveguides into three five-channel WDM transmitters and we demonstrated uniform device performance across fifteen SLG EAMs. We measured open eye diagrams up to 25 Gbit/s in the C-band on each channel of the three WDM transmitters, thus showing potential for data transmission at 5 x 25 Gbit/s.

CHAPTER 5

# DOUBLE-LAYER GRAPHENE ELECTRO-ABSORPTION MODULATORS

In the previous chapter, we have seen that one of the main limitations of single-layer graphene (SLG) electro-absorption modulators (EAMs) is given by the low extinction ratio. In this chapter we propose a solution to this issue, represented by double-layer graphene (DLG) EAMs. First, we discuss advantages and disadvantages of using two graphene layers instead of one. We explain the modeling technique for DLG electro-absorption modulators and compare the simulation results with the ones for SLG modulators. In the second part of the chapter, we show experimental results obtained on DLG EAMs with different materials used as oxide spacers between the two graphene layers. Finally, we conclude with an outlook on how to optimise the performance of these devices. Some of the measurements in section 5.3.2 and the simulations shown in section 5.4 were performed by Owen Marshall.

## 5.1 Why double-layer graphene?

As suggested by the name, double-layer graphene electro-absorption modulators are based on two graphene layers on top of the waveguide (Fig. 5.1). The gate voltage to operate the device is applied across these two layers, which are separated by a dielectric and thus form a graphene-oxide-graphene (GOG) capacitor. The waveguide is an entirely passive component, therefore DLG EAMs can be integrated in any platform, independent of the material used for the waveguide (Si, SiN, ...). The presence of two graphene layers guarantees stronger electro-absorption effect compared to SLG EAMs. This allows to build smaller devices, reducing the footprint and the device capacitance.

Disadvantages are represented by the need of a double graphene transfer

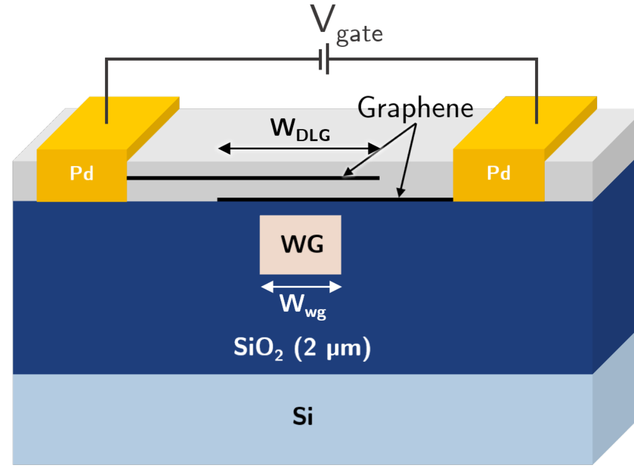



**Figure 5.1:** Schematic cross section of a DLG EAM. The two graphene layers, separated by a dielectric layer, form a graphene-oxide-graphene capacitor.

followed by dielectric deposition, neither of which is trivial. The method used for dielectric deposition and the type of dielectric affect graphene properties, as we have seen in chapter 3. Contact formation is performed by etching through the dielectric to create a side contact to the two graphene layers. As seen before, this step is also vulnerable to processing failures.

## 5.2 Modeling of double-layer graphene EAMs

Simulating and modeling double-layer graphene (DLG) electro absorption modulators (EAMs) is analogous to their single-layer graphene counterpart. The main difference between the two is the presence of two graphene layers instead of one (Fig. 5.1). As the Si waveguide is a passive component, it does not contribute to the RC constant of the device. This makes modeling the GOG capacitance ($C_{GOG}$) far easier than the GOS capacitance, as the only contributions are given by graphene's quantum capacitance ($C_q$) and the oxide capacitance ($C_{ox}$):

$$\frac{1}{C_{GOG}} = \frac{2}{C_q} + \frac{1}{C_{ox}} \tag{5.1}$$

The factor 2 indicates the presence of two graphene layers. $C_q$ and $C_{ox}$ are calculated with the methods explained in chapter 4, section 4.1.3. Fig. 5.2 shows the calculated $C_{GOG}$ as a function of graphene Fermi level $\mu$ and Fermi level shift $\Delta\mu$ (as defined in Eq. 4.6). When graphene's impurity carrier density $n*$ is 0, $C_{GOG}$ is zero for $\mu = 0$. When $n* > 0$, the minimum of the capacitance increases due to higher graphene's conductance, as already analysed in chapter

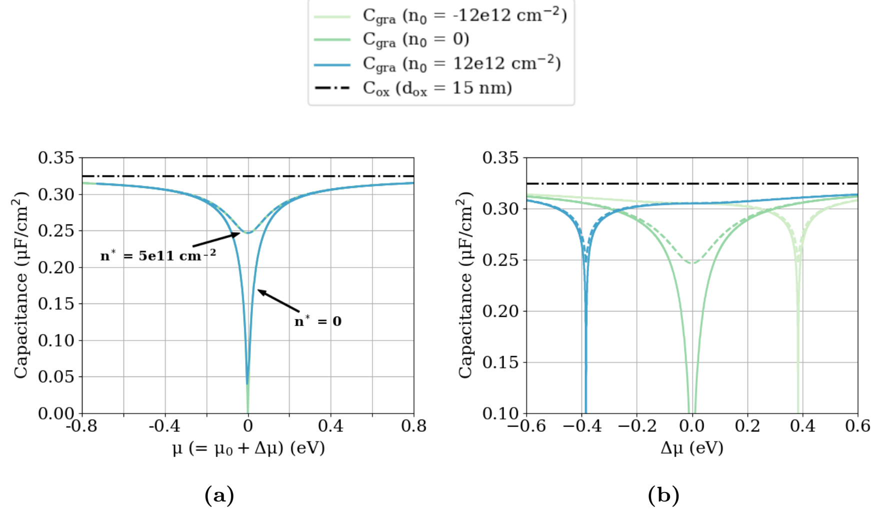



**Figure 5.2:** (a) Calculated graphene-oxide-graphene capacitance (for 15 nm $Al_2O_3$) as a function of graphene's Fermi level $\mu$, for n-doped ($n_0 = -12e12$ cm$^{-2}$), neutral ($n_0 = 0$) and p-doped ($n_0 = 12e12$ cm$^{-2}$) graphene. The full lines are calculated for $n^* = 0$ and the dotted lines for $n^* = 5e11$ cm$^{-2}$. (b) Same as (a), but the capacitance is plotted as a function of Fermi level shift ($\Delta\mu = \mu - \mu_0$).

4 (see Fig. 4.6). In this case, the total capacitance is minimally affected by $C_q$ and its main contribution is given by $C_{ox}$. Therefore, $C_{GOG}$ can be optimised by increasing the oxide spacer thickness or by using a dielectric with lower permittivity in order to reduce $C_{ox}$. An additional decrease in capacitance can be obtained with a smaller capacitor area by reducing the overlap between the two graphene layers. A detailed discussion about device optimisation will be given in section 5.4.

The contributions to the total device resistance $R_{tot}$ come from the sheet and contact resistance ($R_{gra}$ and $R_{graC}$) of the two graphene layers. The same considerations about graphene resistance made for SLG EAMs are also valid here, therefore an improvement in graphene quality is essential to reduce $R_{tot}$.

### 5.2.1 Static performance: SLG vs DLG

The equation governing the relation between the applied voltage and the position of graphene's Fermi level seen for SLG EAMs (Eq. 4.5) is valid also for DLG EAMs, with the difference that $C_{GOS}$ is replaced by $C_{GOG}$:

$$V_g = \frac{q\,(n_0 + n_s)}{C_{GOG}} = \frac{q}{\pi\,(\hbar v_F)^2}\frac{\mu^2}{C_{GOG}} \tag{5.2}$$

As for SLG EAMs, the static electro-optical behaviour of DLG EAMs is

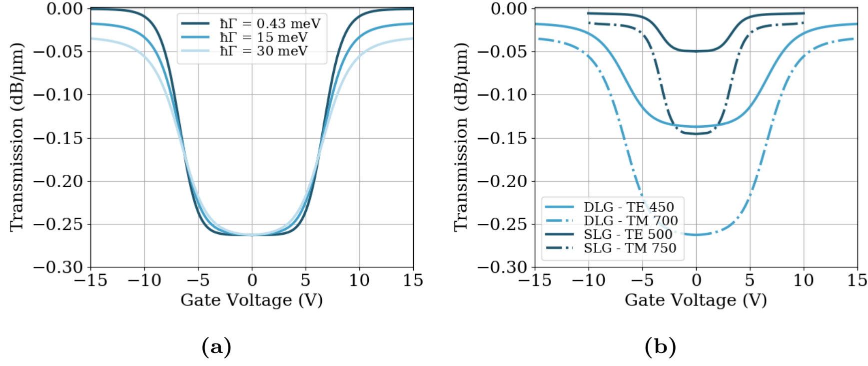



**Figure 5.3:** (a) Simulated transmission as a function of gate voltage at $\lambda = 1560$ nm of a TM ($W_{wg} = 700$ nm) DLG EAM with 15 nm $Al_2O_3$ spacer with scattering rates $\hbar\Gamma = 0.43$, 15, 30 meV. (b) Comparison of transmission between a SLG EAM and a DLG EAM, for TE and TM polarised light ($\hbar\Gamma = 30$ meV).

also affected by graphene's scattering rate ($\hbar\Gamma$). Fig. 5.3a shows the modeled transmission as a function of applied bias for a DLG EAM with 15 nm $Al_2O_3$ spacer, a 700 nm-wide waveguide and TM-polarised light, for various values of $\hbar\Gamma$ (0.43, 15 and 30 meV) and $n_0 = 0$ (neutral graphene). A lower scattering rate, meaning higher graphene quality, results in higher extinction ratio for a given $V_{pp}$ because graphene can reach full transparency. For example, a 75 µm-long DLG EAM with TM-polarised light would show 2.25 dB higher extinction ratio for $\hbar\Gamma = 0.43$ eV compared to $\hbar\Gamma = 30$ eV. The difference amounts to 1.3 dB for TE-polarised light and a waveguide width of 450 nm.

Fig. 5.3b shows a comparison between SLG EAMs and DLG EAMs for both TE and TM polarisation for $n_0 = 0$ (neutral graphene). The SLG EAM is simulated with 5 nm-thick $SiO_2$ between graphene and the Si waveguide (as in Fig. 4.3c). The DLG EAM is simulated with 15 nm-thick $Al_2O_3$ between the graphene layers. Due to the two graphene layers, DLG EAMs show higher insertion loss and extinction ratio, for both polarisation modes. For TE polarisation, the maximum absorption is $\sim 0.14$ dB/µm, while for TM polarisation it reaches almost 0.26 dB/µm. It is important to notice that in case of DLG EAMs, the thickness of the spacer between the two graphene layers has an influence on the device absorption. If the oxide is thicker, the overlap between the optical mode and the top graphene layer is less and, as a consequence, the absorption is lower. For example, with a 30 nm-thick $Al_2O_3$, the absorption for TE polarisation reduces to 0.12 dB/µm, while for TM polarisation no noticeable difference is present due to the TM mode being less confined in the waveguide.

## 5.3 Experimental results

In this section, after introducing the device design and fabrication, we present and analyse optical and electro-optical measurements performed on DLG EAMs. First we use $Al_2O_3$ as spacer between the two graphene layers. Then, in an attempt to improve the device performance, we test another dielectric, $HfO_2$, deposited with the aid of a Si seeding layer [141].

### 5.3.1 Design and fabrication

The DLG EAMs fabricated for our experiments are based on 220 nm SOI waveguides. The fabrication of these graphene devices was performed by lab technicians at imec. Graphene used to fabricate the devices presented in this chapter was grown and transferred in-house. First, the bottom CVD-grown graphene layer is transferred and shaped. After gate dielectric deposition by ALD, the top graphene layer is also transferred and shaped. A final capping dielectric is deposited before etching the dielectric for contact formation. In the first iteration, we used 30 nm-thick $Al_2O_3$ as dielectric. This choice was a result of the passivation-last experiments performed in chapter 3, where measurements performed on graphene FETs passivated with $Al_2O_3$ showed to be promising. On this sample, the two graphene contacts were processed at the same time. In the second iteration, samples were fabricated with $HfO_2$. The dielectric deposition was performed with the aid of a 0.5 nm-thick Si seeding layer, following the methods explained in chapter 3, in order to obtain a more uniform dielectric layer. Two oxide thicknesses were tested in the case of $HfO_2$, namely 6 and 10 nm. $HfO_2$ was chosen because, after some preliminary studies performed in-house on graphene electrical structures, it showed good encapsulation properties, with neutral graphene, low hysteresis and short-term stability. On these samples, the two graphene contacts were fabricated in two separate steps in order to avoid over-etching of the dielectric when contacting the top graphene layer. On all samples, etching the dielectric layer causes the removal of the graphene layer from the contact area, leading to an edge contact between the metal and graphene. Edge contacts to graphene are expected to lead to lower contact resistance due to the stronger bond between graphene's $\sigma$ orbitals compared to the $\pi$ orbitals (top contacts) [135, 167–170]. The full flow used to fabricate these samples is described in appendix A, section A.3.

Devices with graphene length spacing from 25 µm to 150 µm were fabricated simultaneously on the same sample. Waveguides with a width of 450 nm were used for the C-band TE-based devices, while a width of 500 or 700 nm was chosen for the C-band TM devices. O-band TM devices with a waveguide width of 400 nm were also fabricated and characterised. Graphene contacts are placed at 2 µm from the waveguide and the overlap between the two graphene layers on top of the waveguide ($W_{DLG}$) is 2.7 µm. All the measurements performed in this section were carried out with 6 dBm laser power (measured at the laser

output), except for S-parameters which were performed with 12 dBm laser power. If a different laser power was used, we specify it in the text.

### 5.3.2 $Al_2O_3$ spacer

The first sample we characterised was fabricated using a 30 nm-thick $Al_2O_3$ spacer between the two graphene layers. We first performed biased fiber-to-fiber transmission measurements on the C-band TE and TM EAMs, by sweeping the wavelength from 1510 nm to 1600 nm, while applying a DC bias ranging from -20 V to 20 V. Fig. 5.4a shows the extracted transmission as a function of DC bias for devices with length $L_{device}$ = 150 µm for both polarisations at the peak transmission wavelength of 1560 nm. Insertion losses of 9.6 dB (0.064 dB/µm) and 9.0 dB (0.060 dB/µm) are reported respectively for TE and TM polarisations, together with extinction ratios of 8.4 dB (0.06 dB/µm) and 26.0 dB (0.17 dB/µm). As expected, the TM EAM significantly outperforms the TE EAM in terms of extinction ratio, while the two devices are comparable in terms of insertion loss. This makes the TM EAM more interesting as its FOM (= ER/IL) is three times higher than the one of the TE EAM (Table 5.1). With the same measurement method, we characterised O-band TM EAMs by sweeping the wavelength from 1260 nm to 1330 nm. The extracted transmission as a function of DC bias for a 100 µm-long device is reported in Fig. 5.4b. The device exhibits 3.6 dB (0.036 dB/µm) insertion loss and 15.9 dB (0.16 dB/µm) extinction ratio for voltage swing from -12 V to 9 V, resulting in a FOM of 4.4, thus demonstrating the broadband characteristic of graphene on DLG EAMs.

To further analyse the static performance of the DLG EAMs we performed double-sweep electro-optical measurements at different voltage sweep speeds, namely 0.03 V/s and 0.1 V/s. Fig. 5.4c shows such measurement performed on a 70 µm-long C-band TE DLG EAM. To quantify the hysteresis, we extract the voltage difference between the minimum of transmission of the forward sweep and the one of the backward sweep ($\Delta V$). Both the hysteresis ($\Delta V$) and the extinction ratio show significant sweep speed-dependency, due to traps at the interface with the $Al_2O_3$. For higher sweep speed, these traps do not have time to fill, due to high trap lifetime in $Al_2O_3$ (typically of the order of ∼ms [171]).

**Table 5.1:** Summary of the main figures of merit measured on the three types of DLG EAMs fabricated with $Al_2O_3$. The FOM is calculated as ME/IL. The C-band TM DLG EAM offers the best trade-off.

| | $L_{device}$ | IL (dB/µm) | ME (dB/µm) | FOM | $f_{3dB}$ (GHz) |
|---|---|---|---|---|---|
| **C-band TE** | 150 | 0.064 | 0.06 | 0.9 | $< 1$ |
| **C-band TM** | 150 | 0.060 | 0.16 | 2.9 | 2.2 ($L_{device}$ = 50 µm) |
| **O-band TM** | 100 | 0.036 | 0.16 | 4.4 | - |

More electrons contribute to shifting graphene's Fermi level, leading to higher extinction ratio and lower hysteresis ($ER = 6.8$ dB, $\Delta V = 11$ V). When the sweep speed is reduced, traps are filled and emptied, causing reduced extinction ratio and higher hysteresis ($ER = 5.2$ dB, $\Delta V = 12$ V).

To conclude, we measured the high-speed performance of a C-band TM DLG EAM. The electro-optical $S_{21}$ frequency response was measured between 100 MHz and 20 GHz at -15 V DC bias with a vector network analyser, using -8 dBm RF power and 12 dBm laser input power. The best 3 dB frequency response ($f_{3dB}$), extracted on a 50 µm-long EAM, is 2.2 GHz (Fig. 5.4d). To understand the main factors limiting the $f_{3dB}$, we performed a fitting of the $S_{11}$ frequency response. We extracted values of $R_{tot}$ and $C_{GOS}$ of 262 Ω and 199 fF, respectively. The high resistance is linked to low quality graphene, especially the upper graphene layer. This is confirmed by electrical measurements per-

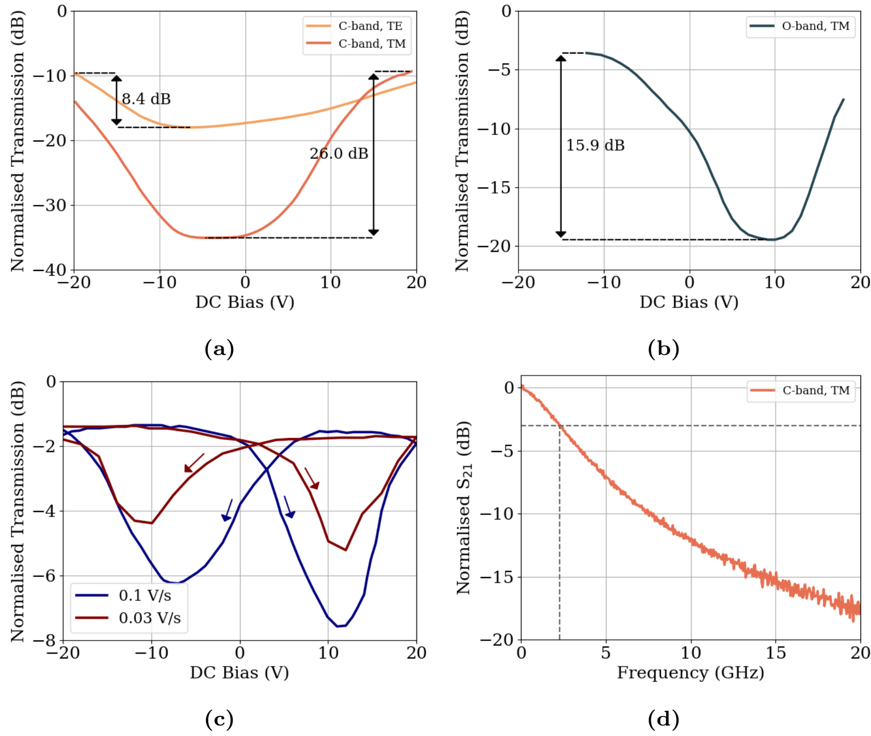



**Figure 5.4:** $Al_2O_3$ spacer. (a) Transmission, normalised to the reference waveguide, as a function of applied DC bias, measured on C-band TE and TM DLG EAMs with $L_{device} = 150$ µm. (b) Same as (a) for a 100 µm-long O-band TM DLG EAM. (c) Sweep-speed dependent hysteresis on a C-band TE DLG EAM with $L_{device} = 70$ µm. (d) $S_{21}$ parameters measured on a 50 µm-long TM C-band DLG EAM at -15 V DC bias.

formed on graphene TLM structures fabricated on the same chip, that allow to extract the sheet and contact resistance of the two layers separately. The best values of $R_{gra}$ and $R_{graC}$ measured on the upper graphene layer are 460 $\Omega/\square$ and 1100 $\Omega$ µm, while on the lower graphene layer we extracted best values of 530 $\Omega/\square$ and 180 $\Omega$ µm. The latter value of $R_{graC}$ is lower than the average $R_{graC}$ extracted from Al2O3-passivated samples fabricated with top contacts and the passivation-last approach (Table 3.2).

In conclusion, two main problems need to be resolved going forward, the device hysteresis and the high total resistance. Devices which offer stable performance at different sweep speeds are important to obtain stable high-speed performance at a fixed DC bias. Gaining better control over the quality of the contact between the metal and the graphene layer is also essential to reduce the total resistance and improve the high speed performance.

### 5.3.3 $HfO_2$ spacer

To improve the hysteretic behaviour we fabricated DLG EAMs with $HfO_2$ as oxide spacer between the two graphene layers. High-$\kappa$ dielectrics are expected to better screen the charged impurities located in proximity of the graphene layer, leading to reduced hysteresis [141]. $HfO_2$ was deposited using 0.5 nm-thick Si as seeding layer, which as seen in chapter 3 helps achieving higher quality oxide and reducing the hysteretic behaviour [143, 172]. Two samples were fabricated using two different oxide thicknesses, 6 nm and 10 nm. The thinner oxide allows to operate the device at lower $V_{pp}$ but leads to higher device capacitance. Waveguide widths of 450 nm and 500 nm were used to characterise devices with TE- and TM-polarised light, respectively.

Fig. 5.5a and Fig. 5.5b show the extracted extinction ratio as function of device length for C-band TE and TM mode EAMs for 6 nm- and 10 nm-thick $HfO_2$, respectively. TE devices were measured up to 100 µm length and TM devices up to 50 µm length, due to high insertion loss for longer graphene coverage. The difference in modulation efficiency between TE and TM mode devices on both samples is less than expected, with TM mode devices reaching only $\sim$ 0.11-0.12 dB/µm and TE mode devices reaching $\sim$ 0.09-0.10 dB/µm. Nevertheless, the extinction ratio scales linearly with the device length. For $L_{device}$ = 50 µm, the ER reaches 4.1 dB for TE polarisation and 6.0 dB for TM polarisation for $t_{ox}$ = 6 nm, and 4.2 and 5.5 dB respectively for $t_{ox}$ = 10 nm. The lower-than-expected extinction ratio can be explained by poor contact between the metal and graphene, leading to high contact resistance and reduced electric field across the GOG capacitor.

As done for the $Al_2O_3$ sample, we performed double-sweep electro-optical measurements at different voltage sweep speeds, ranging from 0.02 V/s to 0.25 V/s, to analyse the hysteretic behaviour of these devices. Fig. 5.6a shows such measurement performed on a DLG EAM with 6 nm-thick $HfO_2$. Hysteretic behaviour is still present, but the extinction ratio and the hysteresis do not show a sweep speed-dependency, indicating increased quality of the interface

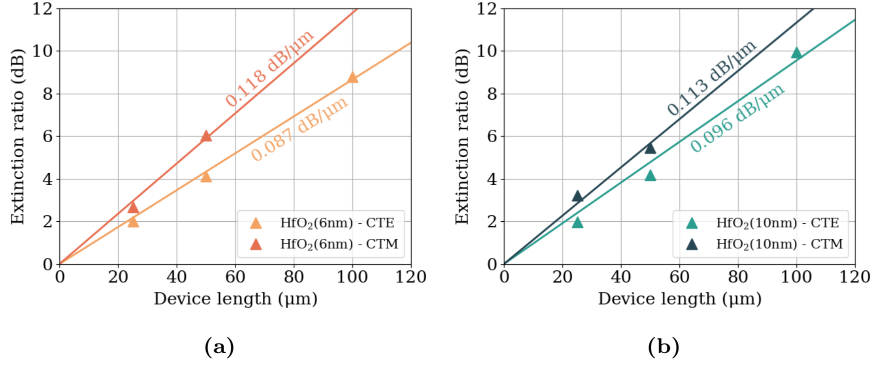



**Figure 5.5:** Comparison of measured extinction ratio between TE and TM mode on C-band DLG EAMs with (a) 6 nm-thick $HfO_2$ and (b) 10 nm-thick $HfO_2$.

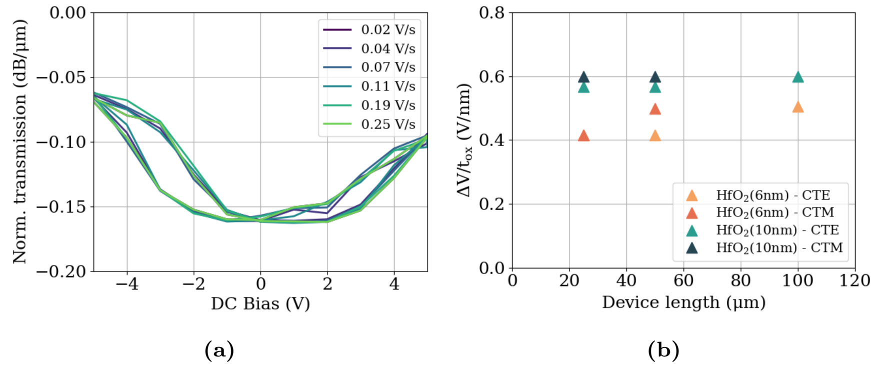
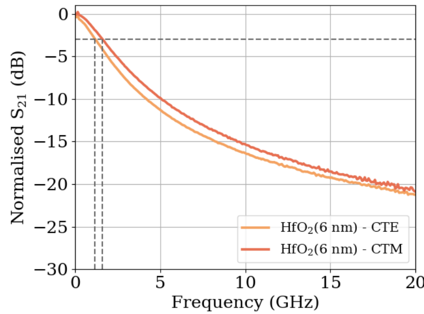



**Figure 5.6:** (a) Double voltage sweep measurements performed on a TE mode DLG EAM with 6 nm-thick $HfO_2$, showing no increase in the hysteresis when the sweep speed is decreased. (b) Values of hysteresis ($\Delta VS$) normalised to the oxide thickness ($t_{ox}$) for TE and TM mode DLG EAMs with 6 nm- and 10 nm-thick $HfO_2$.

between graphene and the oxide spacer compared to the $Al_2O_3$ sample. Fig. 5.6b summarises the extracted values of hysteresis, normalised to the oxide thickness ($\Delta V/t_{ox}$) to allow comparison, for the two samples and for different device lengths. The hysteresis is slightly lower for the sample with 6 nm-thick $HfO_2$ and does not depend on device length.

The electro-optical $S_{21}$ frequency response was measured on C-band TE and TM EAMs on both samples between 100 MHz and 20 GHz at 4 V ($t_{ox}$ = 6 nm) and 6 V ($t_{ox}$ = 10 nm) DC bias with a vector network analyser, using -8 dBm RF power and a 50 Ω load resistor. The best 3 dB frequency responses ($f_{3dB}$), extracted from 25 μm-long EAMs, are 1.1 GHz and 1.6 GHz for TE and TM on the $HfO_2$(6 nm) sample (Fig. 5.7) and 0.5 GHz for TE on the $HfO_2$(10 nm) sample. Once again, we performed a fitting of the $S_{11}$ frequency response




**(a)**

**Figure 5.7:** $S_{21}$ frequency response measured on 25 µm-long C-band DLG EAMs with 6 nm-thick $HfO_2$ at 4 V DC bias with (a) TE mode waveguide and (b) TM mode waveguide.

to understand the limiting factors affecting the low $f_{3dB}$. For the $HfO_2$(6 nm) sample we extracted values of $R_{tot}$ and $C_{GOS}$ of 360 Ω and 320 fF, respectively. The device resistance is higher than the one extracted from the $Al_2O_3$ sample, which might be related to the processing not being very well optimised, leading to very high graphene contact and sheet resistance. This hypothesis is confirmed by the characterisation of graphene electrical test structures, which delivered very inconsistent measurements and could not be properly analysed. The device capacitance is also higher than the $Al_2O_3$ sample. This is expected because $HfO_2$ has a higher dielectric constant compared to $Al_2O_3$ [173] and because the $HfO_2$ used for these samples is much thinner (6 nm) compared to $Al_2O_3$ (30 nm).

In conclusion, the experiments performed using $HfO_2$ as spacer have shown an improvement of the hysteretic behaviour, but have fallen below expectations in terms of static and high-speed performance. The main issue, as encountered with the $Al_2O_3$ sample, is the poor control over the quality of the contact between the metal and the graphene layer, which leads to high device resistance. In addition, a more systematic study of the effect of $HfO_2$ deposition on graphene should be carried out to ensure graphene's properties are retained after encapsulation. This study should include a sweep of parameters used for $HfO_2$ deposition to identify the best ones for this type of application.

## 5.4 Optimisation of DLG EAMs and outlook

The experiments performed on DLG EAMs show that, while some initial results are promising, much work is still needed to improve their performance, both static and high-speed. A systematic study is needed to identify the best parameters to optimise the device performance. At the same time, improvements

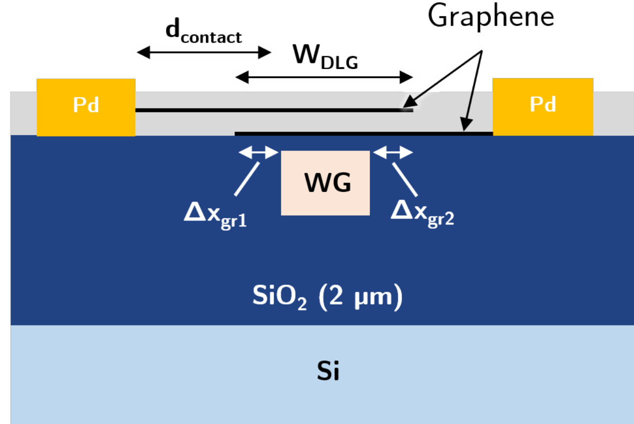



**Figure 5.8:** Cross section of a DLG EAM with the parameters used to perform the device optimisation.

in the fabrication process are necessary.

As mentioned before, the high-speed operation of this type of device is limited by its RC constant. The capacitance can be reduced by decreasing the overlap ($W_{DLG}$) between the two graphene layers on top of the waveguide. If the overlap is reduced, the device performance becomes more sensitive to misalignment that can happen during lithography, which can be overcome by using e-beam lithography. As a consequence, a study of the effects of misalignment of the two graphene layers compared to the waveguide edge is necessary. We identify two parameters, $\Delta x_{gr1}$ and $\Delta x_{gr2}$, which represent the distance from the waveguide edge of each of the two graphene layers (see Fig. 5.8). Sweeping these two parameters allows to simultaneously study the effect of the overlap between the two graphene layers and the sensitivity of the alignment between the graphene layers and the waveguide. For each value of $\Delta x_{gr1}$ and $\Delta x_{gr2}$, a mode simulation is performed to extract the corresponding IL and ER. Fig. 5.9 shows the results of such study performed for TM-polarised light at 1550 nm and a waveguide width of 700 nm. The goal is to reduce the overlap of the two graphene layers as much as possible, while maximising the ER and minimising the IL. If the graphene layers are aligned (centered) to the waveguide, the overlap can be reduced to 900 nm while achieving an ER of 0.19 dB/µm and an IL of 0.07 dB/µm. In terms of FOM (= ER/IL) this means that a value of 2.7 can be maintained, which is 0.95 of the maximum figure of merit.

Another important parameter is the distance of the metal contacts from the waveguide edges ($d_{contact}$), as it affects the graphene resistance. The smaller $d_{contact}$, the lower the sheet resistance. However, if the contacts are too close to the waveguide, losses due to the interaction between the waveguide mode and the metal will arise. Fixing $W_{DLG}$ at 900 nm ($\Delta x_{gr1} = \Delta x_{gr2} = 100$ nm and $W_{wg} = 700$ nm), we performed a sweep of $d_{contact}$ and studied the effect

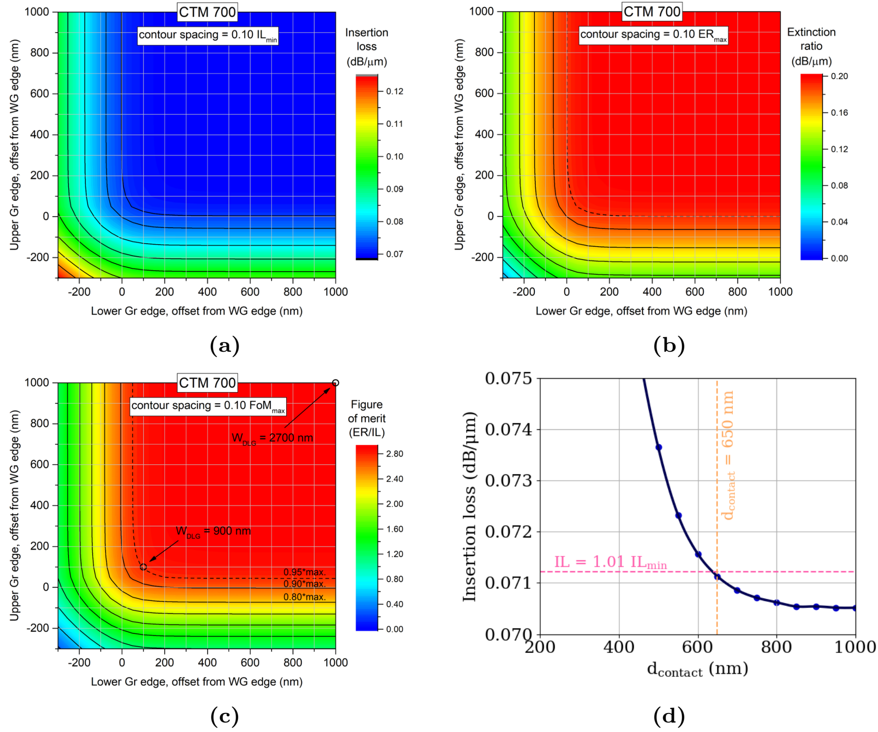



**Figure 5.9:** Contour plots showing the estimated (a) insertion loss, (b) extinction ratio and (c) figure of merit for varying $\Delta x_{gra1}$ (offset of lower graphene edge from waveguide edge) and $\Delta x_{gra2}$ (offset of upper graphene edge from waveguide edge) with TM-polarised light and $W_{wg}$ = 700 nm. (d) Variation of insertion loss as a function of $d_{contact}$.

on the device insertion loss (Fig. 5.9d). If $IL_{min}$ is the minimum achievable insertion loss, when the contacts are far away from the waveguide ($d_{contact}$ = 2 µm), we set a limit on the acceptable insertion loss increase at 1.01 $IL_{min}$ (1% increase). With this limit, we can allow a contact distance of 650 nm. The achievable 3 dB bandwidth using these two optimised parameters ($W_{DLG}$ = 900 nm and $d_{contact}$ = 650 nm) depends on several factors, such as the type of oxide, its dielectric constant, its thickness and graphene's resistance. For a TM DLG EAM with $W_{wg}$ = 700 nm, $t_{ox}$ = 30 nm, $\epsilon$ = 15 ($HfO_2$), $R_{graC}$ = 200 Ω µm, $R_{gra}$ = 200 Ω/□ and a device length of 50 µm we predict a 3 dB bandwidth of 24.1 GHz. Reducing the device length to 25 µm would allow to achieve a 3 dB bandwidth of 40.1 GHz. Improving graphene's resistance by an order of magnitude ($R_{graC}$ = 20 Ω µm, $R_{gra}$ = 20 Ω/□) would lead to an increase in 3 dB bandwidth of one order of magnitude, being graphene's resistance the only contribution to the total resistance.

The same optimisation performed for C-band TM-polarised light and $W_{wg}$

**Table 5.2:** Summary of optimised $W_{DLG}$ and $d_{contact}$ values obtained for different light polarisations and operating wavelengths.

| Waveguide | $W_{DLG}$ (nm) | $d_{contact}$ (nm) |
|---|---|---|
| CTE 450 | 750 | 500 |
| CTE 550 | 750 | 400 |
| CTM 500 | 700 | 800 |
| CTM 700 | 900 | 650 |
| OTE 400 | 700 | 400 |
| OTE 400 | 700 | 350 |
| OTM 400 | 600 | 500 |
| OTM 500 | 650 | 450 |

= 700 nm was performed for other waveguide widths and TE polarisation. In addition, O-band devices were also studied. A summary of the optimised values of $W_{DLG}$ and $d_{contact}$ is reported in Table 5.2. TE mode is better confined in the waveguide than TM mode, allowing for smaller $d_{contact}$. Mode confinement is even better at shorter wavelengths, allowing to bring $d_{contact}$ down to 350 nm for O-band TE DLG EAMs.

Due to the low error margin offered by the proposed parameters, e-beam lithography is necessary in order to successfully fabricate these devices. At the time of writing this thesis, these samples were under fabrication but not yet available for measurements.

## 5.5 Conclusions

In this chapter, we proposed the use of double-layer graphene (DLG) instead of single-layer graphene (SLG) to fabricate graphene-based EAMs. We discussed the modeling technique of this type of device, and presented a comparison of the static performance with the one of SLG EAMs. We have shown that DLG EAMs allow to achieve more than double extinction ratio compared to SLG EAMs, but suffer in insertion loss. We compared results obtained on DLG EAMs fabricated with $Al_2O_3$ and $HfO_2$ as spacer between the two graphene layers. The best static and high-speed performance was obtained on the sample with 30 nm-thick $Al_2O_3$, reaching an extinction ratio of 26 dB and a 3 dB frequency response of 2.2 GHz. Even though the high extinction ratio is comparable to results shown in literature, the 3 dB frequency response is considerably lower than the highest reported 29 GHz for a DLG EAM [111]. This sample also showed significant static hysteretic behaviour and extinction ratio variability, which were depending on the speed of the voltage sweep. Despite

the lower static and high-speed performance, the $HfO_2$ sample showed better device stability, with reduced hysteresis and no dependency of the device extinction ratio on the sweep-speed. At the end of the chapter, we presented a study of the performance optimisation of DLG EAMs, indicating the parameters that allow to obtain the best performance for C-band and O-band, TE and TM devices.

In conclusion, DLG EAMs are promising devices, but introduce a more complex fabrication flow that leads to processing failures. The result is poor control over the contact between the metal and graphene and over the quality of the graphene layer. This is visible in the very high resistance present in both types of devices. Going forward, a systematic study of the processing conditions to be used to fabricate DLG EAMs is necessary. In particular, such study should include a sweep of parameters used for oxide deposition and oxide etching, in order to identify the ones that can deliver better graphene contact and sheet resistance.

# Chapter 6

# Graphene photodetectors

In this chapter, we switch from graphene-based modulators to graphene-based photodetectors, which are equally important for integration of graphene in photonics transceivers. An introduction about photodetection mechanisms in graphene and a literature review were given in chapter 1. Here, we pick up that thread and present results obtained during the course of this thesis on different types of graphene-based photodetectors. We present a graphene photoresistor structure and photodetectors based on a graphene/Si Schottky junction. The former benefits from the same fabrication process used for graphene modulators, but suffers from very high dark current and low photocurrent. The latter introduces non-trivial difficulties to the fabrication process, as it requires a direct junction between graphene and Si. However, it allows to reduce the dark current and achieve better performance, which translates in good responsivity. We show results obtained both with TE- and TM-polarised light, with TM devices exhibiting higher responsivity. All the devices presented in this chapter were fabricated with graphene grown and transferred in-house.

## 6.1 Introduction

Photodetectors are responsible for converting light into an electrical signal. The requirements are high responsivity for low bias voltage, low dark current, high frequency response and integrability in a silicon photonics platform. As introduced in chapter 1, graphene is a zero-bandgap material, it has high carrier mobility and broadband absorption. These characteristics make graphene a great candidate to build photodetectors. The main goal of a graphene photodetector is the absorption of photons, which are responsible for the generation of electron-hole pairs, in the graphene layer. The generated electrons (or holes) need to be collected before recombination occurs. In graphene, this feat is not

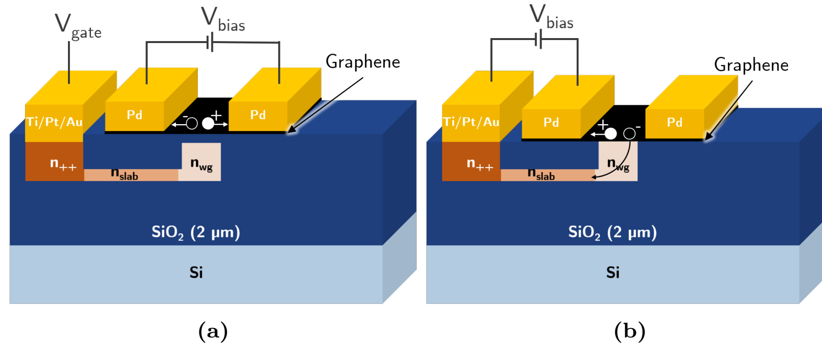



**Figure 6.1:** Schematic cross section of (a) a graphene photoresistor and (b) a graphene/Si Schottky junction.

easy, as the fast carrier dynamics cause a fast recombination rate [174, 175].

During the course of this thesis, we have tested different device concepts to build graphene-based photodetectors, each with its own advantages and disadvantages. The first device concept we explored is called *graphene photoresistor* (Fig. 6.1a) [16,17]. This device is based on a waveguide cross section analogous to the one used to build graphene modulators. Likewise, the Si waveguide is contacted through a highly doped Si slab and is covered by 5 nm-thick $SiO_2$. Graphene is transferred on top of the waveguide and two Pd contacts are fabricated on each side. When light travels through the waveguide, it is absorbed by graphene and electron-hole pairs are generated in the graphene layer. These pairs contribute to an increase in current, and therefore in a reduction of the resistance. The fabrication process of this device is the same as the one followed for graphene modulators, therefore its implementation does not introduce additional difficulties. The main disadvantage is given by the high dark current. The second device concept we explored is based on a *graphene/Si Schottky junction* [20] (Fig. 6.1b). In this configuration, the oxide on top of the Si waveguide is etched before graphene transfer, so that a junction between graphene and Si is formed. The electron-hole pairs, generated in the graphene layer when the light travels through the waveguide, are separated directly at the junction. This allows to achieve more efficient carrier collection, leading to lower carrier recombination and higher photocurrent. Another advantage of this type of device is the low current in dark state. The biggest disadvantage is represented by the complex processing. Achieving a good interface between Si and graphene is extremely important, but it is not easy to control. There is no guarantee that native oxide will not start growing during the lifetime of the sample. This low control over the interface makes it difficult to predict the final results.

In the next sections we will report results and analysis of measurements performed on these two types of graphene photodetectors.

## 6.2 Graphene photoresistor

### 6.2.1 Device concept

The name graphene photoresistor derives from the working principle of this type of device, where carrier generation causes a resistance change in the graphene layer. The SOI substrate used to fabricate this device is the same used for graphene modulators and introduced in chapter 1. Therefore, the Si waveguide is contacted through a Si slab, and three different carrier concentrations are used to define three doped regions in Si. A 5 nm-thick $SiO_2$ layer is thermally grown on top of the waveguide, and subsequently single-layer graphene is transferred. The main difference with single-layer graphene modulators lies in the graphene contacts. Here, two Pd contacts are fabricated on each side of the waveguide, at a distance of 2 µm from the waveguide edge. The full flow used to fabricate these samples is described in appendix A, section A.4.

The measurement of this device is carried out by sweeping the voltage between the two graphene contacts ($V_{bias}$) and measuring the photocurrent, while a fixed backgate voltage ($V_{gate}$) is applied on the Si contact. The measurement is repeated for values of $V_{gate}$ ranging from -4 V to 4 V, which allows to sweep the graphene Fermi level, similarly to the measurement of TLM structures explained in chapter 2. Because of the p-doped nature of graphene in most of our samples, graphene's neutrality point is reached when a positive $V_{gate}$ is applied. Therefore, at higher $V_{gate}$ the resistance will be higher and the dark current ($I_{dark}$), defined as the current measured when the light is switched off, will be lower. As $V_{gate}$ approaches 0 V and proceeds towards -4 V, the resistance will progressively decrease, causing the current to increase. When the light is switched on, for fixed $V_{bias}$ and $V_{gate}$, the current flowing between the graphene contacts will increase due to the photogeneration of electron-hole pairs in the graphene layer. This causes a decrease in graphene's sheet resistance. The net photocurrent ($I_{photo}$), defined as the difference between the current measured in light condition $I_{light}$ and the dark current $I_{dark}$, is expected to be higher closer to graphene's charge neutrality point, therefore at higher $V_{gate}$. In fact, similarly to what we have seen in single-layer graphene modulators in chapter 4, graphene's absorption is maximised closer to its neutrality point, while transparency is approached when the shift of graphene's Fermi level is higher than half of the energy of the incoming photons ($E_F > \hbar\Gamma/2$). The light-induced resistance modulation at fixed $V_{bias}$ and $V_{gate}$ is calculated using Ohm's law as

$$\Delta R = R_{light} - R_{dark} = \frac{V_{bias}}{I_{light}} - \frac{V_{bias}}{I_{dark}} \tag{6.1}$$

### 6.2.2 Experimental results

We measured a 100 µm-long graphene photoresistor with 500 nm-wide waveguide as a function of $V_{bias}$, at variable $V_{gate}$. The waveguide width was op-

**Table 6.1:** Light-induced resistance modulation for varying input laser power (set on laser) at fixed $V_{bias}$ = -1.5 V and $V_{gate}$ = 3 V.

| | **12 dBm** | **9 dBm** | **6 dBm** | **3 dBm** | **0 dBm** | **-3 dBm** |
|---|---|---|---|---|---|---|
| $R_{light}(\Omega)$ | 114.7 | 114.6 | 115.9 | 115.7 | 115.2 | 114.9 |
| $R_{dark}(\Omega)$ | 108.2 | 108.6 | 107.3 | 107.5 | 107.4 | 107.8 |
| $\Delta R(\Omega)$ | 6.5 | 5.9 | 8.6 | 8.1 | 7.8 | 7.1 |

timised for propagation of TE-polarised light. From the measurement of the dark current, we notice that the $I_{dark}$-$V_{bias}$ curve exhibits an almost-ohmic behaviour for any $V_{gate}$ (Fig. 6.2a). As expected, at higher $V_{gate}$, as graphene's Fermi level gets closer to the Dirac point located at $V_{gate} \sim 3$ V, the current decreases and the resistance increases. The dark current reaches maximum values at $V_{bias}$ = -1.5 V of -13.1 mA and -16.3 mA for $V_{gate}$ = 3 V and $V_{gate}$ = -3 V, respectively. For $V_{bias}$ ¡ -1.5 V, the dark current is expected to keep increasing. The light measurement was first performed with input laser power of 12 dBm (at fiber). The extracted photocurrent, calculated as $I_{photo} = I_{light} - I_{dark}$, is greater for higher values of $V_{gate}$ (Fig. 6.2b). At $V_{bias}$ = -1.4 V it reaches maximum and minimum values of -0.8 mA and -0.01 mA for $V_{gate}$ = 3 V and $V_{gate}$ = -3 V, respectively. The same measurement was then repeated at varying input laser power and values of the light-induced resistance modulation were extracted for each of them. Table 6.1 reports extracted values of $\Delta R$ at different input powers at fixed $V_{bias}$ = -1.5 V and $V_{gate}$ = 3 V. The light-induced resistance modulation does not significantly depend on the input power.

By comparing the graphs in Fig. 6.2, it can be seen that the increase in current induced by the photogeneration of electron-hole pairs is very small compared to the dark current of the device. For the optimal gate voltage $V_{gate}$ = 3 V, where the dark current is minimised and the photocurrent is maximised, the ratio $I_{dark}/I_{photo}$ at $V_{bias}$ = -1.5 V is $\sim$ 16.4.

### 6.2.3 Conclusions

The very high values of $I_{dark}$ mean that the power consumption of the graphene photoresistor in off-state would be extremely high, and the induced photocurrent is too small, causing low photodetector sensitivity. For this reason, while this device is an interesting playground to study graphene's response to light absorption in different bias conditions, it is not suitable to be used for applications in telecommunications.

To improve the performance of this type of photodetector, first of all the graphene metal contacts need to be brought closer to the waveguide in order to prevent carrier recombination in the graphene layer. In fact, it has been shown that photogenerated carriers only exist in narrow regions of a few hundreds of nanometers before recombining [26]. Such a device needs to be fabricated

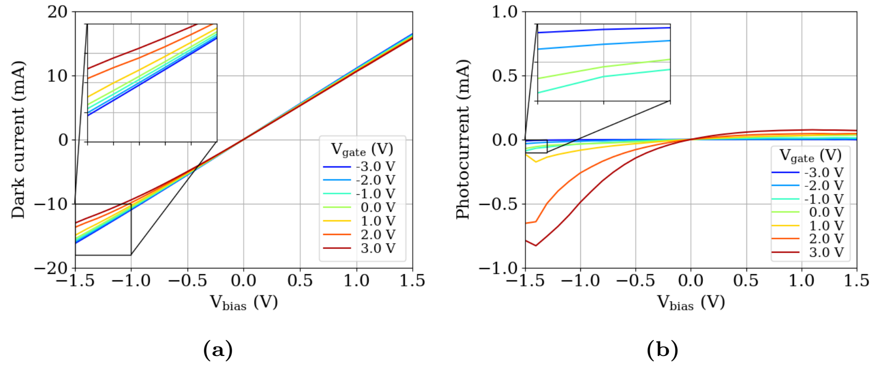


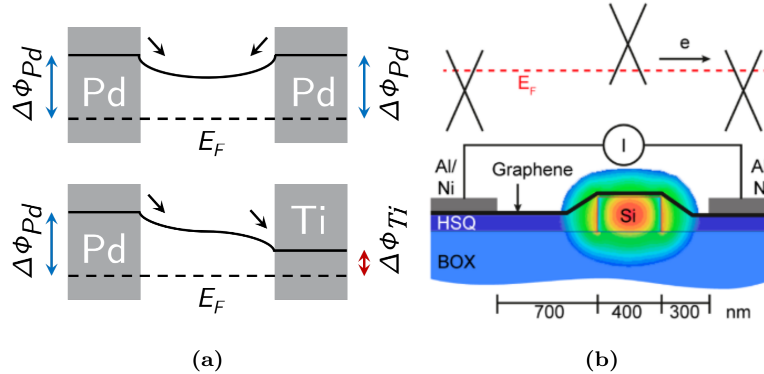

**Figure 6.2:** (a) Dark current and (b) photocurrent ($I_{light} - I_{dark}$) as a function of $V_{bias}$ (as defined in Fig. 6.1a) for varying $V_{gate}$ measured on a graphene photoresistor with $L_{device}$ = 100 µm at 12 dBm laser input power.

with electron beam lithography, as the spacing between the metal contacts and the waveguide would be too small to be controlled with optical lithography. Once the contacts are brought closer to the waveguide, different metals for the two graphene contacts can be implemented [26]. This device concept results in an asymmetric band structure due to the difference in work function between the two metal contacts to create a net positive photocurrent. A schematic band structure using Pd and Ti is shown in Fig. 6.3a (adapted from [26]). An asymmetric band structure can also be achieved by placing the graphene contacts asymmetrically on the two sides of the waveguide (Fig. 6.3b) [16, 19]. In this case, one of the two contacts is close enough to the waveguide to interact with the mode, while the other one is further away. This creates an asymmetry in the generated photocurrent, where the current in one direction is greater than in the other, allowing to achieve a positive net photocurrent.

## 6.3 Photodetectors based on a graphene/Si Schottky junction

### 6.3.1 Device concept

An alternative to the more standard graphene photoresistor is given by photodetectors based on a graphene/Si Schottky junction (Fig. 6.1b). The device is based on a SOI substrate as all the devices discussed so far. The waveguide doping used for our experiments is in the range of $10^{18}$ cm$^{-3}$. Before graphene transfer, the thermal oxide layer covering the waveguide is etched through a BHF step. As a consequence, a graphene/Si junction is created. Both Si and graphene are then contacted using a Ti/Pt/Au contact stack for Si and Pd for graphene. Two contacts are placed on graphene, as the photomask used for graphene photoresistors is used to fabricate also these devices (Fig. 6.1b). How-




**(a)** **(b)**

**Figure 6.3:** (a) Graphene band profile comparing the case with Pd-Pd contacts and Pd-Ti contacts. Adapted from [26]. (b) Graphene photodetector integrated on a silicon waveguide with asymmetric contact configuration. Taken from [19].

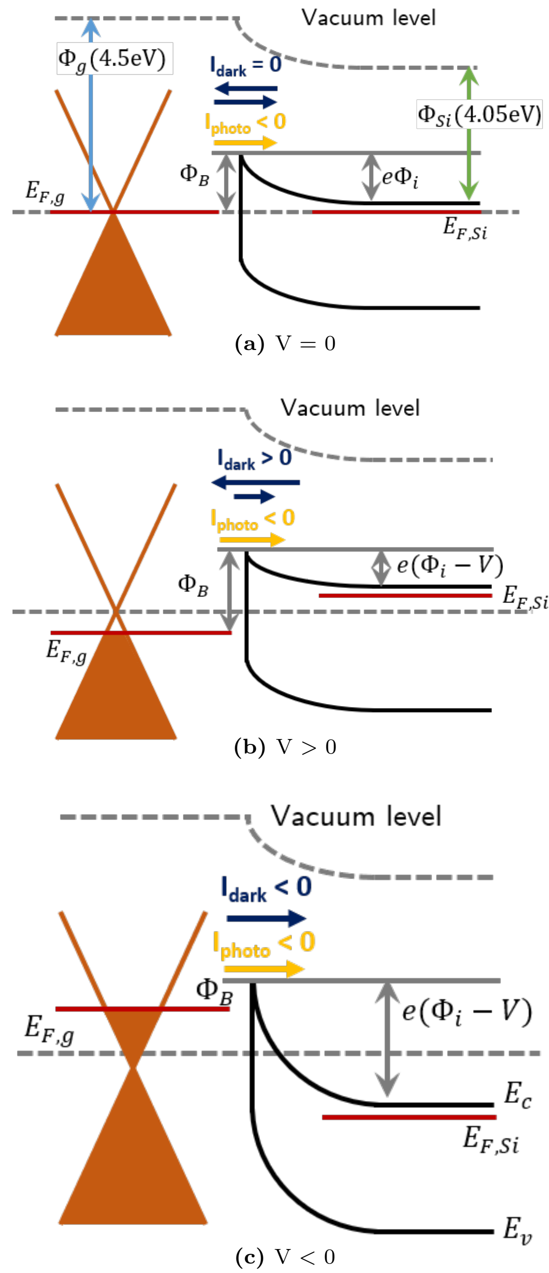
ever, only one contact is biased during measurements. Both graphene contacts are placed at a distance of 2 µm from the waveguide. The internal photoemission process takes place where the evanescent mode of the waveguide interacts with the graphene layer, close to the Schottky interface. Biasing the junction allows to separate the electron-hole pairs directly at the point where they are generated, reducing carrier recombination. Another advantage brought by the Schottky junction is lower current in dark state.

### 6.3.2 Theoretical model

#### Energy band diagram of the graphene/Si Schottky junction

Schottky junction is the name given to the junction formed between a metal and a lightly-doped semiconductor [176]. In this case, the role of the metal is taken by graphene, which is defined as a semi-metal (or zero-bandgap semiconductor). The schematic energy diagram of a graphene/Si junction with undoped graphene and n-doped Si is shown in Fig. 6.4 for different bias conditions. To the left of the junction is the band diagram of graphene, where the Fermi level is at the Dirac point and the states in the valence band are completely filled. Far to the right of the junction, the energy band diagram is the one of n-doped Si. The most important feature of this energy diagram is the barrier at the junction between the two materials, which takes the name of Schottky barrier ($\Phi_B$). This barrier is formed when the materials come in contact and the Fermi levels of graphene and Si align.

At zero bias (Fig. 6.4a), the net dark current across the junction is zero, because electrons on the graphene side and on the Si side have equal (small) probability of having enough energy to cross the Schottky barrier and moving




**(a)** V = 0

**(b)** V > 0

**(c)** V < 0

**Figure 6.4:** Energy band diagram for a graphene/Si Schottky junction with n-doped Si for (a) V = 0, (b) V > 0 and (c) V < 0.

to the opposite side:

$$I_{S\to G} = I_0 = -I_{G\to S} \tag{6.2}$$

$I_{G\to S}$ and $I_{S\to G}$ are the current flowing from graphene to Si and from Si to graphene, respectively. The value of $I_0$ can be calculated using the thermionic emission theory [176, 177], and is given by

$$I_0 = ABT^2 e^{\dfrac{\Phi_B}{k_B T}} \tag{6.3}$$

where $A$ is the junction area, $B$ is the Richardson constant, which is $\sim 100$ AK$^2$cm$^{-2}$ for n-type Si and $\sim 32$ AK$^2$cm$^{-2}$ for p-type Si, $T$ is the temperature and $k_B$ is Boltzmann constant. When a positive bias is applied to graphene (Fig. 6.4b), graphene's Fermi level shifts to the valence band, therefore $I_{G\to S}$ is reduced due to an increase in the Schottky barrier height $\Phi_B$. At the same time, $I_{S\to G}$ increases because the barrier on the Si side is reduced by V (the applied bias). The result is a positive dark current, flowing from Si to graphene. For negative bias (Fig. 6.4c), $I_{G\to S}$ increases, due to a reduction in $\Phi_B$ as graphene's Fermi level moves to the conduction band. On the Si side, the barrier becomes bigger and electrons can't flow from Si to graphene, causing $I_{S\to G}$ to drop to zero. As a result, a negative dark current flows from graphene to Si.

When the light is switched on, electron-hole pairs are generated in the graphene layer, creating an additional photocurrent flowing from graphene to Si. Therefore, at V = 0, $I_{G\to S}$ will be greater than $I_{S\to G}$ due to the photocurrent, and the total current will assume a negative value. At V > 0, the photocurrent keeps flowing from graphene to Si and it has therefore a negative sign. Because the dark current $I_{S\to G}$ has positive sign, the photocurrent causes the total current to decrease. In addition, for large voltage values, the dark current $I_{S\to G}$ becomes too high and the photocurrent becomes small in comparison, making this operating region not interesting for light detection. At V < 0, as the dark current from Si to graphene reduces till becoming zero, the photocurrent becomes more prominent and it adds up to the negative dark current flowing from graphene to Si. This is the ideal operating region.

#### Extraction of Schottky barrier height and ideality factor from measurements

The waveguide doping used for our experiments is in the range of $10^{18}$ cm$^{-3}$. This range coincides with the regime of thermionic field emission, where tunneling through the barrier adds a contribution to the current, normally dominated by emission of thermally excited electrons (or holes) from the semiconductor to the metal (or graphene, in our case). In order to extract the Schottky barrier height and other important parameters from measurements performed on our Schottky junctions, we can therefore make use of the thermionic emission

theory [177, 178]. In the framework of this theory, the total current flowing through the junction can be written as

$$I = I_0 e^{\frac{q(V - R_S I)}{nk_B T}} \tag{6.4}$$

where $n$ is the junction ideality factor, $R_S$ is the total series resistance of the device and $I_0$ is given by Eq. 6.3. For $V \gg R_S I$ and $V \gg k_B T/q$, Eq. 6.4 can be written in logarithmic form as follows:

$$lnI \approx lnI_0 + \frac{1}{nk_B T} V \tag{6.5}$$

By plotting the measurement of current as a function of applied voltage bias in logarithmic form, the value of $I_0$ can be extracted from the intercept (V = 0) and the ideality factor $n$ can be extracted from the slope. The Schottky barrier height $\Phi_B$ can then be calculated from $I_0$ using the following formula:

$$\Phi_B^0 = \frac{k_B T}{q} ln \frac{ABT^2}{I_0} \tag{6.6}$$

Unlike metals, in the case of a graphene/Si junction, the position of graphene's Fermi level at reverse bias changes with varying applied voltage bias. This means that the value of $\Phi_B$ is not constant as it happens with metals, but it will decrease as the reverse voltage increases. As a consequence, in a graphene/Si Schottky junction and in reverse bias conditions, the Schottky barrier height is given by:

$$\Phi_B = \Phi_B^0 + \Delta\Phi_B(V) = \Phi_B^0 - \Delta E_F(V) \tag{6.7}$$

For V = 0, $\Phi_B^0$ can be evaluated from Eq. 6.6 at zero bias. Measurements of the reverse current at V < 0 allow to extract $\Delta\Phi_B(V)$.

In case of p-doped Si, if the bias is applied as shown in Fig. 6.1b, the situation is the same as for n-doped Si but with opposite voltage. Therefore, the reverse bias condition takes place at V > 0. To make the comparison between p-doped and n-doped Si clearer, we have inverted the voltage bias for p-doped Si when plotting the measurements.

### 6.3.3 TE graphene/Si Schottky photodetectors

The first sample (sample A) was fabricated using an average carrier concentration in the waveguide of $n_{wg} = 1.2e18$ cm$^{-3}$ for n-doped Si and $p_{wg} = 1.0e18$ cm$^{-3}$ for p-doped Si. The full flow used to fabricate this sample is described in appendix A, section A.5 (cleaning in DIW). We characterised photodetectors based on 500 nm-wide waveguides optimised for confinement of TE-polarised light. Measurements were performed on Schottky photodetectors with n-doped and p-doped Si. In the case of n-doped Si, the bias was applied as shown in Fig. 6.1b, while for p-doped Si it was reversed.

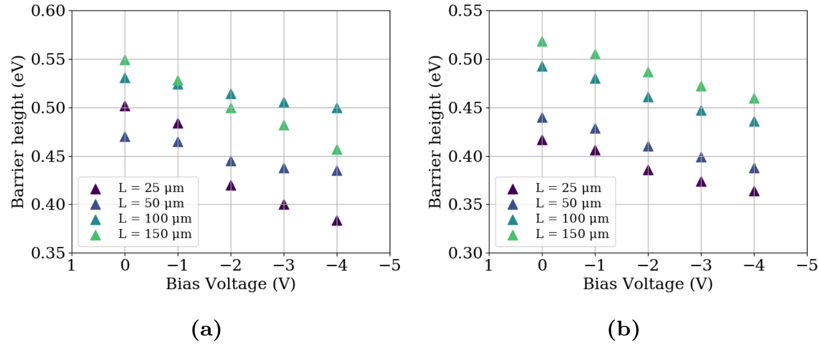



**Figure 6.5:** Schottky barrier height extracted from dark current measurements performed on Schottky photodetectors with (a) n-doped Si and (b) p-doped Si.

**Table 6.2:** Values of ideality factor and Schottky barrier height at 0 V extracted from dark current measurements on Schottky photodetectors with n-doped and p-doped Si.

| | **Gra/n-Si** | | **Gra/p-Si** | |
|---|---|---|---|---|
| | **n** | $\Phi_B^0$ **(eV)** | **n** | $\Phi_B^0$ **(eV)** |
| **25 µm** | 8.9 | 0.50 | 5.4 | 0.42 |
| **50 µm** | 6.9 | 0.47 | 5.3 | 0.44 |
| **100 µm** | 5.8 | 0.53 | 5.9 | 0.49 |
| **150 µm** | 6.1 | 0.55 | 5.7 | 0.52 |

First we measured the current in dark conditions on four photodetectors (for each type of Si doping) with lengths $L_{device}$ = 25, 50, 100 and 150 µm. The bias was applied as shown in Fig. 6.1b and was swept between -4 V and 4 V. From the $I_{dark}$-$V_{bias}$ measurements, we extracted the Schottky barrier height and the ideality factor at reverse bias from -4 V to 0 V (Fig. 6.5). As expected, the Schottky barrier height decreases with higher reverse bias due to graphene's Fermi level shifting to the conduction band. The values of $\Phi_B^0$ (the Schottky barrier height at 0 V) and $n$ are reported in Table 6.2. The devices with p-doped Si exhibit lower ideality factor, but no significant difference between the values of $\Phi_B^0$ is present. These values of $\Phi_B^0$ and $n$ are in line with ones reported in literature, thus validating the extraction method and execution [178].

We then performed light current measurements on Schottky photodetectors with $L_{device}$ = 150 µm for both types of Si doping. The applied bias was swept between -4 V and 4 V and the $I_{light}$-$V_{bias}$ measurement was repeated for varying laser input power from 12 dBm to 0 dBm, with steps of 3 dBm

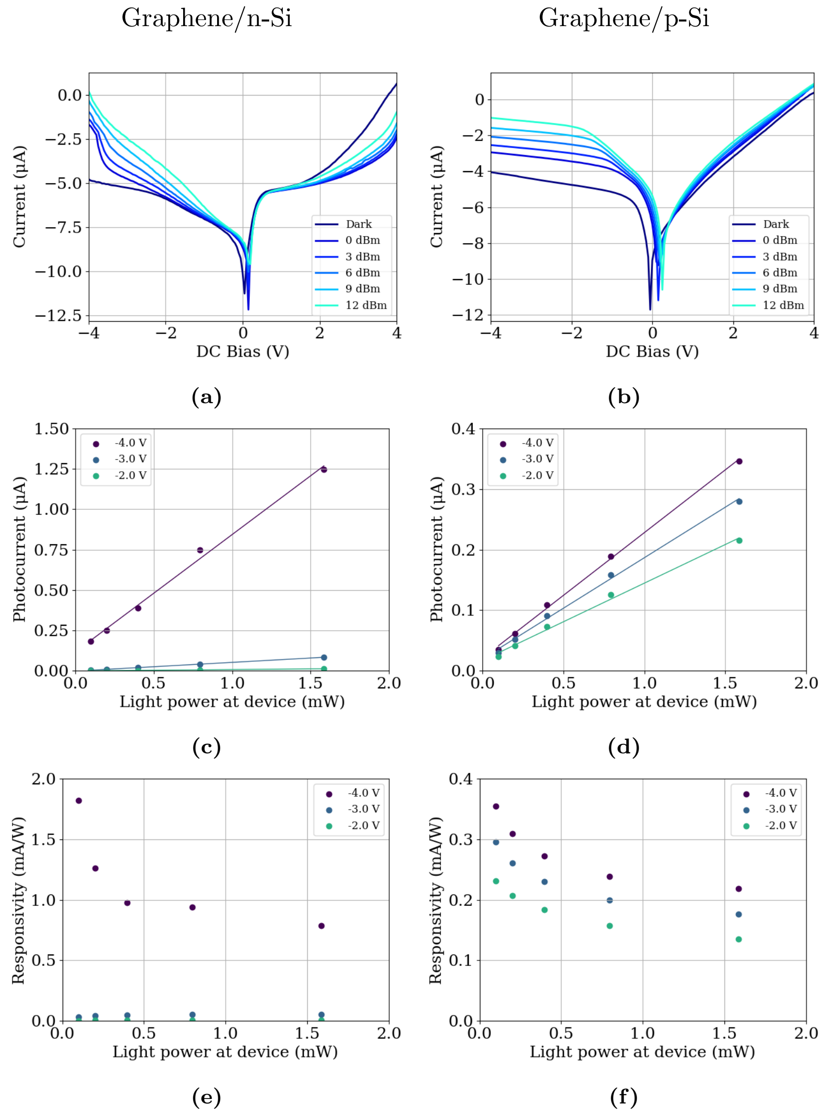



**Figure 6.6:** Left column: graphene/n-Si; right column: graphene/p-Si. (a, b) Light current measurements (in logarithmic scale) performed on graphene Schottky photodetectors with $L_{device}$ = 150 µm. (c, d) Extracted photocurrent as a function of the light power in the device. (e, f) Extracted responsivity as a function of the light power in the device.

(Fig. 6.6a and 6.6b). The photocurrent is calculated by subtracting the dark current from the light current ($I_{light} - I_{dark}$). The obtained value is plotted as a function of the light power at device, which is calculated by measuring

the light power at the fiber tip, right before coupling with the grating coupler takes place, and by subtracting the grating couplers' insertion loss from this quantity. The insertion loss due to the grating couplers is obtained from a reference measurement performed on a waveguide without graphene coverage. The graphs of the photocurrent as a function of the light power at device are shown in Fig. 6.6c for n-doped Si and in Fig. 6.6d for p-doped Si. The linear relation is an indication that the photocurrent is caused by generated photo-carriers in the graphene layer and not due to other phenomena, such as two-photon absorption in Si which would show a parabolic behaviour. The responsivity is calculated as:

$$R = \frac{I_{photo}}{P} \tag{6.8}$$

where $P$ indicates the light power at device. The results of the calculation are plotted as a function of $P$ in Fig. 6.6e and in Fig. 6.6f. The maximum responsivity for both types of Si doping is achieved for the lowest power ($P$ = 0.1 mW) at -4 V and is 1.8 mA/W for graphene/nSi and 0.4 mA/W for graphene/pSi. These values are 2-3 times lower than the best responsivity achieved in literature for graphene/Si Schottky photodetectors [20]. The dark current measured at the same bias voltage (-4 V) is -8.6 nA for graphene/nSi and -1.5 µA for graphene/pSi. One way to improve the responsivity is using TM-polarised waveguides. As seen in chapter 4, with a waveguide width of 750 nm and TM-polarised light, graphene's absorption is doubled compared to a waveguide width of 500 nm and TE-polarised light, as used for this sample. Another way to increase light confinement at the graphene/Si interface is using plasmonic modes by fabricating the graphene metal contact directly on top of the waveguide [20].

### 6.3.4 Improving stability of the graphene/Si Schottky junction

The main problem we identified from measurements performed on sample A is not the low responsivity, but the instability of the dark current. We performed a test on a Schottky junction with graphene and n-doped Si by measuring the dark current as a function of time (from 0 to 360 s) at a fixed voltage bias of 4 V. The test was performed four consecutive times and the results are plotted in Fig. 6.7a. During the first measurement, the dark current drops by one order of magnitude after 60 s time. During the subsequent measurements, performed right after the first one, the initial value of the current at 0 s becomes lower and lower reaching 10 nA for the fourth measurement. The final value of dark current reached after 360 s of measurement is $\sim$ 4 nA for all four measurements. Another feature highlighted by this measurement is the presence of spikes in the curve, which could be the sign of traps at the interface between graphene and Si due to native $SiO_2$ formation.

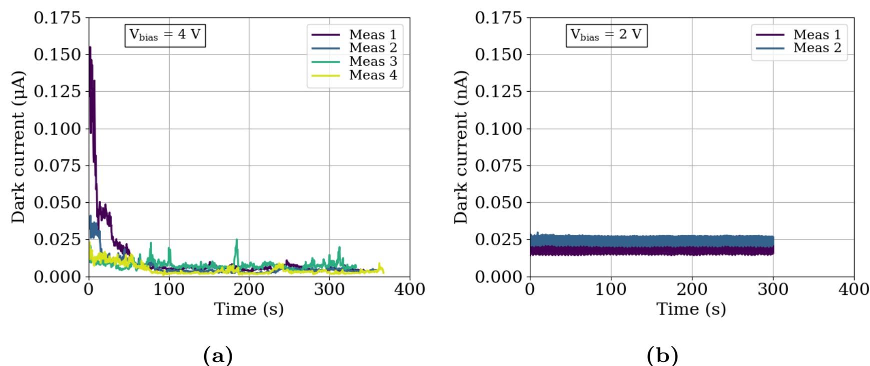



**Figure 6.7:** Measurements of the evolution of the dark current across a graphene/n-Si Schottky junction as a function of time for (a) a sample where transfer was performed in distilled water and (b) a sample where transfer was performed in diluted HF.

With the purpose of creating a more stable interface between graphene and Si, a second sample using a different transfer method was fabricated. For the first sample, graphene transfer was carried out using a wet transfer process in distilled water [86]. For the second sample, we replaced distilled water with diluted HF. The presence of HF at the graphene/Si interface during drying of the sample helps preventing oxide formation [20]. The second sample was fabricated using the same SOI substrate as the first sample with an average carrier concentration in the waveguide of $n_{wg} = 1.2e18$ cm$^{-3}$ for n-doped Si and $p_{wg} = 1.0e18$ cm$^{-3}$ for p-doped Si. The full flow used to fabricate this sample is described in appendix A, section A.5 (cleaning in diluted HF). We repeated the same measurement of dark current as a function of time to check whether the improved transfer method leads to an improved stability of the junction. The data is plotted in Fig. 6.7b, with the y-axis in nA instead of µA to make the measurement data more visible. The dark current is very stable over time (300 s) and lower than in the previous sample ($\sim$ 0.25 nA) for both subsequent measurements. In addition, no spikes are present, which can be interpreted as a reduction in trap sites at the interface between graphene and Si.

We performed additional measurements on this sample to study if the graphene/Si junction behaves in agreement with theoretical predictions (Fig. 6.4). With this goal in mind, we carried out annealing and temperature experiments. When graphene is p-doped, which is the case in most of our samples, graphene's Fermi level is shifted 'downwards' to the valence band. When the junction between graphene and Si is created, the Fermi levels of graphene and Si align. As a consequence, graphene's Dirac cone is 'shifted upwards' causing an increase in Schottky barrier height compared to a junction with undoped graphene (seen in Fig. 6.4a). Right after annealing, graphene's p-doping decreases, there-

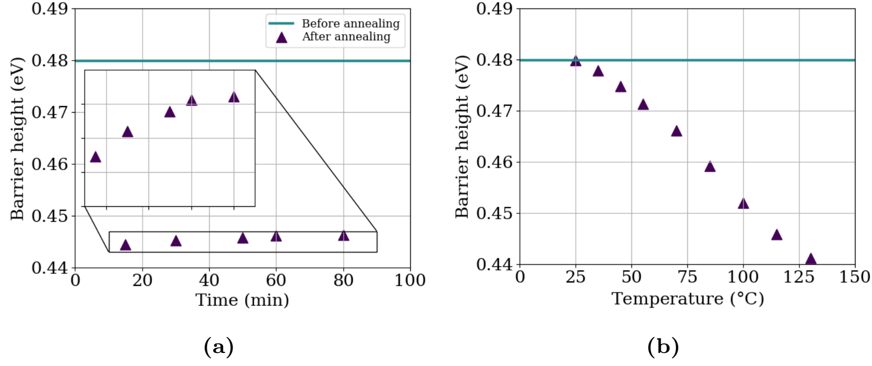



**Figure 6.8:** Extraction of the Schottky barrier height of a graphene/n-Si Schottky junction (a) after sample annealing and (b) at varying temperature.

fore its Fermi level is brought closer to the Dirac point. The 'upwards' shift of graphene's Fermi level causes the Schottky barrier height to decrease and approach the value of a junction with undoped graphene. Because the sample is unpassivated, after annealing graphene is expected to slowly return to its p-doped condition, which leads to an increase of the barrier height with time as graphene's Fermi level shifts 'downwoards'. Eventually, the Schottky barrier height restored to its initial value. For this experiment, we performed an annealing at 150 °C in $N_2$ for one hour on a Schottky photodetector with $L_{device} = 50$ µm and n-doped Si. We then measured the dark current at regular intervals from 10 minutes up to 80 minutes after annealing. The calculation of the Schottky barrier height for each measurement is plotted in Fig. 6.8a. As a reference, the value of $\Phi_B^0$ extracted before annealing is also plotted. As expected, $\Phi_B^0$ increases slowly with time, but it doesn't recover in the time span of the experiment. Measurements performed one day later show a full recovery, with the value of $\Phi_B^0$ back to 0.48 eV. Next, we performed dark current measurements varying the temperature of the chuck from 25 °C to 130 °C. Due to thermally excited electrons, the current is expected to increase, leading to a lower value $\Phi_B^0$ extracted from the formula. This is visible in Fig. 6.8b, where in a range of 105 °C, $\Phi_B^0$ decreases from 0.48 eV to 0.44 eV.

### 6.3.5 TM graphene/Si Schottky photodetectors

In order to improve the responsivity without changing the geometry of our Schottky photodetectors, we measured graphene Schottky photodetectors with n-doped Si, based on 750 nm-wide waveguides, optimised to guide TM-polarised light. We performed light current measurements on Schottky photodetectors with $L_{device}$ of 50 and 100 µm. The applied bias was swept between -2 V and 2 V and the measurement was repeated for varying laser input power from -3 dBm to 6 dBm (Fig. 6.9a and Fig. 6.9b). The bias range and the maximum

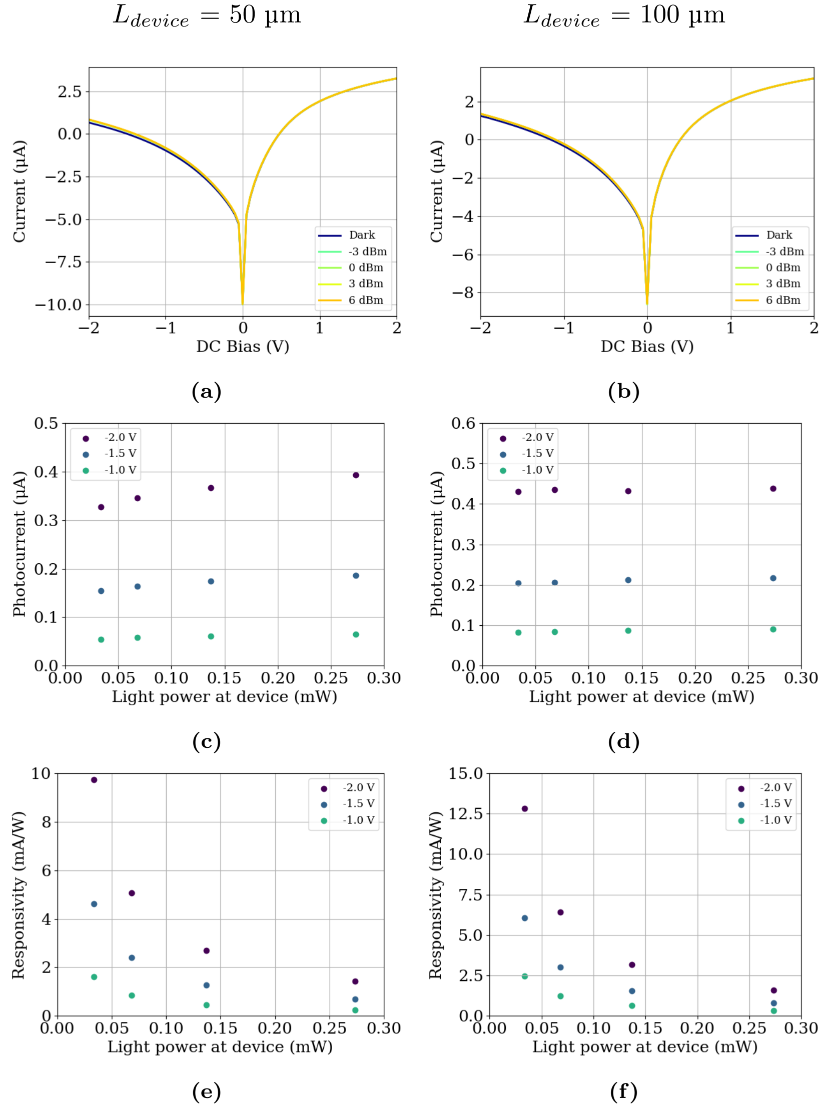



**Figure 6.9:** Left column: $L_{device}$ = 50 µm; right column: $L_{device}$ = 100 µm. (a, b) Light current measurements (in logarithmic scale) performed on graphene Schottky photodetectors with n-doped Si. (c, d) Extracted photocurrent (in logarithmic scale) as a function of the light power in the device. (e, f) Extracted responsivity as a function of the light power in the device.

light input power were reduced compared to previous measurements to avoid pushing the devices to their limits. As before, we calculate the photocurrent and the light power at device to extract the responsivity using Eq. 6.8. The

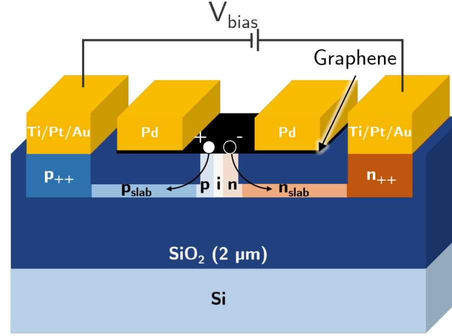



**Figure 6.10:** Schematic cross section of a graphene photodetector based on a $p-i-n$ junction in the Si waveguide and a Schottky junction between graphene and Si.

graphs of the photocurrent as a function of light power at device are shown in Fig. 6.9c for $L_{device}$ = 50 µm and Fig. 6.9d for $L_{device}$ = 100 µm. Once again, the relation between photocurrent and power is linear. The results of the responsivity calculation are plotted in Fig. 6.9e and 6.9f. The maximum responsivity for both device lengths is achieved for the lowest power ($P$ = 0.03 mW) at -2 V and is 9.7 mA/W for $L_{device}$ = 50 µm and 12.8 mA/W for $L_{device}$ = 100 µm. These values of responsivity represent a 5-fold and 7-fold improvement of the best responsivity measured with TE-polarised light. The dark current measured at the same bias voltage (-2 V) is -1.9 µA for $L_{device}$ = 50 µm and -3.5 µA for $L_{device}$ = 100 µm. It's important to notice that the result on TE photodetectors was achieved using $L_{device}$ = 150 µm, meaning that a further improvement could be achieved with longer graphene waveguide coverage using TM-polarised light.

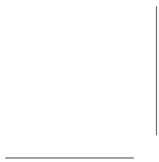
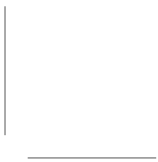
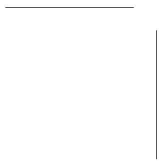
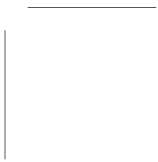
**Table 6.3:** Summary of the main figures of merit measured on the different types of graphene photodetectors presented in this chapter.

| Device type | Wg mode | $L_{device}$ (µm) | $R$ (mA/W) | $I_{dark}$ | $V_{bias}$ (V) | $V_{gate}$ (V) |
|---|---|---|---|---|---|---|
| Photoresistor (n-Si) | TE | 100 | - | -13.1 mA | -1.5 | 3 V |
| Schottky diode (n-Si) | TE | 150 | 1.8 | -8.6 nA | -4 | - |
| Schottky diode (p-Si) | TE | 150 | 0.4 | -1.5 µA | -4 | - |
| Schottky diode (n-Si) | TM | 50 | 9.7 | -1.9 µA | -2 | - |
| Schottky diode (n-Si) | TM | 100 | 12.8 | -3.5 µA | -2 | - |

## 6.4 Outlook

While the responsivity achieved with TM Schottky photodetectors is a good improvement from initial results reported in this chapter (Table 6.3), it is still

worse than the reported responsivities on state-of-the-art graphene photodetectors (see chapter 1). In order to improve the performance of graphene photodetectors based on Schottky junctions, a better control of the interface between Si and graphene is necessary. For example, graphene transfer should take place in controlled conditions, such as in a glove box, to avoid as much as possible Si oxidation. In addition, the devices should be passivated to minimise their deterioration due to environmental effects. As already mentioned earlier, one way to boost the performance of such devices is by stimulating plasmonic modes at the graphene/Si interface [20, 24]. Additionally, or at the same time, different device geometries can be implemented. Inspired by Ge-based photodetectors, a $p-i-n$ junction in the waveguide could be created to collect electrons and holes directly where these are photo-generated (Fig. 6.10). In this scenario, graphene is still directly in contact with Si, thus better control of the interface is of primary importance here as well. During the course of this PhD, we fabricated this type of device and performed some preliminary measurements. However, results were difficult to analyse. Doubts arose as to whether the collected photo-carriers were generated in Si or in graphene due to a parabolic relation between the power at device and the photocurrent. Further improvements in the fabrication process and measurements could allow to dig deeper in the mechanisms governing this device. Another geometry which has already been explored in literature involves the use of two graphene gates to create a $p-n$ junction in the optical absorption region of graphene [21, 24]. This approach has shown very good promise, with some of the highest reported 3 dB frequency responses and responsivities.

# Chapter 7

# Conclusions and Outlook

## 7.1 Conclusions

At the beginning of this PhD thesis, in the first part of chapter 1, optical interconnects (ICs) have been presented as a solution to the challenges posed by the limitations of electrical interconnects. In particular, optical interconnect can tackle the need to achieve high bandwidth at low power consumption for on-board connections in data centers with the implementation of optical transceivers at the chip inputs/outputs (I/Os). Optical transceivers include various components, such as modulators for light modulation and photodetectors for light detection. Photonics ICs have been demonstrated on platforms based on different materials, but the silicon photonics platform has attracted the most interest, being CMOS-compatible and therefore low cost. Several materials, such as III-V materials, InP and Ge, have been integrated in this platform to act as active material for modulators or photodetectors. However, a single technology is not yet capable of meeting all the requirements for optical interconnects, which include high-speed devices with low footprint, insertion loss and energy consumption.

In this scenario, graphene has emerged as a very promising material for applications in optical interconnects. In the second part of 1, graphene and its remarkable properties have been introduced. Graphene's optical properties, specifically its broadband absorption, have been established to be of particular interest in the context of optical interconnects. Following a review of existing literature in the field of graphene photonics, specifically about modulators and photodetectors, several questions have been posed to guide the development of this thesis. For all applications, it is important that graphene devices can be reliably fabricated with long-term stability. Achieving this goal, allows to move on to measure, study and optimize the performance of graphene devices.

For this reason, the first step in this thesis was to successfully create a recipe to fabricate devices based on graphene. In chapter 2, the development and the final result of a 'standard' fabrication process flow were presented, together with results obtained from measurements on graphene electrical test structures fabricated with this recipe. A study of the influence of the underlying doping of silicon on graphene was carried out, showing that these have no detectable effect on graphene's electrical properties. Graphene's stability and electrical properties have however been shown to be affected by ambient exposure and by contact with polymers from fabrication. To tackle this problem, in chapter 3, we developed a different process flow used to fabricate graphene devices with a protective passivation layer. Using this recipe, we fabricated graphene electrical test structures with different passivating materials and we identified $Al_2O_3$ as the right passivation layer to reduce hysteretic behaviour and retain p-doping in graphene. Afterwards, we fabricated $Al_2O_3$-passivated single-layer graphene (SLG) electro-absorption modulators (EAM), obtaining reduced hysteresis in DC performance compared to unpassivated graphene EAMs and excellent stability in the device DC performance and 3 dB frequency response over time.

Once the fabrication flows were established, the focus was shifted to studying and optimising graphene modulators. Two types of EAMs were considered, with single-layer (SLG) or double-layer (DLG) graphene. In chapter 4, we analysed the DC and high-speed performance of SLG EAMs. We presented a theoretical model to study the influence of the type and level of Si doping of the underlying waveguide on the performance of SLG EAMs, and corroborated our findings with experimental data. We found that using p-doped graphene in combination with p-doped Si enables high-speed operation at low DC bias. Using this configuration, we demonstrated SLG EAMs operating in the O-band and in the C-band. Using TM mode waveguides, that allow to achieve higher extinction ratio compared to TE, we obtained open eye diagrams up to 50 Gbit/s, which is to date the fastest demonstrated SLG EAM. Moreover, we integrated SLG EAMs into three five-channel WDM transmitters and demonstrated potential for data transmission at 5 x 25 Gbit/s. In chapter 5, we discussed the modeling techniques of double-layer graphene (DLG) EAMs and compared the performance with the one of SLG EAMs. We showed that DLG EAMs allow to achieve more than double the extinction ratio (ER) of SLG EAMs, up to 0.17 dB/µm for $\sim 20\ V_{pp}$, but suffer from high insertion loss and a more complicated fabrication flow. We then presented a study to identify the design parameters that allow to obtain the best performance for O-band and C-band, TE and TM DLG EAMs. Finally, in chapter 6, we tackled graphene photodetectors with the goal of exploring different geometries and understanding the performance limitations. The demonstrated graphene photodetectors based on graphene/Si Schottky junctions showed responsivities up to 12.8 mA/W. With our device design, better performance was achieved using TM rather than TE waveguides. To conclude, several suggestions to improve the device performance were presented.

## 7.2 Outlook

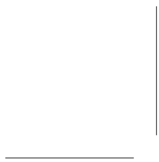
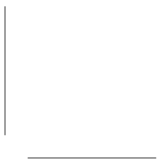
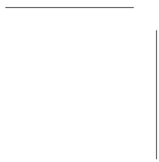
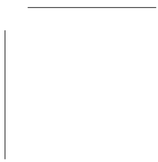
Research in graphene photonics has seen a big surge in the last five years and a lot of progress has been made thanks to the dedication of several groups around the world. In terms of processing, the adoption of graphene offers an advantage compared to other materials, such as III-V and Ge, because graphene devices can be fabricated purely by post-processing on passive waveguide structures. As a consequence, graphene does not have to be fully integrated in the silicon photonics, or silicon nitride, platform. For this reason, fabrication of graphene photonic devices has the potential to be very cost-effective However, before graphene can be considered a viable alternative to well-developed traditional silicon photonics devices, a lot of work still needs to be done. As underlined several times in the course of this thesis, graphene devices suffer from unreliable fabrication processes, that increase the difficulty of obtaining statistically relevant data. It is relatively easy to successfully demonstrate one good device, with good craftsmanship and a bit of luck, but it is hard to achieve the same result over several devices. For this reason, one of the happiest moments of this PhD work was measuring stable device performance on fifteen graphene devices when we demonstrated graphene-based WDM transmitters. Despite this good result, further improvement in the fabrication process of graphene devices needs to be achieved. In particular, the graphene transfer process is a bottleneck for the upscalability of graphene devices. Some initial efforts have already been made to fabricate graphene devices at wafer-scale in a fab, in particular at imec thanks to the great facilities in the 300 mm cleanroom. However, the graphene transfer process still needs to be performed in a cleanroom lab and at smaller scale. Regardless of the application, whether it is for photonics or electronics, the improvement of the graphene transfer process is a goal towards which the whole graphene scientific community should work to make graphene devices a reality. Another issue is given by the high growth temperature of bottom-up processes used to grow graphene, such as CVD and SiC thermal decomposition, which makes these processes not compliant for integration in a fab environment. A further challenge is posed by growing a dielectric on graphene without affecting its electrical performance. As shown in this thesis, a dielectric is necessary to encapsulate graphene, but depositing it without affecting graphene's properties is not an easy task. Finally, a requirement set by CMOS fabs is given by the metals that can be used to fabricate metal contacts. In this thesis, Pd was used to contact graphene. This metal is not CMOS-compatible, therefore an alternative needs to be identified. A possible substitute could be Ni, which has been shown to provide good contact resistance with graphene, especially for edge contacts. An improvement of the graphene fabrication flow, would also allow to make different types of device geometries a viable alternative to more traditional designs presented in this thesis. For example, graphene can be embedded inside the waveguide instead of placing it on top, in order to increase the overlap between the graphene layer and the waveguide mode.

Beyond the silicon photonics platform, graphene's functionality is extremely

interesting also for the silicon nitride (SiN) platform. Silicon nitride has recently proven to be an attractive material for passives, as it is low-loss in a broad spectral range. However, fabrication of active devices has been challenging due to its amorphous structure. Graphene photonics devices, such as DLG EAMs, can be fabricated on SiN with almost no change in the fabrication processes that concern graphene shaping and contacts formation.

Aside from graphene, other bidimensional materials have also recently experienced a new popularity. $MoS_2$ has been used to realise integrated light sources [179], $WS_2$ to demonstrate phase modulators [180], black phosphorus (BP) to build photodetectors [181]. Therefore, graphene will most likely find some company from other 2D materials when it will finally make it onto the big stage of the photonics world.

# Appendices

Appendix A

# Recipes used for devices fabrication

In this appendix we provide details of the different recipes used to fabricate the devices studied in this thesis. All the recipes presented here are based on photolithography.

## A.1 Graphene field-effect transistors

In this section we describe the recipes used to fabricate graphene field effect transistors starting from a $Si/SiO_2$ substrate.

### A.1.1 Standard flow

**Alignment markers**

1. Pre-cleaning: acetone at 45°C for 5 min + IPA rinse at RT + $N_2$ dry
2. Drying bake: hotplate at 120°C for 5 min
3. Spin coating: IX845 at 4000 rpm for 30 sec (3 sec ramp)
4. Curing: hotplate at 120°C for 1 min
5. Exposure: hard contact for 8 sec
6. Development: OPD5262 for 90 sec + DIW rinse
7. Metal deposition: Ti (2nm)/Pd (50 nm) by e-gun evaporation
8. Lift-off: acetone at 45°C for 3 hrs* + IPA rinse at RT + $N_2$ dry

* Put 3 pipettes of hot acetone in a new small beaker. Move the sample in the small beaker very quickly and blow acetone very hard on the sample with the pipette, staying as close as possible to the sample.

**Graphene transfer**
In-house graphene transfer from Pt foil, using electrolysis to delaminate the graphene from the growth substrate and PMMA.

**Graphene shaping**

1. Drying bake: hotplate at 120°C for 5 min
2. Spin coating 1: Chlorobenzene PMMA 3% at 6000 rpm for 60 sec (3 sec ramp)
3. Curing 1: hotplate at 120°C for 3 min
4. Spin coating 2: IX845 at 4000 rpm for 30 sec with 3 sec ramp (photoresist thickness = $\sim$ 1 µm)
5. Curing 2: hotplate at 120°C for 1 min
6. Exposure: hard contact for 8 sec
7. Development: OPD5262 for 90 sec + DIW rinse + $N_2$ dry
8. Graphene etching: $O_2$ plasma for 32 min at 100 W
9. Sample cleaning: acetone at 45°C overnight + IPA rinse at RT + $N_2$ dry

**Graphene contacts**

1. Drying bake: hotplate at 120°C for 5 min
2. Spin coating: IX845 at 4000 rpm for 30 sec (3 sec ramp)
3. Curing: hotplate at 120°C for 1 min
4. Exposure: hard contact for 8 sec
5. Development: OPD5262 for 90 sec + DIW rinse + $N_2$ dry
6. Metal deposition: Pd (50 nm) by e-gun evaporation
7. Lift-off: acetone at 45°C for 3 hrs* + IPA rinse at RT + $N_2$ dry

* Put 3 pipettes of hot acetone in a new small beaker. Move the sample in the small beaker very quickly and blow acetone very hard on the sample with the pipette, staying as close as possible to the sample.

### A.1.2 Passivation-first flow

**Alignment markers**

1. Drying bake: hotplate at 120°C for 5 min
2. Spin coating: IX845 at 4000 rpm for 30 sec (3 sec ramp)
3. Curing: hotplate at 120°C for 1 min
4. Exposure: hard contact for 8 sec
5. Development: OPD5262 for 90 sec + DIW rinse + $N_2$ dry
6. Markers etching: BHF for 5 min + DIW rinse + $N_2$ dry
7. Sample cleaning: acetone at 45°C for 3 hrs + IPA rinse at RT + $N_2$ dry

**Graphene transfer**
In-house graphene transfer from Pt foil, using electrolysis to delaminate the graphene from the growth substrate and PMMA.

**Graphene shaping**

1. Drying bake: hotplate at 120°C for 5 min
2. Spin coating 1: Chlorobenzene PMMA 3% at 6000 rpm for 60 sec (3 sec ramp)
3. Curing 1: hotplate at 120°C for 3 min
4. Spin coating 2: IX845 at 4000 rpm for 30 sec with 3 sec ramp (photoresist thickness = $\sim$ 1 µm)
5. Curing 2: hotplate at 120°C for 1 min
6. Exposure: hard contact for 8 sec
7. Development: OPD5262 for 90 sec + DIW rinse + $N_2$ dry
8. Graphene etching: $O_2$ plasma for 15 min at 100 W
9. Sample cleaning: acetone at 45°C overnight + IPA rinse at RT + $N_2$ dry

**Oxide capping**

1. Seeding layer: Si (0.5 nm) by e-gun evaporation
2. Oxide deposition: $Al_2O_3$ (10 nm) by ALD

**Graphene contacts**

1. Drying bake: hotplate at 120°C for 5 min
2. Spin coating 1: Anisole PMMA 3% at 6000 rpm for 60 sec (3 sec ramp)
3. Curing 1: hotplate at 120°C for 3 min

4. Spin coating 2: IX845 at 4000 rpm for 30 sec with 3 sec ramp (photoresist thickness = ∼ 1 µm)
5. Curing 2: hotplate at 120°C for 1 min
6. Exposure: hard contact for 8 sec
7. Development: OPD5262 for 90 sec + DIW rinse + $N_2$ dry
8. PMMA etching: $O_2$ plasma for 15 min at 100W
9. Oxide etching: RIE with 5 mT, 450 W inductively coupled plasma (ICP) power, 100 V bias and a gas mix of 50% $BCl_3$ and 50% He
10. Metal deposition: Ni (50 nm) by e-gun evaporation
11. Lift-off: acetone at 45°C for 3 hrs* + IPA rinse at RT + $N_2$ dry

* Put 3 pipettes of hot acetone in a new small beaker. Move the sample in the small beaker very quickly and blow acetone very hard on the sample with the pipette, staying as close as possible to the sample.

## A.2 Single-layer graphene electro-absorption modulators

In this section we describe the recipes used to fabricate single-layer graphene electro-absorption modulators starting from a SOI substrate.

### A.2.1 Standard flow

**Graphene transfer**
Graphene transfer performed by *Graphenea* (www.graphenea.com).

**Graphene shaping**

1. Pre-cleaning: acetone at 45°C for 5 min + IPA rinse at RT + $N_2$ dry
2. Drying bake: hotplate at 120°C for 5 min
3. Spin coating 1: $N_2$ blow + Chlorobenzene PMMA 3% at 6000 rpm for 60 sec (3 sec ramp)
4. Curing 1: hotplate at 120°C for 3 min
5. Spin coating 2: $N_2$ blow + IX845 at 4000 rpm for 30 sec with 3 sec ramp (photoresist thickness = ∼ 1 µm)
6. Curing 2: hotplate at 120°C for 1 min
7. Exposure: hard contact for 8 sec
8. Development: Microposit™ 351 for 60 sec + DIW rinse + $N_2$ dry
9. Graphene etching: $O_2$ plasma for 14 min at 100 W
10. Sample cleaning: acetone at 45°C overnight + IPA rinse at RT + $N_2$ dry

**Graphene contacts**

1. Pre-cleaning: acetone at 45°C for 5 min + IPA rinse at RT + $N_2$ dry
2. Drying bake: hotplate at 120°C for 5 min
3. Spin coating: $N_2$ blow + IX845 at 4000 rpm for 30 sec (3 sec ramp)
4. Curing: hotplate at 120°C for 1 min
5. Exposure: hard contact for 8 sec
6. Development: OPD5262 for 90 sec + DIW rinse
7. Metal deposition: Pd (50 nm) by e-gun evaporation
8. Lift-off: acetone at 45°C for 3 hrs* + IPA rinse at RT + $N_2$ dry

* Put 3 pipettes of hot acetone in a new small beaker. Move the sample in the small beaker very quickly and blow acetone very hard on the sample with the pipette, staying as close as possible to the sample.

**Silicon contacts**

1. Pre-cleaning: acetone at 45°C for 5 min + IPA rinse at RT + $N_2$ dry
2. Drying bake: hotplate at 120°C for 5 min
3. Spin coating: $N_2$ blow + IX845 at 4000 rpm for 30 sec (3 sec ramp)
4. Curing: hotplate at 120°C for 1 min
5. Exposure: hard contact for 8 sec
6. Development: OPD5262 for 90 sec + DIW rinse + $N_2$ dry
7. $SiO_2$ etching: BHF for 1 min (right before loading the sample in the metal evaporation tool)
8. Metal deposition: Ti (20 nm)/Pt (20 nm) by thermal evaporation; Au (30 nm) by e-gun evaporation
9. Lift-off: acetone at 45°C for 3 hrs* + IPA rinse at RT + $N_2$ dry

* Put 3 pipettes of hot acetone in a new small beaker. Move the sample in the small beaker very quickly and blow acetone very hard on the sample with the pipette, staying as close as possible to the sample.

### A.2.2 Passivation-first flow

**Graphene transfer**
Graphene transfer performed by *Graphenea* (www.graphenea.com).

**Graphene shaping**

1. Pre-cleaning: acetone at 45°C for 5 min + IPA rinse at RT + $N_2$ dry

2. Drying bake: hotplate at 120°C for 5 min
3. Spin coating 1: $N_2$ blow + Chlorobenzene PMMA 3% at 6000 rpm for 60 sec (3 sec ramp)
4. Curing 1: hotplate at 120°C for 3 min
5. Spin coating 2: $N_2$ blow + IX845 at 4000 rpm for 30 sec with 3 sec ramp (photoresist thickness = ∼ 1 µm)
6. Curing 2: hotplate at 120°C for 1 min
7. Exposure: hard contact for 8 sec
8. Development: Microposit™ 351 for 60 sec + DIW rinse + $N_2$ dry
9. Graphene etching: $O_2$ plasma for 14 min at 100 W
10. Sample cleaning: acetone at 45°C overnight + IPA rinse at RT + $N_2$ dry

**Oxide capping**

1. Sample cleaning: FOG (5% flow 1 l/h) annealing at 350°C for 1 hour; ramp-up 2°C/min; ramp-down 4 °C/min
2. Seeding layer: Si (0.5 nm) by e-gun evaporation
3. Oxide deposition: $Al_2O_3$ (10 nm) by ALD

**Graphene contacts**

1. Drying bake: hotplate at 120°C for 5 min
2. Spin coating: $N_2$ blow + IX845 at 4000 rpm for 30 sec with 3 sec ramp (photoresist thickness = ∼ 1 µm)
3. Curing: hotplate at 120°C for 1 min
4. Exposure: hard contact for 8 sec
5. Development: OPD5262 for 90 sec + DIW rinse + $N_2$ dry
6. PMMA etching: $O_2$ plasma for 15 min at 100W
7. Oxide etching: $Al_2O_3$ etching by RIE with 5 mT, 450 W inductively coupled plasma (ICP) power, 100 V bias and a gas mix of 50% $BCl_3$ and 50% He
8. Metal deposition: Pd (50 nm) by e-gun evaporation
9. Lift-off: acetone at 45°C for 3 hrs* + IPA rinse at RT + $N_2$ dry

* Put 3 pipettes of hot acetone in a new small beaker. Move the sample in the small beaker very quickly and blow acetone very hard on the sample with the pipette, staying as close as possible to the sample.

**Silicon contacts**

1. Pre-cleaning: acetone at 45°C for 5 min + IPA rinse at RT + $N_2$ dry
2. Drying bake: hotplate at 120°C for 5 min
3. Spin coating: $N_2$ blow + IX845 at 4000 rpm for 30 sec (3 sec ramp)
4. Curing: hotplate at 120°C for 1 min
5. Exposure: hard contact for 8 sec
6. Development: OPD5262 for 90 sec + DIW rinse + $N_2$ dry
7. Oxide etching: $SiO_2$ and $Al_2O_3$ etching in BHF for 4 min (right before loading the sample in the metal evaporation tool)
8. Metal deposition: Ti (20 nm)/Pt (20 nm) by thermal evaporation; Au (30 nm) by e-gun evaporation
9. Lift-off: acetone at 45°C for 3 hrs* + IPA rinse at RT + $N_2$ dry

* Put 3 pipettes of hot acetone in a new small beaker. Move the sample in the small beaker very quickly and blow acetone very hard on the sample with the pipette, staying as close as possible to the sample.

## A.3 Double-layer graphene electro-absorption modulators

In this section we describe the recipes used to fabricate double-layer graphene electro-absorption modulators starting from a SOI substrate.

**Graphene transfer**
In-house graphene transfer from Pt foil, using electrolysis to delaminate the graphene from the growth substrate and PMMA.

**Graphene shaping**

1. Pre-cleaning: acetone at 45°C for 5 min + IPA rinse at RT + $N_2$ dry
2. Drying bake: hotplate at 120°C for 5 min
3. Spin coating 1: $N_2$ blow + Chlorobenzene PMMA 3% at 6000 rpm for 60 sec (3 sec ramp)
4. Curing 1: hotplate at 120°C for 3 min
5. Spin coating 2: $N_2$ blow + IX845 at 4000 rpm for 30 sec with 3 sec ramp (photoresist thickness = $\sim$ 1 µm)
6. Curing 2: hotplate at 120°C for 1 min
7. Exposure: hard contact for 8 sec
8. Development: OPD5262 for 60 sec + DIW rinse + $N_2$ dry

9. Graphene etching: $O_2$ plasma for 14 min at 100 W
10. Sample cleaning: acetone at 45°C overnight + IPA rinse at RT + $N_2$ dry

**Oxide deposition**

1. Sample cleaning: FOG (5% flow 1 l/h) annealing at 350°C for 1 hour; ramp-up 2°C/min; ramp-down 4 °C/min
2. Seeding layer: Si (0.5 nm) by e-gun evaporation (only used for $HfO_2$ samples)
3. Oxide deposition: $Al_2O_3$ (30 nm) or $HfO_2$ (6 and 10 nm) by ALD

**Graphene transfer**
In-house graphene transfer from Pt foil, using electrolysis to delaminate the graphene from the growth substrate and PMMA.

**Graphene shaping**

1. Pre-cleaning: acetone at 45°C for 5 min + IPA rinse at RT + $N_2$ dry
2. Drying bake: hotplate at 120°C for 5 min
3. Spin coating 1: $N_2$ blow + Chlorobenzene PMMA 3% at 6000 rpm for 60 sec (3 sec ramp)
4. Curing 1: hotplate at 120°C for 3 min
5. Spin coating 2: $N_2$ blow + IX845 at 4000 rpm for 30 sec with 3 sec ramp (photoresist thickness = $\sim$ 1 µm)
6. Curing 2: hotplate at 120°C for 1 min
7. Exposure: hard contact for 8 sec
8. Development: OPD5262 for 60 sec + DIW rinse + $N_2$ dry
9. Graphene etching: $O_2$ plasma for 14 min at 100 W
10. Sample cleaning: acetone at 45°C overnight + IPA rinse at RT + $N_2$ dry

**Oxide deposition**

1. Sample cleaning: FOG (5% flow 1 l/h) annealing at 350°C for 1 hour; ramp-up 2°C/min; ramp-down 4 °C/min
2. Seeding layer: Si (0.5 nm) by e-gun evaporation (only used for $HfO_2$ samples)
3. Oxide deposition: $Al_2O_3$ (30 nm) or $HfO_2$ (6 and 10 nm) by ALD

**Graphene contacts** The two graphene contacts needed for DLG EAMs can be fabricated simultaneously or separately. In either case, the recipe is the following.

1. Drying bake: hotplate at 120°C for 5 min
2. Spin coating 1: $N_2$ blow + Chlorobenzene PMMA 3% at 6000 rpm for 60 sec (3 sec ramp)
3. Curing 1: hotplate at 120°C for 3 min
4. Spin coating 2: $N_2$ blow + IX845 at 4000 rpm for 30 sec with 3 sec ramp (photoresist thickness = $\sim$ 1 µm)
5. Curing 2: hotplate at 120°C for 1 min
6. Exposure: hard contact for 8 sec
7. Development: OPD5262 for 90 sec + DIW rinse + $N_2$ dry
8. PMMA etching: $O_2$ plasma for 15 min at 100W
9. Oxide etching: $Al_2O_3$ etching by RIE with 5 mT, 450 W inductively coupled plasma (ICP) power, 100 V bias and a gas mix of 50% $BCl_3$ and 50% He
10. Metal deposition: Pd (50 nm) by e-gun evaporation
11. Lift-off: acetone at 45°C for 3 hrs* + IPA rinse at RT + $N_2$ dry

## A.4 Graphene photoresistors

The flow used to fabricate graphene photoresistors is the same used for graphene electro-absorption modulators detailed in Section A.2.1.

## A.5 Photodetectors based on a graphene/Si Schottky junction

In this section we describe the recipes used to fabricate photodetectors based on a graphene/Si Schottky junction starting from a SOI substrate. It's not the goal of this thesis to describe in detail how graphene transfer works. However, the cleaning step during transfer plays an important role for these devices, so the two recipes used are described here briefly.

**Graphene transfer in DIW**
In-house graphene transfer from Pt foil, using electrolysis to delaminate the graphene from the growth substrate and PMMA. The cleaning step was performed in DIW.

**Graphene transfer in diluted HF**
In-house graphene transfer from Pt foil, using electrolysis to delaminate the graphene from the growth substrate and PMMA. The cleaning step was performed in diluted HF.

The rest of the flow (graphene shaping, graphene contacts and silicon contacts) is identical to the one used for graphene electro-absorption modulators detailed in Section A.2.1.

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# List of Publications

## Publications in international journals

**C. Alessandri**, I. Asselberghs, S. Brems, C. Huyghebaert, J. Van Campenhout, D. Van Thourhout, M. Pantouvaki, "High speed graphene-silicon electro-absorption modulators for the O-band and C-band", *Japanese Journal of Applied Physics*, 59(5), 2020. DOI: 10.35848/1347-4065/ab8920

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## Publications in international conferences

**C. Alessandri**, C. Wu, F. Peyskens, I. Asselberghs, S. Brems, C. Huyghebaert, J. Van Campenhout, M. Pantouvaki, and D. Van Thourhout, "Prospects for Hybrid Integration of Si and SiN Waveguides with Graphene and Other 2D-materials", *Advanced Photonics Congress* (***invited***), paper ITh3A.2, online event (2020).

**C. Alessandri**, C. Wu, X. Wu, I. Asselberghs, S. Brems, C. Huyghebaert, J. Van Campenhout, D. Van Thourhout, and M. Pantouvaki, "Influence of passivation layer on graphene properties for optoelectronic applications", *Graphene Week*, Helsinki, Finland (2019).

**C. Alessandri**, I. Asselberghs, S. Brems, C. Huyghebaert, J. Van Campenhout, D. Van Thourhout, and M. Pantouvaki, "Graphene-Based Optical Modulators for Next Generation Datacom," *Solid State Devices and Materials* (***invited***), Nagoya, Japan (2019).

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**C. Alessandri**, I. Asselberghs, Y. Ban, S. Brems, C. Huyghebaert, J. Van Campenhout, D. Van Thourhout, M. Pantouvaki, "Broadband 20 Gbit/s Graphene-Si Electro-Absorption Modulator," *European Conference on Optical Communication*, paper We4C.2, Rome, Italy (2018). DOI: 10.1109/ECOC.2018.8535513

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